Glossary

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A

Altera Consultants Alliance Program (ACAP) An alliance created to provide expert design assistance to users of Altera® programmable logic devices (PLDs). ACAP℠ consultants provide their expertise and services to designers.

Altera Hardware Description Language (AHDL) Altera's design entry language. A high-level, modular language that is integrated into the Quartus™ and MAX+PLUS® II development systems. You can create AHDL Text Design Files (**.tdf**) with the Quartus and MAX+PLUS II Text Editors or any standard text editor, then compile, simulate, and program your projects within the Quartus and MAX+PLUS II software. AHDL supports Boolean equations, state machines, and conditional and decode logic. AHDL also allows you to create and use parameterized functions, and includes full support for functions in the library of parameterized modules (LPM).

Altera Megafunction Partners Program (AMPP) An alliance between Altera and developers of synthesizable megafunctions. The AMPP℠ program was created to bring the advantages of megafunctions to users of Altera PLDs.

APEX 20K An Altera embedded programmable logic device family based on the Advanced Programmable Embedded Matrix (APEX™) architecture, which integrates look-up table logic, product-term logic, and memory in a single device. This family offers complete system integration on a single device. The APEX 20K device family includes the EP20K100, EP20K100E, EP20K160E, EP20K200, EP20K200E, EP20K300E, EP20K400, EP20K400E, EP20K600E, and EP20K1000E devices.

array clock A clock signal that passes through the logic array of a device before arriving at the clock input of a register.

Assignment & Configuration File (.acf) An ASCII file for the MAX+PLUS II software that stores information about probe, resource, and device assignments for a hierarchy tree, as well as configuration information for the Compiler, Simulator, Timing Analyzer, and Programmer. All information that can affect output files containing design information for the current hierarchy tree is controlled by the ACF.

B

ball-grid array (BGA) A high-performance device package offered by Altera that allows for higher pin counts in significantly less board area than quad flat pack (QFP) packages and have better thermal characteristics than most QFP packages. BGA packages are rapidly becoming the preferred packages for high-density PLDs. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

BitBlaster cable A serial download cable that allows both PC and UNIX workstation users to program and configure devices in-system or in-circuit. The BitBlaster™ serial download cable provides programming support for MAX® 9000, MAX 7000S, MAX 7000A, MAX 7000AE, and MAX 3000A devices, and configuration support for APEX 20K, FLEX® 10K, FLEX 8000, and FLEX 6000 devices.

FLEX 6000 and FLEX 10K devices can be configured together in a FLEX chain; FLEX 8000 devices cannot be configured in the same chain with other FLEX devices.

ByteBlaster cable (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable) A parallel download cable that allows PC users to program and configure devices in-system. The ByteBlaster™ parallel port download cable provides programming support for MAX 9000, MAX 7000S, MAX 7000A, and MAX 3000A devices, and configuration support for APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 devices. FLEX 6000 and FLEX 10K devices can be configured together in a FLEX chain; FLEX 8000 devices cannot be configured with other FLEX devices.

ByteBlasterMV cable A parallel download cable that allows PC users to program and configure devices in-system. The ByteBlasterMV™ parallel port download cable provides programming support for MAX 9000, MAX 7000S, MAX 7000A, MAX 3000A, and configuration support for APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 devices. FLEX 6000 and FLEX 10K devices can be configured together in a FLEX chain; FLEX 8000 devices cannot be configured with other FLEX devices.

C

carry chain A dedicated architectural feature of the APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 device families that provides a high-performance carry-forward function between logic elements (LEs). The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the look-up table (LUT) and the next portion of the carry chain. This carry-forward function is ideal for adders, counters, and comparators.

cascade chain A dedicated architectural feature of the APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 families that allows implementation of high-performance, wide fan-in functions. Adjacent LUTs can be used to compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain is available only in FLEX 10K, FLEX 8000, and FLEX 6000 devices.

ceramic dual in-line package (CerDIP) A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

Classic An Altera device family based on Altera's original EPROM-based EPLD architecture. The Classic™ device family includes the EP610, EP610I, EP910, EP910I, EP1800I, and EP1810 devices.

ClockBoost An Altera high-density programmable logic device feature available in APEX 20K and selected FLEX 10K devices that uses a phase-locked loop (PLL) to increase clock frequencies by as much as sixteen times the incoming clock rate, improving system performance. Combining the ClockBoost™ and ClockLock™ features provides significant advantages in system performance and bandwidth.

ClockLock An Altera high-density programmable logic device feature available in APEX 20K and selected FLEX 10K devices that uses a phase-locked loop (PLL) to increase clock frequencies by as much as sixteen times the incoming clock rate, improving system performance. Combining the ClockBoost™ and ClockLock™ features provides significant advantages in system performance and bandwidth.

configuration device Altera's family of serial devices, which are designed to configure APEX and FLEX devices. See the *Configuration Devices for APEX & FLEX Devices* Data Sheet for more information.

configuration scheme The method used to load data into FLEX devices.

Five configuration schemes are available for APEX 20K and FLEX 10K devices: configuration device, passive serial (PS), passive parallel asynchronous (PPA), passive parallel synchronous (PPS), and IEEE Std. 1149.1 Joint Test Action Group (JTAG). For complete information on FLEX 10K configuration schemes, see *Application Note 59 (Configuring FLEX 10K Devices)*.

Six configuration schemes are available for FLEX 8000 devices: active serial (AS), active parallel up (APU), active parallel down (APD), PPA, PPS, and PS. For complete information on FLEX 8000 configuration schemes, see *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

Three configuration schemes are available for FLEX 6000 devices: configuration device, passive serial (PS), and passive serial asynchronous (PSA). For complete information on FLEX 6000 configuration schemes, see *Application Note 87 (Configuring FLEX 6000 Devices)*.

continuity checking A test for open circuits between device pins and programming adapter sockets. This test verifies that a device is properly seated in the socket of the adapter.

ceramic quad flat pack (CQFP) A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

D

dedicated input pin A pin that can only be used as an input to the device.

development socket A prototyping socket for high-pin-count QFP packages.

device Refers to an Altera programmable logic device, including APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 3000A, MAX 5000, and Classic devices. Altera also offers configuration devices that are used to configure APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 devices.

device family A group of Altera programmable logic devices with the same fundamental architecture. Altera device families include the APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 3000A, MAX 5000, and Classic device families. Altera also offers a configuration device family that includes devices used for configuring APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 devices.

dual in-line package (DIP) A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information. Ceramic (CerDIP) and plastic (PDIP) versions are available.

dual-port RAM The APEX 20K embedded system block (ESB) and FLEX 10KE embedded array block (EAB) supports dual-port RAM with independent read/write ports, synchronous or asynchronous access, and 150-MHz first-in first-out (FIFO) buffer performance. This system-level memory integration efficiently supports the various RAM requirements of a system-level design, such as cache RAM, dual-port FIFO buffers, or ROM.

E

Electronic Design Interchange Format (EDIF) An industry-standard format for the transmission of design data. You can generate an EDIF 2 0 0 or 3 0 0 netlist file from a schematic design or from a VHDL or Verilog HDL design that has been processed with an appropriate industry-standard synthesis tool. You can then import the file into

the Quartus and MAX+PLUS II software as an EDIF Input File (**.edf**). The Quartus and MAX+PLUS II software supports EDIF Input Files that contain functions from the library of parameterized modules (LPM). The Quartus and MAX+PLUS II Compilers can also generate one or more EDIF Output Files (**.edo**) in either EDIF 2 0 0 or 3 0 0 format that contain functional and timing information for simulation with a standard EDIF simulator.

EDIF Input File (.edf) An EDIF version 2 0 0 or 3 0 0 netlist file generated by any industry-standard EDIF netlist writer. EDIF Input Files can be compiled by the Quartus and MAX+PLUS II Compilers. The Quartus and MAX+PLUS II software supports EDIF Input Files that contain functions from the library of parameterized modules (LPM).

EDIF Output File (.edo) An EDIF version 2 0 0 or 3 0 0 netlist file generated by the EDIF Netlist Writer module of the Quartus and MAX+PLUS II Compiler. This file can be exported to an industry-standard UNIX workstation or PC environment for simulation.

electrically erasable programmable read-only memory (EEPROM) A form of reprogrammable semiconductor memory in which the contents can be erased by subjecting the device to appropriate electrical signals. See the *Operating Requirements for Altera Devices Data Sheet* for more information.

embedded array A series of embedded array blocks (EABs) in FLEX 10K devices used to implement a variety of memory functions or complex logic functions, such as digital signal processing (DSP), microcontroller, wide data-path manipulation, and data transformation functions.

embedded array block (EAB) The building block of embedded arrays in FLEX 10K devices. Each EAB provides 2,048 or 4096 bits of configurable RAM, ROM, FIFO, or dual-port RAM. When implementing logic, each EAB can contribute 100 to 300 gates towards complex logic functions.

embedded system block (ESB) The embedded system block resides in the MultiCore architecture of the APEX 20K. Each ESB contains 2,048 programmable bits that can be configured as product-term logic, look-up table-based logic, or dual-port RAM, ROM, or content addressable memory (CAM). Each ESB can be configured with up to 16 macrocells, and can contain up to 32 product terms, XOR logic, 16 D-flipflops, and parallel expanders.

EP Family signature on a part number that refers to the APEX 20K and Classic device families. See the *APEX 20K Programmable Logic Device Family* and the *Classic EPLD Family* data sheets for more information.

EPC Family signature on a part number that refers to the configuration device family.

EPF Family signature on a part number that refers to the FLEX device family.

EPM Family signature on a part number that refers to the MAX device family.

erasable programmable logic device (EPLD) Altera EPLD device families include MAX 9000, MAX 7000, MAX 3000A, MAX 5000, and Classic.

erasable programmable read-only memory (EPROM) A form of reprogrammable semiconductor memory in which the contents can be erased by subjecting the device to the proper wavelength of ultraviolet light. See the *Operating Requirements for Altera Devices Data Sheet* for more information.

expander product term A single product term with an inverted output that feeds back into the logic array block (LAB) of a MAX 9000, MAX 7000, MAX 3000A, or MAX 5000 device.

An uncommitted expander product term that can be shared with other logic cells in the same LAB is called a shareable expander; a product term that has been shared in this manner is called a shared expander. In MAX 9000, MAX 7000, and MAX 3000A devices only, an expander product term that is "borrowed" from an adjacent logic cell in the same LAB is called a parallel expander.

external timing parameters Factory-tested, worst-case values specified by Altera. In this data book, external timing parameters are shown in bold type. In the device family data sheets, external timing parameters are listed under "External Timing Characteristics."

extraction tool A tool used to extract QFP devices from QFP carriers. Extraction tools are available from Altera for 100-, 160-, 208-, 240-, and 304-pin QFP packages. See the *QFP Carrier & Development Socket Data Sheet* for more information.

F

FastFLEX I/O In the FLEX 6000 family, the FastFLEX™ I/O feature provides a direct path from LEs to an I/O pin for fast clock-to-output timing. See the *FLEX 6000 Programmable Logic Device Family Data Sheet* for more information.

fast I/O A logic option you can use to specify that a register should be implemented in an I/O cell for APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000S, MAX 7000A, MAX 7000E, or MAX 3000A devices. This logic option can be applied to individual logic functions. However, it cannot be incorporated into a logic synthesis style or applied to an entire project.

FastTrack Interconnect Dedicated connection paths that span the entire width and height of an APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, or MAX 9000 device. The FastTrack® Interconnect allows signals to travel between all logic array blocks (LABs) in a device.

FineLine BGA FineLine BGA™ packages available for APEX 20K, FLEX 10K, and MAX 7000 devices use only half the board area of traditional BGA packages and are offered with as many as 900 pins for the EP20K1000E device. This new package allows designs to be effectively implemented into higher density, higher pin count devices into designs while decreasing board space and costs. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

Fitter The MAX+PLUS II Compiler module that fits a project into one or more devices. The Fitter selects appropriate interconnection paths as well as the pin and logic cell assignments. It also generates part of the Report File (**.rpt**) and Fit File (**.fit**) for the project. The (**.fit**) file is not used in Quartus.

FLEX 10K An Altera device family based on the Flexible Logic Element MatriX (FLEX) architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices with embedded arrays. The embedded arrays are used to efficiently implement memory or complex logic functions. See the *FLEX 10K Embedded Programmable Logic Family* and *FLEX 10KE Embedded Programmable Logic Data Sheets* for more information.

FLEX 6000 An Altera device family based on the OptiFLEX™ architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices. See the *FLEX 6000 Programmable Logic Device Family Data Sheet* for more information.

FLEX 8000 An Altera device family based on the Flexible Logic Element MatriX (FLEX) architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices.

See the *FLEX 8000 Programmable Logic Device Family Data Sheet* for more information.

flipflop An edge-triggered, clocked storage unit that stores a single bit of data. A low-to-high transition on the clock signal changes the output of the flipflop based on the value of the data input(s). This value is maintained until the next low-to-high transition of the clock, or until the flipflop is preset or cleared. Depending on the architecture of the device family, a register can be programmed as a level-sensitive flow-through latch or as an edge-triggered D, T, JK, or SR flipflop.

G

Graphic Design File (.gdf) A schematic design file created with the MAX+PLUS II Graphic Editor. The Quartus software can only read.gdf files.

global clear A signal from a dedicated input pin or logic element (LE) that does not pass through the logic array before arriving at the clear input of a register. In FLEX 8000 devices, a global clear can come from any of the dedicated inputs. In APEX 20K, FLEX 10K and FLEX 6000 devices, a global clear can come from any dedicated input or from an LE. MAX 9000, MAX 7000 and MAX 3000A devices have input pins that can be used either as global clear sources or as dedicated inputs to the device.

global clock A signal from a dedicated input pin or LE that does not pass through the logic array before arriving at the clock input of a register. In FLEX 8000 devices, a global clock can come from any of the four dedicated input pins. APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 3000A, MAX 5000, and EP1810 devices have input pins that can be used as either global clock sources or dedicated inputs to the device. EP910 and EP610 devices have dedicated clock input pins.

In FLEX 10K and FLEX 6000 devices, an LE can also generate a global clock signal.

H

Hexadecimal (Intel-Format) File (.hex) A hexadecimal file in the Intel Hex format. The Quartus and MAX+PLUS II Compilers and Simulators can use Hex Files as inputs to specify the initial memory contents. After compilation, you can also create Hex Files that support configuration schemes for APEX and FLEX devices.

I

internal timing parameters Worst-case delays based on external timing parameters. Internal timing parameters cannot be measured explicitly, and should only be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance. In this data book, internal timing parameters are shown in italic type.

I/O cell Also known as an I/O element. A register that exists on the periphery of an APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, or MAX 9000 device, or a fast input-type logic cell that is associated with an I/O pin in MAX 7000E, MAX 7000S, MAX 7000A, or MAX 3000A devices. I/O cells give short setup and clock-to-out times.

in-system programmability (ISP) The capability of EEPROM-based devices to be programmed after they have been mounted on a printed circuit board. Altera's MAX 9000, MAX 7000S, MAX 7000A, MAX 7000AE and MAX 3000A devices support ISP.

The Quartus and MAX+PLUS II Programmers support in-system programming via the BitBlaster serial, the ByteBlaster parallel port (the ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable), and

ByteBlasterMV parallel port download cable. The Programmer also provides the capability to program multiple devices in a JTAG chain.

J

Jam language An open-standard language for programming ISP-capable devices. The Jam™ language is supported by the Quartus software and MAX+PLUS II software versions 8.0 and higher. Jam is an interpreted language that is optimized for programming devices via the Joint Test Action Group (JTAG) interface. The Jam language is platform independent, supports both new and existing ISP-capable devices, and has a small interpreter code and file size.

Jam File (.jam) An ASCII Jam programming and test language file that stores programming data for programming, verifying, and blank-checking one or more ISP-capable devices in a JTAG chain. Jam Files are used in embedded processor or in-circuit test (ICT) equipment programming environments. Altera's APEX 20K, MAX 9000, MAX 7000S, MAX 7000A and MAX 7000AE devices can be programmed with Jam Files; APEX 20K and FLEX 10K devices can be configured with Jam Files. In addition to the device(s) to be programmed or configured, the JTAG chain can contain any device that complies with the IEEE Std. 1149.1 specification.

JEDEC File (.jed) An ASCII file that contains programming information. JEDEC Files provide an industry-standard format for transferring information between a data preparation system and a logic device programmer. The MAX+PLUS II Compiler automatically generates JEDEC Files for the following devices during compilation: EP610, EP610I, EP910, EP910I, and EP1810 devices (Classic family) as well as EPM5032 devices (MAX 5000 family). The MAX+PLUS II Programmer can use a JEDEC File created with the MAX+PLUS II software for DOS platforms, A+PLUS, or PLDshell Plus™ to program the Altera devices listed above, in addition to FLASHlogic devices (All FLASHLOGIC™ devices are obsolete). The Programmer can also optionally save programming data plus functional test vectors in JEDEC File format. The Quartus software does not support JEDEC files.

Ceramic J-lead chip carrier (JLCC) A device package offered by Altera. Both JLCC and plastic J-lead chip carrier (PLCC) packages are available. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

Joint Test Action Group (JTAG) A set of specifications that enables a designer to perform board- and device-level functional verification of a board during production.

JTAG boundary-scan testing Testing that isolates a device's internal circuitry from its I/O circuitry. This testing is made possible by the JTAG boundary-scan test (BST) architecture that is available in all APEX 20K, FLEX 10K devices, all FLEX 8000 devices except the EPF8452A and EPF81188A, and all FLEX 6000, MAX 9000, MAX 7000S, MAX 7000A and MAX 3000A devices. Serial data is shifted into boundary-scan cells in the device; observed data is shifted out and externally compared to expected results. Boundary-scan testing offers efficient PC board testing, providing an electronic substitute for the traditional "bed of nails" test fixtures.

L

library of parameterized modules (LPM) An architecture-independent library of logic functions that are parameterized to achieve scalability and adaptability. Altera has implemented parameterized modules from LPM version 2.0.1 to 2.1.0 that offer architecture-independent design entry for all Quartus and MAX+PLUS II-supported devices.

The Quartus and MAX+PLUS II compilers include built-in compilation support for LPM functions used in schematics, AHDL TDFs, and EDIF Input Files.

logic array A series of logic array blocks (LABs) that is used to implement general logic, such as counters, adders, state machines, and multiplexers. The logic array performs the same function as the sea-of-gates in gate arrays.

logic array block (LAB) A physically grouped set of logic resources in an Altera device. The LAB consists of a logic cell array and, in some device families, an expander product term array. Any signal that is available to any one logic cell in the LAB is available to the entire LAB. In APEX 20K, FLEX 10K, FLEX 8000, FLEX 6000, and MAX 9000 devices, the LAB is fed by FastTrack interconnect paths and a dedicated input bus. In MAX 7000, MAX 3000A and MAX 5000 devices, the LAB is fed by a programmable interconnect array (PIA) and a dedicated input bus. In Classic devices, the logic in the LAB shares a global clock signal. The LAB is fed by a global bus and a dedicated input bus. In the EP1810 devices, LABs are called quadrants.

logic cell The generic term for the basic building block of an Altera device. In APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 devices, logic cells are called logic elements. In MAX 9000, MAX 7000, MAX 3000A, MAX 5000, and Classic devices, logic cells are called macrocells.

logic element (LE) A basic building block of APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 devices. A logic element consists of a look-up table (LUT)—i.e., a function generator that quickly computes any function of four variables—and a programmable register to support sequential functions. The register can be programmed as a flow-through latch, as a D, T, JK, or SR flipflop, or bypassed entirely for pure combinatorial logic. The register can feed other logic cells or feed back to the logic cell itself. Some logic elements feed output or bidirectional I/O pins on the device.

Logic Programmer card The expansion card required to run the MAX+PLUS II Programmer and program Altera devices. The MAX+PLUS II software currently supports the LP6 Programmer card for use with PCs.

look-up table (LUT) A function that generates outputs based on inputs and a set of stored data. The logic element of FLEX 10K, FLEX 8000, and FLEX 6000 devices includes a four-input LUT that can be configured to emulate any logical function of four inputs.

M

macrocell The basic building block in Altera MAX 9000, MAX 7000, MAX 3000A, MAX 5000, and Classic devices. A macrocell consists of two parts: combinatorial logic and a configurable register. The combinatorial logic can implement a wide variety of logic functions. Depending on the architecture of the device family, the register can be programmed as a flow-through latch, as a D, T, JK, or SR flipflop, or bypassed entirely for pure combinatorial logic. The register can feed other macrocells or feed back to the macrocell itself. Some macrocells feed output or bidirectional I/O pins on the device. APEX 20K ESBs can also implement product term based macrocells. Macrocells in FLEX 10K, FLEX 8000, and FLEX 6000 devices are called logic elements.

macrofunction A high-level building block that can be used together with gate and flipflop primitives in MAX+PLUS II design files. In general, a macrofunction is a lower-level design file in a MAX+PLUS II hierarchical project.

MasterBlaster Communications Cable The MasterBlaster™ communications cable uses a PC serial or USB port hardware interface. This cable provides configuration data to

APEX 20K, FLEX 10K, FLEX 8000, and FLEX 6000 devices, as well as programming data to MAX 9000, MAX 7000S, MAX 7000A, and MAX 3000A devices. The MasterBlaster communications cable also supports in-circuit debugging with the SignalTap embedded logic analyzer in APEX 20K devices.

Master Programming Unit (MPU) A hardware module that works with zero-insertion-force sockets and individual adapters to program and test Altera devices. The PL-MPU base unit and PLM-prefix adapters support both device programming and device testing. The PLE3-12 base unit, as well as adapters with other prefixes, support device programming only.

MAX 3000A An Altera device family based on the Multiple Array MatriX (MAX) architecture. MAX 3000A devices offer up to six pin- or logic-driven output enable signals, fast input setup times to logic cells, and multiple global clocks with optional inversion. In addition, MAX 3000A devices feature ISP and JTAG boundary-scan test circuitry. The MAX 3000A devices are also optimized for MultiVolt operation. See the *MAX 3000AProgrammable Logic Device Family Data Sheet* for more information.

MAX 5000 An EPROM-based Altera device family based on the first generation of Multiple Array MatriX (MAX) architecture. See the *MAX 5000 Programmable Logic Device Family Data Sheet* for more information.

MAX 7000 An Altera device family based on the second generation of Multiple Array MatriX (MAX) architecture. MAX 7000A, MAX 7000S, and MAX 7000E devices are enhanced versions of MAX 7000 devices and are function-, pin-, and programming file-compatible with MAX 7000 devices. MAX 7000A, MAX 7000E, and MAX 7000S devices offer up to six pin- or logic-driven output enable signals, fast input setup times to logic cells, and multiple global clocks with optional inversion. In addition, MAX 7000S and MAX 7000A devices feature ISP and JTAG boundary-scan test circuitry. The MAX 7000A devices are also optimized for 3.3-V operation. See the *MAX 7000 Programmable Logic Device Family Data Sheet* for more information.

MAX 9000 An Altera device family based on the third generation of Multiple Array MatriX (MAX) architecture, with a higher density than the MAX 7000 device family. See the *MAX 9000 Programmable Logic Device Family Data Sheet* for more information.

MAX+PLUS II Altera's Multiple Array MatriX Programmable Logic User System. The MAX+PLUS II software is a set of computer programs and hardware support products that allow design and implementation of custom logic with FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, MAX 7000, MAX 3000A, MAX 5000, and Classic devices.

MegaCore function Altera-created megafunctions that are optimized for use with Altera devices. MegaCore™ functions are add-on products to the Quartus and MAX+PLUS II software.

megafunction An off-the-shelf building block that implements useful functions such as processors, digital signal processing (DSP) functions, bus controllers, and interfaces. Both MegaCore and AMPP megafunctions are available.

MegaLAB structure The APEX 20K device family uses the MegaLAB™ structure as the base for its MultiCore architecture. The MegaLAB structure is made up of a combination of ten logic elements (LEs). Each MegaLab structure contains 16 LABs and an advanced embedded structure called an embedded system block (ESB). The MultiCore architecture enhances the continuous metal FastTrack® Interconnect routing structure by introducing a fourth level to the routing

hierarchy. In addition to the global row and column interconnect, the MegaLAB interconnect connects all 16 LABs and the ESB within a MegaLAB structure without requiring global routing resources.

MultiCore architecture Altera's new MultiCore embedded architecture (featured in the APEX 20K device family) is made up of logic array blocks (LABs) and combines three different types of PLD structures: look-up tables (LUTs), product-term blocks, and enhanced embedded memory blocks. Together, these structures make the integration of complex functions, such as megafunctions, an easy and efficient process.

MultiVolt feature An interface that separates the power supply from the output voltage, enabling Altera devices powered at a specific core voltage level to interface with devices using different voltage levels. For example, Altera's FLEX 10KA family, which has the MultiVolt™ feature, supports 5.0-V, 3.3-V, and 2.5-V levels.

O

OptiFLEX architecture Highly efficient programmable logic architecture, used by the FLEX 6000 family. The OptiFLEX™ architecture is targeted at producing maximum performance and utilization in the smallest possible die area. See the *FLEX 6000 Programmable Logic Device Family Data Sheet* for more information.

P

parallel expander An expander product term that is "borrowed" from an adjacent logic cell in the same MAX 9000, MAX 7000 or MAX 3000A logic array block (LAB). A parallel expander is also a logic option that you can apply to a logic function to allow it to borrow such parallel expanders. This option can reduce the number of shared expander product terms required in your project and increase the speed of your project. However, the project may use additional logic cells, and may be more difficult to fit. Parallel expanders can also be borrowed among APEX 20K macrocells in the same ESB.

passive parallel asynchronous (PPA) A configuration scheme in which an external controller (e.g., a CPU) loads the design data into a FLEX 10K or FLEX 8000 device via a common data bus.

plastic dual in-line package (PDIP) A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

peripheral component interconnect (PCI) An industry-established, high-speed bus standard for 32- and 64-bit applications.

pin-grid array (PGA) A ceramic device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

plastic quad flat pack (PQFP) A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

PLAD3-12 An adapter that plugs into the Master Programming Unit (MPU). This adapter allows you to use PLE-prefix adapters originally designed for use with the PLE3-12A programming unit.

plastic J-lead chip carrier (PLCC) A device package option offered by Altera. Both ceramic J-lead chip carrier (JLCC) and PLCC packages are available. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

PLDshell Plus Altera's obsolete Programmable Logic Shell. The PLDshell Plus™ software is a set of computer programs for designing and

implementing custom logic circuits for Altera FLASHlogic and Classic devices. The MAX+PLUS II Programmer can program FLASHlogic and Classic devices with JEDEC Files (.**jed**) created by PLDshell Plus. All FLASHlogic devices are obsolete.

programmable interconnect array (PIA) The portion of a MAX 7000, MAX 3000A or MAX 5000 device that routes signals between different logic array blocks (LABs).

product term Two or more factors in a Boolean expression combined with an AND operator constitute a product term, where "product" means "logic product".

Programmer Object File (.pof) A binary file generated by the Quartus and MAX+PLUS II Compiler's Assembler module. This file contains the data used by the MAX+PLUS II Programmer to program an Altera device. The MAX+PLUS II Programmer has the option to save functional test vectors in a POF.

programmable logic devices (PLDs) Digital, user-configurable integrated circuits used to implement custom logic functions. PLDs can implement any Boolean expression or registered function with built-in logic structures.

programming file A file containing data for programming Altera devices. Both the MAX+PLUS II Compiler and Programmer can generate programming files. The following programming file formats are available.

Quartus: SRAM Object File (**.sof**), Programmer Object File (**.pof**), Jam File (**.jam**), JAM Byte-Code File (**.jbc**), Serial Vector Format File (**.svf**), Hexadecimal Output File (**.hexout**), Serial Bitstream File (**.sbf**), and Raw Binary File (**.rbf**).

MAX+PLUS II: FLEX Chain File (**.fcf**), Hexadecimal (Intel-Format) File (**.hex**), Jam File (**.jam**), JEDEC File (**.jed**), JTAG Chain File (**.jcf**), Programmer Object File (**.pof**), Raw Binary File (**.rbf**), Serial Bitstream File (**.sbf**), Serial Vector Format File (**.svf**), SRAM Object File (**.sof**), and Tabular Text File (**.ttf**).

FLEX Chain Files, JTAG Chain Files, Programmer Object Files, SRAM Object Files, and JEDEC Files are used to program or configure devices with the MAX+PLUS II Programmer. Test vectors for functional testing can be saved in POFs and JEDEC Files. All other file formats are used to configure FLEX 10K, FLEX 8000, and FLEX 6000 devices by other means. JTAG Chain Files are used to program or configure one or more FLEX 10K, MAX 9000, MAX 7000S, MAX 7000A or MAX 3000A devices in a multi-device JTAG chain. The Programmer can save data read from an examined device in POF or JEDEC File format.

Q

quad flat pack (QFP) A device package offered by Altera. Windowed ceramic QFP (CQFP), plastic QFP (PQFP), power QFP (RQFP), and plastic thin QFP (TQFP) packages are available. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

Quartus The Quartus™ software is Altera's fourth generation development system for programmable logic and allows designers to process multi-million gate designs for the APEX 20K device family. Features of the Quartus software include: work group computing, integrated logic analysis functionality, electronic design automation (EDA) tool integration, multi-processor support, incremental recompilation, and intellectual property (IP) integration.

R

register *See* flipflop.

Report File (.rpt) An ASCII text file, generated by the Quartus and MAX+PLUS II Compiler's Fitter module, that shows how device resources are used by the project. If a module preceding the Partitioner generates an error, this file is not generated. If the Partitioner generates an error, the Report File is generated in most cases.

power quad flat pack (RQFP) A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

S

security bit A bit that prevents an EPROM- or EEPROM-based Altera device from being interrogated. This bit also prevents EPROM-based Altera devices from being inadvertently reprogrammed. The security bit can be turned on or off for each device in a project, or for the entire project.

shared expanders and **shareable expanders** A feature of the MAX 9000, MAX 7000, MAX 3000A and MAX 5000 device architecture that allows logic cells to use uncommitted product terms within the same logic array block (LAB). A product term that is eligible to be shared in this manner is called a sharable expander; a product term that has been shared in this manner is called a shared expander. The MAX+PLUS II Compiler automatically allocates shareable expanders when a project is compiled. A shared expander also can be allocated with an EXP primitive.

SignalTap SignalTap™ is Altera's new logic analysis solution that works with the Quartus software. SignalTap reduces verification times by allowing engineers to conduct APEX 20K verification via internal signal values. The SignalTap solution consists of the SignalTap megafunction, a JTAG communications cable, and the Quartus waveform editor software.

small-outline integrated circuit (SOIC) A device package option offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

static random access memory (SRAM) A read-write memory that stores data in integrated flipflops. See the *Configuration Elements Data Sheet* for more information.

SRAM Object File (.sof) A binary file generated by the MAX+PLUS II Compiler's Assembler module that contains the data for configuring Altera FLEX 10K, FLEX 8000, or FLEX 6000 devices.

T

Tabular Text File (.ttf) A MAX+PLUS II supported ASCII text file in tabular format containing configuration data for the sequential passive parallel synchronous (PPS), passive parallel asynchronous (PPA), and passive serial (PS) configuration schemes for FLEX 8000 devices, and the PS configuration scheme for FLEX 10K devices.

Text Design File (.tdf) An ASCII text file written in AHDL format. Text Design Export Files (**.tdx**) and Text Design Output Files (**.tdo**) can be saved as TDFs and compiled with the Quartus and MAX+PLUS II software.

Text Design Output File (.tdo) An ASCII text file in AHDL format that is optionally generated when you compile any design. It contains a cell-by-cell description of the design as by the MAX+PLUS II software.

timing simulation A MAX+PLUS II Simulator mode that uses a timing Simulator Netlist File (**.snf**) to simulate the logical and timing performance of a project. Because the timing SNF is generated after logic synthesis, partitioning, and fitting are performed,

timing simulation allows you to simulate only the nodes in a project that have not been removed by logic optimization.

thin quad flat pack (TQFP) A device package offered by Altera. See the *Altera Device Package Information Data Sheet* and *Ordering Information* for more information.

Turbo Bit A control bit for choosing the speed and power characteristics of an Altera device. If the Turbo Bit™ feature is on, the speed increases; if it is off, the power consumption decreases. The Turbo Bit feature can be turned on or off in a design file or in the Compiler.

U

user I/O The total number of I/O pins and dedicated inputs on a device.

V

Verilog HDL A hardware description language (HDL) from Cadence. You can create a Verilog HDL description with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with the MAX+PLUS II software. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a Verilog HDL design that has been processed with a Verilog HDL synthesis tool. The netlist file can then be imported into the MAX+PLUS II software as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a Verilog Output File (**.vo**).

Verilog Output File (.vo) A Verilog HDL standard netlist file generated by the Verilog Netlist Writer module of the Compiler. A Verilog Output File contains functional and timing information for simulation with a standard Verilog HDL simulator.

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language. You can create a VHDL Design File (**.vhd**) with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with the MAX+PLUS II software. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a VHDL design that has been processed with a VHDL synthesis tool. The netlist file can then be imported into the MAX+PLUS II software as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a VHDL Output File (**.vho**).

VHDL Design File (.vhd) An ASCII text file created with the MAX+PLUS II Text Editor or another standard text editor. The VHDL Design File contains design logic that is defined with VHDL.

VHDL Output File (.vho) A VHDL standard netlist file that is generated by the VHDL Netlist Writer module of the Compiler. A VHDL Output File contains functional and timing information for simulation with a standard VHDL simulator.