PCI Bus Master/Target MegaCore Function

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Target Application:
Bus Interface

Family:
FLEX 10K

Vendor:

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Features

- Optimized for the Altera® FLEX® 10K EPF10K30RC240-3 device
- Includes a 32-bit peripheral component interconnect (PCI) bus that can support 33-MHz operation
- Supports zero-wait state burst mode

General Description

The PCI bus master/target (`pci_a`) MegaCore™ function offers the flexibility and high performance of programmable logic device (PLD) implementation and the board space benefits of single-chip integration. The function can perform a zero-wait state PCI read at a throughput rate of 107 Mbytes/second and a zero-wait state PCI write at a throughput rate of 102 Mbytes/second. The function can be easily "dropped in" to a design so that a designer can quickly implement an entire PCI design onto a single PLD.

The `pci_a` MegaCore function is optimized for the EPF10K30RC240-3 device. Since the function takes up less than 50% of the usable gates on the EPF10K30RC240-3 device, there is ample room for the user to implement custom logic for single-chip integration of an entire PCI design.

A PCI prototype board is also available with the function for implementing and testing PCI designs. The PCI prototype board contains an EPF10K30RC240-3 device, which can be configured with a PCI design. The board provides a connector socket for the PCI bus interface and other sockets for accessing the EPF10K30RC240-3 device I/O pins. The board also has 256 Kbytes of SRAM for the target address space and a VGA interface that displays the function.

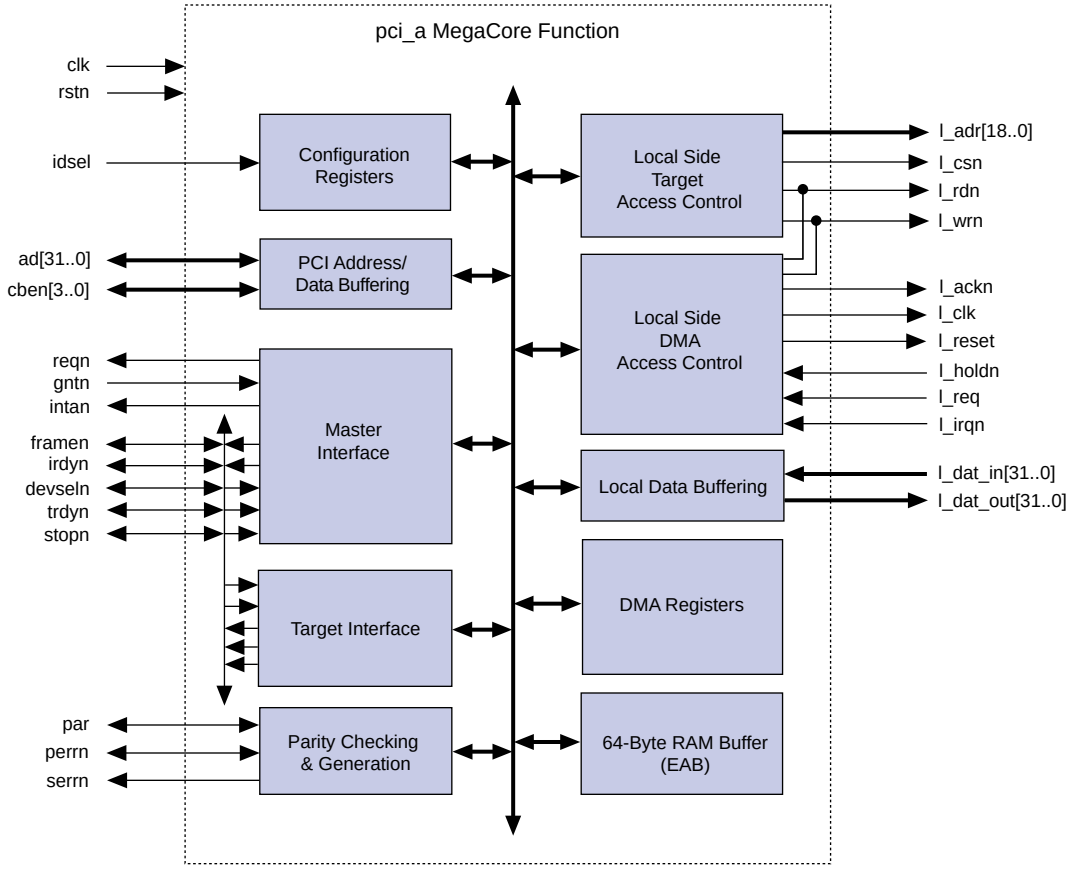
Functional Description

The `pci_a` MegaCore function has the following functional components:

- PCI bus master/target interface
  - Master functions
    - 512 Kbyte address space
    - PCI single cycle read and write
    - PCI burst read and write
  - Target functions
    - Header type 0 configuration
    - PCI target read and write
    - Parity generation and parity error detection
    - Disconnect, retry, and abort functions
- Embedded DMA control engine with an internal 64-byte RAM buffer
- 32-bit customer logic support interface
- PCI configuration registers

Figure 1 shows a block diagram of the `pci_a` MegaCore function.

Figure 1. pci_a MegaCore Function Block Diagram



The pci_a MegaCore function contains a DMA control engine that supports burst read and write data transfers. To transfer data on the PCI bus, the system software loads the internal DMA registers. The function is then ready to accept the local DMA request signal that enables the master to initiate data transfers on the bus.

For example, in a burst read, the master stores the read information in the RAM buffer from the PCI bus. After the burst transaction is completed, the pci_a MegaCore function indicates to the local side that it will transfer data from the RAM buffer to the local side memory. Similarly, in a burst write, the function indicates to the local side that it is ready to transfer data from the local side to the RAM buffer. When the RAM buffer is full, or the pci_a MegaCore function has the last data word, the function requests access to the PCI bus. After the arbiter grants the function access, the function will transfer all data from the RAM buffer to the PCI bus.

In the pci_a MegaCore function, the target capability is used for single data phase accesses. Target accesses are typically used for accessing the configuration registers, internal DMA registers, and external target memory space.

For additional information on the pci_a MegaCore function, refer to the *PCI Master/Target MegaCore Function with DMA Data Sheet*.

OpenCore Evaluation

The designer can evaluate the pci_a MegaCore function before purchase by using the OpenCore™ feature that is provided with the MAX+PLUS® II development software. This pre-purchase evaluation system allows designers to instantiate and simulate the pci_a MegaCore function.

Performance & Implementation

The pci_a MegaCore function offers high data bandwidth and zero-wait state burst data transfers. It also supports a 256-byte, header type-0 configuration. Table 1 shows the key performance characteristics for the pci_a MegaCore function.

Table 1. pci_a MegaCore Function Performance Characteristics

Characteristic	Values
Clock rate	33 MHz
Read data burst transfer rate	107 Mbytes/second
Write data burst transfer rate	102 Mbytes/second

The pci_a MegaCore function uses less than 50% of the logic elements (LEs) available in an EPF10K30RC240-3 device. The remaining logic elements (LEs) can be used for user-defined local-side customization. Table 2 shows the typical device utilization for the pci_a MegaCore function in the EPF10K30RC240-3 device with 1,728 LEs available.

Table 2. Typical Device Utilization

Function	LEs
pci_a MegaCore function (includes a complete DMA circuit)	850
Local side with custom logic	878

Compliance

Table 3 describes timing elements for the EPF10K30RC240-3 device that are compliant with the PCI Special Interest Group's (PCI-SIG) ***PCI Local Bus Specification***, revision 2.1.

Table 3. Timing Elements for the EPF10K30RC240-3 Device

Timing Element	Specification
Clock-to-output time	11 ns
Set-up time	7 ns
Maximum clock rate	33 MHz

Reference

PCI Special Interest Group. ***PCI Local Bus Specification***. Rev. 2.1. Hillsboro, Oregon: PCI Special Interest Group, 1995.

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