Viterbi Decoder Megafunction

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Target Applications:
Data Communications
Telecommunications

Family:
FLEX® 10K & FLEX 6000

Vendor:

CAST, Inc.
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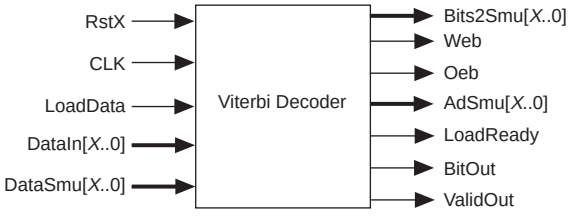
Features

- Hard decision decoder
- Trace-back method for survivor memory
- Branch metric computations can be added for different applications
- Developed in VHDL and synthesized to approximately 950 logic elements (LEs)
- Parameterized architecture allows users to customize the following functions:
  - Number of states in the trellis
  - Number of bits to represent transition values
  - Number of Add-Compare-Select (ACS) cells
  - Length of the trace-back
  - Length of the received burst transaction
  - Initial path metric for state 0
  - Survivor memory (RAM) word length

General Description

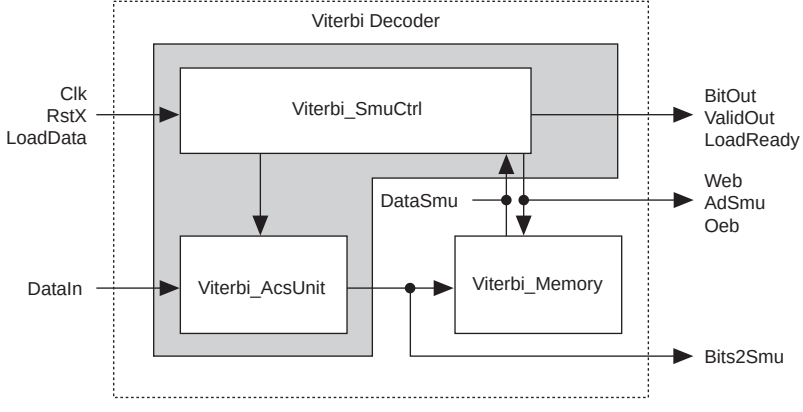
The Viterbi decoder megafunction is used to decode convolutional codes. It can also be used to produce the best estimate of a transmitted sequence over a channel with inter-symbol interference (ISI). Figure 1 shows the symbol for the Viterbi decoder megafunction.

Figure 1. Viterbi Decoder Symbol



The megafunction is available as an encrypted file or as VHDL source code. The VHDL source code is parameterizable, and it can be easily adapted to a wide variety of applications. Figure 2 shows the block diagram for the Viterbi decoder megafunction.

Figure 2. Viterbi Decoder Block Diagram



Functional Description

The Viterbi decoder megafunction is partitioned into three modules: Viterbi_AcsUnit, Viterbi_SmuCtrl, and Viterbi_Memory.

Viterbi_AcsUnit Module

The Viterbi_AcsUnit module calculates the path metrics to find the minimum path. The number of ACS units is parameterizable.

Viterbi_SmuCtrl Module

The Viterbi_SmuCtrl module manages the survivor memory. The state machine controls the alternate reading of new branch metrics and the trace-back. During trace-back, the megafunction reads the decision values from memory and outputs the decoded bits. The megafunction reconstructs the encoder's actions in reverse order by updating the state register with a decision value pointed by the former state value. As a result, the decoded bits are also output in reverse order.

Viterbi_Memory Module

The Viterbi_Memory module is an optional RAM memory that stores the trace-back values during calculation.

Ports

Table 1 describes the Viterbi decoder megafunction ports.

Table 1. Viterbi Decoder Megafunction Ports

Name	Type	Description
RstX	Input	Asynchronous reset (active low)
Clk	Input	Common clock
LoadData	Input	Enables data loading
DataIn[*x*..0]	Input	Transition values input; the width depends on the number of ACS units
DataSmu[*x*..0]	Input	Input data from external memory
Bits2Smu[*x*..0]	Output	Output data to external memory
Web	Output	Write enable to external memory
Oeb	Output	Read enable to external memory
AdSmu[*x*..0]	Output	Address to external memory
LoadReady	Output	Indicates read for data
BitOut	Output	Decoded output bit
ValidOut	Output	Indicates the valid output data

Verification Methods

The megafunction has been extensively tested using various parameter settings. A special encoder circuit is used as a testbench for full testing.

Ordering Information

The Viterbi decoder megafunction can be purchased directly from CAST, Inc. For an Altera Hardware Description Language (AHDL) netlist format, designers must supply parameter settings to CAST, who will create the netlist file. Contact CAST for more information.

Modifiable Parameters

CAST, Inc. can customize the megafunction with the parameters shown in Table 2.

Table 2. Modifiable Parameters

Parameter	Description
N	Number of states in trellis
NB	Number of bits to represent transition values
ACS	Number of ACS cells
LTB	Length of the trace-back
LRB	Length of the received burst
IP	Initial path metric for state 0
MWL	Survivor memory (RAM) word length

Utilization

Table 3 lists the typical device utilization results for the megafunction.

Table 3. Typical Device Utilization for the Viterbi Decoder Megafunction

Device	Speed Grade	Utilization		Performance (f_{MAX})	Parameter Settings
		LEs	EABs		
EPF6016	-2	954	–	17 MHz	N = 16, NB = 8, ACS = 4, LTB = 30, LRB = 5, IP = –4, MWL = 8
EPF10K30A	-1	960	0	31 MHz	

Deliverables

The following files are provided with the encrypted license:

- Post-synthesis AHDL netlist file
- Assignment & Configuration File (**.acf**)
- Symbol File (**.sym**)
- Include File (**.inc**)
- Graphic Design File (**.gdf**) of test circuit
- Vectors for testing the functionality of the megafunction

The following files are provided with the VHDL source license:

- VHDL RTL source code
- Testbench
- Example testbench wrapper for post-route simulation
- Vectors for testbench
- Simulation script
- Synthesis script
- Expected results for testbench

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