

# IEEE 1394-Compatible LLC-I Megafunction

Solution Brief 36

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## Target Applications:

Bus & Interfaces  
Processors & Peripherals  
Telecommunications & Data  
Communications

## Family:

FLEX<sup>®</sup> 10K



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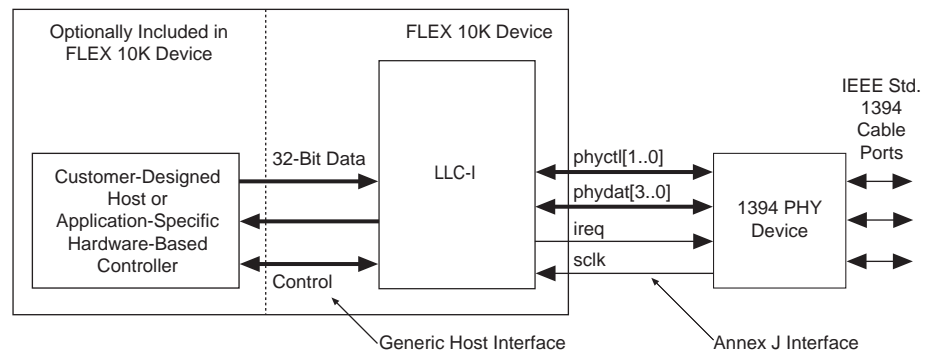
## Features

- Conforms to IEEE Std. 1394-1995 standards for cable environments
- Supports IEEE Std. 1394a, which has been submitted for approval
- Generic 32-bit host bus interface
- Optional asynchronous host clock/cable clock
- Supports IEEE Std. 1394 Annex-J physical interface

## General Description

The IEEE 1394-compatible link layer controller (LLC-I) megafunction provides IEEE Std. 1394 asynchronous packet link layer support between a controller implementing the IEEE Std. 1394 transaction layer and an external device implementing the IEEE Std. 1394 physical layer. Figure 1 shows the block diagram for the IEEE 1394-compatible LLC-I megafunction.

Figure 1. IEEE 1394-Compatible LLC-I Megafunction Block Diagram



## Functional Description

The IEEE 1394-compatible LLC-I megafunction is controlled through a 32-bit host bus interface by either a hardware-based controller or a firmware-based processor. The megafunction handles IEEE Std. 1394 link layer functions, which includes formatting packets for asynchronous write/lock operations and checking packets for asynchronous read/lock operations. The megafunction manages the Annex J interface to an external IEEE Std. 1394 physical layer device. These tasks include bus arbitration management and transfer-rate dependent data serialization.

### Ports

Table 1 describes the ports for the IEEE 1394-compatible LLC-I megafunction.

Table 1. IEEE 1394-Compatible LLC-I Megafunction Ports (Part 1 of 2)		
Name	Type	Description
hclk	Input	Host clock interface
din[31..0]	Input	Data in bus
txvld#	Input	Data in valid

Name	Type	Description
txlast	Input	Data in last word
rxrdy#	Input	Data out accepted
addr[7..0]	Input	Register address bus
regwr	Input	Register write enable
regrd	Input	Register read enable
rst#	Input	Asynchronous reset
sclk	Input	IEEE Std. 1394 Annex J interface clock
int#	Output	Host interrupt (to host/controller)
txrdy#	Output	Data in
dout[31..0]	Output	Data out bus
rxvld#	Output	Data out valid
rxlast	Output	Data out last word
ireq	Output	Link layer request
phyct[1..0]	Bidirectional	IEEE Std. 1394 Annex J control bus
phydat[3..0]	Bidirectional	IEEE Std. 1394 Annex J data bus

## Utilization

Table 2 describes the logic cell requirements for the IEEE Std. 1394-compatible LLC-I megafunction.

Device	Speed Grade	Utilization		f <sub>MAX</sub> (MHz) <i>Note (2)</i>	Availability
		Logic Cells	EABs (1)		
EPF10K100A	-1	3,352	5	24.576	Now

### Notes:

- (1) EAB = embedded array block.
- (2) Data on the Annex J interface is clocked at 49.152 MHz.

## Applications

The IEEE Std. 1394-compatible LLC-I megafunction is ideal for embedded applications that require an IEEE Std. 1394 interface. These applications include printers, scanners, modems, and home entertainment devices. The megafunction is also appropriate for custom applications, such as remote data acquisition, that require high bandwidth communication through the IEEE Std. 1394 interface.

## Deliverables

The IEEE 1394-compatible LLC-I megafunction is available in synthesizable register transfer language (RTL), Verilog HDL, and as a synthesized Altera Hardware Description Language (AHDL) netlist file.



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