64-Bit PCI Bus Target Megafunction

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Target Applications:
Bus Interfaces
Bus Migration
Digital Signal Processing (DSP)
High-Speed Communications

Family:
FLEX 10K & FLEX 6000

Vendor:

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Features

- 64-bit, 33-MHz peripheral component interconnect (PCI) function
- Fully compliant with PCI Special Interest Group (PCI-SIG) ***PCI Local Bus Specification, Revision 2.1***
- Optimized for the Altera® FLEX® 10K and FLEX 6000 device architectures
- Fully synchronous design
- Does not contain pre-routed or pre-placed logic
- Supports full-speed burst up to 266 Mbytes per second
- Provides zero-wait state data transfers
- Medium-speed decoder
- Fully customizable megafunction
- 3 to 5 minute compilation time

General Description

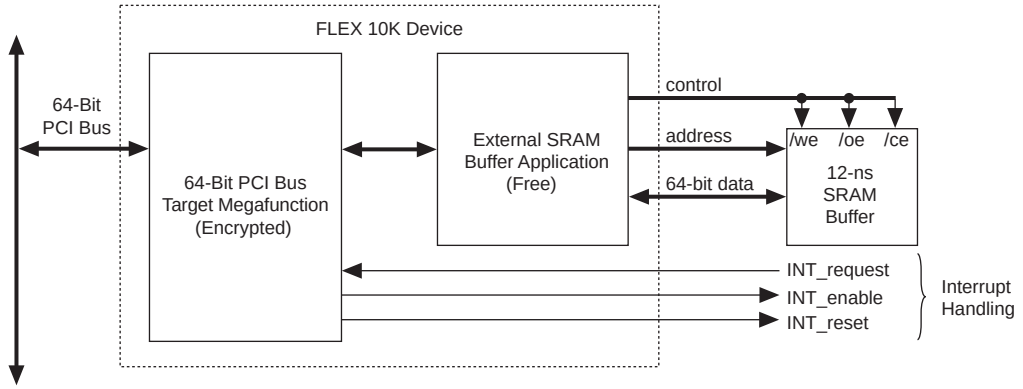
The 64-bit PCI bus target megafunction is a 64-bit, 33-MHz PCI bus interface that is used for high-speed data transfer applications capable of supporting burst transfers up to 266 Mbytes per second.

Functional Description

The 64-bit PCI bus target megafunction provides a simple and flexible interface between the PCI bus and a user-developed back-end design. The megafunction interfaces with external user applications through an internal back-end design, which users can build from the device's free resources. The megafunction comes with Altera Hardware Description Language (AHDL) and VHDL back-end reference designs that designers can customize for their projects.

Figure 1 shows the block diagram of a sample FLEX 10K internal back-end application. In this sample, the external SRAM buffer application interfaces the megafunction to a 12-ns SRAM buffer via a 64-bit data path. The internal back-end design has exclusive access to the 12-ns SRAM buffer; however, designers can easily implement a non-exclusive access by adding a synchronization mechanism.

Figure 1. Sample Internal Back-End Application Block Diagram



Ports

The megafunction provides a reduced local-side interface that is easy to use. Table 1 describes the local-side ports for the 64-bit PCI bus target megafunction.

Table 1. Local-Side Ports for the 64-Bit PCI Bus Target Megafunction

Name	Type	Description
INT_request	Input	Local interrupt request
data_in[63..0]	Input	Local data input bus
S_disco	Input	Local disconnect request
S_ws	Input	Local wait-state request
Com_reg_in[*m*..0]	Input	Local configurable input port register
64bit_enable	Input	Local 64-bit transfer enable
SM_out[6..0]	Output	PCI megafunction state machine bus
PCI_RWn	Output	Target transaction direction
RST_hard	Output	Local reset
INT_reset	Output	Interrupt reset
INT_enable	Output	Interrupt enable
data_out[63..0]	Output	Multiplexed address/data output bus
S_data_valid	Output	Data valid signal
M_data_valid	Output	Data valid signal
Com_reg_out[*n*..0]	Output	Configurable output port register
S_64bit	Output	Nature of transfer (i.e., 32 or 64 bits)

Modifiable Parameters

Designers can customize the 64-bit PCI bus target megafunction with the parameters shown in Table 2.

Table 2. Modifiable Parameters

Parameter	Description
VENDOR_ID	Vendor identifier
DEVICE_ID	Device identifier
REVISION_ID	Revision number
CLASS_CODE	Class code identifier
PREFETCH	Memory attributes
SERR_ENABLE	SERR# control
SPACE_TYPE	Device memory space type (I/O or MEM)
SPACE_SIZE	Device memory space size
MEM_LOCATE	Device memory space location
COM_IN	User-configurable input port size
COM_OUT	User-configurable output port size

Utilization

Table 3 describes the logic cell requirements for the 64-bit PCI bus target megafunction.

Table 3. 64-Bit PCI Bus Target Megafunction Logic Cell Requirements

Device	Speed Grade	Utilization		f_{MAX} (MHz)	Implementation
		Logic Cells	EABs *(1)*		
EPF10K50V	-1	440/2,280	0/10	63	Megafunction only
EPF10K30	-3	440/1,728	0/6	39	Megafunction only
	-1	440/1,728	0/6	98	Megafunction only
EPF10K20	-3	440/1,152	0/6	49	Megafunction only
EPF6016	-2	440/1,320	–	49	Megafunction only
		530/1,320	–	49	Megafunction with external SRAM support

Note:
(1) EABs = embedded array blocks.

Deliverables

The 64-bit PCI bus target megafunction includes the following items:

- 64-bit PCI bus target megafunction license
- Encrypted Text Design File (**.tdf**) netlist
- Symbol File (**.sym**)
- Top-level Assignment & Configuration File (**.acf**)
- Simulator Channel File (**.scf**)
- User guide
- Installation guide

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