I²C Master Interface Megafunction

Solution Brief 39 **June 1999, ver. 1**

Target Applications:
Bus & Interfaces
Processor & Peripherals

Family:
FLEX® 10K & FLEX 6000

Vendor:

SICAN Microelectronics Corp.
400 Oyster Point Blvd. Suite 512
S. San Francisco, CA 94080
http://www.sican.com
Tel. (650) 871-1494
Fax (650) 871-1504

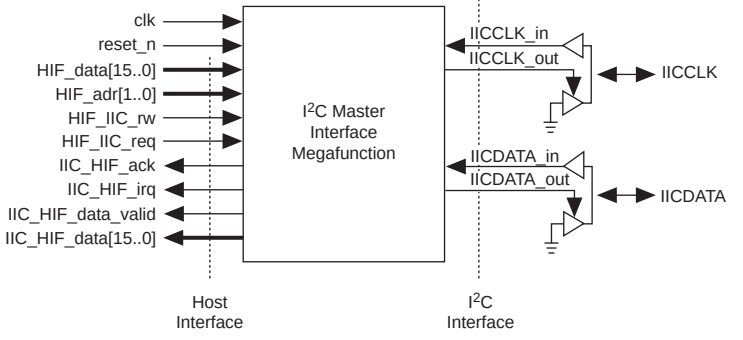
Features

- Supports system clocks up to 50 MHz
- Supports inter integrated circuit (I²C) fast mode up to 400 kHz
- Reads and writes data bursts
- Supports special mode for I²C read and write access to a dedicated register address
- Generates wait states
- Filters spikes on the I²C bus
- Fully synchronous design

General Description

The I²C master interface megafunction interfaces a host CPU with an I²C bus. This megafunction is essentially a parallel-to-serial/serial-to-parallel converter, converting a host CPU's parallel data into serial format for transfer over the I²C bus, and vice versa. Thus, a host CPU can control other devices on the same I²C bus. The I²C master interface megafunction also takes care of all interface timing, data structure, and error handling. Figure 1 shows the symbol for the I²C master interface megafunction.

Figure 1. I²C Master Interface Megafunction Symbol



Functional Description

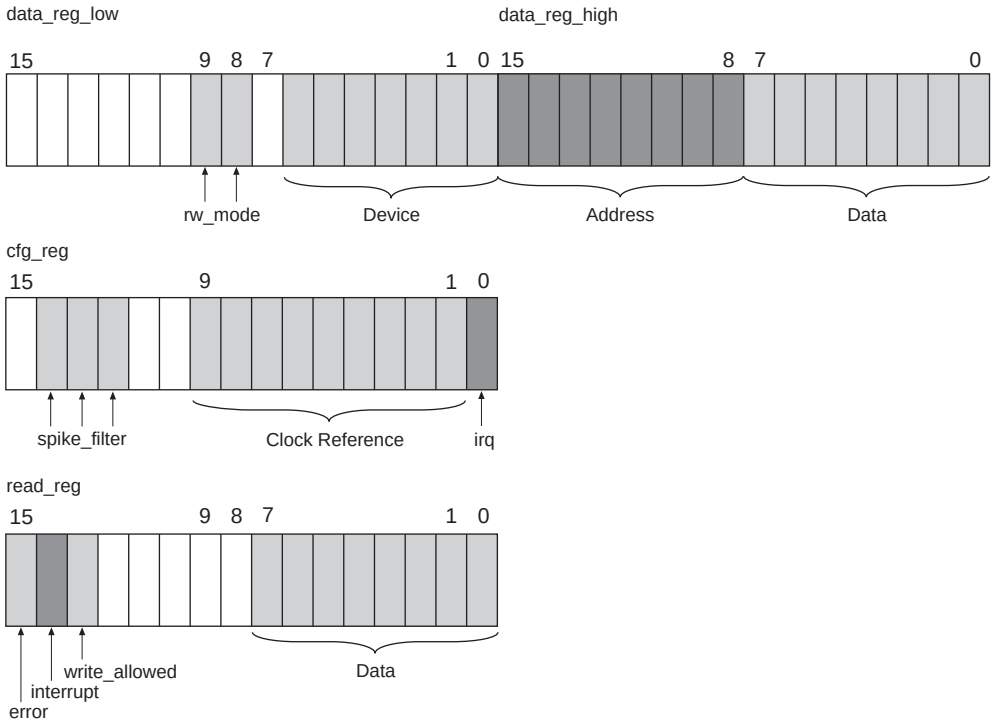
The I²C master interface megafunction includes three registers for communication between the host CPU and the I²C bus. See Table 1.

Table 1. I²C Master Interface Registers

Register Name	Width (Bits)	Address	Mode
data_reg	32	0 × 0 and 0 × 1	Write
cfg_reg	16	0 × 2	Write
read_reg	16	0 × 3	Read

The data_reg register is a 32-bit writeable data register consisting of two 16-bit registers, data_reg_high[31..16] and data_reg_low[15..0]. These two registers handle the 16-bit data bus of the host CPU. Figure 2 shows the information stored in all megafunction registers.

Figure 2. I2C Master Interface Registers



All writeable registers (i.e., `data_reg_high[31..16]`, `data_reg_low[15..0]`, and `cfg_reg`) must be loaded to initialize the I2C master interface megafunction. When `data_reg_low[15..0]` is loaded, data begins transferring on the I2C bus. During the direct read and direct write modes, a new data packet begins transfer when both the `read_reg` and `data_reg_low[15..0]` registers are accessed. The direct read or direct write mode stops when the `data_reg_high[31..16]` or `cfg_reg` register is accessed.

The megafunction monitors the status of the `IICCLK_in` and `IICCLK_out` signals; if a component on the I2C bus holds `IICCLK` low, the megafunction stays in a wait state.

For noisy environments, you can apply a spike filter, stored in the `cfg_reg` register, to the incoming I2C data and clock signals. The spike filter evaluates the signals for a programmed number of clock cycles (up to a maximum of eight clock cycles). During this time, the spike filter removes any spikes in the signals.

The I2C master interface megafunction supports four operating modes. See Table 2.

Table 2. I2C Master Interface Operating Modes

Mode	Description
Direct write	Writes a burst of data.
Direct read	Reads a burst of data.
Random access write	Writes one data byte to a specified address.
Random access read	Reads one data byte from a specified address.

Tables 3, 4, and 5 describe the megafunction's global signals, interface signals to the host CPU, and interface signals to the I²C bus, respectively.

Table 3. I²C Master Interface Megafunction Global Signals

Name	Type	Description
clk	Input	Device clock signals.
reset_n	Input	Low active asynchronous reset signal.

Table 4. Interface Signals to the Host CPU

Name	Type	Description
HIF_data[15..0]	Input	16-bit data bus from the host CPU.
HIF_adr[1..0]	Input	2-bit address bus for addressing internal registers.
HIF_IIC_rw	Input	Read/write select. A 0 indicates a write, and a 1 indicates a read.
HOST_IIC_req	Input	Request. Host CPU requests the next read/write data.
IIC_HIF_ack	Output	Acknowledge. The megafunction acknowledges a read/write request.
IIC_HIF_irq	Output	Interrupt. Data must be read from the megafunction's data register.
IIC_HIF_data_valid	Output	Data valid on the bus.
IIC_HIF_data[15..0]	Output	16-bit data bus to the host CPU.

Table 5. Interface Signals to the I²C Bus

Name	Type	Description
IICCLK_in	Input	Clock input to the megafunction.
IICDATA_in	Input	Data input to the megafunction.
IICCLK_out	Output	Clock output for the megafunction.
IICDATA_out	Output	Data output for the megafunction.

Performance

Table 6 describes the megafunction's logic element (LE) requirements for FLEX 10K and FLEX 6000 devices.

Table 6. I²C Master Interface Megafunction LE Requirements

Device	Speed Grade	Utilization		Performance (MHz)
		LEs	EABs *(1)*	
EPF10K10	-3	309	0	34
	-4	309	0	28
EPF10K10A	-1	313	0	47
	-2	313	0	39
	-3	313	0	29
EPF10K30E	-1	313	0	53
EPF10K50E	-1	313	0	49
	-2	313	0	40
	-3	313	0	31
EPF10K100B	-1	313	0	45
	-2	313	0	40
EPF10K200E	-1	313	0	41
EPF10K250A	-1	313	0	34
	-2	313	0	29
EPF6010A	-1	356	–	27
	-2	356	–	23
	-3	356	–	19
EPF6016	-2	356	–	20
EPF6016A	-1	356	–	28
	-2	356	–	24
EPF6024A	-1	356	–	27
	-2	356	–	24
	-3	356	–	19

Note:
(1) EABs = embedded array blocks.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com