Development Tools Selector Guide

June 2000

Introducing Altera Programmable Logic Development Tools

Altera offers the fastest, most powerful, and most flexible programmable logic development software and programming hardware in the industry. The Altera® Quartus™ and MAX+PLUS® II development tools provide a broad range of features with an easy-to-use graphical user interface. In addition, they offer interfaces to industry-standard EDA tools that allow easy integration with your chosen design environment. Altera development tools include the following features:

- Support for all Altera programmable logic devices (PLDs), including APEX™, ACEX™, FLEX®, and MAX® architectures.
- Multi-platform support, including Windows 98/NT for PCs (Windows 2000 support available 2H'00), as well as Sun SPARCstation, and HP 9000 Series 700/800.
- Support for hardware description languages, including the VHDL 1987 and 1993 standards, Verilog HDL, and the Altera Hardware Description Language (AHDL).
- Interfaces to EDA tools that utilize EDIF 2 0 0 and 3 0 0 netlists, the library of parameterized modules (LPM), Standard Delay Format (SDF) files, VHDL, and Verilog HDL.

World-Class Synthesis and Simulation

Altera has entered into agreements with Mentor Graphics and Synopsys to provide world-class HDL synthesis and simulation products. Altera-specific versions of Synopsys FPGA *Express*, Exemplar Logic LeonardoSpectrum, and Model Technology ModelSim synthesis and simulation tools are now included with all subscriptions.

Using This Guide

This Development Tools Selector Guide will help you choose the Altera design environment that best meets your needs. Creating your Altera design environment consists of three simple steps:

- Step 1 – Select a subscription product
- Step 2 – Add megafunction IP products
- Step 3 – Select appropriate programming hardware

At the end of this guide, you will find a list of recommended system configurations for all platforms supported by the Quartus and MAX+PLUS II software, as well as descriptions of Altera's Commitment to Cooperative Engineering Solutions (ACCESS℠) program, and the Altera Consultants Alliance Program (ACAP®).

Step 1 — Select a Subscription Product

Your Altera design environment begins when you register for the Altera Development Tools Subscription Program. As a subscriber, you will receive complete access to all Altera development tools and updates for a 12-month period. You will also receive Synopsys FPGA *Express* synthesis software supporting VHDL and Verilog HDL synthesis, Exemplar Logic LeonardoSpectrum software supporting either VHDL **or** Verilog HDL synthesis, and Model Technology ModelSim HDL simulator software supporting either VHDL **or** Verilog HDL simulation and test benches. Once your 12-month subscription expires, your current Altera software will continue to work, but you will not receive the updated and new features that come in subsequent releases of the software. *Licensing policies for the third-party synthesis and simulation products included with subscriptions are set by the third-party companies and may differ.* Your subscription includes:

- The most current, full-featured versions of the Altera Quartus and MAX+PLUS II software
- Altera-specific versions of the FPGA *Express* software supporting VHDL and Verilog synthesis, LeonardoSpectrum software supporting VHDL **or** Verilog synthesis, and ModelSim software supporting VHDL **or** Verilog HDL simulation
- All software updates as they are released during the 12-month subscription period
- Support for the latest Altera devices
- New software features
- Performance enhancements
- The most current on-line and printed documentation

Ordering Your Subscription

Altera offers flexible licensing models to easily fit into your design environment. To join Altera's subscription program, choose the appropriate product based on your system configuration environment as shown in Table 1. The FPGA *Express* software is available for the PC platform only. All other software is available for both PC and UNIX platforms.

Table 1. Altera Subscription Products

PRODUCT	DESCRIPTION OF COVERAGE
FIXEDPC	Stand-alone, single-user license for PC users
FLOATPC	Multiple-user network licensing for PC clients only
ADD-FLOATPC	Add additional PC-client seats to run off the FLOATPC server
FLOATNET	Multiple-user network licensing for PC, UNIX, or PC/UNIX clients
ADD-FLOATNET	Add additional PC or UNIX seats to run off the FLOATNET server

Device Architecture Support

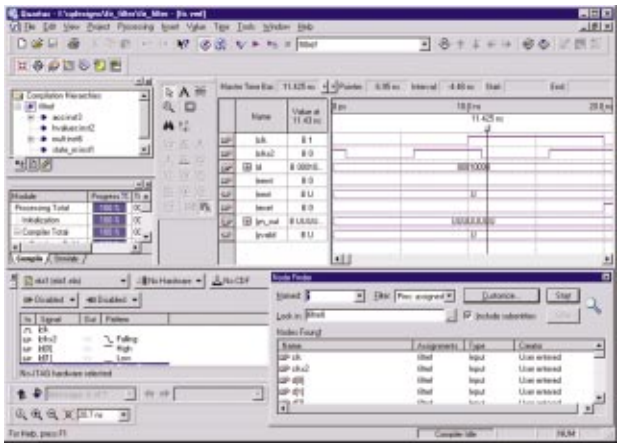
Your subscription provides you with support for all the Altera device architectures, including those shown in Table 2. For more information on Altera devices, refer to the Altera *Component Selector Guide*, the current Altera *Device Data Book*, or the Altera web site at **http://www.altera.com**.

Quartus Development Software

The Quartus software—Altera's fourth-generation development system for programmable logic—offers state-of-the-art features to shorten design cycles and increase designer productivity.

- System-on-a-programmable-chip methodology with block-level editing, workgroup computing, and expanded support for megafunctions streamlines the development flow and increases productivity.
- Enhanced Timing Analyzer performs multiple clock frequency analysis and accommodates designs with multicycle paths.
- SignalTap™ logic analysis tool reduces verification time by enabling engineers to see internal chip signal values while the system is running at speed.
- NativeLink™ integration provides seamless interfaces with third-party EDA software, allowing designers to synthesize and validate designs for Altera devices with familiar, easy-to-use tools.
- An unmatched level of technical support—including access to Altera's on-line solutions database from within Quartus—makes Altera effectively a member of the design team.
- Support for the APEX architecture, which offers high-performance, system-on-a-programmable-chip solutions, and support for enhanced features such as content-addressable memory (CAM), advanced I/O standards including LVDS, and phase-locked-loops (PLLs).

Altera Quartus Development Software



CoreSyn Synthesis

The Quartus Compiler uses Altera's CoreSyn™ synthesis capability to allow designers to guide the implementation of their designs. Designers can instruct the Compiler to partition functions into the appropriate type of look-up-table (LUT)-based logic element, product-term-based macrocell, or embedded memory logic block within the device architecture. This high level of control allows the designer to achieve optimal results.

Improved Verification Flow and SignalTap Logic Analysis

The Quartus software reduces verification time by providing a full-featured timing simulator and a native register transfer level (RTL)-based simulator. Quartus also provides tight integration with third-party simulators via NativeLink™ integration. The SignalTap logic analysis capability integrates the functionality of a logic analyzer within the software, allowing the design team to perform hardware verification on a device running at system speed.

SignalTap Plus

The SignalTap Plus system analyzer is a powerful system-level debug tool from Altera that enhances the on-chip debug capabilities of the SignalTap embedded logic analyzer (ELA) by adding 32 channels of external logic analysis capability. SignalTap Plus enables you to capture signals from internal PLD nodes **and** external board-level nodes simultaneously, and view them all in a single, time-correlated display. The new SignalTap Front Panel software provides stand-alone debugging capabilities. SignalTap Front Panel software runs separately or from within the Quartus software to control APEX device configuration, the SignalTap ELA, and the SignalTap Plus System Analyzer.

NativeLink Integration with Third-Party EDA Tools

NativeLink™ integration facilitates the seamless transfer of information between the Quartus software and other EDA tools to enhance the overall productivity of the designer's EDA tool suite. The NativeLink flow allows designers to use Quartus pre-place-and-route estimates in third-party EDA tools to optimize synthesis strategies.

Error Location and Timing Optimization Capability

While most interfaces allow design information to be passed from one tool to another, they provide little or no interaction between tools. Using the Quartus software, error correction and timing optimization are easier than ever before. The Quartus software can identify the source of errors directly in the EDA tool's source design file, enhancing the process of correcting errors and adjusting timing parameters.

MAX+PLUS II Development Software

The MAX+PLUS II software offers a wide variety of design entry, compilation, verification, and programming options. You can quickly implement and test changes to your design, program Altera PLDs at your desktop, and utilize these PLDs to eliminate the long lead times typically associated with gate arrays.

Table 2 summarizes all the features, devices, and enhancements you will receive when you register for the Altera Development Tools Subscription Program.

World-Class Synthesis and Simulation

All Altera subscriptions now include world-class synthesis and behavioral simulation tools from third-party OEM partners. These leading-edge tools are tightly integrated with Quartus and MAX+PLUS II to provide best-in-class quality of results.

The Synopsys FPGA *Express* compiler supports VHDL and Verilog HDL synthesis. FPGA *Express* provides a complete synthesis environment including Altera-specific architecture optimizations, static timing analysis, constraint management, and a schematic viewer. Designers have a full range of synthesis flows under their control in an easy-to-use interface. These flows include push-button, constraint-based, hierarchical, and script-based synthesis. The compiler can be integrated with the Quartus software, allowing designers to launch the Quartus software from within the FPGA *Express* environment.

The Exemplar Logic LeonardoSpectrum tool supports VHDL **or** Verilog HDL synthesis. The LeonardoSpectrum synthesis tool combines push-button ease-of-use with powerful control and optimization features normally associated with workstation-based ASIC tools.

The Model Technology ModelSim software supports VHDL **or** Verilog HDL simulation. ModelSim is the world leader in HDL simulation tools offering unprecedented performance and flexibility. The Altera-specific version of ModelSim is a full-featured VHDL or Verilog HDL simulator with support for VHDL or Verilog HDL test benches and Tcl scripting for user-defined functions and automation.

Table 2. Altera Development Tools Device Support & Features

	DEVICES & FEATURES SUPPORTED	DESCRIPTION	MAX+PLUS II	QUARTUS
Device Support	APEX 20K	New Advanced Programmable Embedded MatriX (APEX) architecture designed for system-level integration with multi-million-gate densities. APEX 20KE devices offer additional features such as support for LVDS and other advanced I/O standards, CAM, enhanced ClockLock™ clock circuitry, and additional global clocks.		●
	ACEX 1K	Mid-range density, LUT-based programmable logic devices (PLDs) offering the low cost and high performance needed for price-sensitive communications applications.	●	
	FLEX 10K	High-density, high-performance Flexible Logic Element MatriX (FLEX) architecture device family featuring embedded array blocks (EABs).	●	
	FLEX 6000	Low-cost, high-volume alternative to gate arrays.	●	
	MAX 9000	High-density, 5.0-V Multiple Array MatriX (MAX) architecture device family that supports in-system programmability (ISP).	●	
	MAX 7000	High-speed MAX architecture that supports 5.0-, 3.3-, and 2.5-V ISP.	●	
	MAX 3000	Low-cost, high-speed MAX architecture that supports 3.3-V ISP.	●	
Design Entry	Schematic Design Entry	The Graphic Editor allows you to use basic building blocks for creating a design, including the library of parameterized modules (LPM), TTL, and custom functions. The Symbol Editor allows you to create or modify a symbol for any design file.	●	●
	Block Design Entry	The Block Editor allows you to enter and edit design information in the form of logical blocks, allowing for a higher level of abstraction in specifying system designs.		●
	Text-Based Design Entry: AHDL, VHDL or Verilog HDL	The MAX+PLUS II and Quartus software support a high-level design methodology based on a variety of HDLs, including the Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL. Also, Exemplar LeonardoSpectrum and Synopsys FPGA Express tools included with subscription provide world-class support for VHDL and Verilog HDL design entry and synthesis.	●	●
	Waveform Design Entry	The Waveform Editor is used to specify logic by entering input and output waveforms.	●	
	EDA Interfaces	The bidirectional EDIF interface and the VHDL and Verilog HDL netlist writers allow designers to import and export design files between the MAX+PLUS II or Quartus software and industry-standard EDA tools.	●	●
	NativeLink Integration	NativeLink integration provides a seamless interface from the Quartus software to major EDA software tools. This interface helps support existing design flows and offers enhanced integration features.		●
	Floorplan Editing	The Floorplan Editor provides a graphical method of assigning logic cells and pins.	●	●
	Hierarchical Design Management	The Hierarchy Display allows you to easily traverse hierarchical designs.	●	●
	Library of Parameterized Modules (LPM)	The LPM offers parameterized functions that can be used as building blocks to simplify design entry.	●	●
	MegaCore Functions	MegaCore functions are pre-verified HDL design files for complex, system-level functions that are created by Altera and optimized for Altera device architectures.	●	●
Design Compilation	Timing-Driven Synthesis & Fitting	Timing-driven synthesis and fitting allow you to specify timing constraints for any portion of the design, thereby controlling MAX+PLUS II and Quartus synthesis and fitting.	●	●
	Logic Synthesis & Fitting	Logic synthesis and fitting ensures optimal device utilization by automatically noticing design requirements with device resources, eliminating manual routing.	●	●
	Automatic Error Location	The Message Processor quickly locates and highlights syntax and logic errors in all design editors for swift design debugging.	●	●
	Design-Rule Checking	The Design Doctor checks designs with customizable design rules and flags potentially unreliable circuitry.	●	●
	Multi-Device Partitioning	Multi-device partitioning automatically divides large designs into two or more devices from the same family.	●	
	OpenCore Evaluation	OpenCore evaluation enables designers to compile and simulate MegaCore and AMPP functions before licensing the function.	●	●
	CoreSyn Synthesis	The CoreSyn capability invokes the appropriate synthesis technology to optimize the logic for the target device architecture.		●

Continued on following page

Table 2. Altera Development Tools Device Support & Features - Continued

	DEVICES & FEATURES SUPPORTED	DESCRIPTION	MAX+PLUS II	QUARTUS
Design Verification	Timing Analysis	The Timing Analyzer traces all possible signal paths to determine the speed-critical and performance-limiting paths of a design.	✓	✓
	Waveform Editing	The Waveform Editor allows designers to create a file containing the input waveforms that drive simulation and the node names to be simulated, and then view the simulation results.	✓	✓
	Functional Simulation	The Simulator uses design information to model the logical function of a design with zero propagation delays.	✓	✓
	Timing Simulation	The Simulator tests the logical funciton and worst-case timing of a fully synthesized and optimized design.	✓	✓
	SignalTap Logic Analysis	SignalTap logic analysis allows capture and analysis of any internal node or I/O signal for system-level verification of devices running at actual system speed.		✓
	SignalTap Plus System Analyzer	The SignalTap Plus system analyzer enhances SignalTap logic analysis by adding a 32-channel, 166-MHz, PC-hosted logic analyzer for capturing board-level signals. SignalTap Plus lets you capture signals from internal PLD nodes and external, board-level nodes simultaneously and view them all in a single, time-correlated display.		✓
	HDL Simulation & Test Bench Support	Model Technology ModelSim provides support for VHDL or Verilog HDL behavioral simulation and test bench support.	✓	✓
Device Programming	Device Programming	Together with the appropriate programming hardware, the MAX+PLUS II and Quartus software programs, configures, verifies, examines, blank-checks, and functionally tests Altera devices on your desktop. It supports in-system programmability (ISP), in-circuit reconfigurability (ICR), and traditional programming methods.	✓	✓
	Jam™ Standard Programming and Test Language (STAPL)	MAX+PLUS II and Quartus software support the JEDEC-approved Jam STAPL format, which is an interpreted language optimized for programming devices via the IEEE 1149 standard JTAG interface.	✓	✓
Other	Floating-Node Capability	Floating-node capability allow multiple users to share a single design site over a network.	✓	✓
	On-line Help	MAX+PLUS II and Quartus Help provides complete documentation for the software features, design guidelines, and detailed device information. Available in both English and Japanese.	✓	✓
	Internet-Based Support	The Quartus software connects directly over the Internet to an Altera solutions database, allowing you to find immediate solutions to common design problems, or to submit service requests directly to Altera Applications. The Quartus software also automatically communicates daily notifications of software updates, new device support, and on-line help updates.		✓

Step 2 – Add Megafunction Products

After you have chosen a subscription option, you can add megafunction products, including Altera MegaCore™ functions or functions from the Altera Megafunction Partners Program (AMPP℠).

Altera MegaCore Functions

MegaCore functions are developed and pre-tested by Altera, and are optimized for specific Altera device architectures, allowing you to rapidly implement the functions you need rather than building them from the ground up. Table 3 lists the MegaCore functions available today, which can be purchased on-line from the Altera IP MegaStore™ site at **http://www.altera.com/IPmegastore**.

Altera Megafunction Partners Program

AMPP megafunctions are produced by individual partners working in close cooperation with Altera. This alliance provides a broad portfolio of megafunctions that are optimized for Altera devices and facilitate high-density design. AMPP megafunctions range from simple building-block logic to very complex system-level cores, such as Reed-Solomon CODECs.

A list of all the AMPP partners is available on the Altera web site at **http://www.altera.com/IPmegastore**. Contact the individual partners directly to obtain AMPP functions.

MegaWizard Plug-In

Altera MegaWizard™ Plug-In is a parameterization tool that allows you to customize megafunctions with minimal effort and then integrate them into any standard design flow with a standard EDA tool. Both Altera and its AMPP partners offer parameterized megafunctions that you control and configure by applying a MegaWizard Plug-In. Megafunctions powered by a MegaWizard Plug-In enable designers to handle customization efficiently in their own design environment, saving time and money.

Altera OpenCore Feature

The Altera OpenCore™ evaluation feature, available in both the Quartus and MAX+PLUS II software, allows you to instantiate, compile, and simulate a function to verify its size and performance before making a license decision. You can download MegaCore functions for OpenCore evaluation at no cost from the Altera web site at **http://www.altera.com/IPmegastore**.

Table 3. Altera MegaCore Functions

ORDERING CODE	DESCRIPTION
PCI-BOARD2	FLEX 10KE 64-bit PCI Development Board Kit
PLSM-16450	Universal asynchronous receiver/transmitter
PLSM-6402	Universal asynchronous receiver/transmitter
PLSM-6850	Asynchronous communications interface adapter
PLSM-8237	Programmable DMA controller
PLSM-8251	Programmable communications interface
PLSM-8255	Programmable peripheral interface adapter
PLSM-8259	Programmable interrupt controller
PLSM-CRC	Parameterized cyclic redundancy code generator & checker
PLSM-CSC	RGB-to-YCrCb & YCrCb-to-RGB color space converters
PLSM-FIR	FIR compiler
PLSM-FFT	Parameterized Fast Fourier Transform function
PLSM-HC-8B10B	8-bit 10-bit encoder/decoder
PLSM-HC-DES	Data encryption software
PLSM-HC-EQUALIZER	Adaptive equalizer
PLSM-HC-FFT	FFT processor
PLSM-HC-RSDEC/C	Reed-Solomon continuous decoder
PLSM-HC-RSDEC/ERAS	Reed-Solomon decoder with erasures
PLSM-HC-RSDEC/V	Reed-Solomon variable decoder
PLSM-HC-RSENC/V	Reed-Solomon variable encoder
PLSM-HC-VITERBI/HS	High-speed Viterbi decoder
PLSM-HC-VITERBI/SS	Slow-speed Viterbi decoder
PLSM-INLV	Parameterized symbol interleaver/deinterleaver
PLSM-MICROLIB	Library of UART, DMA controller, & parallel port controller functions
PLSM-NCO	Numerically-controlled oscillator compiler
PLSM-PCI/A	32-bit, 33-MHz PCI master-target with DMA
PLSM-PCI/MT32	32-bit, 66-MHz parameterized PCI master-target interface
PLSM-PCI/MT64	64-bit, 66-MHz parameterized PCI master-target interface
PLSM-PCI/T32	32-bit, 66-MHz PCI target interface
PLSM-PCI/T64	64-bit, 66-MHz PCI target interface
PLSM-RSDEC	Reed-Solomon standard decoder
PLSM-RSENC	Reed-Solomon standard encoder
PLSM-TURBO/DEC	Turbo Decoder
PLSM-TURBO/ENC	Turbo Encoder
PLSM-UTOPIA2MS	Utopia 2 master core
PLSM-UTOPIA2SL	Utopia 2 slave core
SOPC-BOARD/A4E	System-on-a-programmable-chip development board (APEX EP20K400E device)

Additional Megafunction Information

Altera provides additional reference documentation on-line. You can find the latest information about MegaCore and AMPP megafunctions at the Altera world-wide web site at **http://www.altera.com/IPmegastore**.

Step 3 – Select the Appropriate Programming Hardware

Altera configuration cables, shown in Table 4, are available for in-circuit reconfiguration of APEX 20K, FLEX 10K, and FLEX 6000 devices, and in-system programming of MAX 9000, MAX 7000, and MAX 3000 devices. The configuration cables download device data from the Quartus and MAX+PLUS II software or directly from a system prompt.

The ByteBlaster™ MV, MasterBlaster™, and SignalTap Plus configuration cables also provide SignalTap logic analysis when used with the Quartus software. The SignalTap Plus system analyzer adds a powerful system-level debug tool for use with the Quartus software that enhances the on-chip debug capabilities of the SignalTap embedded logic analyzer (ELA) by adding 32 channels of external logic analysis.

The Altera Stand-Alone Programmer (PL-ASAP2), used with the appropriate programming adapters, provides the hardware and software needed for programming all Altera devices. The PL-ASAP2 includes an LP6 Logic Programmer card for Windows-based PC and compatible computers, a Master Programming Unit (MPU), and programming software.

SignalTap Plus System Analyzer

Use Table 5 to select the appropriate programming adapters for your devices. Adapters for new devices are available when the devices are introduced. Refer to the Altera web site for a complete list of Altera programming adapters.

Tables 6 and 7 on page 10 describe the recommended system configurations for the Altera Quartus, MAX+PLUS II, and partnership development tools.

Table 4. Altera Configuration Cables

ORDERING CODE	CABLE	HARDWARE INTERFACE	ADDITIONAL FEATURES
PL-BITBLASTER	BitBlaster™ serial download cable	RS-232 port	
PL-BYTEBLASTERMV	ByteBlasterMV™ parallel download cable	PC parallel port	Provides SignalTap logic analysis capability
PL-MASTERBLASTER	MasterBlaster™ communication cable	USB/RS-232 port	Provides SignalTap logic analysis capability Supports 1.8-, 2.5-, 3.3-, and 5.0-V systems
PL-SIGNALTAP_PLUS	SignalTap™ Plus system analyzer	USB/RS-232 port	Provides SignalTap logic analysis capability Supports 1.8-, 2.5-, 3.3-, and 5.0-V systems Includes 32-channel, 166-MHz PC-hosted logic analyzer for capturing board-level signals

Table 5. Altera Programming Adapters

DEVICE(S)	PACKAGE	ADAPTER
EPC1441 (1)	DIP J-Lead TQFP	PLMJ1213 PLMJ1213 PLMT1064
EPC1 (1)	DIP J-Lead	PLMJ1213 PLMJ1213
EPC2 (2)	PLCC (20-Pin) TQFP (32-Pin)	PLMJ1213 PLMT1064
EPC4E	TQFP (44-Pin) TQFP (100-Pin) FBGA (144-Pin)	PLMTEPC-44 PLMTEPC-100 PLMFEPC-144
EPC9E	TQFP (100-Pin) FBGA (144-Pin)	PLMTEPC-100 PLMFEPC-144
EPM9320	J-Lead (84-Pin) RQFP (208-Pin) PGA (280-Pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-Lead (84-Pin) RQFP (208-Pin)	PLMJ9320-84 PLMR9000-208NC (3)
EPM9400	J-Lead (84-Pin) RQFP (208-Pin) RQFP (240-Pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-Pin) RQFP (240-Pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-Pin) RQFP (240-Pin) PGA (280-Pin) RQFP (304-Pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-Pin) RQFP (240-Pin)	PLMR9000-208NC (3) PLMR9000-240NC (3)
EPM7032	J-Lead (44-Pin) PQFP (44-Pin) TQFP (44-Pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032B	J-Lead (44-Pin) TQFP (44-Pin) J-Lead (44-Pin) TQFP (44-Pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-44 PLMQ7000-44
EPM7064	J-Lead (44-Pin) TQFP (44-Pin) J-Lead (68-Pin) J-Lead (84-Pin) PQFP (100-Pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7064S EPM7064AE	J-Lead (44-Pin) J-Lead (84-Pin) TQFP (44-Pin) TQFP (100-Pin) FBGA (100-Pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC (3) PLMF7000-100
EPM7064B	J-Lead (44-Pin) TQFP (44-Pin) UFBGA (49-Pin) FBGA (100-Pin) TQFP (100-Pin)	PLMJ7000-44 PLMT7000-44 PLMU7000-49 PLMF7000-100 PLMQ7000-100NC (3)
EPM7096	J-Lead (68-Pin) J-Lead (84-Pin) PQFP (100-Pin)	PLMQ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128E	J-Lead (84-Pin) PQFP (100-Pin) PQFP (160-Pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128AE	J-Lead (84-Pin) TQFP (100-Pin) FBGA (100-Pin) TQFP (144-Pin) FBGA (256-Pin)	PLMJ7000-84 PLMT7000-100NC (3) PLMF7000-100 PLMT7000-144NC (3) PLMF7000-256
EPM7128B	UFBGA (49-Pin) FBGA (100-Pin) TQFP (100-Pin) TQFP (144-Pin) FBGA (256-Pin)	PLMU7000-49 PLMF7000-100 PLMT7000-100vNC (3) PLMT7000-144NC (3) PLMF7000-256
EPM7128S	J-Lead (84-Pin) PQFP (100-Pin) TQFP (100-Pin) PQFP (160-Pin)	PLMJ7000-84 PLMQ7000-100NC (3) PLMT7000-100NC (3) PLMQ7128/160-160NC (3)
EPM7160E	J-Lead (84-Pin) PQFP (100-Pin) PQFP (160-Pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-Lead (84-Pin) PQFP (100-Pin) PQFP (160-Pin)	PLMJ7000-84 PLMQ7000-100NC (3) PLMQ7128/160-160NC (3)
EPM7192E	PGA (160-Pin) PQFP (160-Pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-Pin)	PLMQ7192/256-160NC (3)
EPM7256E	PQFP (160-Pin) PGA (192-Pin) PQFP (208-Pin) RQFP (208-Pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256AE	FBGA (100-Pin) PQFP (208-Pin) RQFP (208-Pin) FBGA (256-Pin)	PLMF7000-100 PLMR7256-208NC (3) PLMR7256-208NC (3) PLMF7000-256
EPM7256B	TQFP (100-Pin) TQFP (144-Pin) UFBGA (169-Pin) PQFP (208-Pin) FBGA (256-Pin)	PLMT7000-100NC (3) PLMR7000-144NC (3) PLMU7000-169 PLMR7256-208NC (3) PLMF7000-256
EPM7256S	PQFP (208-Pin) RQFP (208-Pin)	PLMR7256-208NC (3) PLMR7256-208NC (3)
EPM7512AE	TQFP (144-Pin) PQFP (208-Pin) FBGA (256-Pin) FBGA (256-Pin)	PLMT7000-144NC (3) PLMR7256-208NC (3) PLMF7000-256 PLMB7000-256
EPM7512B	TQFP (144-Pin) UFBGA (169-Pin) PQFP (208-Pin) FBGA (256-Pin) SBGA (256-Pin)	PLMT7000-144NC (3) PLMU7000-169 PLMR7256-208NC (3) PLMF7000-256 PLMB7000-256
EPM3032A	J-Lead (44-Pin) TQFP (44-Pin)	PLMJ3000-44 PLMT3000-44
EPM3064A	J-Lead (44-Pin) TQFP (44-Pin) TQFP (100-Pin)	PLMJ3000-44 PLMT3000-44 PLMT3000-100NC (3)
EPM3128A	TQFP (100-Pin) TQFP (144-Pin)	PLMT3000-100NC (3) PLMT3000-144NC (3)
EPM3256A	TQFP (144-Pin) PQFP (208-Pin)	PLMT3000144NC (3) PLMQ3000-208NC (3)

Notes: (1) FLEX configuration device.
(2) APEX and FLEX configuration devices.
(3) These devices are not shipped in carriers.

Recommended System Configurations

Table 6. Recommended System Configurations for Quartus and OEM Partner Tools

Memory Requirements

APEX Device	Minimum Physical RAM	Minimum Additional Swap Space on Hard Disk Drive
EP20K60E, EP20K100, EP20K100E, EP20K160E, EP20K200, EP20K200E	256 MB	256 MB
EP20K300E, EP20K400, EP20K400E, EP20K600E	512 MB	512 MB
EP20K1000E	1,024 MB	1,024 MB
EP20K1500E	1,024 MB*	1,024 MB*

*Designs with >40K logic elements require 1,331 Mbytes.

Windows-Based PC

- Pentium-based PC or compatible computer
- CPU speed: 450 MHz
- Operating system software:
  - Microsoft Windows NT version 4.0 or higher, or
  - Microsoft Windows 98, or
  - Microsoft Windows 2000 (2H'00)
- SVGA graphics card and monitor compatible with Microsoft Windows
- CD-ROM drive

Windows-Based PC - Continued

- 2- or 3-button mouse compatible with Microsoft Windows
- Full-length 8-bit ISA slot for programming card
- Parallel port/USB port
- Internet Explorer version 4.0 or higher

Sun SPARCstation

- Sun SPARCstation with color or monochrome monitor
- Sun Solaris version 2.6
- ISO 9660-compatible CD-ROM drive
- Internet Explorer version 4.0 or higher

HP 9000 Series 700/800 Workstation

- HP 9000 Series 700/800 workstation with color or monochrome monitor
- HP-UX version 10.2x (versions 11.0 and higher are not supported)
- HP-CDE
- ISO 9660-compatible CD-ROM drive
- Internet Explorer version 4.0 or higher

Table 7. Recommended System Configurations for MAX+PLUS II and OEM Partner Tools

Memory Requirements

Device Family	Minimum Physical RAM	Minimum Additional Swap Space on Hard Disk Drive
ACEX 1K	128 MB	128 MB
FLEX 10K*	128 MB	128 MB
FLEX 6000	32 MB	32 MB
MAX 9000	32 MB	32 MB
MAX 7000	16 MB	32 MB
MAX 3000	16 MB	32 MB

*Additional RAM (256 Mbytes to 512 Mbytes) provides significant improvement in compilation times for designs targeting EPF10K100/A/B/E, EPF10K130V/E, EPF10K200E/S, and EPF10K250A devices.

Windows-Based PC

- Pentium-based PC or compatible computer
- Operating system software:
  - Microsoft Windows NT version 3.51 or higher, or
  - Microsoft Windows 95 or Windows 98
- SVGA graphics card and monitor compatible with Microsoft Windows
- CD-ROM drive
- 2- or 3-button mouse compatible with Microsoft Windows
- Full-length 8-bit ISA slot for programming card
- Parallel port
- HTML browser (e.g., Netscape Navigator)

Sun SPARCstation

- Sun SPARCstation with color or monochrome monitor
- Sun Solaris version 2.5 or 2.6
- ISO 9660-compatible CD-ROM drive
- HTML browser (e.g., Netscape Navigator)

HP 9000 Series 700/800 Workstation

- HP 9000 Series 700/800 workstation with color or monochrome monitor
- HP-UX version 10.2x (versions 11.0 and higher are not supported)
- HP-CDE
- ISO 9660-compatible CD-ROM drive
- HTML browser (e.g., Netscape Navigator)

IBM RISC System/6000 Workstation

- IBM RISC System/6000 workstation with color or monochrome monitor
- AIX version 4.1 or higher
- ISO 9660-compatible CD-ROM drive
- HTML browser (e.g., Netscape Navigator)

Download MAX+PLUS II BASELINE & E+MAX Development Software for Free

You can test drive Altera's powerful development tools by using the MAX+PLUS II BASELINE or the E+MAX™ software, which are entry-level versions of the MAX+PLUS II software. Your company can install an unlimited number of BASELINE or E+MAX design sites at no cost. To take advantage of these development systems you must register and obtain a license file from the Altera web site. You can download the software free of charge from the Altera web site or install it directly from the MAX+PLUS II CD-ROM or the Altera Digital Library CD-ROM.

The BASELINE software features a seamless development flow that allows you to enter, compile, and perform timing analysis on your design and also program a wide range of Altera PLDs—including the new ACEX 1K family, FLEX 6000, MAX 7000, and MAX 3000 devices.

The E+MAX software is a subset of the BASELINE software targeted at the industry's most popular product-term architectures—the MAX 7000 and MAX 3000 devices. This software offers shorter download times to designers using MAX 7000 and MAX 3000 devices only.

World-Class Synthesis Included with BASELINE and E+MAX Software

MAX+PLUS II BASELINE and E+MAX customers can download and license world-class synthesis software from the Altera web site. Customers can license Synopsys FPGA *Express* software to support VHDL and Verilog HDL synthesis, and Exemplar LeonardoSpectrum software for either VHDL or Verilog HDL synthesis.

The MAX+PLUS II BASELINE and E+MAX software support the following features:

- Schematic- and AHDL-based design entry
- Functional and timing simulation
- Timing analysis
- Floorplan editing
- Interfaces to popular EDA tools
- Hierarchical design management
- Logic synthesis and automatic fitting
- Automatic error location
- OpenCore evaluation
- Device programming
- On-line help

ACCESS Program and Partners

Altera's Commitment to Cooperative Engineering Solutions (ACCESS℠) program includes EDA vendors who have developed design entry, synthesis, verification, and/or device programming products that support Altera's PLD families. Through this program, Altera supports the industry-standard EDA tools common to many of today's design environments. Altera is continually evaluating and adding new ACCESS partners to benefit customers.

Interfaces to Synopsys, Cadence, Synplicity, Exemplar Logic, Innoveda, and Mentor Graphics tools are provided on all Quartus and MAX+PLUS II CD-ROMs. In addition, the NativeLink integration feature provides a seamless interface between the Quartus software and all ACCESS partner tools.

Contact Altera for more information about interfaces to other ACCESS partner tools.

Altera Consultants Alliance Program

The Altera Consultants Alliance Program (ACAP™) is designed to provide expert design assistance to Altera PLD users and help them quickly get their products to market. ACAP consultants are highly trained on Altera devices and tools; Altera carefully selects each ACAP consultant based on their knowledge of Altera devices, tools, and their design background. By recruiting a diverse group of consultants, Altera offers a group of experts who can help designers accelerate their design cycle times.

For more information, refer to the Altera web site at **http://www.altera.com.**

Altera Offices

Corporate Headquarters
Altera Corporation
101 Innovation Drive
San Jose, CA 95134
USA
Telephone: (408) 544-7000
http://www.altera.com

Altera European Headquarters
Altera U.K. Limited
Holmers Farm Way
High Wycombe
Buckinghamshire
HP12 4XF
United Kingdom
Telephone: (44) 1 494 602 000

Altera Japan, Limited
Shinjuku Mitsui Building 36F
1-1, Nishi-Shinjuku, 2 Chome
Shinjuku-ku, Tokyo 163-0436
Japan
Telephone: (81) 3 3340 9480
http://www.altera.com/japan

Altera International, Limited
Suite 908-920, Tower 1
Metroplaza
223 Hing Fong Road
Kwai Fong, New Territories
Hong Kong
Telephone: (852) 2487 2030

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