The Advantages of LPM

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High-density programmable logic devices (PLDs), such as Altera® FLEX® 10K devices, have created a paradigm shift in design methodology. To take full advantage of the capacity and performance of high-density devices, designers are moving away from traditional schematic-based design techniques and are turning to modern design techniques that use hardware description languages (HDLs), megafunctions, and the library of parameterized modules (LPM). This technical brief discusses the advantages of using the LPM when designing with FLEX 10K, FLEX 8000, and FLEX 6000 devices.

Library of Parameterized Modules

The primary objective of the LPM is to enable architecture-independent design without sacrificing silicon efficiency. By using the LPM, designers do not have to decide on a target architecture until late in the design flow. The design entry and simulation tools remain architecture-independent, relying on the synthesis or fitting tools to efficiently map the design to various architectures.

The LPM currently contains the 25 functions listed below. Each function is parameterized (i.e., designers can customize the size and behavior of the function to meet their design requirements). For example, designers can specify the number of pipeline stages in the `lpm_mult` function by changing the value of its `LPM_LATENCY` parameter.

- `lpm_constant`
- `lpm_latch`
- `lpm_rom`
- `lpm_add_sub`
- `lpm_fsm`
- `lpm_inv`
- `lpm_ff`
- `lpm_decode`
- `lpm_mult`
- `lpm_ttable`
- `lpm_and`
- `lpm_shiftreg`
- `lpm_mux`
- `lpm_counter`
- `lpm_inpad`
- `lpm_or`
- `lpm_ram_dq`
- `lpm_clshift`
- `lpm_abs`
- `lpm_outpad`
- `lpm_xor`
- `lpm_ram_io`
- `lpm_compare`
- `lpm_bustri`
- `lpm_bipad`

LPM Support

The LPM is supported by a wide variety of integrated circuit (IC) and EDA tool vendors, including Altera and Synopsys. Table 1 lists the LPM support from various IC vendors. Table 2 lists the EDA tools that currently support the LPM.

Table 1. Industry Support of the LPM

Vendor	LPM Committee Member	Tools Support LPM	Comment
Altera	✓	✓	Industry leader in LPM support. All MAX+PLUS® II configurations support the LPM.
Xilinx	✓		Supports its proprietary XBLOX and LogiBLOX methodologies over LPM.
Lucent			No LPM roadmap.
Actel	✓	✓	Supports several LPM functions.

Table 2. EDA Tools that Support the LPM

Tool Description	Cadence	Mentor Graphics	Synopsys	ViewLogic
Behavioral Simulator	Leapfrog	QuickHDL	*Note (1)*	*Note (1)*
Synthesis	Synergy	Exemplar, Galileo	FPGA Express	ViewSynthesis
Gate Level Simulator	Verilog XL	QuickSim II	*Note (1)*	ViewSim
Schematic Capture	Concert	Design Architect	*Note (1)*	ViewDraw

Note:
(1) The vendor does not currently offer products that support this function.

Altera provides substantial support for the LPM by serving as a member on the Electronic Industries Association's (EIA) LPM committee and providing tools that support the LPM. Altera's MAX+PLUS II development system supports all LPM functions, except `lpm_fsm`, `lpm_ttable`, `lpm_inpad`, `lpm_outpad`, and `lpm_bipad`.

LPM functions take maximum advantage of the FLEX architecture, which enables LPM functions to achieve high performance in FLEX devices. For example, a multiplier function implemented in a FLEX device out-performs a multiplier function implemented in competing devices, as shown in Table 3. Multiplier performance is critical because it is a basic building block of most DSP systems and it impacts system performance.

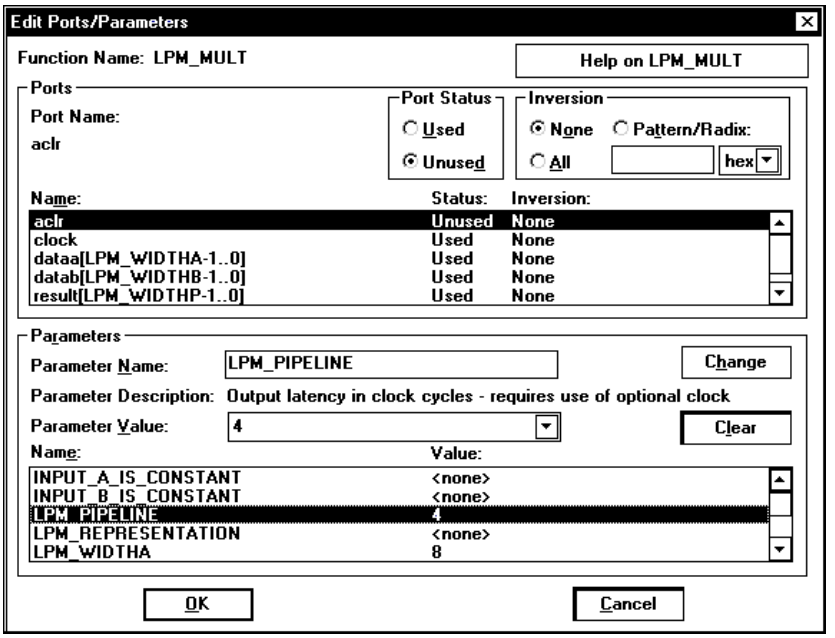
Table 3. Multiplier Comparison

Logic	Performance (MHz)					
	Altera FLEX 10K *(1)* **-3 Speed Grade**	**Altera FLEX 8000** *(1)* **-2 Speed Grade**	**Altera FLEX 6000** *(1)* **-2 Speed Grade**	**Xilinx XC4000E -2 Speed Grade**	**Lucent OR2C15A** *(2)* **-4 Speed Grade**	**Actel 1200XL** *(3)* **-1 Speed Grade**
8 × 8 multiplier pipelined	131	132	114	52, *Note (4)*	96	44
8 × 8 multiplier non-pipelined	37	44	38	29, *Note (5)*	24	14
12 × 12 multiplier pipelined	80	81	78	38, *Note (4)*	*Note (6)*	*Note (6)*
12 × 12 multiplier non-pipelined	21	22	22	21, *Note (5)*	*Note (6)*	*Note (6)*
16 × 16 multiplier pipelined	53	69	59	*Note (6)*	55	28
16 × 16 multiplier non-pipelined	19	21	20	18, *Note (5)*	7	8
32 × 32 multiplier pipelined	28	–	–	*Note (6)*	*Note (6)*	*Note (6)*

Notes:
(1) Source: Altera Applications. Altera's multipliers have a 4-stage pipeline, except the 8 × 8 multiplier, which has a 3-stage pipeline.
(2) Sources: *Synario App Review*, September 9, 1996, page 11. Lucent Microelectronics *Field-Programmable Gate Array Data Book*, October 1996. Lucent's multipliers use various levels of pipelining, including 3-, 6-, and 9-stage pipelines.
(3) Source: Actel Application Note *Implementing Multipliers in Actel FPGAs*. Actel's multiplier uses a 3-stage pipeline.
(4) Source: *Synario App Review*, September 9, 1996, page 20.
(5) Sources: *Synario App Review*, September 9, 1996, page 20. Xilinx *The Programmable Logic Data Book*, September 1996. The performance value was obtained by adding the setup time, clock-to-output time, routing delay, and then inverting it to obtain the frequency. Xilinx's multipliers have a 4-stage pipeline.
(6) No data is currently available.

Using the LPM and the MAX+PLUS II development system, designers can automatically create a multiplier of any size in minutes. For maximum performance, designers can use the LPM_LATENCY parameter (e.g., LPM_LATENCY = 2) to create a pipelined multiplier that is optimized for the FLEX architecture, utilizing the carry chains. Furthermore, the speed and efficiency of the LPM enables designers to quickly test various pipeline lengths to optimize an application for speed and logic efficiency. Figure 1 shows the dialog box for the lpm_mult function in the MAX+PLUS II software.

Figure 1. lpm_mult Dialog Box



In contrast, competing vendors provide significantly less, if any, support for the LPM. For example, rather than supporting the LPM, Xilinx supports its proprietary XBLOX and LogiBLOX methodologies, which are graphical interface tools for creating and simulating high-level functions. The XBLOX methodology does not support signed multipliers, and the LogiBLOX methodology does not support multipliers, which are vital for digital signal processing (DSP) applications.

The following document provides more detailed information. The part number is in parenthesis.

- ***LPM Quick Reference Guide*** *(A-CAT-LPM-01)*

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