

# Advantages of ISP-Based CPLDs

The Altera® MAX® 9000 and MAX 7000S in-system programmable devices offer designers flexibility, advanced features, and high performance at a low price. Combining these features with the most complete development tools environment offers designers the best solution for their design needs. This technical brief focuses on the programming time, performance, die size, and power consumption advantages of MAX 9000 and MAX 7000S devices.

When choosing an in-system programmable device, it is important to evaluate the complete solution. In an effort to show the benefits of MAX 9000 and MAX 7000S devices, Altera Applications recently compared several aspects of the Altera and Xilinx in-system programmable device families.

## Programming Times

Altera MAX 9000 and MAX 7000S devices can be programmed quickly in both production and development environments. In contrast, the device programming times for Xilinx XC9500 devices can be 10 to 50 times higher in development environments than in production environments. According to the Xilinx *Application Note XAPP068 In-System Programming Times*, this increase is due to the overhead spent in the real-time generation of programming vectors from the JEDEC bitmap, the bandwidth limitations for outputting JTAG vectors, and the time required to erase the device. [Table 1](#) shows the in-system programming times for Xilinx XC9500 and Altera MAX 7000S devices with comparable densities.

Table 1. MAX 7000S & XC9500 In-System Programming Times

Altera, <i>Note (1)</i>			Xilinx, <i>Note (2)</i>		
Device	Production Time (s)	Development Time (s)	Device	Production Time (s)	Development Time Ranges (s)
	f <sub>TCK</sub> = 10 MHz	f <sub>TCK</sub> = 100 kHz		f <sub>TCK</sub> = 10 MHz	
EPM7032S	1.53	7.00	XC9536	4.80	48 to 240
EPM7064S	1.71	9.86	XC9572	5.40	54 to 270
EPM7128S	1.97	15.55	XC95108	4.80	48 to 240
EPM7160S	2.08	18.46	XC95144	6.90	69 to 345
EPM7192S	2.24	21.72	XC95180	9.60	96 to 480
EPM7256S	2.55	28.70	XC95216	12.60	126 to 630
EPM9320	4.82	52.07	XC95288	18.30	183 to 915

Notes:

(1) Source: Altera *Application Note 85 (In-System Programming Times)*, April 1997, version 1.

(2) Source: Xilinx *Application Note XAPP068 In-System Programming Times*, January 1997, version 1.1.

## Performance

When evaluating device performance, it is important to use comparable operating conditions. Altera Applications recently compared the operating frequencies of MAX 7000S and XC9500 devices using equivalent parameters (see [Table 2](#)).

Table 2. Equivalent Performance Parameters

Altera		Xilinx	
Parameter	Description	Parameter	Description
$f_{CNT}$	Maximum internal global clock frequency	$f_{CNT}$	Operating frequency for 16-bit counters
$f_{ACNT}$	Maximum internal array clock frequency	$f_{SYSTEM}$	Internal operating frequency for general-purpose system designs spanning multiple function blocks

When compared under the same operating conditions, Altera MAX 7000S devices out-perform Xilinx XC9500 devices (see Table 3). In addition, Altera’s performance advantage will increase with the future release of the 5-ns EPM7032S devices, 6-ns EPM7128S devices, and 7.5-ns EPM7160S and EPM7192S devices.

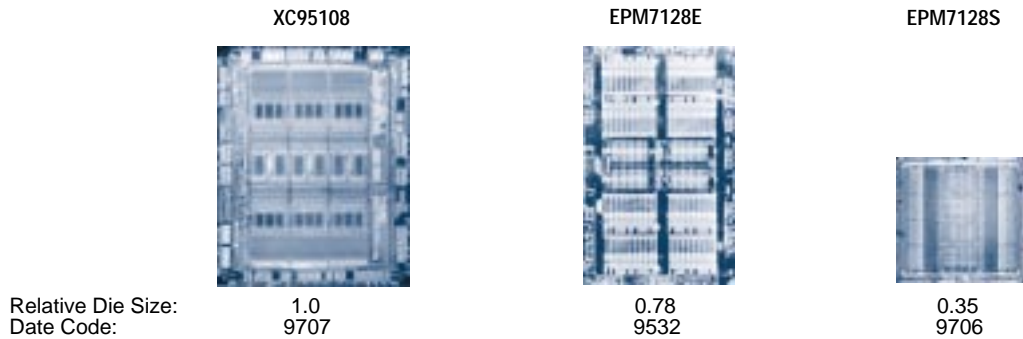
Table 3. MAX 7000S & XC9500 Device Performance

Device	$t_{SU}$ (ns)	$t_{CO}$ (ns)	$f_{CNT}$ (MHz)	$f_{SYSTEM}$ (MHz)
EPM7032S	4	3.5	178.6	178.6
EPM7064S	5	4	151.5	151.5
EPM7128S	5	4	151.5	151.5
EPM7160S	6	4.5	125	125
EPM7192S	6	4.5	125	125
EPM7256S	6	4.5	125	125
XC9536	4.5	4.5	125	100
XC9572	5.5	5.5	125	83
XC95108	5.5	5.5	125	83
XC95144	5.5	5.5	125	83
XC95180	6.5	6.5	111	67
XC95216	6.5	6.5	111	67

## Die Size

Altera aggressively pursues the most advanced manufacturing processes, enabling designers to benefit from the highest performance devices at the lowest price. For example, Altera has migrated its 128-macrocell device offerings from a 0.8-micron, dual-layer metal process in 1992, to a 0.5-micron, triple-layer metal process in 1997. Migrations allow Altera to continue providing extremely competitive prices. In contrast, the Xilinx XC9500 device family is manufactured on a 0.6-micron, dual-layer metal process. Figure 1 compares the die sizes of the XC95108, EPM7128E, and EPM7128S devices.

Figure 1. Die Size Comparison

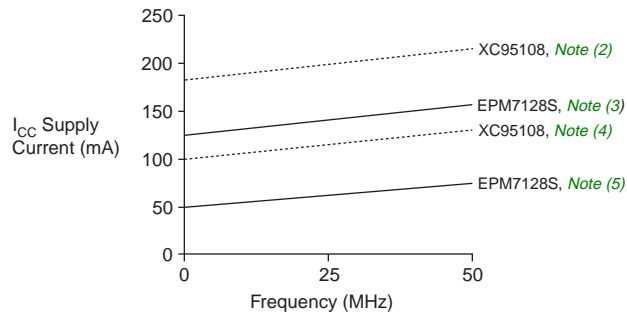


In addition, Altera plans to manufacture the next-generation product-term based family, Michelangelo, on a 0.35-micron, quad-layer metal process beginning in early 1998. Thus, Altera continues to aggressively pursue the most efficient manufacturing process.

### Power Consumption

The Altera MAX 7000S device family offers a power-efficient interconnect structure. In fact, MAX 7000S devices consume less power than XC9500 devices when operating under similar conditions (see Figure 2).

Figure 2. MAX 7000S & XC9500 Power Consumption Note (1)



**Notes:**

- (1) Source: Xilinx 1996 Data Book and Altera 1996 Data Book.
- (2) Power consumption for an XC95108 device set for high performance.
- (3) Power consumption for an EPM7128S device with the Turbo Bit™ logic option turned on.
- (4) Power consumption for an XC95108 device set for low performance.
- (5) Power consumption for an EPM7128S device set with the Turbo Bit logic option turned off.

## References

The following documents provide more detailed information. The part numbers are in parentheses.

- *MAX 9000 Programmable Logic Device Family Data Sheet (A-DS-M9000-04)*
- *MAX 7000 Programmable Logic Device Family Data Sheet (A-DS-M7000-04)*
- *In-System Programmability Handbook (M-HB-ISP-01)*
- *In-System Programmability CD-ROM (M-CD-ISP-02)*

You can request these documents from:

- Altera Literature Services at (888) 3-ALTERA
- World-wide web site at <http://www.altera.com>
- Your local Altera sales representative