Internal Tri-State Emulation

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When designing with internal tri-state buffers, designers should consider criteria such as ease of use, ease of fitting, and low cost. Altera offers an approach to using internal tri-state buffers that not only meets these criteria, but also supports hardware description language (HDL) design entry techniques, better routing utilization, and contention-free busing. This technical brief discusses Altera's internal tri-state capabilities and how designers can benefit from using this approach in their programmable logic device (PLD) designs.

Ease of Use

The Altera® MAX+PLUS® II software emulates an internal tri-state buffer—either by inference or instantiation—allowing designers to simply enter a behavioral description of a design without worrying about manual fitting and proper implementation. The MAX+PLUS II software automatically provides an optimized logic implementation of the tri-state buffer's functionality, even when the internal tri-state buffer is inferred. When instantiating an internal tri-state buffer, the library of parameterized modules (LPM) provides the most effective solution by allowing designers to customize the size and behavior of an internal tri-state function to meet their design requirements. Whether an internal tri-state buffer is inferred or instantiated, the MAX+PLUS II software gives the most optimized emulation of the internal tri-state function.

Easy Fitting & Better Routing Utilization

Altera's internal tri-state buffers are implemented using general-purpose logic and use only a few FastTrack™ Interconnect channels, thereby conserving routing resources and providing an easier fit. In contrast, implementing tri-state buffers in Xilinx devices causes the tri-state buffers to consume critical routing resources that may be needed for high fan-out and speed-critical paths. For example, the Xilinx XC4028EX device, which has a 32×32 configurable logic block (CLB) architecture, has two tri-state buffers for each CLB, and each buffer drives a single long line. If both tri-state buffers are used, they will consume 2 of the 6 available long lines, which reduces the availability of these high-speed, high-fan-out resources by 30%. Because the two long lines used by the tri-state buffers may need to connect to other CLBs or to the switch matrix, routing resources are reduced for other signals. If routing resources are used for tri-state buffering, device utilization and fitting are also compromised.

Low Cost

By offering internal tri-state emulation, Altera aggressively reduces die size, which results in low device cost. In comparison, Xilinx has dedicated internal tri-state buffers that require additional silicon area, resulting in larger die size, lower yields, and higher device cost. Additional time is needed during the manufacturing flow to test the functionality of the tri-state buffers, which also increases device cost. Table 1 compares the cost of Altera FLEX® 10K devices with the Xilinx XC4028EX device.

Table 1. Cost Comparison of FLEX 10K Devices vs. XC4028EX Device

Device	100-Unit Price *Note (1)*
XC4028EX-4HQ208C	$229.00
EPF10K20RC208-4	$57.50
EPF10K30RC208-4	$94.50
EPF10K40RC208-4	$126.00

Note:
(1) Source: Altera second quarter North American price list and Xilinx Distributor May 1997 price list.

Logic Usage

Logic usage may increase if designers implement a large multiplexer in an Altera device. For example, a 32-to-1 multiplexer requires 24 logic elements (LEs) when implemented in a FLEX 10K device. Although large multiplexers use more logic for internal tri-state emulation, designers have the flexibility to migrate to larger Altera devices. For example, designers can move from an EPF10K20 to an EPF10K40 device, maintain the same pin-out, and still receive a low price (see Table 1).

Supports HDL Design Entry Techniques

Altera's tri-state emulation supports HDL design entry techniques, allowing designers to describe designs at the behavioral level and rely on design tools such as the MAX+PLUS II development system for architecture optimization. In contrast, Xilinx tools force designers to break away from HDL design entry techniques by requiring manual manipulation for a successful fit.

Contention-Free Busing

Because the functionality of Altera's internal tri-state is implemented using general purpose logic, designers do not have to worry about possible bus contention. In contrast, Xilinx internal tri-state buffers must be closely monitored for bus contention, because internal contention on the long lines may cause the device to draw high current, resulting in higher power consumption.

The documents listed below provide more detailed information. Part numbers are in parentheses.

- *FLEX 10K Embedded Programmable Logic Family Data Sheet (A-DS-F10K-02)*
- *TB 24: The Advantages of LPM (M-TB-024-01)*

You can request documents from:

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