FLEX 10KA-1 Devices: The Fastest High-Density Devices Available

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As increasing bandwidth and system performance continue to challenge today's system designers, programmable logic vendors race to produce the fastest, high-density devices. For example, Altera's FLEX® 10KA-1 devices offer more than twice the system performance than the original FLEX 10K-3 devices and are the fastest high-density programmable logic devices (PLDs) available. This technical brief describes FLEX 10KA-1 device performance.

FLEX 10KA-1 Device Performance

In applications where enhanced speed is critical, FLEX 10KA-1 devices can provide a new level of system performance. Table 1 shows FLEX 10KA-1 device performance for specific benchmark applications.

Table 1. FLEX 10KA-1 Performance *Note (1)*

Application	FLEX 10KA-1 Performance
8-bit, 16-tap finite impulse response (FIR) filter	119 MHz
a16450 universal asynchronous receiver/ transmitter (UART) MegaCore™ function	31 MHz
16-to-1 multiplexer	3.4 ns
256 × 8 RAM read cycle	143 MHz
256 × 8 RAM write cycle	106 MHz

Note:
(1) Source: Altera Applications Engineering

Performance Comparison of FLEX 10KA-1 Devices & XC4000XL-09 Devices

Altera Applications tested FLEX 10KA-1 devices using the metrics listed below. The results of these tests are summarized and compared against the results published in the Xilinx *Application Brief XBRF015 (Speed Metrics for High-Performance FPGAs)*, which compares the Xilinx XC4000XL-09 devices (the fastest speed grade XC4000XL device available) with FLEX 10KA-2 devices. FLEX 10KA-1 devices are approximately 20-30% faster than FLEX 10KA-2 devices. All performance metric numbers represent register-to-register delays.

- I/O frequency
- *n*-to-1 multiplexer
- *n*-bit wide AND term
- *n*-level combinatorial logic
- Chained adders

I/O Frequency

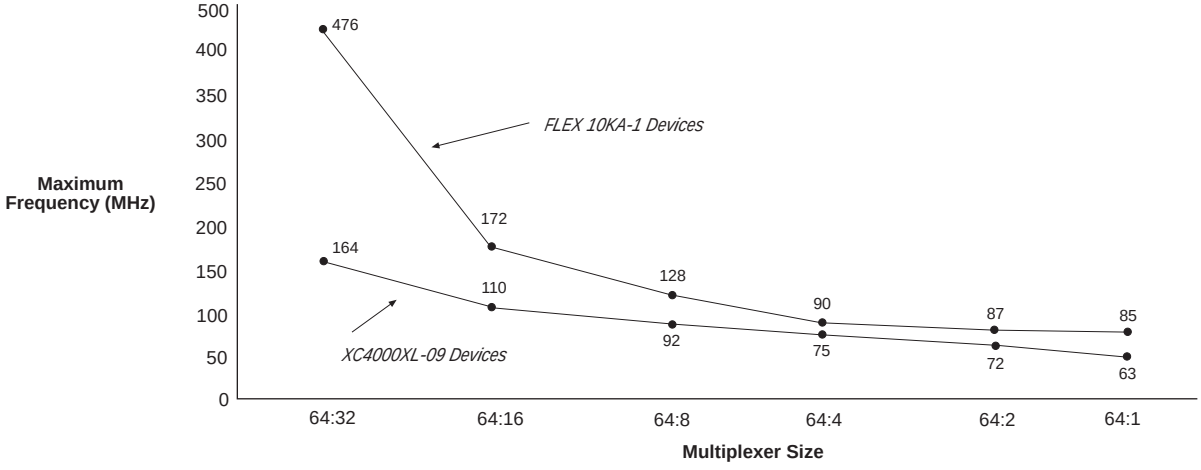
The I/O frequency metric is the sum of clock-to-output delay (t_{CO}) and input data setup time (t_{SU}). Table 2 shows the external I/O frequency comparison between FLEX 10KA-1 and XC4000XL-09 devices. The global clock buffer and clock distribution delays are included when determining the external I/O frequency.

Table 2. External I/O Frequency Results		
I/O Frequency	**EPF10K100A-1**	**XC4062XL-09**
External	86 MHz	73 MHz

n-to-1 Multiplexer

The *n*-to-1 multiplexer metric includes 64:1 to 64:32 multiplexers with registered inputs and outputs. The multiplexers in the FLEX 10KA-1 devices are implemented using the `lpm_mux` function from the library of parameterized modules (LPM). The multiplexer results in the XC4000XL-09 devices are as shown in the Xilinx *Application Brief XBRF015 (Speed Metrics for High-Performance FPGAs)*. Figure 1 shows multiplexer performance results with FLEX 10KA-1 and XC4000XL-09 devices.

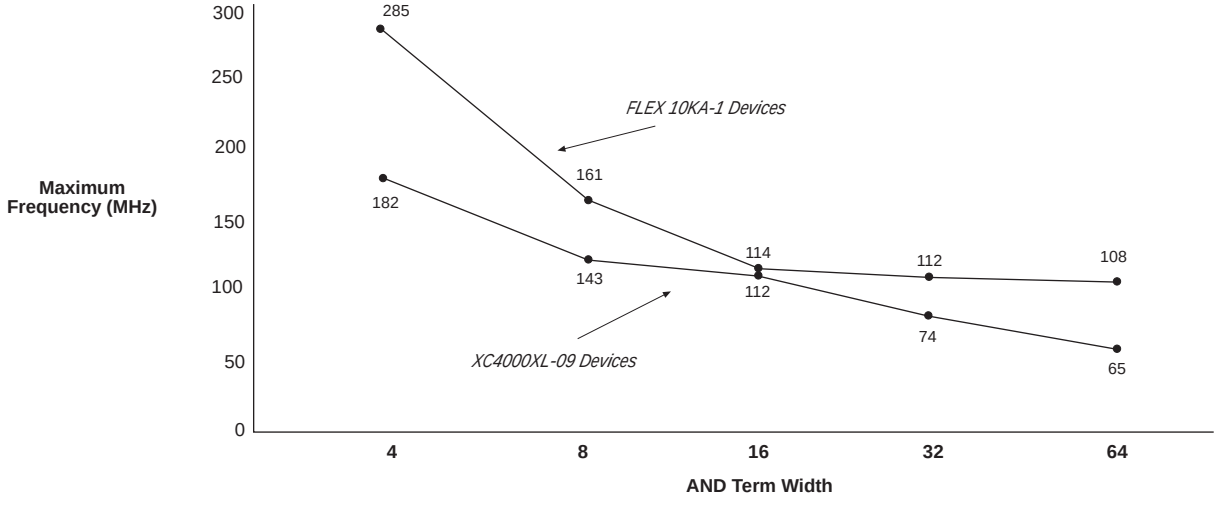
Figure 1. Multiplexer Performance Results



n-Bit Wide AND Term

The *n*-bit wide `AND` term metric measures performance of `AND` gates that are 4 to 64 bits wide with registered inputs and outputs. A wide comparator is an example of a typical function that requires large `AND` gate usage. Figure 2 compares FLEX 10KA-1 and XC4000XL-09 device results.

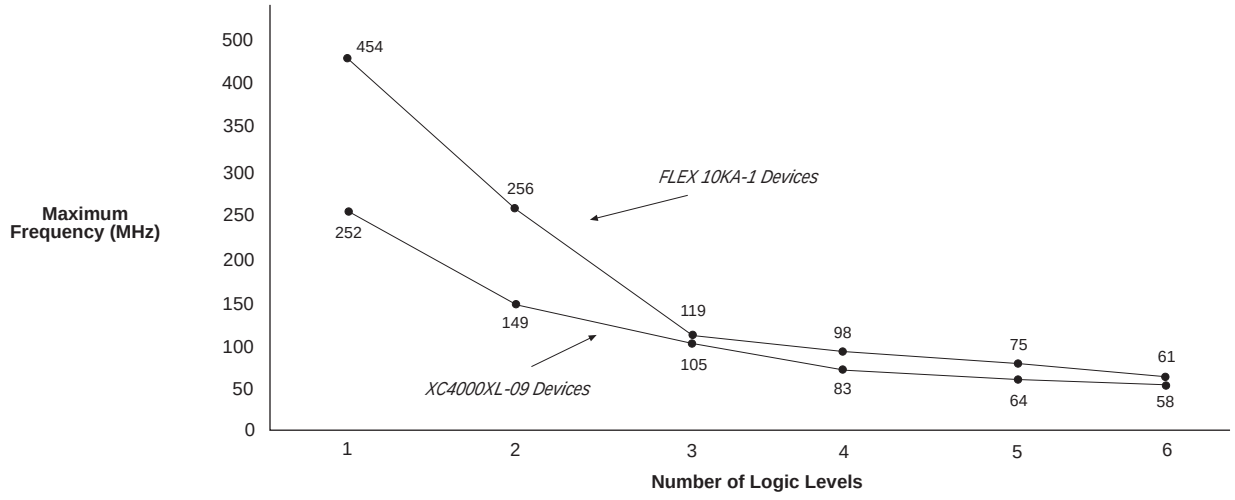
Figure 2. AND- Term Performance Results



n-Level Combinatorial Logic

The *n*-level combinatorial logic metric measures logic performance that is one to six levels deep. Each level refers to a set of four, 4-input look up tables (LUTs). The four LUTs increase fan-out. To increase the number of levels, more banks of LUTs are added. In each case, all inputs and outputs are registered. Figure 3 shows the LUT performance results with FLEX 10KA-1 and XC4000XL-09 devices.

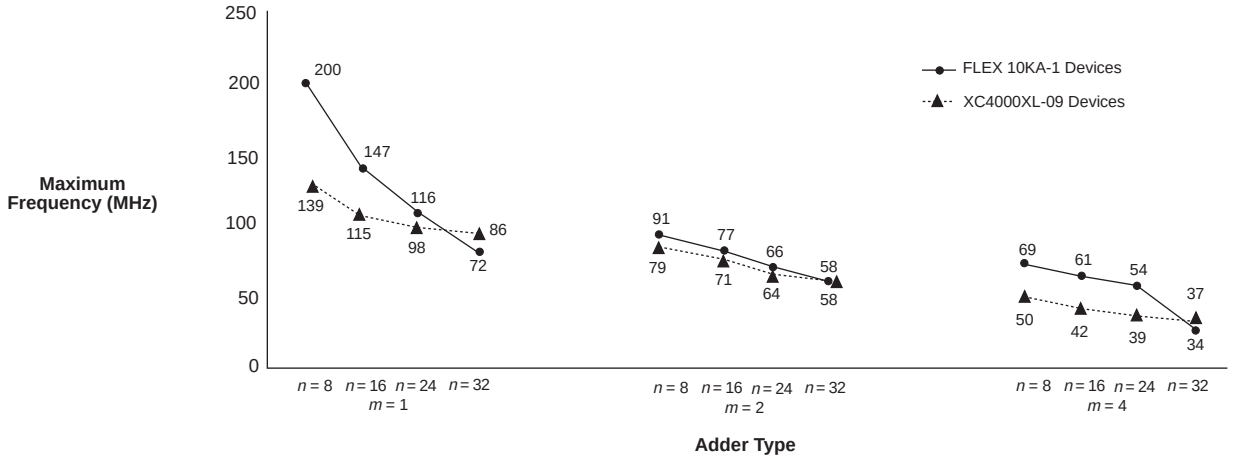
Figure 3. Combinatorial Performance Results



Chained Adders

The chained adders metric is a set of 8-, 16-, 24-, and 32-bit adders chained together. The various-sized adders give an indication of device performance using complex functions. The chains are 1, 2, and 4 levels deep, and all the inputs and outputs are registered. Figure 4 shows adder performance results with FLEX 10KA-1 and XC4000XL-09 devices.

Figure 4. Adder Performance Results



Note:
(1) *n* = bit width of adder and *m* = depth level.

Device Pricing

FLEX 10KA devices provide higher performance at a significantly lower price than XC4000XL devices. Table 3 shows 100-unit list pricing for FLEX 10KA-1 and XC4000XL-09 devices.

Table 3. 100-Unit List Pricing for FLEX 10KA-1 & XC4000XL-09 Devices

Device	Density	100-Unit Price, *Note (1)*
XC4062XL-09BG432C	4,608 equivalent logic elements (LEs)	$1,520
EPF10K100ABC356-1	4,992 LEs plus 24,576 embedded RAM bits	$398

Note:
(1) Source: Altera and Xilinx First Quarter 1998 North American distributor price lists.

Conclusion

With the introduction of FLEX 10KA-1 devices, system designers can now obtain new and higher levels of system performance. In addition to offering much higher system performance, FLEX 10KA-1 devices cost significantly less than competing FPGAs.

The documents listed below provide more detailed information and are available in the Altera ***1998 Data Book***.

- *FLEX 10K Embedded Programmable Logic Family Data Sheet*
- *Application Note 91 (Understanding FLEX 10K Timing)*

You can request documents from:

- Altera Literature Services at (888) 3-ALTERA
- World-wide web at **http://www.altera.com**
- Your local Altera sales representative