Using Synopsys FPGA Express Software to Synthesize Designs for MAX+PLUS II Software

SYNOPSYS®

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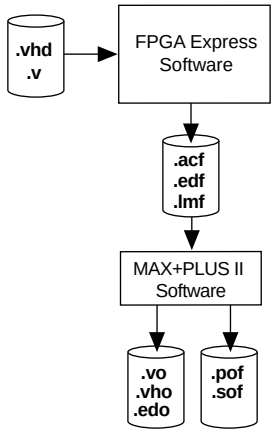
Introduction

The Altera® MAX+PLUS® II software easily interacts with third-party EDA tools such as the Synopsys FPGA Express software. With the MAX+PLUS II software, you can target Altera programmable logic devices (PLDs) using the FPGA Express software as your synthesis tool. The Altera / Synopsys FPGA Express tool lets you quickly synthesize and implement designs for Altera devices, and even perform multiple design iterations in a single day.

This technical brief describes how to use the FPGA Express environment to target an Altera device and to generate an EDIF netlist file, Assignment & Configuration File (**.acf**), and Library Mapping File (**.lmf**) for use in the MAX+PLUS II software.

Figure 1 shows a flow diagram of the Altera / Synopsys FPGA Express interface for PCs.

Figure 1. Altera / Synopsys FPGA Express Interface for PCs



For complete instructions on how to synthesize a design using the FPGA Express software and then import it into the MAX+PLUS II software for compilation, you should refer to the MAX+PLUS II Altera Commitment to Cooperative Engineering Solution (ACCESS℠) Key Guidelines, which are available in the Altera Technical Support (Atlas℠) section of the Altera web site at **http://www.altera.com**. The guidelines are also available in HTML format in the **\lit\html\maxkey** directory on the *MAX+PLUS II CD-ROM* (version 8.2 and higher).

Using the FPGA Express Software

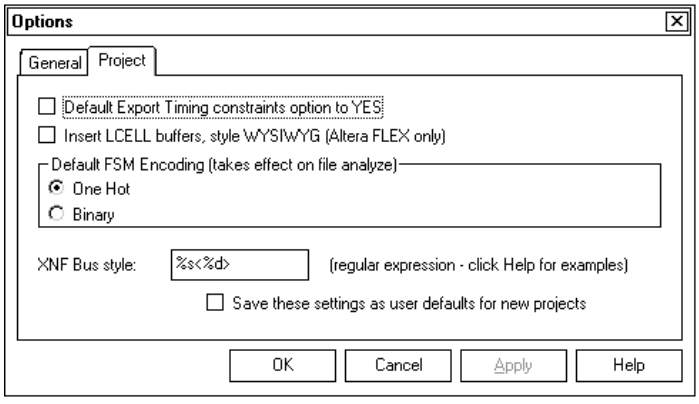
The following procedure describes how to set up the FPGA Express environment to target an Altera device and to generate an EDIF netlist file.

1. To create a new project, select **New** (File menu).
2. Specify a project name in the *Name* box and choose **Create**.
3. In the **Identify Sources** dialog box, select your source files. Choose **Open**.

The source files are analyzed and errors are identified. You should correct all errors and reanalyze the source files before continuing to set up the FPGA Express environment. You can also invoke the built-in text editor to correct errors by double-clicking on the error messages.

4. Choose **Options** (Synthesis menu). Click on the **Project** tab. You can choose to turn on the *Default Export Timing Constraints Option* option, turn on the *Insert LCELL Buffers, Style WYSIWYG* option (for FLEX devices only), or select a state machine style from *Default-FSM Encoding* option. Choose **OK**. See Figure 2.

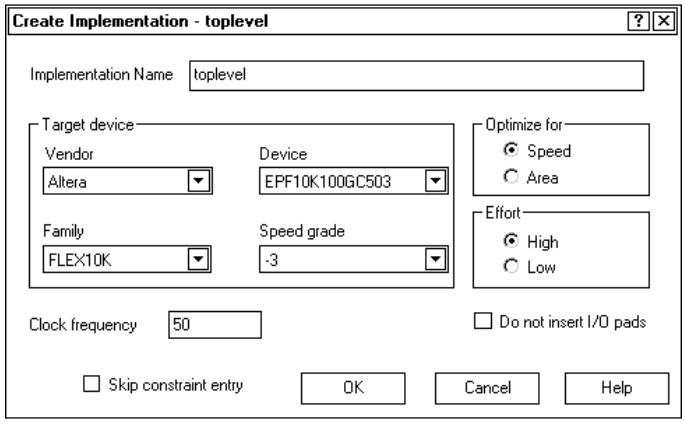
Figure 2. Options Dialog Box



Turning on the *Default Export Timing Constraints Option* option tells the FPGA Express software to export all timing constraints to a MAX+PLUS II ACF. The *Insert LCELL Buffers, Style WYSIWYG* option instructs the FPGA Express software to map to architecture-specific logic resources and directs the ACF synthesis style to WYSIWYG. The *Default FSM Encoding* option selects the state machine encoding methodology.

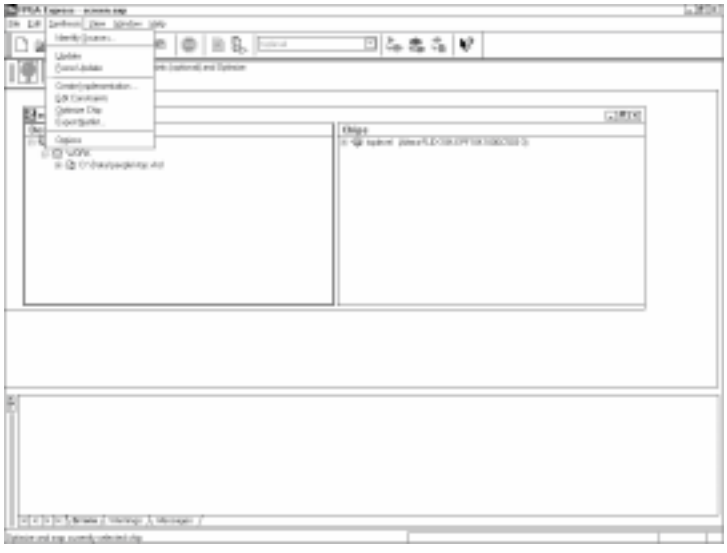
5. Select the top-level module or entity from your project and choose **Create Implementation** (Synthesis menu). Verify that the name of the top-level module or entity appears in the *Implementation Name* box. Then select the desired *Vendor, Device, Family, Speed Grade* to target your selected Altera device. Choose **OK**. See Figure 3.

Figure 3. Create Implementation Dialog Box



6. Click on the **Design Implementation** icon and select **Optimize Chip** (Synthesis menu) to map to logic resources. You may also edit constraints optimizing the design. See Figure 4.

Figure 4. Optimize Chip Dialog Box



7. Click on the **Design-Optimized** icon and choose **Export Netlist** (Synthesis menu). Specify a destination folder to save the EDIF Input File (**.edf**). Choose **Save**.

   The destination folder should contain an EDIF file, ACF, and LMF.

You can now import the EDIF netlist file into the MAX+PLUS II software for compilation. In the MAX+PLUS II Compiler, select *Custom* in the **EDIF Netlist Reader Settings** dialog box (Interfaces menu). Then, make sure *LMF#1* points to the LMF generated by the FPGA Express software. Refer to MAX+PLUS II Help for complete details.

More Information

Altera provides extensive support documentation to help you successfully interface the MAX+PLUS II software with third-party EDA design entry tools. For technical support, contact Altera Applications at (800) 800-EPLD. You can also e-mail your technical questions to Altera at **sos@altera.com**. For answers to common questions regarding the Altera / Synopsys interface, search Atlas Solutions on the Altera web site.

The following documents also provide more detailed information:

- MAX+PLUS II ACCESS Key Guidelines
- *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*
- *EDA Software Support*

The documents are available by contacting Literature Services at (888) 3-ALTERA; you can also download them from the Altera web site at **http://www.altera.com**.

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