Using Synplicity Synplify Software to Synthesize Designs for MAX+PLUS II Software

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Introduction

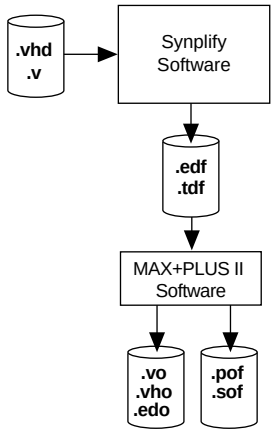
The Altera® MAX+PLUS® II software easily interacts with third-party EDA tools such as the Synplicity Synplify software. With the MAX+PLUS II software, you can target Altera programmable logic devices (PLDs) using the Synplicity Synplify software as your synthesis tool. The Altera / Synplicity interface lets you quickly synthesize and implement designs for Altera devices and perform multiple iterations in a single day.

This technical brief describes how to:

- Set up the Synplify design environment
- Generate an EDIF netlist file or an Altera Hardware Description Language (AHDL) design file for the MAX+PLUS II software

Figure 1 shows a flow diagram of the Altera / Synplicity interface.

Figure 1. Altera / Synplicity Interface



For complete instructions on how to synthesize and simulate a design using the Synplify software and then import the design into the MAX+PLUS II software for compilation, you should refer to the MAX+PLUS II Altera Commitment to Cooperative Engineering Solution (ACCESS℠) Key Guidelines, which are available in the Altera Technical Support (Atlas™) section of the Altera web site at **http://www.altera.com**. The guidelines are also available in HTML format in the **\lit\html\maxkey** directory on the *MAX+PLUS II CD-ROM* (version 8.2 and higher).

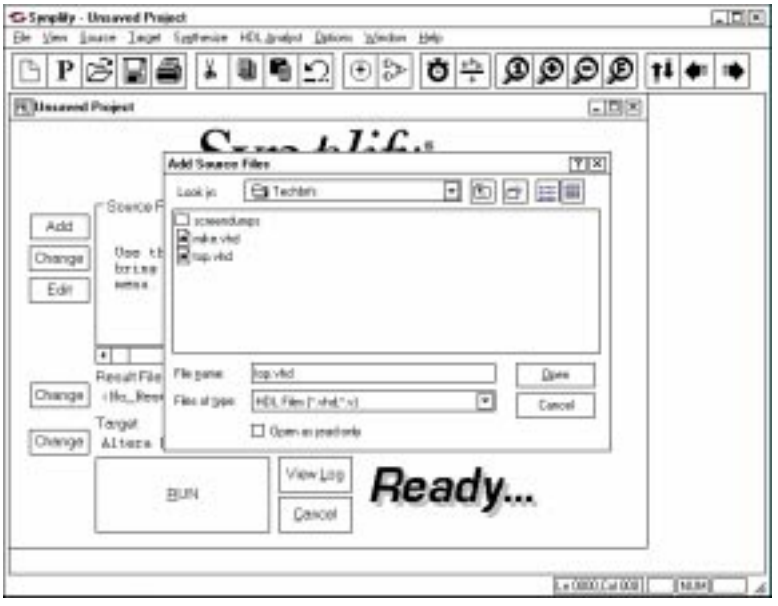
Using the Synplify Software to Target an Altera Device

The Synplify software graphical user interface (GUI) makes it easy to set up the Synplify environment and to generate an EDIF netlist file or AHDL design file. To target an Altera device, follow these procedures:

1. Select **New** (File menu) and choose **Project**. Then choose **OK**.

2. In the **Synplify** project window, choose **Add** in the *Source Files* section to specify source files in the **Add Source Files** dialog box. See Figure 2.

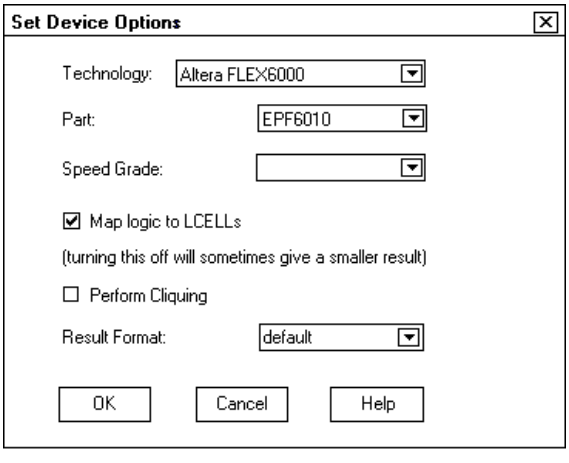
Figure 2. Add Source Files Dialog Box



Make sure that the top-level file appears in reverse hierarchical order in the *Source Files* window (i.e., the highest-level file appears at the bottom of the list.)

3. Choose **Change** in the *Target* section to open the **Set Device Options** dialog box. Select the desired Altera device family and device. See Figure 3.

Figure 3. Set Device Options Box



4. (Optional) Turn on *Map logic to LCELLS* to instruct Synplify to determine the best method of partitioning logic into logic cells. Enabling this option will guide the software to achieve a higher performance at higher resource utilization. If you turn on *Map logic to LCELLS* when targeting a FLEX Device, the *Perform Cliquing* option is available, which instructs Synplify to place logic in cliques for better performance optimization. When you turn on *Map logic to LCELLS* for MAX devices, the following controls are available for MAX devices:

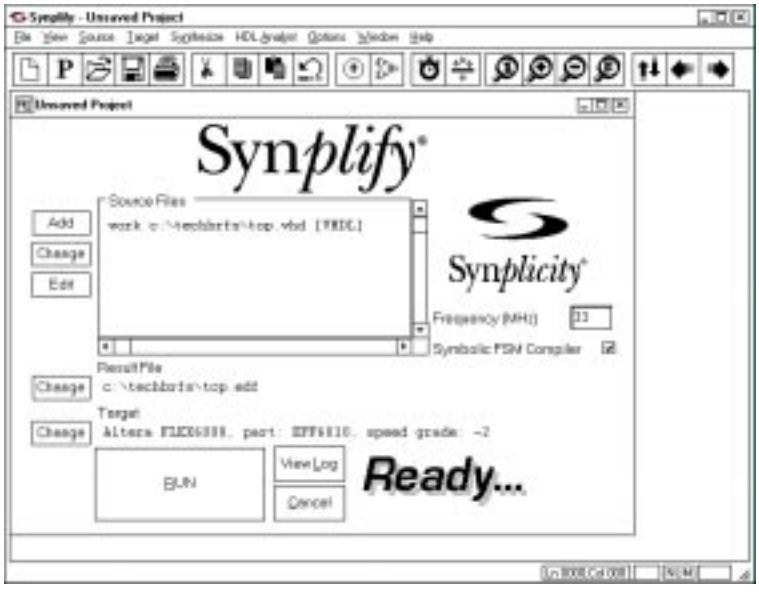
   - The *Percent of Design to Optimize for Timing* field lets you adjust the number of logic cell levels in the design. Increasing this percentage lowers the number of levels of logic cells and increases the number of inputs to logic cells along the critical paths, which can put a strain on fitting.
   - The *Maximum Cell Fanin* field affects the number of logic cells with few inputs. Lowering the maximum fan-in increases the logic cells with fewer inputs. Unless there is a high resource utilization issue, logic cells with fewer inputs allows the MAX+PLUS II software more flexibility in achieving a successful route.
   - Turning on *Make Non-Critical Cells Soft* allows the MAX+PLUS II software to reduce the number of logic cells used in implementing non-timing critical portions of the design.

5. In the *Result Format* drop-down list box, specify the result file as an EDIF netlist file (**.edf**) or an AHDL Text Design File (**.tdf**) for importing into the MAX+PLUS II software. To preserve Synplicity clique assignments, you must choose the EDIF netlist file format.

6. Choose **OK** to save your changes.

7. (Optional) In the *Synplify* project window, enter a value for target frequency in the *Frequency (MHz)* field. The default value for this option is 0 MHz. This default setting guides the Synplicity software to achieve optimal logic utilization. See Figure 4.

Figure 4. Synplify Project Window



8. (Optional) You can also turn on *Symbolic FSM Compiler* for performance optimization of state machines. This option directs Synplify to find the state machines in your design and automatically optimize them for Altera devices. However, there is a performance versus area trade-off associated with this setting. Enabling this option may achieve higher performance, but it also may result in higher resource utilization.

9. Choose **Run** to start VHDL / Verilog HDL design synthesis.

Compiling in the MAX+PLUS II Software

After successful synthesis, the result file is placed in the destination directory that you specified in Step 5 on page 3. You can import this file into the MAX+PLUS II software. Before you compile the file, you must assign the vendor in the **EDIF Netlist Reader Settings** dialog box to Synplicity by performing the following steps in the MAX+PLUS II Compiler:

1. Choose **EDIF Netlist Reader Settings** (Interfaces menu).

2. Choose *Synplicity* from the *Vendor* drop-down list box.

3. Choose **OK**.

For more information on assigning vendor settings, specifying an appropriate Library Mapping File (**.lmf**) for compilation, and specifying a specific device in the MAX+PLUS II software, refer to *TB 43 (Importing Synthesized Files from EDA Software into the MAX+PLUS II Software for Place & Route)*.

More Information

Altera provides extensive support documentation to help you successfully use the MAX+PLUS II software with third-party EDA design entry tools. For technical support, contact Altera Applications at (800) 800-EPLD. You can also e-mail your technical questions to Altera at **sos@altera.com**. For answers to common questions regarding the Altera / Synplicity interface, search Atlas Solutions on the Altera web site.

The following documents provide more detailed information:

- MAX+PLUS II ACCESS Key Guidelines
- *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*
- *EDA Software Support*

The documents are available by contacting Literature Services at (888) 3-ALTERA; you can also download them from the Altera web site at **http://www.altera.com**.

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