Increasing Performance Using ATOM Netlist Files

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
https://websupport.altera.com

Introduction

The Quartus™ development software provides third-party synthesis tools with an unprecedented level of control over the final mapping of APEX™ 20K designs. Third-party synthesis software can now synthesize VHDL and Verilog HDL design code directly to the APEX 20K architecture, resulting in increased design performance and reduced area utilization. This technical brief describes the benefits of using ATOM netlist files generated by third-party synthesis tools.

ATOM Netlist Files

An ATOM netlist file represents one level of hierarchy above the basic primitives and can be viewed as a configured logic element (LE). Instead of generating gate-level EDIF files, third-party synthesis software now generates ATOM netlist files that map directly to APEX 20K LEs. After synthesis, the Quartus software performs only place-and-route on the design's logic. ATOM netlist files eliminate the need to re-synthesize the design's logic in the Quartus software.

The following is a list of third-party synthesis tools that can generate ATOM netlist files:

- Synopsys FPGA Express/FPGA Compiler, versions 3.2 and higher
- Mentor Graphics Leonardo Spectrum, versions 1999.1C and higher
- Synplicity Synplify, versions 5.21 and higher

Comparing ATOM Netlist Files & Gate-Level EDIF Files

Altera® Applications compared 14 customer designs ranging in size from 2,000 to 10,000 LEs, using third-party synthesis software and the Quartus software. The comparison included the following steps:

- Altera synthesized each design twice, generating both a gate-level EDIF file and an ATOM netlist file.
- Altera compiled the two files in the Quartus software targeting the APEX 20K family.
- Altera compared the resulting design performance and area utilization.

When comparing the compilation results, the ATOM netlist file's average design performance (f_{MAX}) was 80% faster than the EDIF file and used an average of 15% less area. Additionally, third-party synthesis tools were able to provide more accurate area and timing estimates when using the ATOM netlist file design methodology.

☞ All improvements in design performance and area utilization are design dependent.

Figure 1 summarizes the average design performance for the two file types.

Figure 1. Average Design Performance

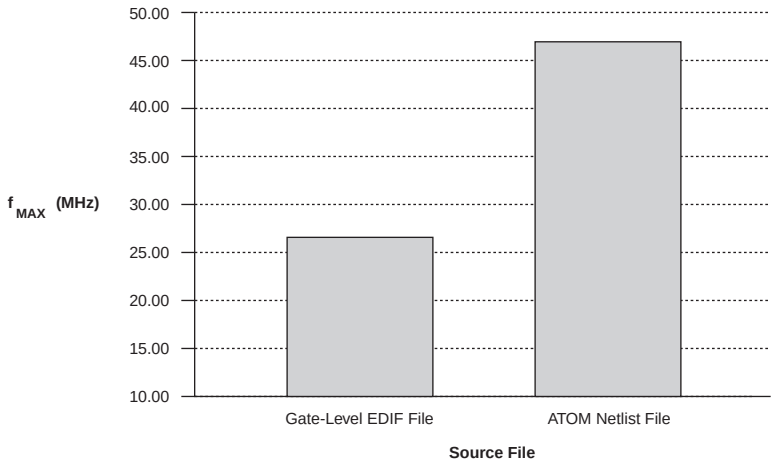
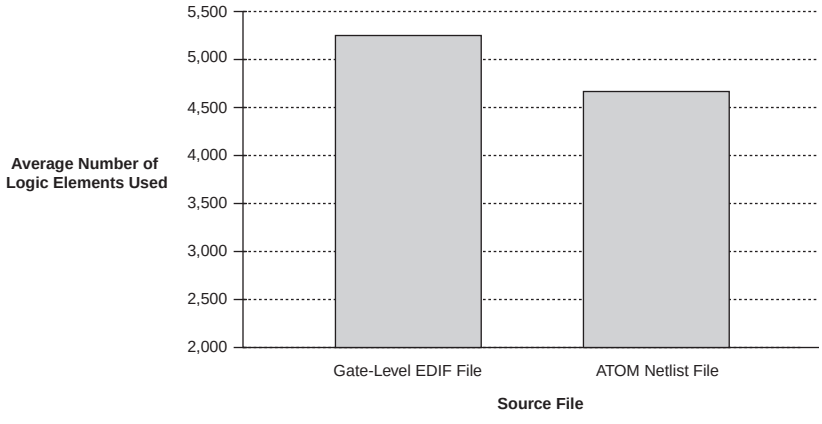


Figure 2 summarizes the average device utilization for the two file types.

Figure 2. Device Utilization



Conclusion

The Quartus software provides third-party synthesis software with the ability to map a design's logic directly to the APEX 20K architecture, which increases design performance and decreases area utilization. Using ATOM netlist files, enables third-party synthesis vendors to provide better results for designs targeting APEX 20K devices.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com