Power Consumption Comparison: APEX 20K vs. Virtex Devices

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Introduction

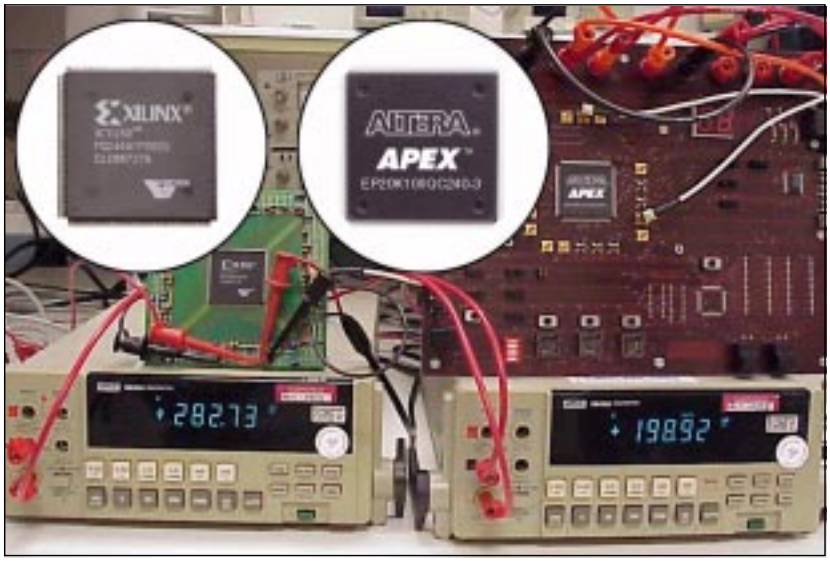
Many factors, such as supply voltage, current consumption, die size, and routing structure, affect semiconductor power consumption. For devices with the same supply voltages, the device current determines power consumption. Although modeling can be an effective tool for estimating the current consumption of a particular design, it is not appropriate for comparing the relative current consumption of the same design in different devices. Modeling current consumption in complex programmable logic devices (CPLDs) or field programmable gate arrays (FPGAs) is difficult because many factors must be considered, including the percentage of signals switching, channel capacitance, die size, device utilization, routing structure, and embedded memory utilization.

Device vendors provide power estimators and models as tools to estimate the power consumed by specific devices. These power estimators are built under different assumptions and conditions, and do not provide a good power consumption comparison between devices from different semiconductor manufacturers. The most accurate way to compare power consumption between devices from different semiconductor manufacturers is to perform experiments. Altera® Applications recently tested four typical designs to determine the actual power consumed by Altera APEX™ EP20K100 and Xilinx Virtex XCV150 devices.

Lab Setup

During the experiment, Altera Applications used a Hewlett-Packard 8110A 150-MHz pulse generator to generate clock signals. Each device was mounted on a test circuit board, programmed with identical designs, and powered with separate power supplies. Core voltage (V_{CCINT}) was set at 2.5 V, and I/O voltage (V_{CCIO}) was set at 3.3 V. The designs required one or two input control signals to set the mode of operation and one output signal to monitor circuit operation. The unused I/O pins were tri-stated. Figure 1 shows the lab setup used in the experiment.

Figure 1. Current Consumption Comparison *Note (1)*



Note:
(1) Current was measured using a Fluke 8840A volt-ohm meter.

Power Consumption Experiments

The Altera APEX EP20K100 and Xilinx Virtex XCV150 devices were chosen because they have a similar number of logic elements (LEs) and a similar number of RAM bits. Designs using RAM functions were implemented in the EP20K100 device's embedded system blocks (ESBs) and the XCV150 device's RAM blocks. Table 1 describes the devices used in the experiment.

Table 1. Devices Used in the Comparison

Feature	Altera EP20K100	Xilinx XCV150
Package	240-pin RQFP *(1)*	240-pin RQFP *(1)*
Speed Grade *(2)*	-3 *(2)*	-4 *(2)*
RAM Bits	52 K	48 K
Logic Elements	4,160	3,456
Core Voltage	2.5 V	2.5 V

Notes:
(1) RQFP = power quad flat pack.
(2) Slowest speed grade.

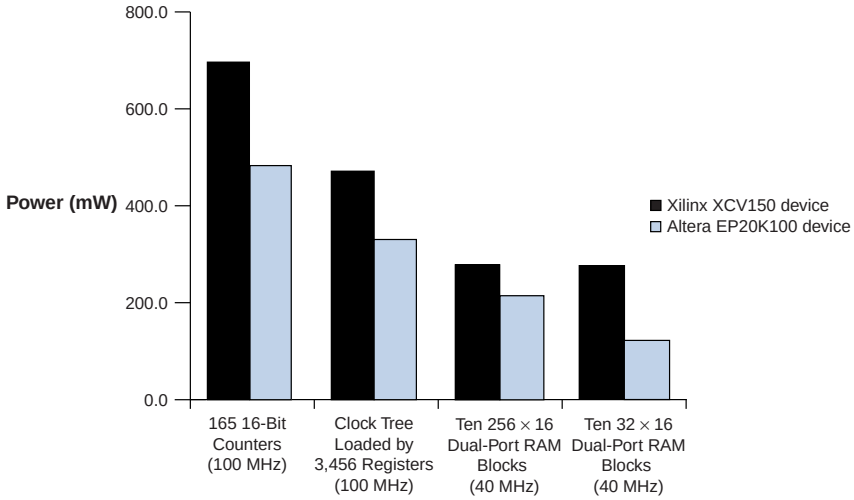
The experiment tested typical designs that have both combinatorial and registered logic that load the clock tree, and that test the current consumption of various RAM implementations. Each design utilized the test devices equally. Table 2 shows the designs used in the experiments, and Figure 2 shows the results.

Table 2. Designs Used in the Experiments

Design	Operating Frequency (MHz)	EP20K100 Device Utilization	XCV150 Device Utilization *(1)*
165 16-Bit Counters	100	2,640 LEs	2,640 LEs
Clock Tree (Loaded By 3,456 Registers)	100	3,456 LEs	3,456 LEs
Ten 256 × 16 Dual-Port RAM Blocks	40	40 Kbits	40 Kbits
Ten 32 × 16 Dual-Port RAM Blocks	40	5 Kbits	5 Kbits

Note:
(1) One Xilinx Virtex configurable logic block (CLB) is equivalent to four LEs.

Figure 2. Power Consumption

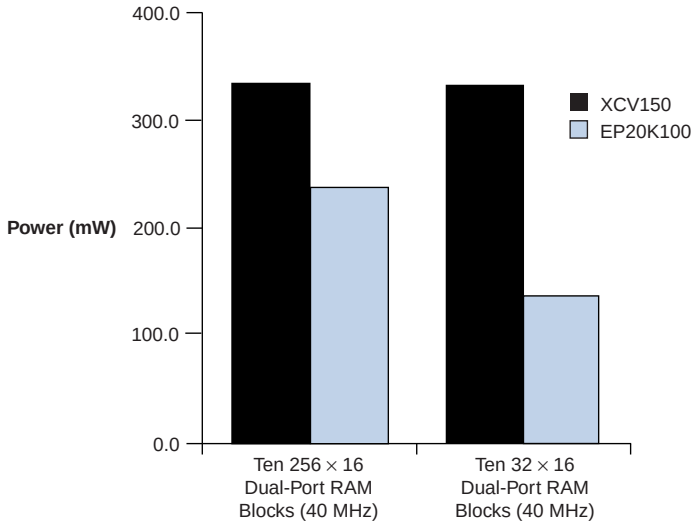


The EP20K100 device consumed between 24% and 54% less power than the XCV150 device. On average, the EP20K100 device consumed 33% less power than the XCV150 device.

RAM Power Consumption

Figure 3 shows the power consumed by an EP20K100 device and an XCV150 device when implementing the two dual-port RAM designs. The EP20K100 device used, on average, 39% less power than the XCV150 device when implementing RAM.

Figure 3. RAM Power Consumption Comparison



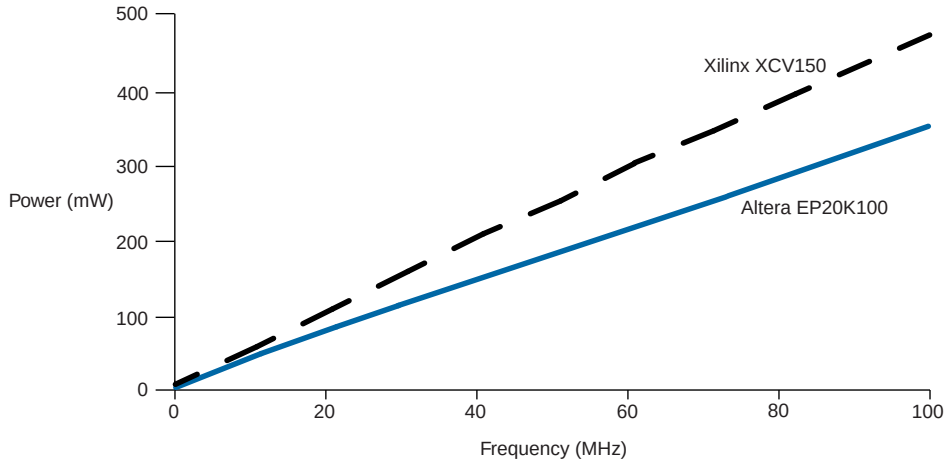
In an XCV150 device, each RAM block is 4,096 Kbits; in an EP20K100 device, each ESB is 2,048 Kbits. In this comparison, 256 × 16 dual-port RAM blocks were implemented in one XCV150 device RAM block. The same RAM was implemented using two EP20K100 ESBs. When implementing deep RAM, the two EP20K100 ESBs consumed 24% less power than one Virtex RAM block.

When implementing 32 × 16 dual-port RAM, one XCV150 RAM block and one EP20K100 ESB were used. When implementing 32 × 16 dual-port RAM, the EP20K100 consumed 54% less power than the XCV150 device. In designs using embedded RAM, the EP20K100 device consumed, on average, 39% less power than the XCV150 device. The smaller ESBs in the EP20K100 device provide more flexibility when implementing RAM and consume less power.

Clock Tree Power Consumption

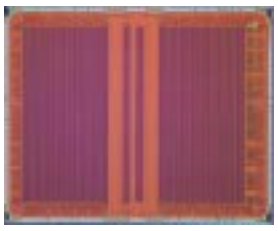
A global clock tree is a network of buffers and signal lines that are connected to registers in a device and ensure that destinations simultaneously receive signal transitions. In this experiment, the EP20K100 clock tree consumed 26% less power than the XCV150 clock tree (see Figure 4).

Figure 4. Clock Tree Power Consumption



Clock tree power consumption is directly affected by the size of the clock tree, which, in turn, is directly related to the relative die size of a device. The XCV150 die is 1.10 times larger than the EP20K100 die (see Figure 5). Therefore, the XCV150 clock tree consumes more power than the EP20K100 clock tree. In addition to a smaller die size, the EP20K100 device offers 20% more LEs and 8% more RAM bits.

Figure 5. Die Size Comparison



Altera EP20K100
Relative Die Size = 1
0.22 µm, 6 Layers
4,160 LEs

Xilinx XCV150
Relative Die Size = 1.10
0.22 µm, 5 Layers
3,456 LEs

Continuous Interconnect Routing Versus Segmented Routing

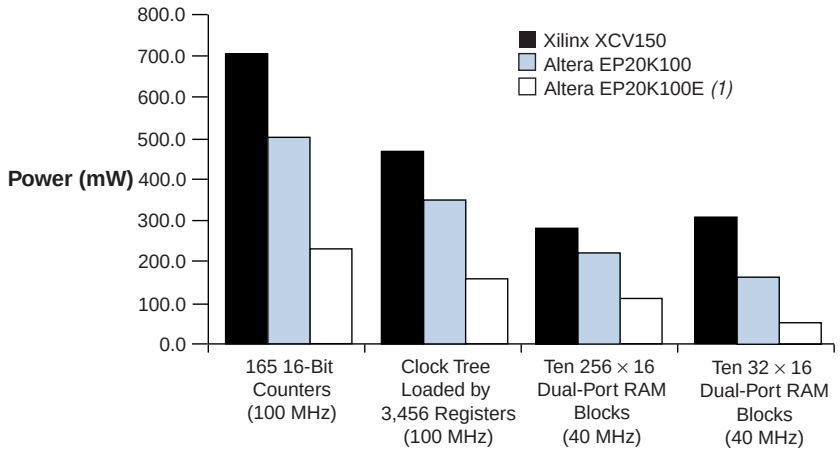
Several factors contribute to the lower power consumption of Altera EP20K100 devices over Xilinx XCV150 devices. The most significant factor is the device interconnect structure. EP20K100 devices use a continuous routing structure that is better suited for interconnect routing than the pass transistors used in XCV150 devices.

Because an interconnect path uses more pass transistors in the segmented Virtex architecture than in the continuous APEX architecture, the capacitance for a given path is lower in APEX devices, resulting in lower power consumption.

APEX 20KE Power Consumption

APEX 20KE devices will further reduce power consumption. APEX 20KE devices operate at a core voltage of 1.8 V and are based on a 0.18-µm, six-layer-metal process. Less capacitance from a smaller process and lower core voltage is expected to reduce power consumption in APEX 20KE devices by about 50% over APEX 20K devices. Figure 6 shows the projected power consumption for APEX 20KE devices.

Figure 6. Power Consumption in Virtex, APEX 20K & APEX 20KE Devices

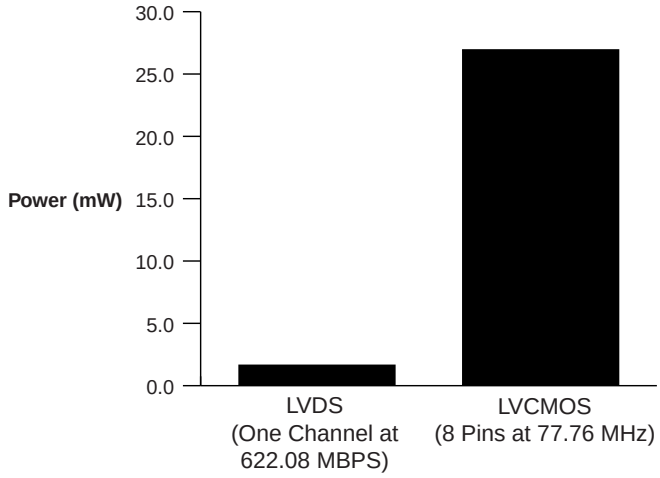


Note:
(1) Projected power consumption.

LVDS Power Consumption

APEX 20KE devices support the low voltage differential signaling (LVDS) I/O standard. Using LVDS on high-frequency signals reduces power consumption by 93.5%. Using one LVDS channel at 622.08 million bits per second (MBPS) is equivalent to using eight low-voltage CMOS (LVCMOS) signals at 77.76 MHz. The voltage swing on the LVDS signals is 350 mV, and the voltage swing on LVCMOS signals is 3.3 V. Toggling eight LVCMOS pins at 77.75 MHz consumes 27.09 mW of power. Toggling one LVDS channel at 622.08 MBPS consumes 1.83 mW of power. Figure 7 compares the power consumption of LVDS and LVCMOS.

Figure 7. LVDS & LVCMOS Power Consumption Comparison



References

For detailed information about APEX 20K devices, see the *APEX 20K Programmable Logic Device Family Data Sheet* and *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*. You can obtain these documents from:

- Altera Literature Services at (888) 3-ALTERA
- Altera web site at **http://www.altera.com**
- Your local Altera sales representative

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