

Programming Time Comparison: MAX 7000AE vs. XC9500XL Devices



Altera Corporation
101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>
<https://websupport.altera.com>

Introduction

The Altera® MAX® 7000AE family of high-density, high-performance programmable logic devices (PLDs) takes the Altera Multiple Array Matrix (MAX) architecture to the next level. Fabricated with advanced CMOS technology, the 3.3-V EEPROM-based MAX 7000AE devices provide a wide variety of system-level features, including 3.3-V in-system programmability (ISP), built-in Joint Test Action Group (JTAG) boundary-scan test (BST) support, and MultiVolt™ I/O capability, with devices ranging from 32 to 512 macrocells and 600 to 10,000 usable gates. An enhanced programming algorithm enables these devices to save users both time and money. Devices can be programmed in-system using in-circuit testers, embedded processors, or programming hardware.

This technical brief summarizes the results of in-system programming tests comparing Altera MAX 7000AE and Xilinx XC9500XL devices and discusses the advanced ISP features available in MAX 7000AE devices.

Programming Time Comparison

Altera Applications recently compared the in-system programming times of MAX 7000AE and XC9500XL devices when using PCs and in-circuit testers. Altera chose to test devices at a commonly used density level, the 128-macrocell EPM7128AE device and the 144-macrocell XC95144XL device. Both devices were programmed through the IEEE Std. 1149.1 JTAG interface and support a maximum clock frequency of 10 MHz.

For the first test, Altera measured the programming times on a 400-MHz Pentium III PC using a download cable. For the second experiment, the programming times were derived from each vendor's HP 3070 Pattern Capture Format/Vector Control Language (.pcf/.vcl) file. The files showed all literal vectors and programming wait times.

In-System Programming with a PC

Table 1 shows the results for in-system programming through a PC and a download cable. The experiment showed that the EPM7128AE device programmed in one-fourth the time required to program the XC95144XL device. When the XC95144XL device required the erase step, the EPM7128AE device programmed in almost one-fifth the time.

Table 1. Programming Times with a PC

Device	Test Clock (TCK) Rate 200 KHz (Seconds)	Tool Used
EPM7128AE (Erase and Program)	3.0	MAX+PLUS® II version 9.4
XC95144XL (Erase and Program)	14.0	WebPack v2.1WP2.x
XC95144XL (Program Only)	12.5	WebPack v2.1WP2.x

In-System Programming with In-Circuit Testers

The difference is more pronounced with in-circuit testers; the XC95144XL device required one and a half minutes to program, but the EPM7128AE device required only 2.2 to 4.0 seconds to program, depending on the TCK rate (see Table 2). This comparison shows that MAX 7000AE devices provide a clear programming time advantage over XC9500XL devices.

Table 2. Programming Times with an In-Circuit Tester

Device	TCK Rate		Tool Used
	2 MHz	100 KHz	
EPM7128AE (Erase, Program, and Verify)	2.2 Seconds	4.0 Seconds	MAX+PLUS II version 9.4
XC95144XL (Erase, Program, and Verify)	1.6 Minutes	1.6 Minutes	WebPack v2.1WP2.x and svf2vcl version 1.43 (1)
XC95114XL (Program and Verify Only)	1.5 Minutes	1.6 Minutes	WebPack v2.1WP2.x and svf2vcl version 1.43 (1)

Note:

(1) The **svf2vcl** utility was used on a UNIX machine running the HP-UX operating system.

In-System Programming Methodology

A shorter programming pulse width and a fewer number of addresses enable MAX 7000AE devices to program in considerably less time than XC9500XL devices. The programming pulse width measures the length of time that the programming pulse must be applied at each address. The majority of the total programming time is spent in the program stage, so you can significantly reduce the overall programming time by reducing the programming pulse width. Because the worst-case programming pulse width is 20 ms for MAX 7000AE devices and 50 ms for XC9500XL devices, MAX 7000AE devices program considerably faster than their Xilinx counterparts.

EEPROM-based devices, like MAX 7000AE devices, also require fewer addresses; these devices can program up to 1,000 addresses at a time. The FLASH-based XC9500XL devices program a much smaller number of addresses at one time, requiring that the programming pulse width be applied for a larger number of addresses.

The combination of a smaller programming pulse width and a fewer number of addresses to program yields a total MAX 7000AE programming time that is only 2% of the time required to program XC9500XL devices.

ISP via In-Circuit Testers

In-system programming via in-circuit testers is accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from a device and adapts subsequent programming steps to achieve the fastest possible programming time for that specific device. A constant algorithm uses a pre-defined programming sequence. MAX 7000AE devices can work with either algorithm.

Testers using Serial Vector Format (**.svf**) files do not support adaptive programming algorithms and must program at the device's worst-case programming pulse width. Therefore, XC9500XL devices must be programmed at their worst-case pulse width of 50 ms. Because MAX 7000AE devices have a worst-case programming pulse width of 20 ms, they provide faster overall programming times.

MAX 7000AE Enhanced ISP Feature Set

MAX 7000AE devices have an enhanced ISP feature set, including pull-ups on the I/Os during programming, a programming done bit, and an enhanced ISP algorithm for faster programming. The `ISP_Done` bit prevents all I/O pins from driving until the final bit is programmed, improving device operation safety. The enhanced ISP algorithm includes an auto-increment feature; during in-system programming, MAX 7000AE devices automatically increment the device counter. In contrast, Xilinx XC9500XL devices do not have these features and require an address to be shifted in for each piece of data.

Conclusion

High-performance, feature-rich MAX 7000AE devices offer superior programming times, which are critical when programming with in-circuit tester equipment. These smaller programming times can translate into large cost savings; programming a device on an in-circuit tester can total \$15 per minute. Table 3 shows the hidden in-system programming costs associated with EPM7128AE and XC95144XL devices, using an average programming time of 3.0 seconds and 1.6 minutes, respectively.

Table 3. Hidden Programming Cost Per Device

Device	Cost
EPM7128AE (Erase and Program)	\$0.55
XC95144XL (Erase and Program)	\$24.00
XC95144XL (Program Only)	\$22.50

With a programming cost nearly 2% that of XC9500XL devices, MAX 7000AE devices provide the most cost-effective solution for in-circuit testers.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>

Copyright © 2000 Altera Corporation. Altera, MAX, MAX+PLUS, MAX+PLUS II, EPM7128AE, Jam, MAX 7000, MAX 7000A, and MAX 7000AE are trademarks and/or service marks of Altera Corporation in the United States and other countries. Other brands or products are trademarks of their respective holders. The specifications contained herein are subject to change without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. All rights reserved.