New Features of the Quartus Software Version 2000.02

Technical Brief 64

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QUARTUS™ Altera Corporation 101 Innovation Drive San Jose, CA 95134 (408) 544-7000 http://www.altera.com https://websupport.altera.com The Quartus[™] software version 2000.02 is now shipping to all Altera customers with a current subscription. This latest version of the Quartus software features significant timing-driven compilation (TDC) enhancements and new device support. This technical brief details key features available in the Quartus software version 2000.02.

New TDC Algorithms Improve Performance

The optimized compilation algorithms in the Quartus software version 2000.02 improve design performance (f_{MAX}) by over 40% for designs that target high-density APEXTM devices (i.e., EP20K400E and larger devices).

The Quartus software version 2000.02 has compiler setting options that allow designers to separately assign timing constraints for both I/O settings and internal (core) logic. Figure 1 shows the Compiler dialog box for setting this option.

Figure 1. Compiler Settings Dialog Box

General Chips & Devices Mo	de Synthesis & Fitting Verification
Specify options for logic synthe entity that is the current compile	esis and fitting. These options apply to all logic within the ation focus.
Changes apply to Compiler sett	tings 'filtref'
Timing-driven compilation	
Optimize 1/0 timing	
Dptimize internal timing	Normal compilation
	Normal compilation
	Extra effort

TDC for I/O Timing

The I/O timing optimization option allows designers to set the clock setup time (t_{SU}) and the clock-to-output delay (t_{CO}) assignments. To meet timing requirements, these assignments force the Quartus Compiler to implement input and output registers in respective I/O cells. Designers can improve on-chip and off-chip system performance by using this timing specification option.

TDC for Internal (Core) Timing

The internal timing optimization option maintains the user's timing assignments, including inverted clocks and relationships between different clocks. There are two settings for this optimization option: **Normal compilation** (default setting) and **Extra effort**.

Table 1 lists the Quartus software version 2000.02 Compiler settings and compares the results with those of the Quartus software version 1999.10.

Table 1. Performance Improvements for Each Compiler Setting in the Quartus Software Version 2000.02			
Compiler Settings Enabled	Quartus Version 2000.02 Performance Results		
No TDC setting	20% faster compilation time with no impact on f _{MAX}		
TDC internal timing optimization, normal compilation setting	15% faster \mathbf{f}_{MAX} with no impact on compilation time		
TDC internal timing optimization, extra effort setting	Over 40% faster f_{MAX} with longer compile times (up to twice as long)		
TDC I/O timing optimization setting	Compiles for optimum ${\boldsymbol{t}}_{{\boldsymbol{S}}{\boldsymbol{U}}}$ and ${\boldsymbol{t}}_{{\boldsymbol{C}}{\boldsymbol{O}}}$ without affecting compile time		

Setting the TDC option to **Extra effort** forces the Compiler to work harder and provide a faster f_{MAX} ; however, this setting increases the design's compilation time.

New Device Support

Table 2 shows the new APEX 20K and APEX 20KE devices that the Quartus software version 2000.02 supports.

Table 2. New Device Support for the Quartus Software Version 2000.02 Note (1)			
Support	Device	Packages	
Full Device Support (Compilation, Simulation, Pin-Out, and Programming Support)	EP20K200-X	240-pin RQFP	
	EP20K400 (2)	652-pin BGA	
		Industrial grade	
	EP20K400E-X	672-pin FineLine BGA [™]	
Advanced Device Support	EP20K100-X	144-pin TQFP, 208-pin PQFP,	
(Compilation, Simulation, and Pin-Out		240-pin PQFP, 324-pin FineLine BGA,	
Support Only)		356-pin BGA	
	EP20K200-X	208-pin RQFP, 356-pin BGA,	
		484-pin FineLine BGA, 652-pin BGA, 672-	
		pin FineLine BGA	
	EP20K300E-X	652-pin BGA, 672-pin FineLine BGA	
Advanced Device Support	EP20K60E	144-pin TQFP, 208-pin PQFP,	
(Compilation and Simulation Support		240-pin PQFP, 356-pin BGA,	
Only)		324-pin FineLine BGA	
	EP20K60E-X	144-pin TQFP, 208-pin PQFP,	
		240-pin PQFP, 356-pin BGA,	
		324-pin FineLine BGA	

Notes:

(1) APEX 20K and APEX 20KE device package types include power quad flat pack (RQFP), ball-grid array (BGA), plastic quad flat pack (PQFP), and thin quad flat pack (TQFP).

(2) For -2 speed grade devices only.

Other New Features

The Quartus software version 2000.02 includes drivers that allow you to use the ByteBlaster MV^{TM} download cable with the Windows 98 operating system.

Conclusion

Featuring TDC enhancements that allow designers to separately specify I/O and internal timing constraints, the Quartus software version 2000.02 increases the flexibility and design performance for high-density APEX 20K designs. The optimized compilation algorithms in the Quartus software version 2000.02 can improve f_{MAX} in high-density APEX devices by over 40%. The Quartus software version 2000.02 also supports new APEX 20K and APEX 20KE devices.



For more information on the Quartus software version 2000.02, see the Quartus web site at http://websupport.altera.com or contact your local Altera sales representative.



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