Design Fitting: MAX 7000AE vs. ispLSI 2000VE Devices

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Introduction

An important criteria in selecting a programmable logic device (PLD) is its success rate for implementing, or fitting, designs. Measuring this success rate is a way of determining a device architecture's flexibility and the effectiveness of its implementation software. A good architecture and software combination yields a high success rate, whereas a poor architecture and software combination yields a low success rate. Combined with the MAX+PLUS® II development software, MAX® 7000AE devices offer superior fitting results compared to Lattice's ispLSI 2000VE architecture and the ispEXPERT implementation software.

This technical brief compares the ability of Altera® MAX 7000AE devices and Lattice ispLSI 2000VE devices to fit benchmark designs. Table 1 lists the features of both devices.

Table 1. MAX 7000AE vs. ispLSI 2000VE Devices

Features	Altera MAX 7000AE	Lattice ispLSI 2000VE
Macrocells	Up to 512	Up to 192
Product terms per macrocell	Up to 32	Up to 20
Clock inversion	Yes	No
Asynchronous clocking	1 per macrocell	1 per 4 macrocells
Shareable expanders	Yes	No
Parallel expanders	Yes	Yes

Benchmark Experiment

In a recent benchmark study, Altera tested the ability of EPM7128AE devices and ispLSI 2128VE devices to fit a suite of benchmark designs. These benchmark tests consisted of 23 VHDL designs with requirements ranging from 70 to 128 macrocells and 35 to 94 I/O pins. Table 2 shows the synthesis and place-and-route tools used to conduct the benchmark tests.

Table 2. Development Tools Used in Benchmark Tests *Note (1)*

Device	Synthesis	Place & Route
EPM7128AE-5	Synopsys FPGA Compiler II version 3.2.0	Altera MAX+PLUS II version 9.5
ispLSI 2128VE-180	Synopsys FPGA Compiler II version 3.2.0	Lattice ispEXPERT version 7.1

Note:
(1) All designs were compiled using area optimization settings.

The tests show that Altera EPM7128AE devices provide superior fitting results over Lattice ispLSI 2128VE devices (see Figure 1). The EPM7128AE device successfully fit all 23 tested designs, but the ispLSI 2128VE device fit only 16 of the 23 designs.

Figure 1. Benchmark Design Implementation Results

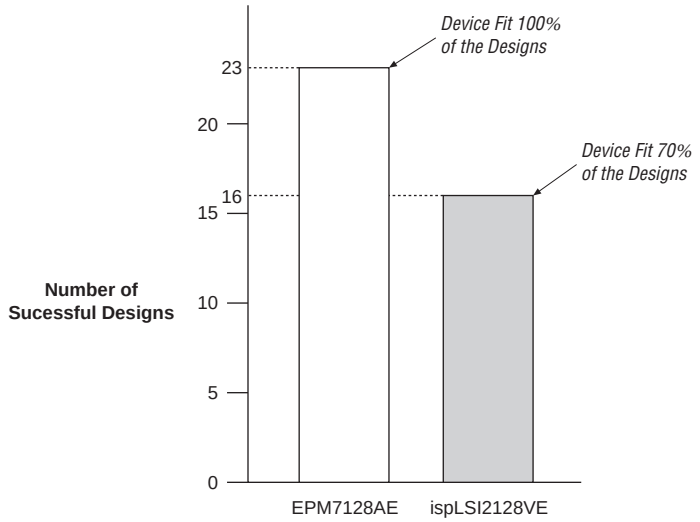

Table 3 shows the reasons these fit-failures occurred in the ispLSI 2128VE device.

Table 3. Reasons for ispLSI 2128VE Device Implementation Failures

Reason	Number of Failed Designs
High macrocell utilization	2
Failed to route	5

In two failed designs in the ispLSI 2128VE device, macrocell utilization exceeded the number of macrocells available. Although these failures may be caused by a synthesis problem rather than an architecture problem, Altera's EPM7128AE device successfully fit all designs using the same synthesis software. Therefore, the ispLSI 2128VE fitting-failures most likely occurred as a result of its rigid architecture.

A failure to route was the primary cause of five other unsuccessful fitting attemps. There are two possible reasons why these routing failures occurred: lack of sufficient routing within the architecture or the implementation software's inability to properly place-and-route the device. It is difficult to pinpoint which of the two types of routing failures occured, thus stressing the need for both a feature-rich architecture and robust software. The Altera EPM7128AE device successfully routed all of the designs, demonstrating its superior software and architecture solution.

Conclusion

Recent benchmark tests demonstrate that MAX 7000AE devices offer superior fitting results over the Lattice ispLSI 2000VE devices. The MAX 7000AE architecture, combined with the advanced MAX+PLUS II development system, provides added flexibility for your designs.

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