HDL Simulation with the Model*Sim*–Altera Software

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Introduction

Altera now provides all customers who have an active subscription with a full-featured Altera® version of the Mentor Graphics Corporation's Model*Sim*-Altera version 5.3c software. This world-class simulation software allows designers to verify their hardware description language (HDL) design and enhances designer productivity.

All customers who have an active subscription will receive the Model*Sim*–Altera software version 5.3c with their Quartus™ version 2000.05 software upgrade shipment.

Model*Sim*–Altera Version 5.3c Software Features

The Model*Sim*–Altera software includes the following features:

- Support for tool command language (Tcl) scripts
- Functional simulation capability for HDL designs before synthesis or place and route
- Timing simulation capability with the VHDL or Verilog HDL output files (VHO, VO) along with the Standard Delay Format (SDO) File generated from the Quartus or MAX+PLUS® II software
- Complete debugging environment with an intuitive user interface
- VHDL and Verilog HDL test bench support
- IEEE VHDL 1076 - '87 and '93, IEEE Verilog 1264 - '95 and the SDF specifications 1.0, 2.0 and 2.1 compliant
- Supports both Windows (Windows 98/NT) and Unix environments (Solaris and HP-UX)

Advanced Capabilities for Quartus & MAX+PLUS II Software Users

Altera customers now have access to world-class simulation software with extensive test bench support in VHDL and Verilog HDL. VHDL and Verilog HDL cannot be mixed. Designers must specify their HDL simulation environment when requesting a license file for the Model*Sim*–Altera software.

Support for Tcl Scripts

The Model*Sim*–Altera software supports Tcl scripts for automating simulation between multiple design revisions and simulations. The Tcl script files can open windows, transfer signals to the waveform viewer, set initial values before simulation, provide stimulus interactively to signals, define breakpoints, and report errors.

Functional & Timing Simulation

Users now have the ability to functionally simulate their HDL designs in the Model*Sim*–Altera software before synthesis or place and route. Functional models (**220model.vhd**, **220model.v**) for the library of parameterized modules (LPMs) and other megafunctions (CAM, PLL, LVDS) are available with the Quartus or MAX+PLUS II software and are installed in the **EDA/sim_lib** and **lpmsim** directories, respectively.

Users can perform timing simulations in the Model*Sim*–Altera software with the VHDL or Verilog HDL output files (.**vho** and .**vo**) along with the SDF File (.**sdo**), generated from the Quartus or MAX+PLUS II software. The same test bench used for the functional simulation can be reused with little or no modifications.

Easy-to-Use Debugging Interface

The Model*Sim*–Altera software provides a complete debugging environment with an intuitive user interface. The interface includes a waveform viewer, source code editor, signal and variable viewer, and hierarchy structure viewer. Designers can view and monitor signals and variables in different levels of the hierarchy.

VITAL Compliant

The Model*Sim*–Altera software is VITAL compliant, but does not contain VITAL or RTL acceleration primitives. The Model*Sim*–Altera software is fully compliant with the IEEE VHDL 1076-'87 and '93, IEEE Verilog 1264-'95 language specifications and the SDF specifications 1.0, 2.0 and 2.1.

Advantages of HDL Test Benches

The Model*Sim*–Altera software gives designers advanced test-bench capabilities for faster simulation and faster time-to-market. Designers can write test benches in the same language as the design source code, i.e., VHDL or Verilog HDL, as the original design. Since VHDL and Verilog HDL are IEEE standardized languages, the models and test benches work with different design tools available on the market today.

Module Stimulus

Test benches can apply stimulus to a module and monitor its outputs. Test benches can monitor outputs and appropriate messages or warnings can be displayed as required by the user. Interactive test benches monitor the current outputs from the module under test and a new set of stimuli can be applied based on current outputs.

Code Re-Usability

Designers can also use functions and procedures in HDL test bench code. By using generalized functions and procedures, code can be reused. When an older design is being updated, the same test bench can be used with little modification. In most cases, test benches used for simulating RTL code can be used for timing simulation without any modifications.

Conclusion

The Model*Sim*–Altera software enhances designer productivity by providing the designer with powerful verification capabilities. With advanced features such as test bench support and a complete debugging environment, the Model*Sim*–Altera software allows designers to quickly integrate system-on-a-programmable-chip designs.

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