Simulating the a6402 Model

with the Visual IP Software

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Introduction

Altera® intellectual property (IP) MegaCore™ functions are developed and pre-tested by Altera, and are optimized for specific Altera device architectures. You can test-drive these functions for free via the OpenCore™ feature by downloading the functions from the Altera web site and installing them on your PC or UNIX workstation. To help in your evaluation, Altera also provides Visual IP simulation models for these functions.

The Visual IP software from Innoveda lets you create simulation models that can be used in third-party VHDL and Verilog HDL simulation tools. Altera distributes the Visual IP software for the end user along with Visual IP models of Altera IP functions.

Altera's Visual IP models are parameterizable, RTL level, functional simulation models. The models let you instantiate Altera IP in your design and simulate it in your choice of simulation tool. This user guide describes how to install and use the Visual IP simulation model for the Altera `a6402` universal asynchronous receiver / transmitter (UART).

Before using the `a6402` model, you must download and install the Visual IP software, which is available for free from the Altera IP MegaStore site at **http://www.altera.com/IPmegastore**. Follow the instructions in the *Installing the Visual IP Software User Guide*.

Altera recommends that you also obtain the *a6402 Universal Asynchronous Receiver/Transmitter Data Sheet* from the Altera web site. This data sheet describes the technical specifications of the `a6402` function.

The a6402 Visual IP model contains the following elements:

Table 1. a6402 Visual IP Model Elements

Element	Description
a6402.*	The VHDL or Verilog HDL a6402 UART MegaCore function model file.
A6402_vectors.*	A set of VHDL or Verilog HDL test vectors.
A6402_top.*	Top-level VHDL or Verilog HDL file that references the a6402 function and test vectors.

Download the Models

If you have not already done so, download Visual IP models from Altera's web site at **http://www.altera.com** by following the instructions below.

1. Point your web browser to **http://www.altera.com/IPmegastore**.
2. Search in the IP MegaStore for the function / model you wish to obtain.
3. On the search results page, click the name of the function / model you wish to obtain.
4. Click the Free Test Drive icon and follow the on-line instructions to download the function and / or model.

PC Installation

Execute the **a6402_vip_pc.exe** file and follow the on-line instructions to install the model. The following files are installed:

<*installation path*>**\vip_simulation\A6402**
- **doc**
  - **a6402_vipug.pdf**
- **verilog**
  - **A6402.v**
  - **A6402_vectors.v**
  - **A6402_top.v**
- **vhdl**
  - **mti**
    - **A6402.vhd**
    - **A6402_vectors.vhd**
    - **A6402_top.vhd**
  - **leapfrog**
    - **A6402.vhd**
    - **A6402_vectors.vhd**
    - **A6402_top.vhd**

vss
A6402.vhd
A6402_vectors.vhd
A6402_top.vhd
<*installation path*>**\vip_models\a6402***

Before using the Visual IP model, set the VIP_MODELS_DIR environment variable to <*installation path*>**/vip_models**. The installation process sets all other required environment variables in the system registry.

All Altera Visual IP models use the VIP_MODELS_DIR environment variable. If you only wish to use one Visual IP model, you can install the model into any directory and set up the variable to point to that directory. However, if you wish to use several models (e.g., both the a6402 and a8259 models) you should install all Visual IP models into the same directory.

Solaris Installation

The a6402 model is a tape archive file (**.tar**) that has been compressed using the **gzip** utility. To extract the files, move the **a6402_vip_solaris.tar.gz** file to the location in which you would like to install the models and type the following commands at a UNIX prompt:

```
gunzip a6402_vip_solaris.tar.gz ↵
tar xvf a6402_vip_solaris.tar ↵
```

The following directories and files are created:

<*installation path*>**/vip_simulation/A6402/**
setup.csh
doc/
a6402_vipug.pdf
verilog/
A6402.v
A6402_vectors.v
A6402_top.v
vhdl/
mti/
A6402.vhd
A6402_vectors.vhd
A6402_top.vhd
leapfrog/
A6402.vhd
A6402_vectors.vhd
A6402_top.vhd
vss/
A6402.vhd

A6402_vectors.vhd
A6402_top.vhd
<*installation path*>**/vip_models/a6402/***

Before using the Visual IP models, performperform the following steps:

1. Set the VIP_MODELS_DIR environment variable to <*installation path*>**/vip_models**.

   ☞ All Altera Visual IP models use the VIP_MODELS_DIR environment variable. If you only wish to use one Visual IP model, you can install the model into any directory and set up the variable to point to that directory. However, if you wish to use several models (e.g., both the a6402 and a8259 models) you should install all Visual IP models into the same directory.

2. Set the VIP_EU_ROOT environment variable to the root directory in which you installed the Visual IP software.

3. Source the **setup.csh** file to complete the configuration of the Visual IP environment.

Running Test Vectors

This section describes how to use the test vectors provided with the a6402 simulation model.

Verilog HDL

If you are using Verilog HDL, perform the following steps:

1. Set up the Visual IP PLI interface as described in *Installing the Visual IP software User Guide*.

2. Make sure the VIP_MODELS_DIR environment variable is set properly.

3. Change to the <*installation path*>**/vip_simulation/A6402/verilog** directory.

4. Compile the **A6402.v** and **A6402_vectors.v** files. These modules attach to the appropriate Visual IP models using the Verilog-XL PLI interface.

5. Compile the **A6402_top.v** file.

6. Simulate **A6402_top**.

VHDL

If you are using VHDL, perform the following steps:

1. Set up the Visual IP C language interface as described in *Installing the Visual IP software User Guide*.
2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.
3. Change to the directory <*installation path*>**/vip_simulation/A6402/vhdl/**<*simulator*>, where <*simulator*> is to the VHDL simulation tool you are using.
4. Compile the **A6402.vhd** and **A6402_vectors.vhd** files into your work library. These components attach to the appropriate Visual IP models using the C language interface of your VHDL simulator.
5. Compile the **A6402_top.vhd** file into your work library.
6. Simulate **work.A6402_top(struct)**.

Using the a6402 Model

This section describes how to use the `a6402` simulation model in your designs.

Verilog HDL

If you are using Verilog HDL, perform the following steps:

1. Set up the Visual IP PLI interface as described in *Installing the Visual IP software User Guide.*
2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.
3. Go to the <*installation path*>**/vip_simulation/A6402/verilog** directory
4. Compile **A6402**. This module attachs to the appropriate Visual IP model using the Verilog-XL PLI interface.
5. Instantiate **A6402** in your Verilog HDL design.

VHDL

If you are using VHDL, perform the following steps:

1. Set up the Visual IP C language interface as described in *Installing the Visual IP software User Guide*.
2. Make sure the `VIP_MODELS_DIR` environment variable is set properly.
3. Go to the<*installation path*>**/vip_simulation/A6402/vhdl/**<*simulator*> directory, where <*simulator*> is the VHDL simulation tool you are using.
4. Compile **A6402.vhd** into your work library. This component attaches to the appropriate Visual IP model using the C language interface of your VHDL simulator.
5. Instantiate **work.A6402(behave)** in your VHDL design.

Known Issues

Visual IP models do not support checkpoint/restart. Therefore, you must reload the simulation model to restart the simulation.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com