

The Visual IP software from Innoveda lets you create simulation models that can be used in third-party VHDL and Verilog HDL simulation tools. Altera distributes the Visual IP software for the end user along with Visual IP models of Altera IP functions. This guide describes how to install the Visual IP software on PCs and UNIX workstations.

Installing on PCs

This section describes the system requirements and installation process for the Visual IP software on Windows PCs.

Installation Requirements

The Visual IP software requires a Pentium-based PC that has:

- At least 64 MBytes of RAM, 88 MBytes is recommended
- Windows NT 4.0, Windows 95, or Windows 98
- At least 200 MBytes of free disk space
- A SuperVGA display (800 x 600 is the recommended working resolution)

Download the Software

To download the software, perform the following steps:

1. Point your web browser to <http://www.altera.com/IPmegastore>.
2. Click the Functional Simulation link in the **IP Tools** section.
3. Follow the on-line instructions to download the software.

Running the Installation Script

The installation procedure for the Visual IP software is the same for Windows 95, Windows 98, and Windows NT 4.0.



Network users should use a 32-bit network protocol to take advantage of new file naming features such as case sensitivity and unlimited name length.

To install Visual IP for Windows, perform the following steps:

1. Place the Visual IP CD-ROM into your PC's CD-ROM drive.
2. Choose **Run** from the **Start** menu; the **Run** dialog box appears.
3. Type `<CD-ROM drive letter>:\VisualIPEndUser<version>.exe` and click **OK**.
4. Follow the on-screen instructions.



The default installation directory is `C:\VIP_EndUser<version>`; you can change this directory if you wish.

The default folder in which the Visual IP icons appear is named Visual IP End User `<version>`; you can change this folder name if you wish.

Linking to a Host Simulator

The following sections describe how to link the Visual IP software to different host simulators.

ModelSim for VHDL

Before invoking the *ModelSim* for VHDL simulator, you must link it to the Visual IP software by adding both the Visual IP binary directory and the *ModelSim* binary directory to your path:

```
set path=c:\VIP_EndUser_<version>\bin;c:\ModelSim\bin\;  
%path% ←
```

ModelSim for Verilog HDL

Before invoking the *ModelSim* for Verilog HDL simulator, perform the following steps:

1. Link to the Visual IP software by adding a **veriuser** entry pointing to the shared file `<installation path>\bin\libplimtivip`.

You can also use the **vsim -pli** command line option or the `PLIOBJS` environment variable. See the *ModelSim* documentation for more information.

2. Before invoking the ModelSim for VHDL simulator, you must link it to the Visual IP software by adding both the Visual IP binary directory and the ModelSim binary directory to your path:

```
set path=c:\VIP_EndUser_<version>\bin;  
c:\ModelSim\Win32\; %path% ↵
```

Installing on UNIX Workstations

This section describes the system requirements and installation process for the Visual IP software on UNIX workstations.

The procedures in this document use > to represent the system prompt (which you do not type) at the start of a command. If a command is split over two lines, you should still enter it as a single line following the system prompt.

System Requirements

To run the Visual IP software, you need a workstation that meets the following system requirements:

- At least 32 MBytes of RAM
- Solaris 2.5.1 or higher
- At least 70 MBytes of free disk space
- At least 50 MBytes of swap space (more is required if your IP models are more complex)

Download the Software

To download the software, perform the following steps:

1. Point your web browser to <http://www.altera.com/IPmegastore>.
2. Click the Functional Simulation link in the **IP Tools** section.
3. Follow the on-line instructions to download the software.

Running the Installation Script

The Visual IP software for UNIX is a tape archive file (**.tar**) that has been compressed using the **gzip** utility. To extract the files, move the **VIP_EndUser_<version>.tar.gz** file to the location in which you would like to install the models and type the following commands at a UNIX prompt:

```
gunzip VIP_EndUser<version>.tar.gz ↵  
tar xvf VIP_EndUser<version>.tar ↵
```



After you run the script, you can refer to the **readme** file at `<path>/VIP_EndUser_<version>/README/README_USER`.

Linking to a Host Simulator

The following sections describe how to link the Visual IP software to different host simulators. Innoveda provides a setup script for setting the environment variables Visual IP software needs when simulating an embedded IP function. You should run this script before invoking any of the host simulators listed below. To run the script, do the following steps:

1. Make sure you are using a C shell.
2. Create a command history buffer by typing the following command:

```
set history=n ↵
```

where *n* is the number of lines to buffer (must be greater than or equal to 1).

3. Change to `<path>/VIP_EndUser_<version>/<platform>/bin/`, where `<path>` is the location in which you installed the Visual IP software, `<version>` is the Visual IP version, and `<platform>` is **SunOS5** or **hp10**.
4. Execute the command:

```
> source vip.setup ↵
```

Verilog-XL

Before invoking the Verilog-XL simulator, you must link it to the Visual IP software by building a new **verilog** executable. Perform the steps below to build a new executable.

1. Run the **vip.setup** script as described previously.
2. If you plan to use Altera's Visual IP model in a design that already uses PLI functions, you must merge the Visual IP **veriuser_vip.c** and **veriuser.c** files with your versions of these files before building the new **verilog** executable.

- a. Copy the following lines from `<path>/VIP_EndUser_<version>/<platform>/veriuser_vip.c` to your `veriuser.c` file:

```
extern int Vip_pli_checktf ();
extern int Vip_pli_calltf ();
extern int Vip_pli_misctf ();
```

- b. Add the following information to your `veriusertfs` table:

```
{usertask, 0, Vip_pli_checktf, 0, Vip_pli_calltf,
  Vip_pli_misctf, "$Vip_pli_entry", 1},
```

3. Invoke **vconfig** to build a script.
4. Answer **Yes** to the question "Do you want to include the CDC in this Verilog-XL executable?" (The default answer is **No**.)
5. If you are using PLI, point to your edited `veriuser.c` file to your file list when prompted. If you are not using PLI, add the file:

```
<path>/VIP_EndUser_<version>/<platform>/verilog_src/
  veriuser_vip.c
```

6. Add the following file to the list of files when you are prompted:

```
<path>/VIP_EndUser_<version>/<platform>/verilog_src/libvip_pli.a
```

7. Finish building the executable as usual by running the script created by **vconfig**.



If you are using Verilog-XL version 2.6.x or higher on a workstation running Solaris or HP-UX, you can dynamically link the Visual IP software with your host simulator. To do so, reference the shared library:

```
<path>/VIP_EndUser_<version>/<platform>/lib/libpli.so
```

Leapfrog

Before invoking the Leapfrog simulator, you must link it to the Visual IP software by performing the steps below.

1. Run the **vip.setup** script as described previously.
2. If you are using FMI, add the following lines to your **table.c** file before creating the **libfmi** library. You can copy these lines from `<path>/VIP_EndUser_<version>/<platform>/vhdl_src/lfguser_vip.c`.

- a. Add the line:

```
extern fmiModelTableT VipLibModelTable;
```

- b. Add the following text to **fmiLibraryTableT**:

```
{ "Viplib", VipLibModelTable },
```

3. When you compile and link your model, add `<path>/VIP_EndUser_<version>/<platform>/vhdl_src/libvip_fmi.a` to the list of files that you provide.

ModelSim for VHDL

Before invoking the ModelSim for VHDL simulator, you must link it to the Visual IP software by performing the following steps:

1. Run the **vip.setup** script as described previously.
2. Add the Visual IP library directory to your `LD_LIBRARY_PATH` environment variable by typing the following command:

```
setenv LD_LIBRARY_PATH <installation  
path>/<platform>/lib:$LD_LIBRARY_PATH ←
```

ModelSim for Verilog HDL

Before invoking the ModelSim for Verilog HDL simulator, you must link it to the Visual IP software by performing the steps below.

1. Run the **vip.setup** script as described previously.
2. Add a **veriususer** entry pointing to the shared library `<path>/VIP_EndUser_<version>/<platform>/lib/libplimtivip.so`. You can also use the **vsim -pli** command line option or the `PLIOBJS` environment variable. See the ModelSim documentation for more information.

VCS

Before invoking the VCS simulator, you must link it to the Visual IP software by performing the steps below.

1. Run the **vip.setup** script as described previously.
2. When you compile your model, use the following command-line option to include the files **pli.tab** and **libvip_pli.a**:

```
> -P <path>/VIP_EndUser_<version>/<platform>/
    verilog_src/pli.tab <path>/VIP_EndUser_<version>/
    <platform>/verilog_src/libvip_pli.a
```

VSS

Before invoking the VSS simulator, you must link it to the Visual IP software by performing the steps below.

1. Compile the model interface by running the VHDL analyzer as follows:

```
vhdlan [options] ←
$VIP_MODELS_DIR/<model name>/interface/vss/
<model name>.vhd ←
```

2. Add the compiled model to the list of available model using either of the commands below:

```
cli -add -cv <C filename> <model name> [options] ↵
```

or

```
cli -add -cvl <library name> <C filename> <model name> [options] ↵
```

Where <C filename> is the file `$VIP_MODELS_DIR/<model name>/interface/vss/<model name>.c`

3. Update the VSS simulator with the current model by typing the command:

```
cli -build -libs <installation directory>/VIP_EndUser_<version>/<platform>/vhdl_src/libv ip_vss.a [options] ↵
```

4. Run the **vip.setup** script by performing these steps:
 - a. Change directory to `<installation directory>/VIP_EndUser_<version>/<platform>/bin` where `<platform>` is **SunOS**, **AIX4**, or **HP-UX10**.
 - b. Type `source vip.setup` ↵.

For more information, see “Using the C Language Interface” in the VSS documentation provided by Synopsys.

This version contains updated information and supercedes previous versions.

Version 1.3

This version provides updated instructions for downloading the Visual IP software from the Altera web site.

Version 1.2

This version contains updated path names for the Visual IP installation directory, and instructions for linking the software with the VSS simulator for UNIX. It removes information about linking the software to the VCS simulator on PCs.

Revision History

Version 1.1

This revision contains updated instructions for running the setup script that links the Visual IP software to a UNIX host simulator.



101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>
Applications Hotline:
(800) 800-EPLD
Customer Marketing:
(408) 544-7104
Literature Services:
lit_req@altera.com

Altera, MegaCore, and OpenCore are trademarks and/or service marks of Altera Corporation in the United States and other countries. Altera acknowledges the trademarks of other organizations for their respective products or services mentioned in this document. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

Copyright © 2000 Altera Corporation. All rights reserved.

