White Paper

Reed-Solomon FEC Demonstration

Features

- DVB standard Reed-Solomon (RS) parameters
- Results displayed on LCD
- Demonstrates decoder behavior with exaggerated bit error rates (BERs).

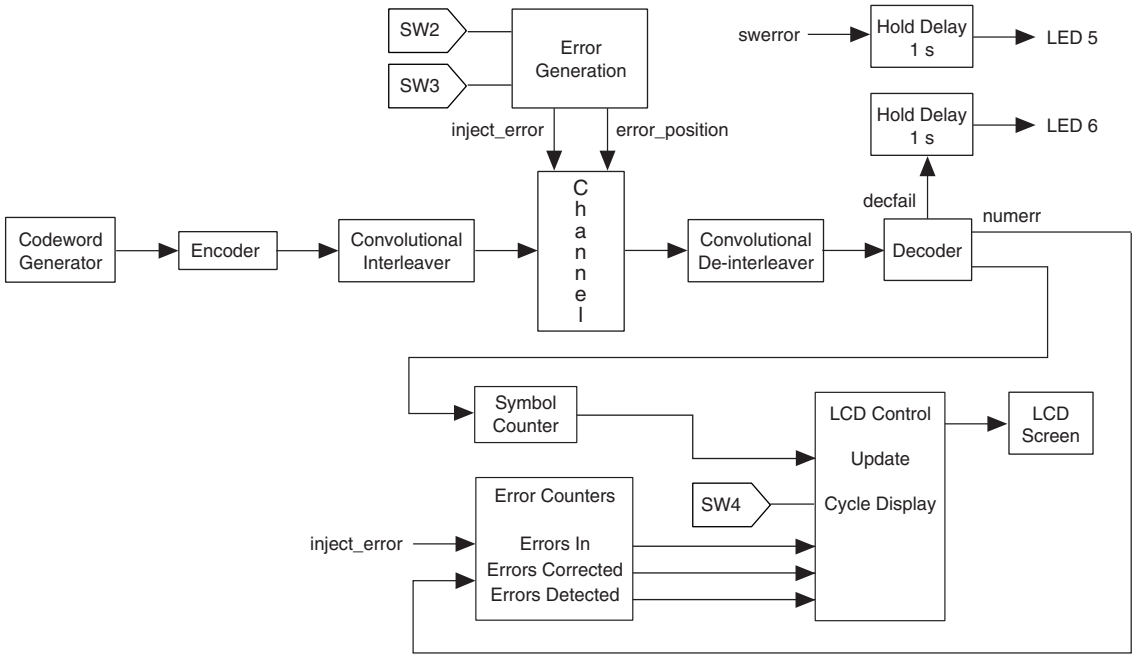
General Description

The RS forward error correction (FEC) demonstration is designed to show the capabilities of the Altera® RS compiler MegaCore™ function in correcting and detecting errors. The demonstration is to be used in conjunction with the system-on-a-programmable-chip (SOPC) board. The SOPC board includes an APEX 20K400E device and an LCD, which allows monitoring and setting-up of the demonstration. The demonstration is a hardware implementation of the reference design supplied with the RS compiler megafunction, with the addition of a modified channel allowing the selection of a BER, and modules to collate and display the error information on the LCD. The RS FEC demonstration codeword generator generates traffic, which passes to the channel via the RS encoder and convolutional interleaver. The error generator introduces channel errors at the selected rate. The codeword is de-interleaved and then enters the RS decoder where the errors are corrected. The number of errors introduced and the number of errors corrected are output to the error counters and the results displayed on the LCD. The interleaver and RS megafunction's parameters are preset to match the DVB standards:

- Half, standard, streaming Reed-Solomon (RS) decoder
- RS parameters:
  - 8-bit symbol width
  - 204 symbols per codeword
  - 16 check symbols
- Interleaver with:
  - Symbol delay of 17
  - Symbol depth of 12

The demonstration runs at 33 or 66 MHz. Figure 1 shows the RS FEC demonstration block diagram.

Figure 1. RS FEC Demonstration Block Diagram



Note:
(1) The hold delay of 1 s is for 33 MHz operation. When 66 MHz operation is used, the hold delay is 0.5 s.

RS FEC Demonstration Walkthrough

To use the RS FEC demonstration you need:

- An SOPC board and the *Advanced SOPC Users Manual*.
- A PC with the Quartus™ software installed.
- ByteBlasterMV™ cable

The *Altera Reed-Solomon Compiler MegaCore Function User Guide* gives further information on the RS megafunction; the *Altera Symbol Interleaver/Deinterleaver MegaCore Function User Guide* gives further information on the interleaver.

1. Connect the power supply to the SOPC board
2. Connect your PC to the SOPC board via a ByteBlasterMV connector (see the *Advanced SOPC Users Manual).*
3. Ensure that JP12 on the SOPC board is set for the desired device; either the APEX device (volatile), or the EPC devices (non-volatile).
4. Set JP9 to pins 2 and 3 (33 MHz operation); or pins 1 and 2 (66 MHz operation).
5. Open the Quartus software and **Open Programmer** (Processing Menu). In the **Mode** drop-down box select **JTAG**. Under **Programming Hardware** click **Setup** (refer to Quartus Help for details on the set-up).

You can now program your selected device as described.

To Program the APEX Device

1 In the programmer click **Add Device**. Select the EP20K400EBC652.

2. Right click on the device, select **Change File**, find and select **RSDEMO.sof** . Click **Start**.

To Program the EPC Devices

1. In the programmer click Add Device. Select EPC2TC32. You need to add three of these devices.

2. Right click on the first device, select **Change File**, find and select RSdemo.pof. Repeat for the other two devices, the files are RSdemo1.pof and RSdemo2.pof. Click **Start**.

3. Cycle the SOPC board power once.

You are now ready to use the demo.

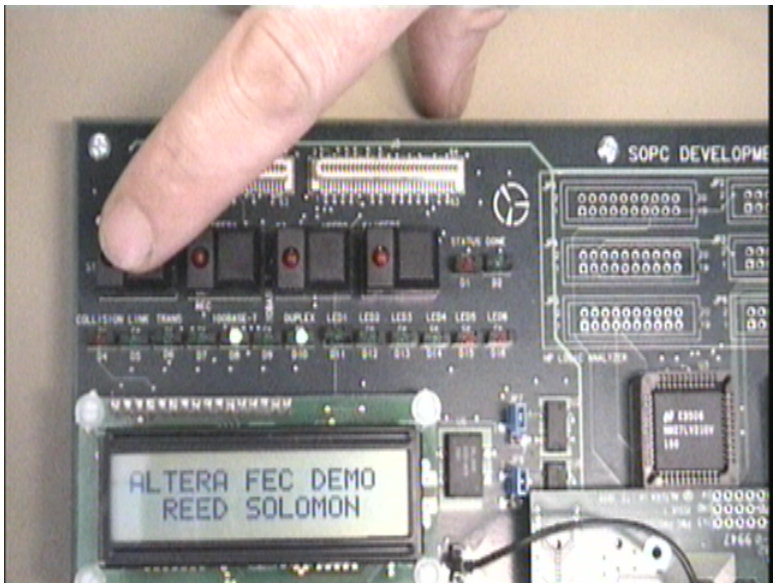
Using the FEC Demo

The SOPC board has four switches, these are:

SOPC Reset (switch 1) – Reset. Used at the start, and to reset the demo at any time
SOPC S2 User1 (switch 2)—Error rate up. Used to increase the BER during setup.
SOPC S3 User 2 (switch 3)—Error rate down. Used to decrease the BER during setup.
SOPC S4 User 3 (switch 4)—Screen cycle. Used to cycle through the LCD screens.

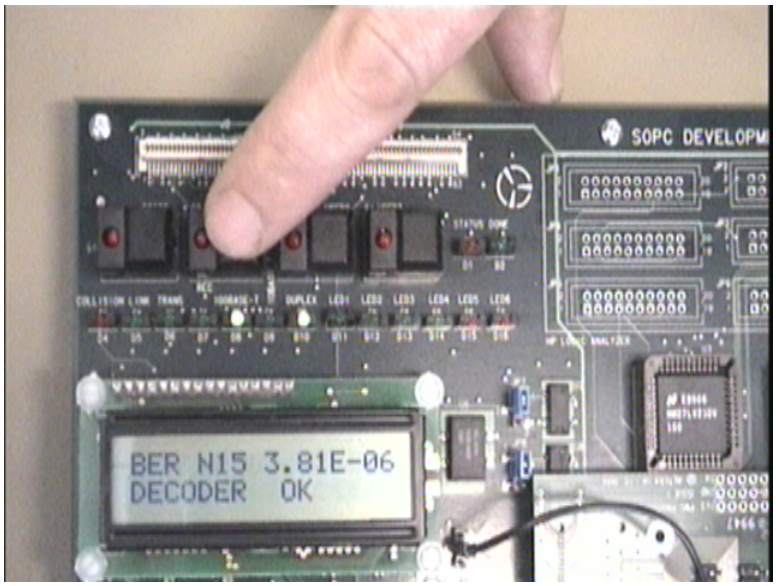
1. Press switch 1 to reset the demonstration (see Figure 2). The LCD reads 'Altera FEC Demo, Reed-Solomon'. Switch 1 can be used at anytime to reset the demo and choose a new BER.

Figure 2. Reseting the Demonstration



2. Press switch 4 once, the LCD reads 'BER N* *.**E–0*, Decoder OK' (see Figure 3). Use switch 2 or switch 3 to select the required BER (see Table 1); switch 2 increases the BER, switch 3 decreases the BER.

Figure 3. Selecting the BER



3. Press switch 4 and the demo starts, the LCD reads 'Errors in *, corrected *' (see Figure 4). Press switch 4 again, the LCD reads 'Errors in *, detected' (see Figure 5). Further pressing of switch 4 cycles through the previous three LCD messages. Pressing switch 1 resets the demo.

Figure 4. Starting the Demonstation

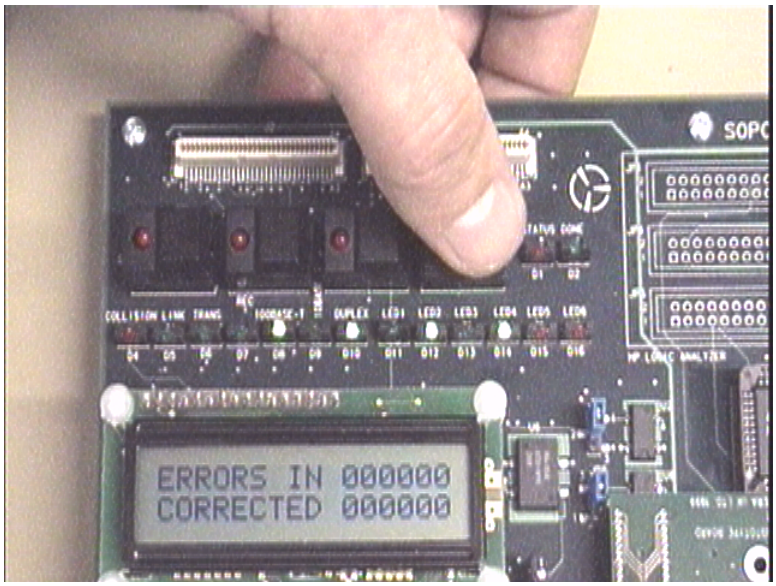
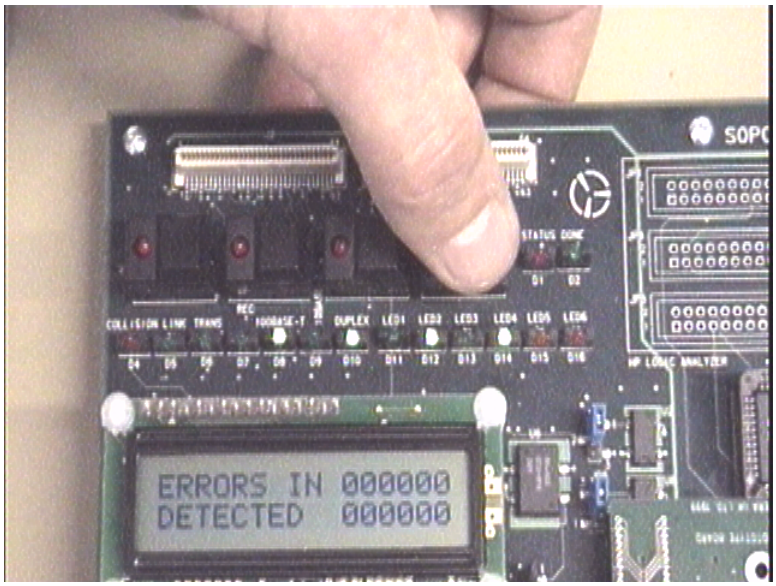


Figure 5. Errors Detected



If the decoder fails (this can be expected for certain exaggerated BERs), LED 6 illuminates red. The LCD is updated once every 1 s (33 MHz operation) or once every 0.5 s (66 MHz operation). If two or more switches are pressed simultaneously, LED 5 illuminates for 1 s to indicate an error.

Table 1. BERs

Error Name	P(Serror) *Note (1)*	BER *Note (2)*	Errors/second	Errors/codeword *Note (3)*
1	5.00E–01	6.25E–02	1.53000E+07	1.02E+02 *Note (4)*
2	2.50E–01	3.13E–02	7.65000E+06	5.10E+01 *Note (4)*
3	1.25E–01	1.56E–02	3.82500E+06	2.55E+01 *Note (4)*
4	6.25E–02	7.81E–03	1.91250E+06	1.28E+01 *Note (4)*
5	3.12E–02	3.91E–03	9.56250E+05	6.38E+00
6	1.56E–02	1.95E–03	4.78125E+05	3.19E+00
7	7.81E–03	9.77E–04	2.39062E+05	1.59E+00
8	3.91E–03	4.88E–04	1.19531E+05	7.97E–01
9	1.95E–03	2.44E–04	5.97653E+04	3.98E–01
10	9.77E–04	1.22E–04	2.98828E+04	1.99E–01
11	4.88E–04	6.10E–05	1.49414E+04	9.96E–02
12	2.44E–04	3.05E–05	7.47070E+03	4.98E–02
13	1.22E–04	1.53E–05	3.73535E+03	2.49E–02
14	6.10E–05	7.63E–06	1.86767E+03	1.25E–02
15	3.05E–05	3.81E–06	9.33837E+02	6.23E–03
16	1.53E–05	1.91E–06	4.66918E+02	3.11E–03
17	7.63E–06	9.54E–07	2.33459E+02	1.56E–03
18	3.81E–06	4.77E–07	1.16729E+02	7.78E–04
19	1.91E–06	2.38E–07	5.83648E+01	3.89E–04
20	9.54E–07	1.19E–07	2.91824E+01	1.95E–04
21	4.77E–07	5.96E–08	1.45912E+01	9.73E–05
22	2.38E–07	2.98E–08	7.29561E+00	4.86E–05
23	1.19E–07	1.49E–08	3.64780E+00	2.43E–05
24	5.96E–08	7.45E–09	1.82390E+00	1.22E–05
25	2.98E–08	3.73E–09	9.11951E–01	6.08E–06
26	0	0	0	0

Notes:

(1) The probability of a symbol error. This is the probability that an error is introduced in to the channel during a symbol.

(2) The BER = P(Serror)/8 for 8-bit symbols.

(3) Errors/codeword = N.P(Serror), where N is the number of symbols per codeword

(4) For this BER the decoder fails. The 16 check symbols only allows the correction of 8 errors per codeword, and the detection of 16 errors.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
http://www.altera.com