White Paper

Turbo Codec FEC Demonstration

Features

- Demonstrates decoder's ability to correct errors—results displayed on LCD
- 32-bit Nios™ embedded processor implementation

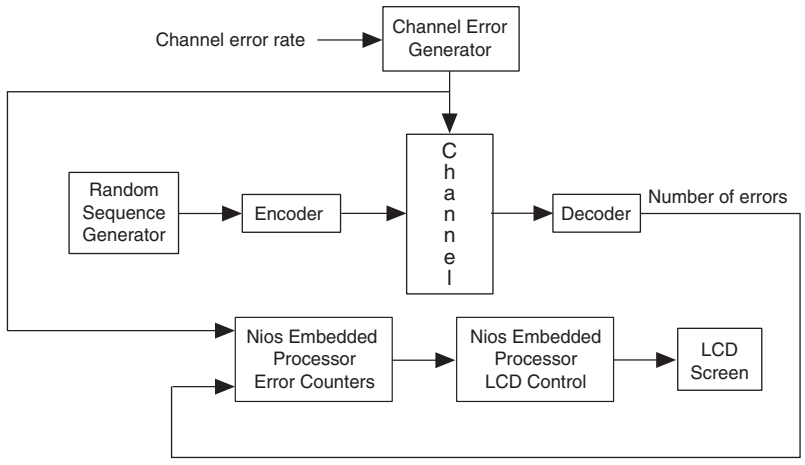
General Description

The turbo encoder/decoder (codec) forward error correction (FEC) demonstration is designed to show the capabilities of the Altera® turbo encoder/decoder MegaCore® function in correcting errors. The demonstration is for use with the system-on-a-programmable-chip (SOPC) board and uses the 32-bit Nios family of soft-core embedded processors. The SOPC board includes an APEX™ 20K400E device and an LCD, which allows you to monitor the demonstration. The Nios embedded processor sets up the codec, controls the channel error rate, and collates and displays the error information on the LCD. The channel error rate is 2^N errors in every 255 bits (where N is cycled from 0 to 7 by the Nios embedded processor). Errors are applied randomly to the information and parity bits as they pass through the channel. The channel error generator is free running, however the turbo codec resets every time there is a change in channel error rate (every 300 ms) and runs for one block. The demonstration runs at 33 MHz. The turbo codec parameters are:

- SOFTBITS = 3
- BLOCK SIZE = 5114
- ITERATIONS = 2

Figure 1 shows the turbo codec FEC demonstration block diagram.

Figure 1. Turbo FEC Demonstration Block Diagram



Walkthrough

To use the turbo FEC demonstration you need:

- An SOPC board with an APEX 20K400E and the *Advanced SOPC Users Manual*
- A PC with the Quartus™ software installed (version 2000.05 or higher) and Microsoft HyperTerminal
- A ByteBlasterMV™ cable
- A 0.64-socket-to-0.64-socket lead
- A female-to-female straight-through serial cable

The *Altera Turbo Encoder/Decoder MegaCore Function User Guide* gives further information on the turbo codec function.

1. On the SOPC board connect JP9 pin 3 to JP11 pin 2, using the 0.64-socket to 0.64-socket lead.

2. Connect the power supply to the SOPC board.

3. Connect your PC to the SOPC board via a ByteBlasterMV connector (see the *Advanced SOPC Users Manual).*

4. Connect COM1 (or COM2) of your PC to J13 on the SOPC board; you need a female-to-female adaptor to do this, as J13 on the SOPC board is male.

5. Ensure that JP12 on the SOPC board is set for the APEX device.

6. Open the Quartus software and **Open Programmer** (Processing Menu). In the **Mode** drop-down box select **JTAG**. Under **Programming Hardware** click **Setup** (refer to Quartus Help for details on the set-up) and select **ByteBlaster**.

You can now program the APEX device as described.

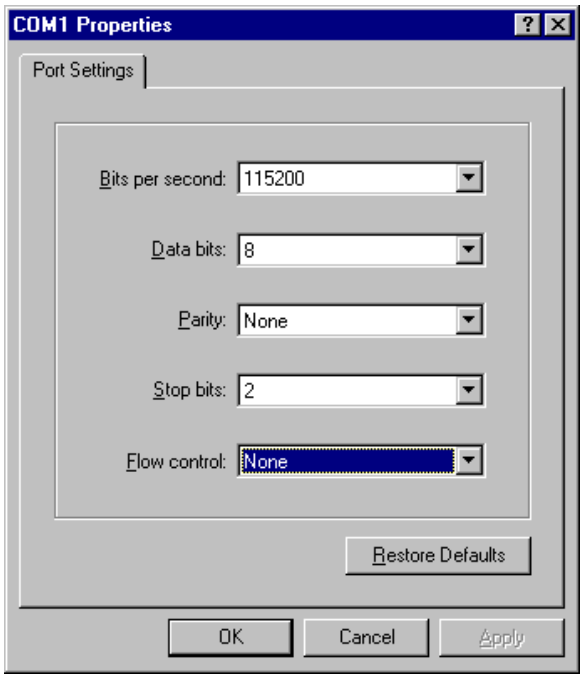
To Program the APEX device

1 In the programmer click **Add Device**. Select the EP20K400EBC652.

2. Right click on the device, select **Change File**, find and select **aukt_sopc_turbo_nios32_top.sof**. Click **Start**.

3. Minimize Quartus and open Microsoft HyperTerminal. Enter a name for the connection, e.g., Nios. In the **Connect To** dialog box, select the relevant COM port. Figure 2 shows the COM port property values. Set the values and click **OK**.

Figure 2. COM Port Properties



4. The SOPC board has four buttons; only SOPC Reset (Button 1) is used. Press SOPC Reset. HyperTerminal displays 'Welcome to Nios. Boot Version 1.6', and LED 5 on the SOPC board flashes at 3 Hz.

5. Select **Send Text File** (**Transfer** menu), find and open the **TurboCodec.srec** file. When you click OK, the demonstration begins.

Using the FEC Demo

Once the demonstration is running, the LCD shows 'Channel Err: ****' and 'Error out: ****'. The first number is the number of channel errors; the second is the number of codec errors.

You can use SOPC reset to reset the demonstration at any time.

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