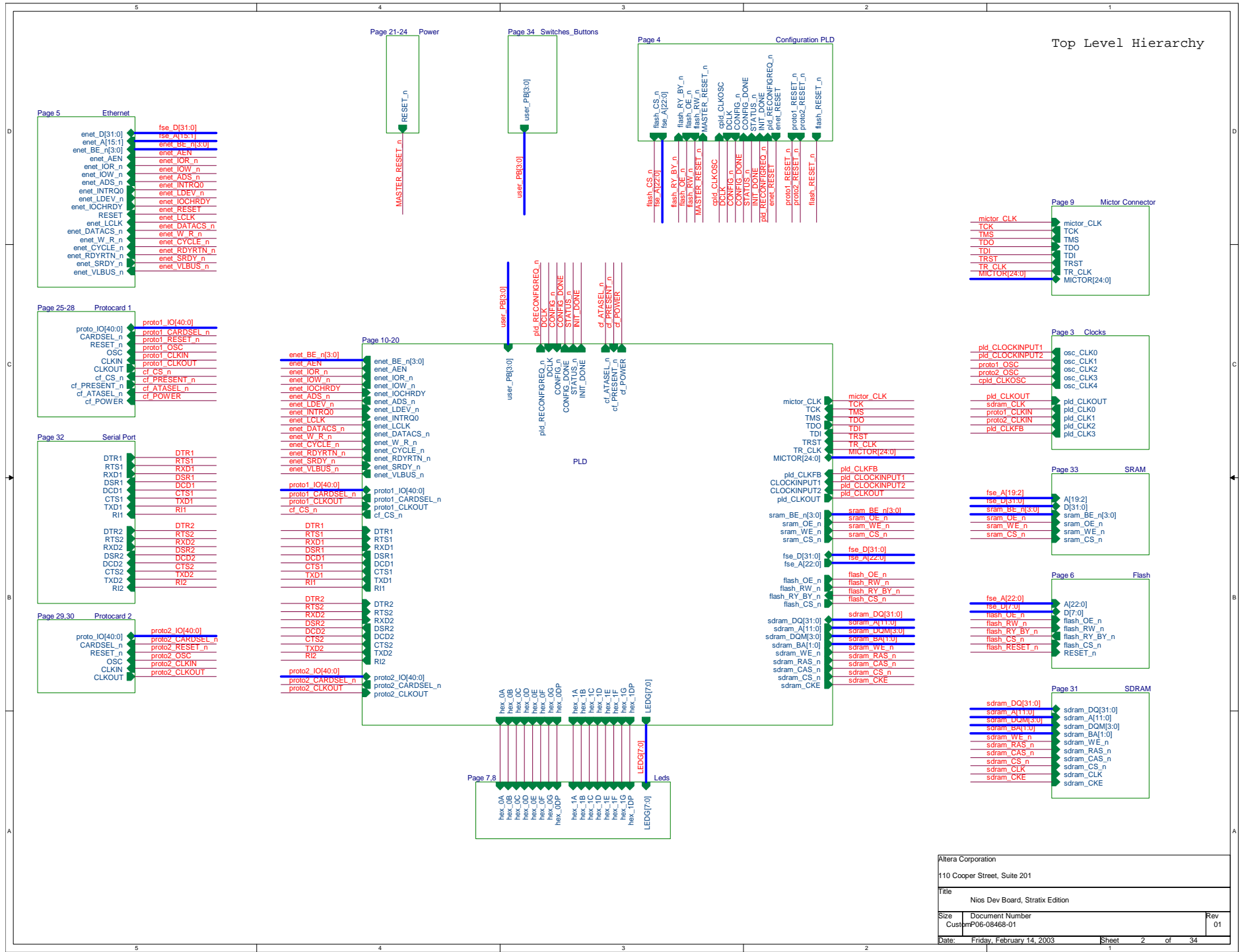


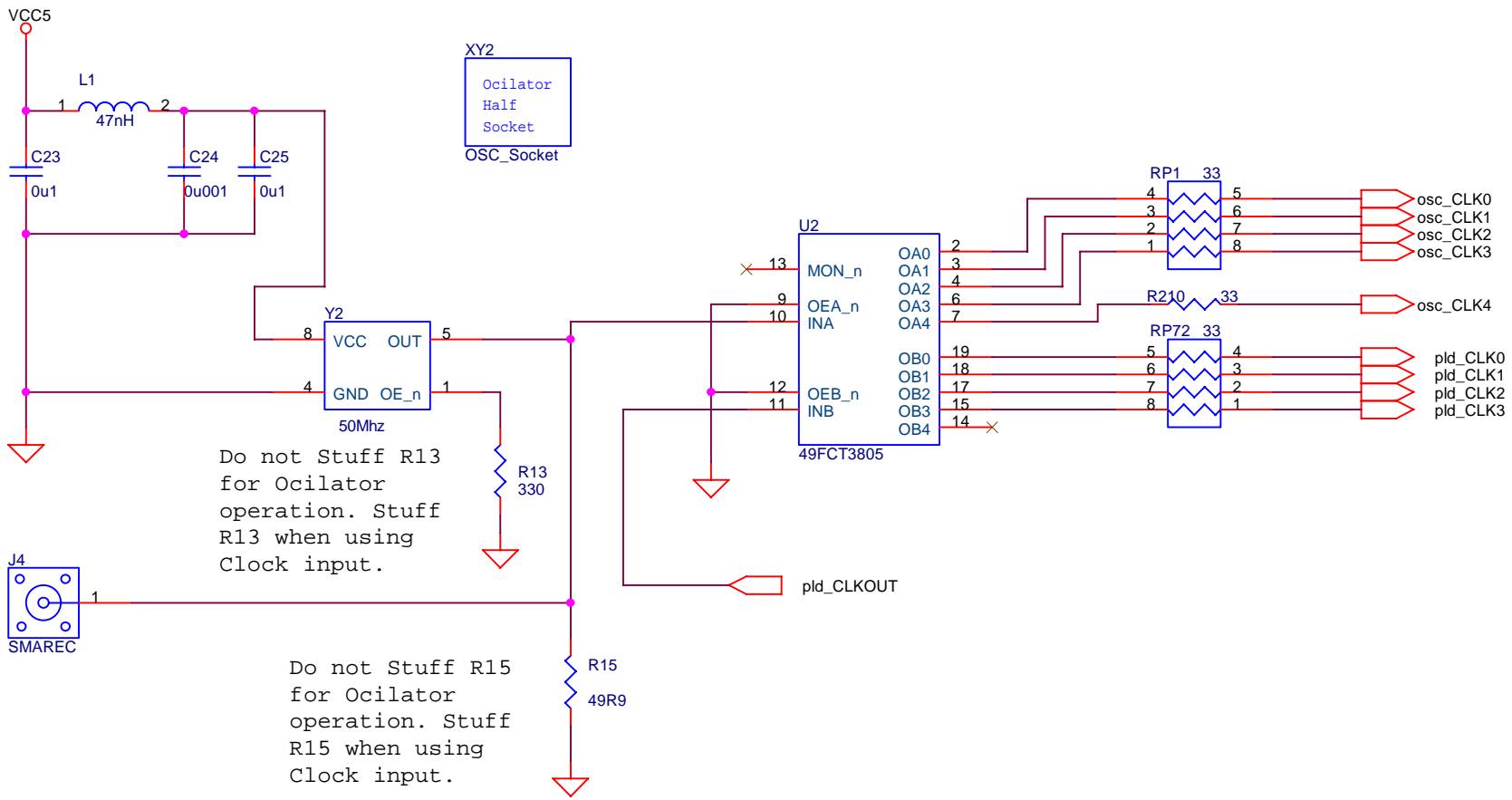
Nios Development Board
Stratix Edition
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Top Level Hierarchy

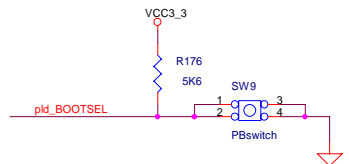
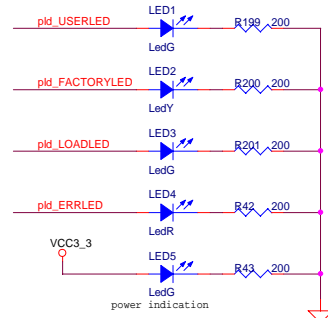
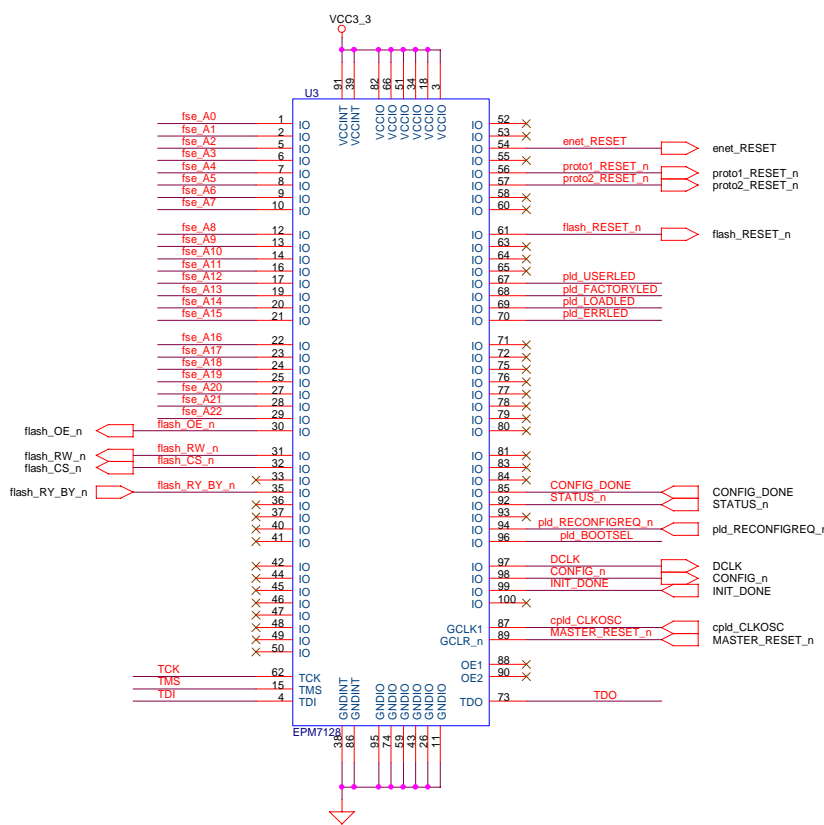


Clocks

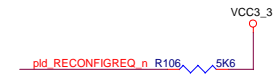
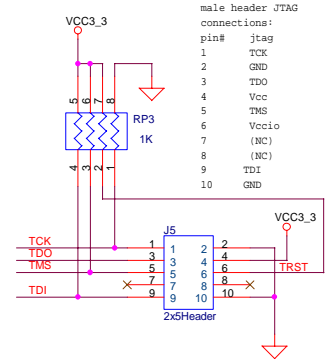


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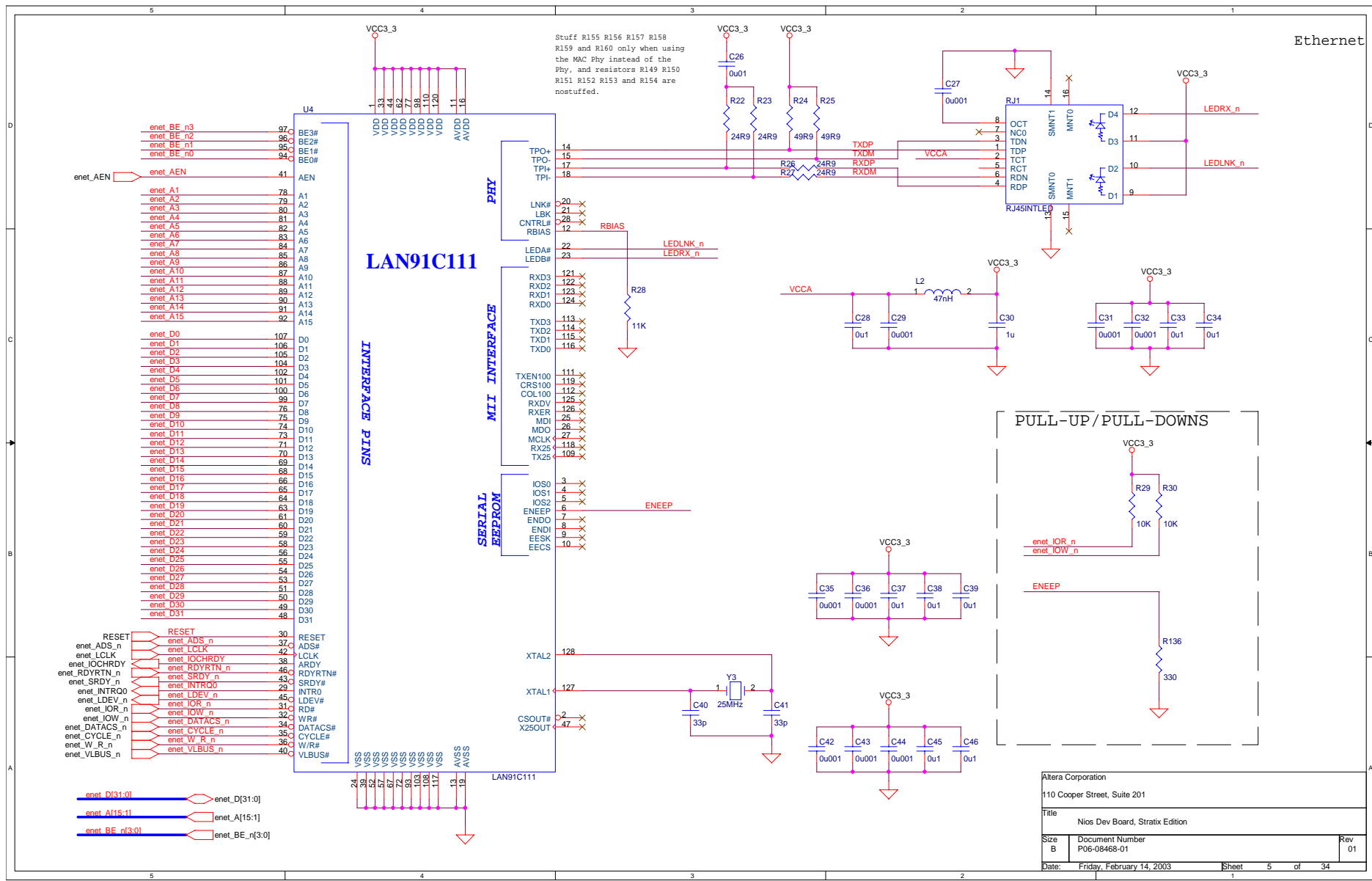
fse_A[22:0] ← fse_A[22:0]



pld_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.



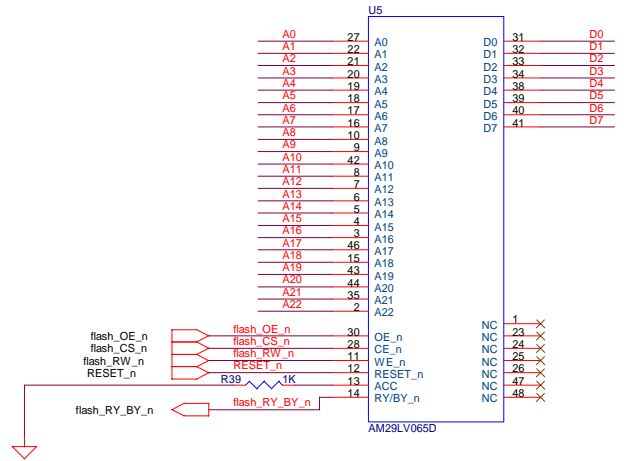
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A[22:0]  A[22:0]

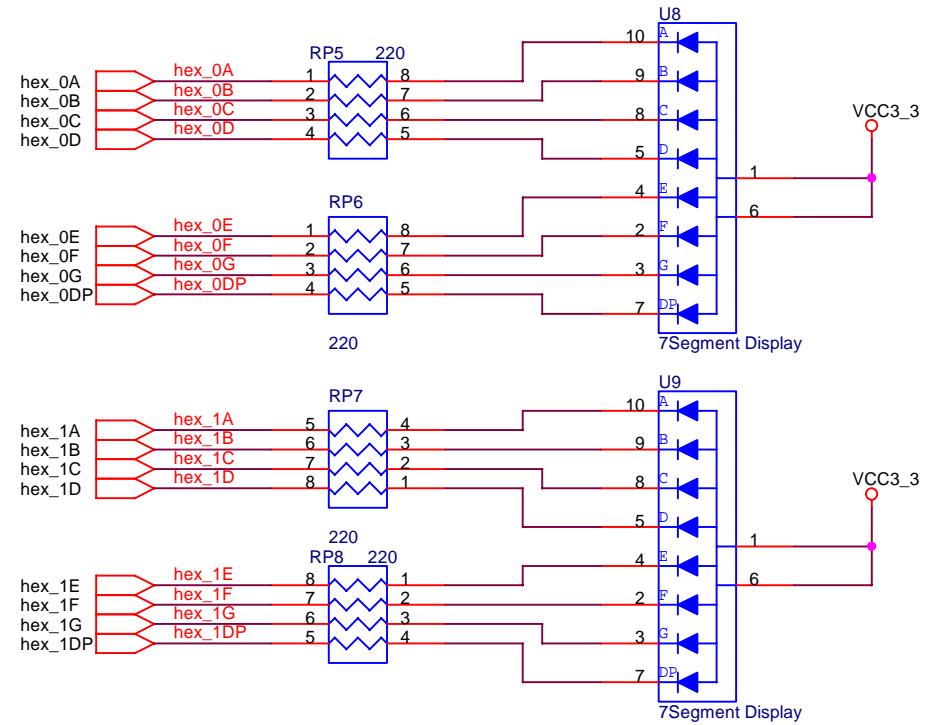
D[7:0]  D[7:0]



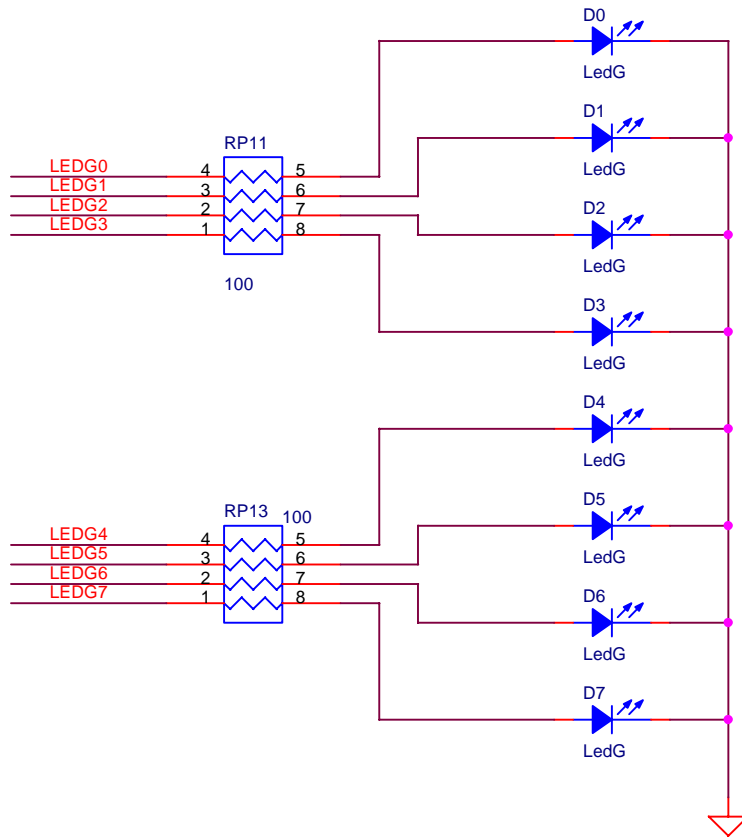
Flash chip is 8M x 8 for 8Mbytes of flash

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Hex Display

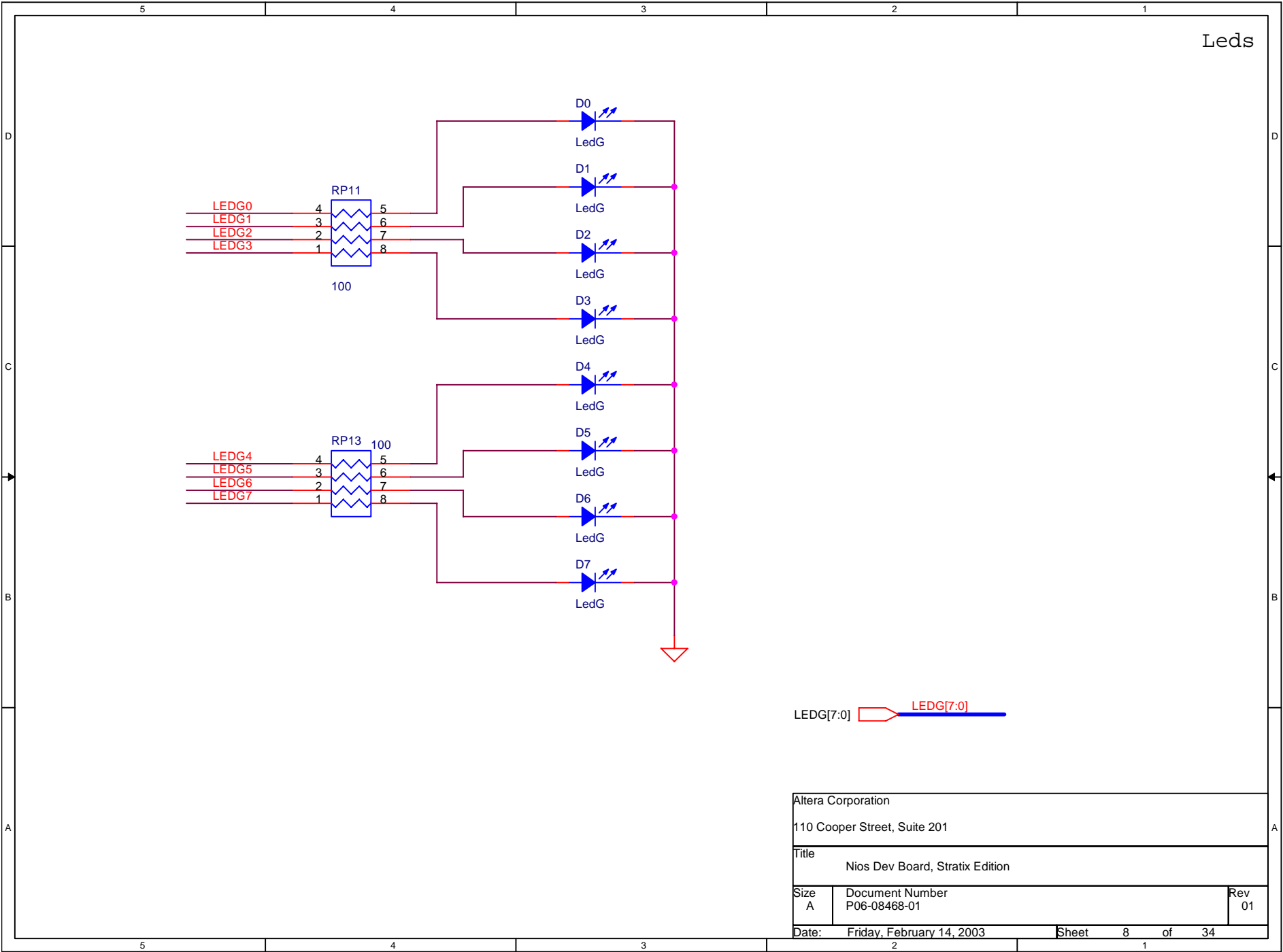


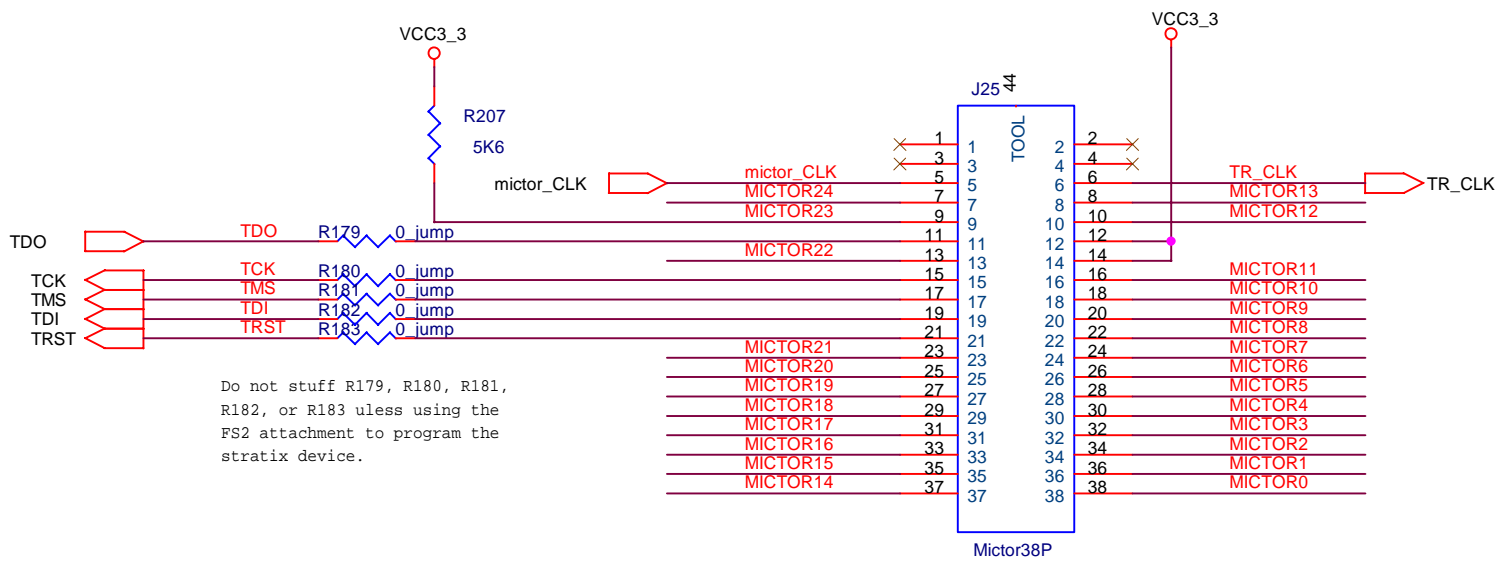
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LEDG[7:0] LEDG[7:0]

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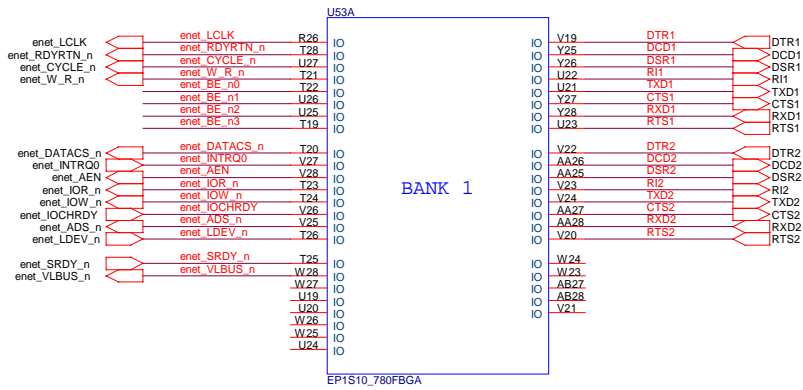


Do not stuff R179, R180, R181, R182, or R183 unless using the FS2 attachment to program the stratix device.

MICTOR[24:0] MICTOR[24:0]

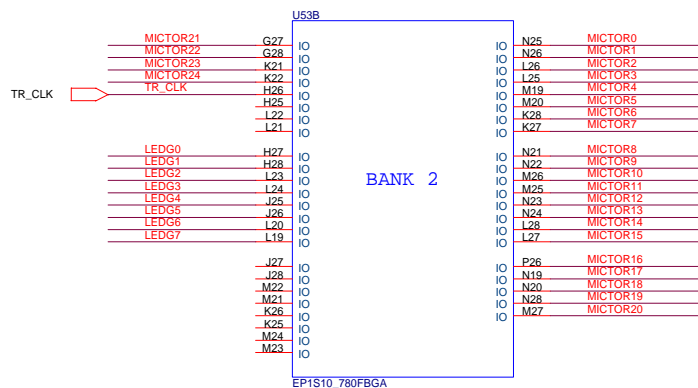
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PLD Bank 1



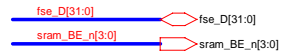
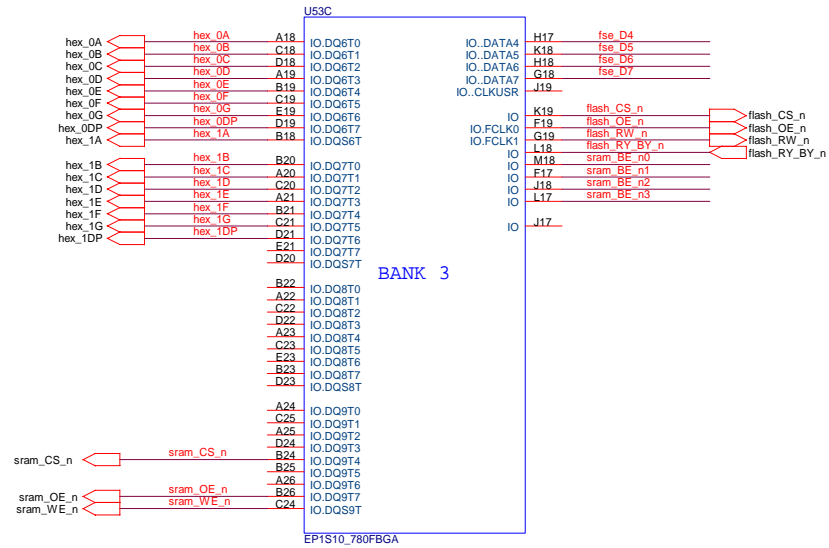
enet_BE_n[3:0] ← enet_BE_n[3:0]

PLD Bank 2

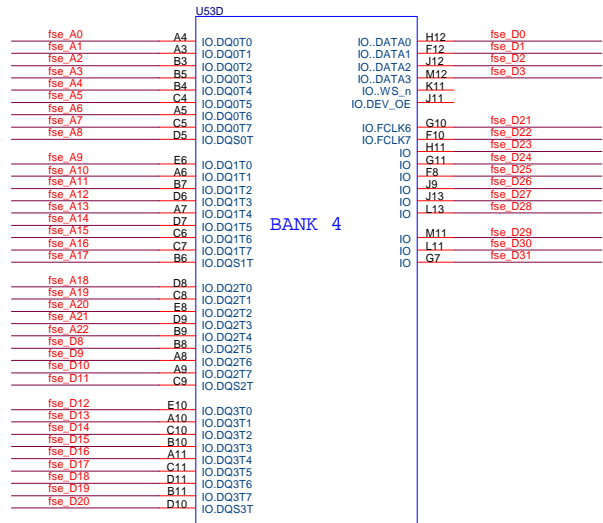


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PLD Bank 3

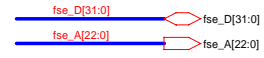


PLD Bank 4

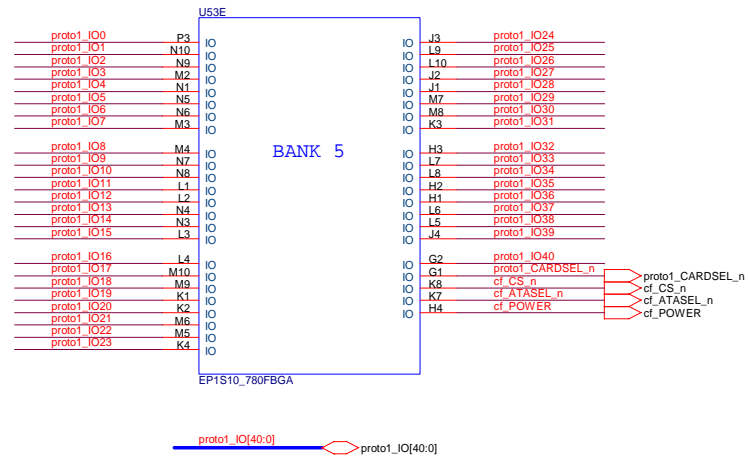


BANK 4

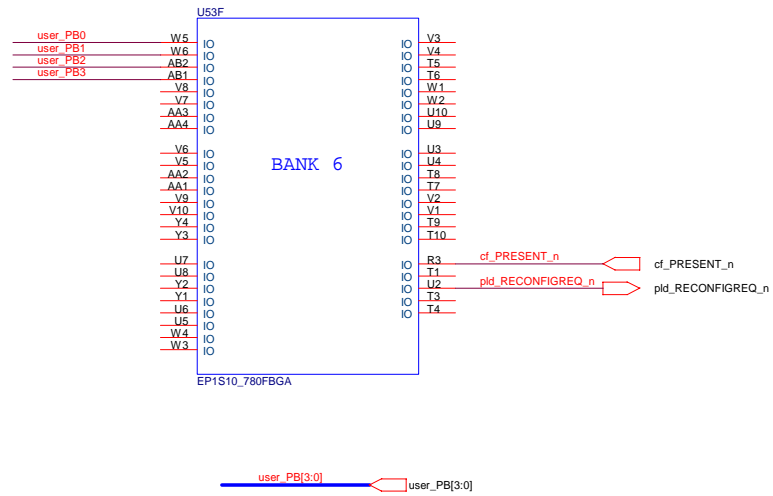
EP1S10_780FBGA



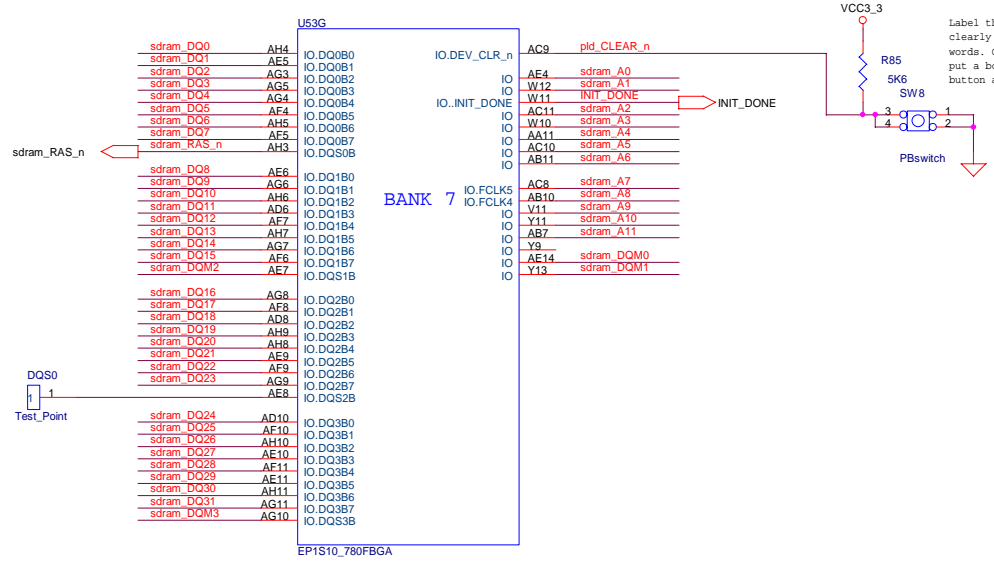
PLD Bank 5



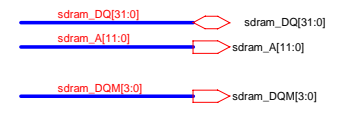
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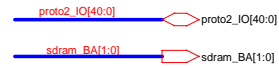
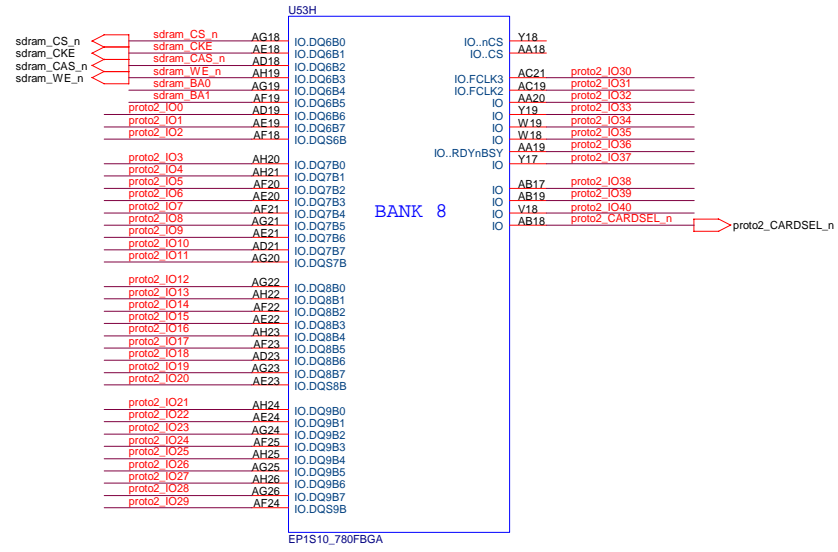


Label this button very clearly with the words. CPU RESET and put a box around the button and text.

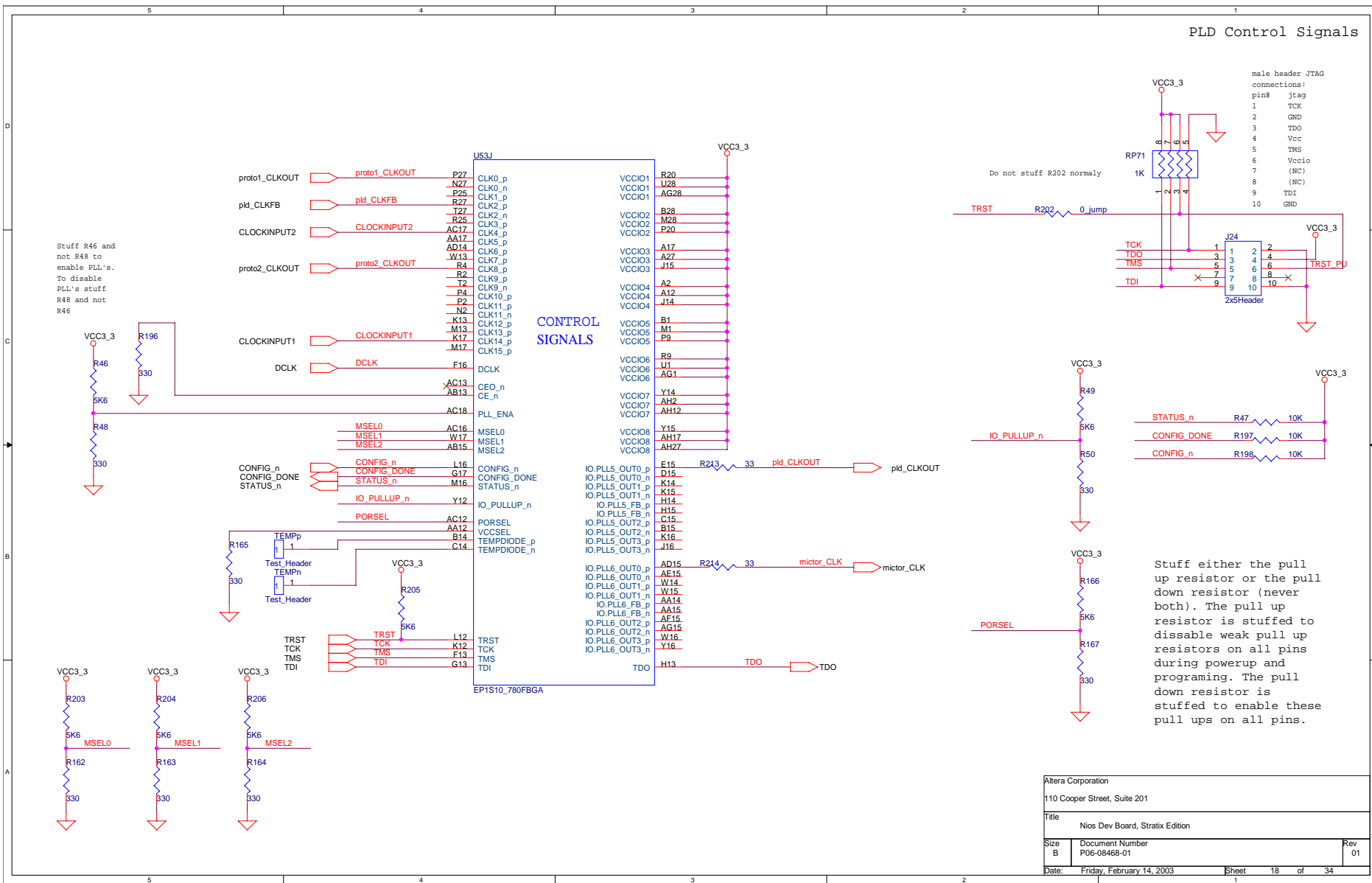


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PLD Bank 8



PLD Control Signals

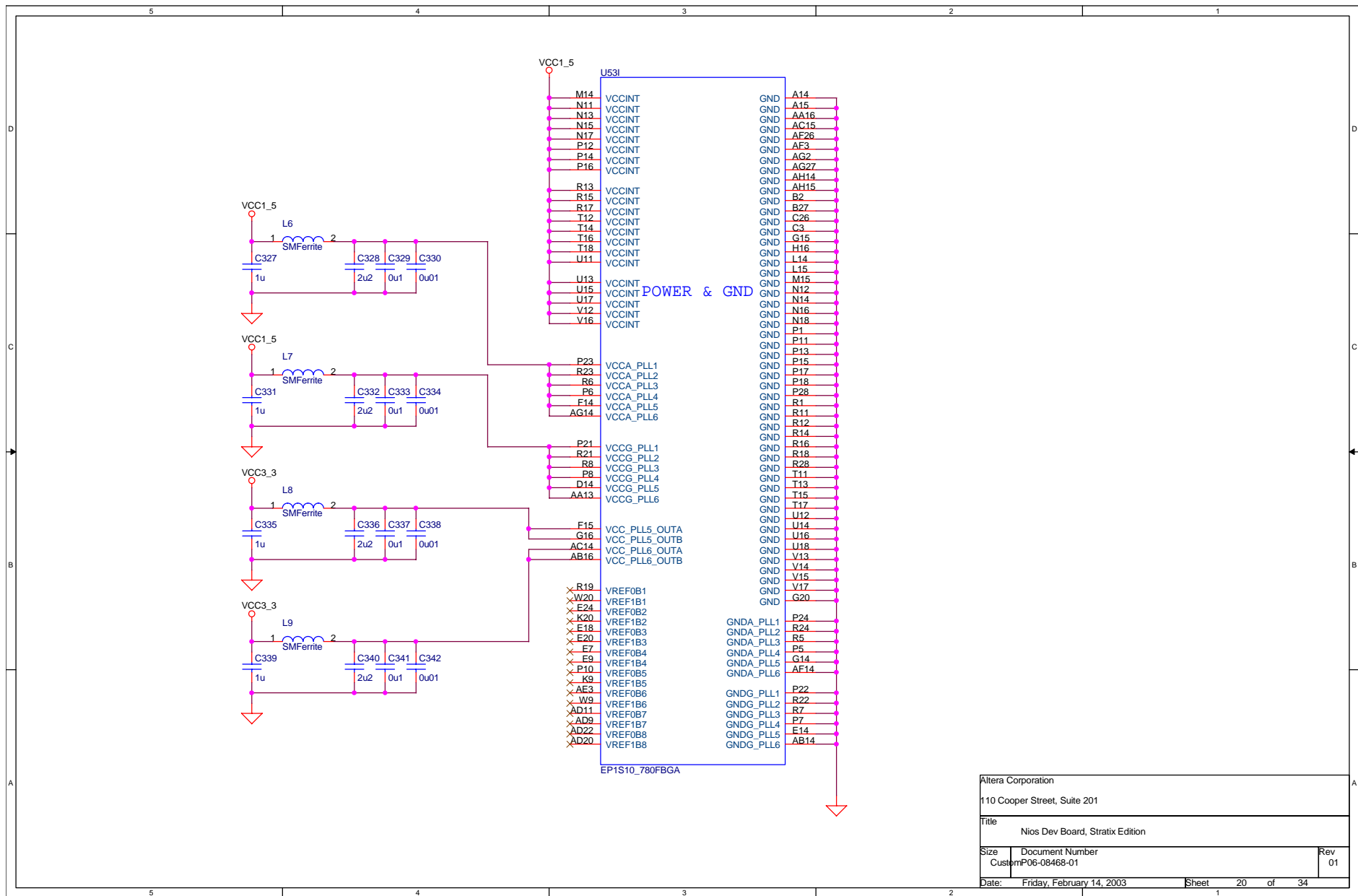


U53K

A13	NC	NC	AF27
A16	NC	NC	AF28
AA10	NC	NC	AG12
AA21	NC	NC	AG13
AA22	NC	NC	AG16
AA23	NC	NC	AG17
AA24	NC	NC	AH13
AA5	NC	NC	AH16
AA6	NC	NC	AH18
AA7	NC	NC	B12
AA8	NC	NC	B13
AA9	NC	NC	B16
AB12	NC	NC	B17
AB20	NC	NC	C1
AB21	NC	NC	C12
AB22	NC	NC	C13
AB23	NC	NC	C16
AB24	NC	NC	C17
AB25	NC	NC	C2
AB26	NC	NC	C27
AB3	NC	NC	C28
AB4	NC	NC	D1
AB5	NC	NC	D12
AB6	NC	NC	D13
AB8	NC	NC	D16
AB9	NC	NC	D17
AC1	NC	NC	D2
AC2	NC	NC	D25
AC20	NC	NC	D26
AC22	NC	NC	D27
AC23	NC	NC	D28
AC24	NC	NC	D3
AC25	NC	NC	D4
AC26	NC	NC	E1
AC27	NC	NC	E11
AC28	NC	NC	E12
AC3	NC	NC	E13
AC4	NC	NC	E16
AC5	NC	NC	E17
AC6	NC	NC	E2
AC7	NC	NC	F1
AD1	NC	NC	F11
AD12	NC	NC	F18
AD13	NC	NC	F2
AD16	NC	NC	F20
AD17	NC	NC	F21
AD2	NC	NC	F22
AD24	NC	NC	F23
AD25	NC	NC	F24
AD26	NC	NC	F25
AD27	NC	NC	F26
AD28	NC	NC	F27
AD3	NC	NC	F28
AD4	NC	NC	F3
AD5	NC	NC	F4
AD7	NC	NC	F5
AF2	NC	NC	F6
AF17	NC	NC	F7
AF16	NC	NC	F9
AF13	NC	NC	G12
AF12	NC	NC	G21
AF1	NC	NC	G22
AE28	NC	NC	G23
AE27	NC	NC	G24
AE26	NC	NC	G25
AE25	NC	NC	G26
AE2	NC	NC	G3
AE17	NC	NC	G4
AE16	NC	NC	G5
AE13	NC	NC	G6
AE12	NC	NC	G8
AE1	NC	NC	G9
E5	NC	NC	H10
E4	NC	NC	H19
E3	NC	NC	H20
E28	NC	NC	H21
E27	NC	NC	H22
E26	NC	NC	H23
E25	NC	NC	H24
E22	NC	NC	H5
J5	NC	NC	H6
J24	NC	NC	J6
J23	NC	NC	J7
J22	NC	NC	J8
J21	NC	NC	K10
J20	NC	NC	K23
J10	NC	NC	K24
H9	NC	NC	K5
H8	NC	NC	K6
H7	NC	NC	P19
Y21	NC	NC	Y22
Y20	NC	NC	Y23
Y10	NC	NC	Y24
W8	NC	NC	Y5
W7	NC	NC	Y6
W22	NC	NC	Y7
W21	NC	NC	Y8
R10	NC	NC	

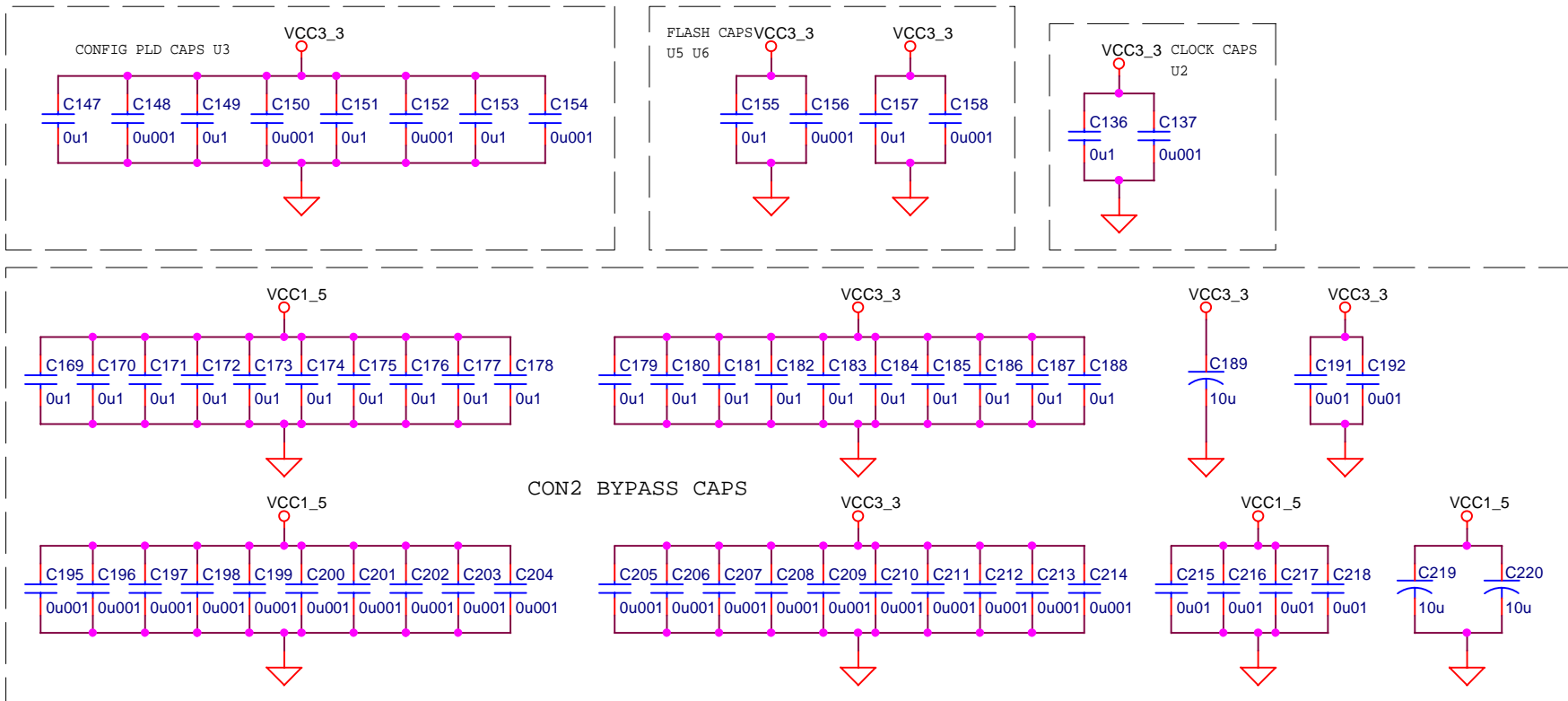
EP1S10_780FBGA

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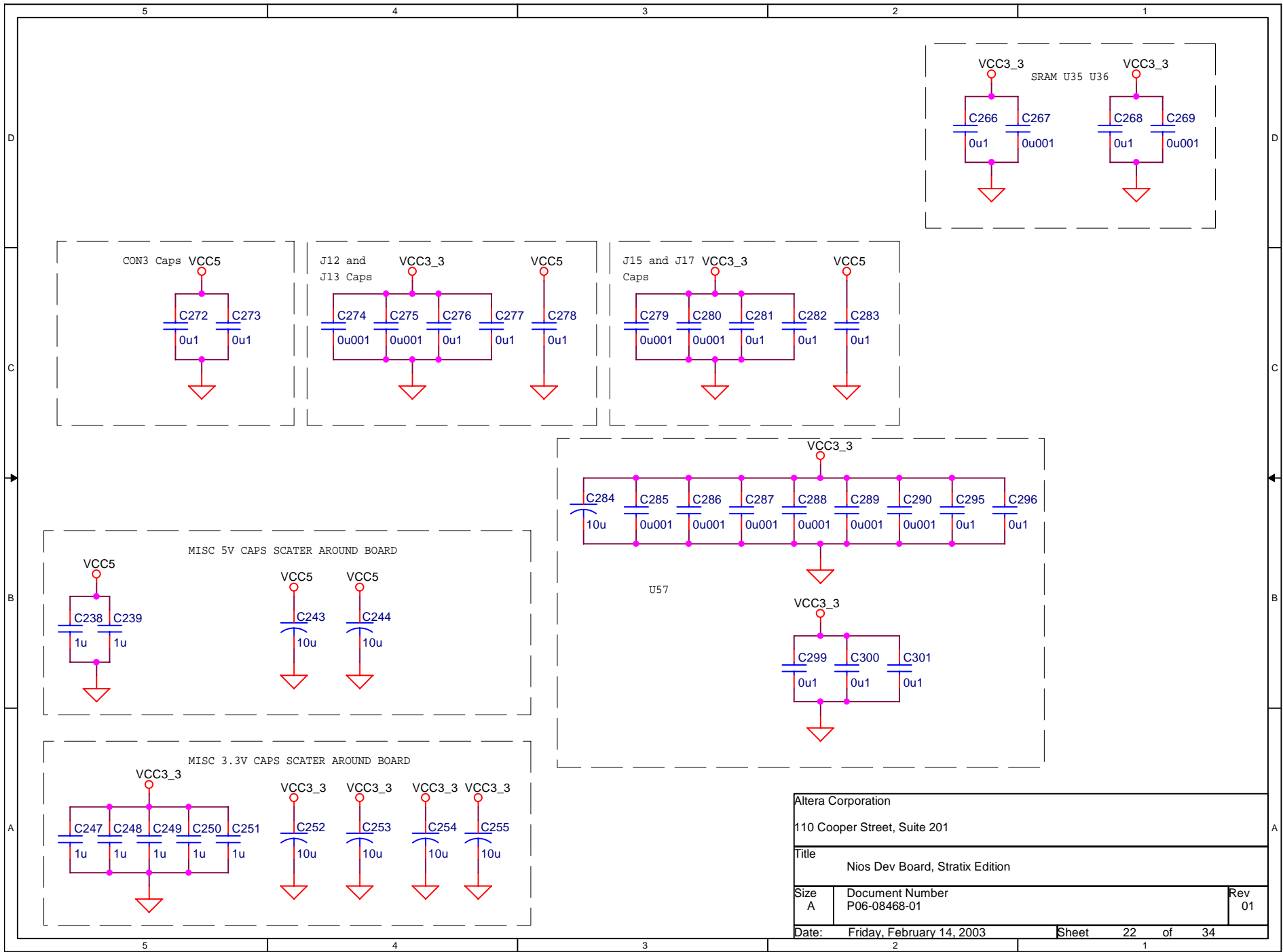


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Bypass CAPS

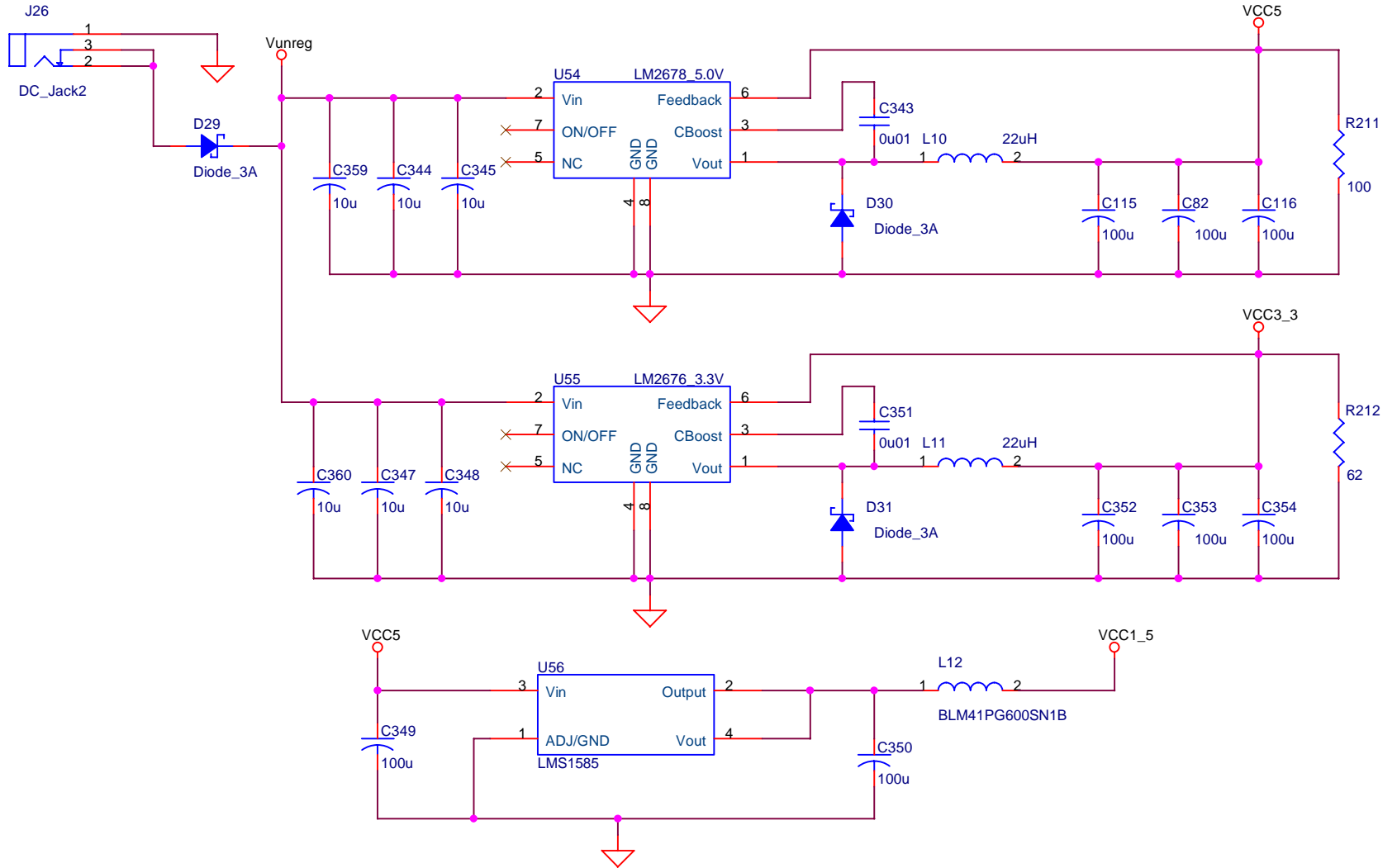


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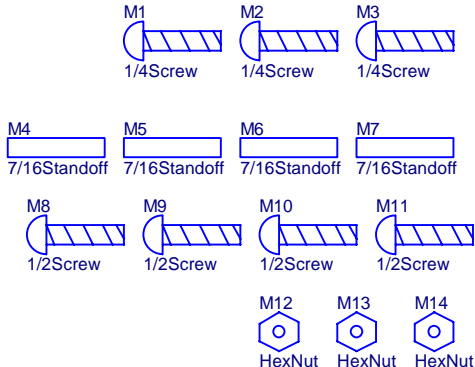
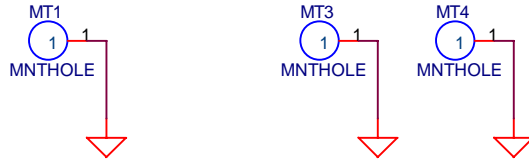
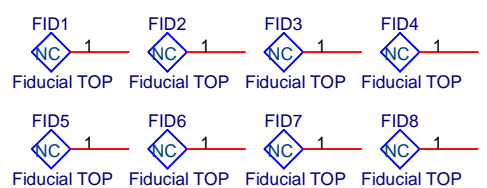
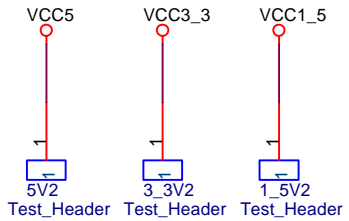
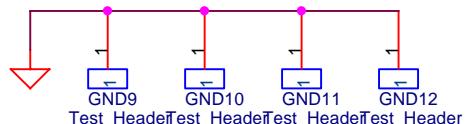
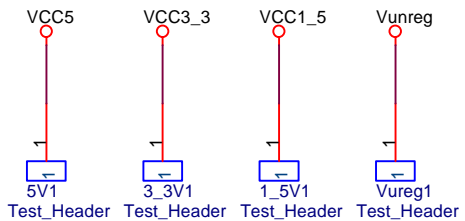
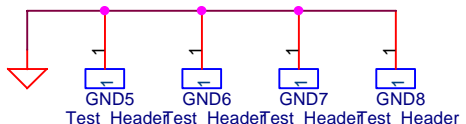
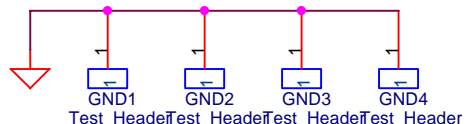
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Power Connector

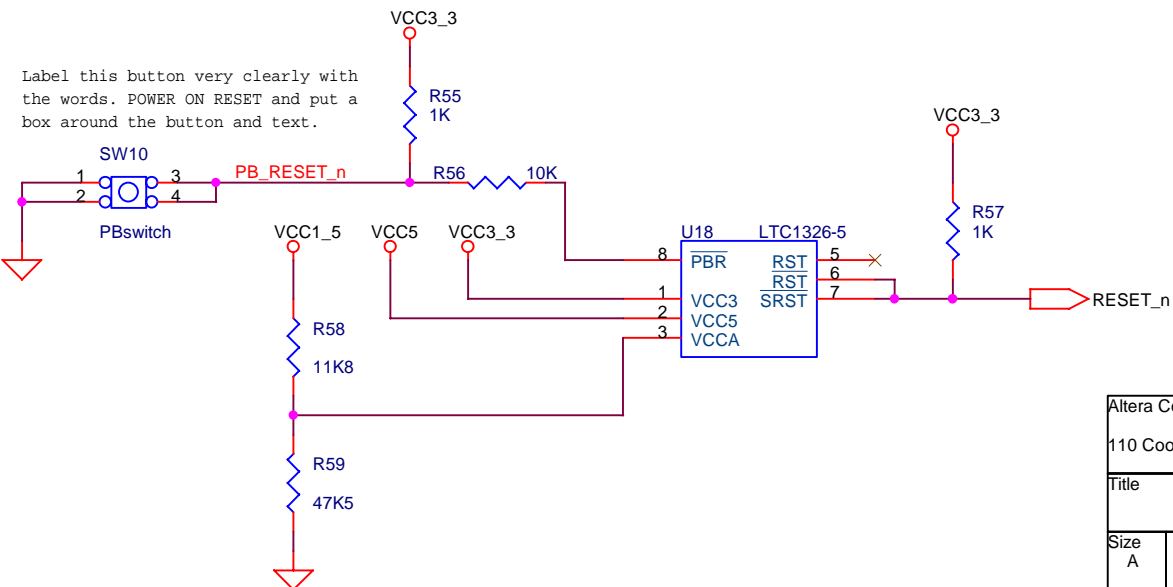


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Reset and Test headers

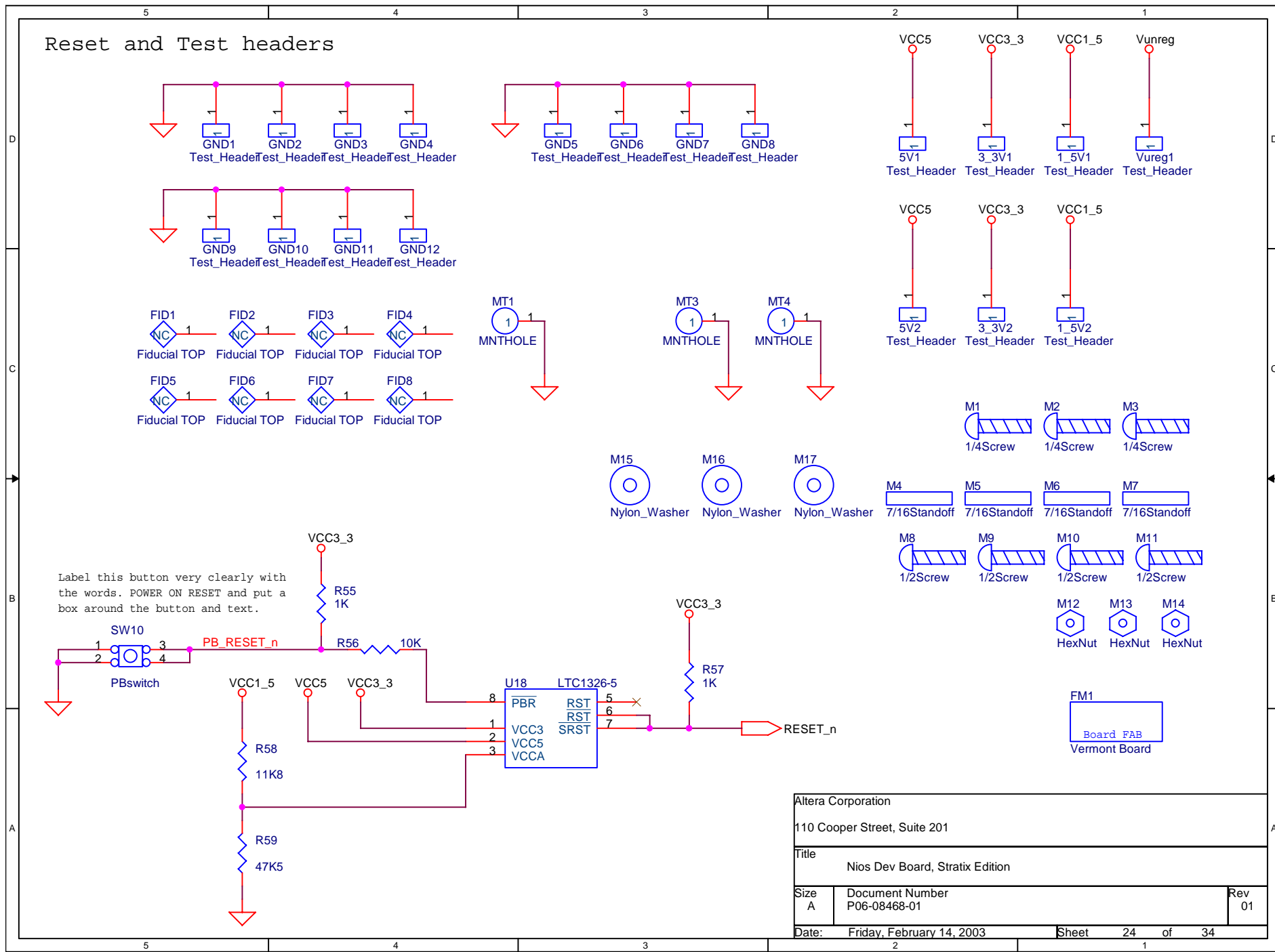


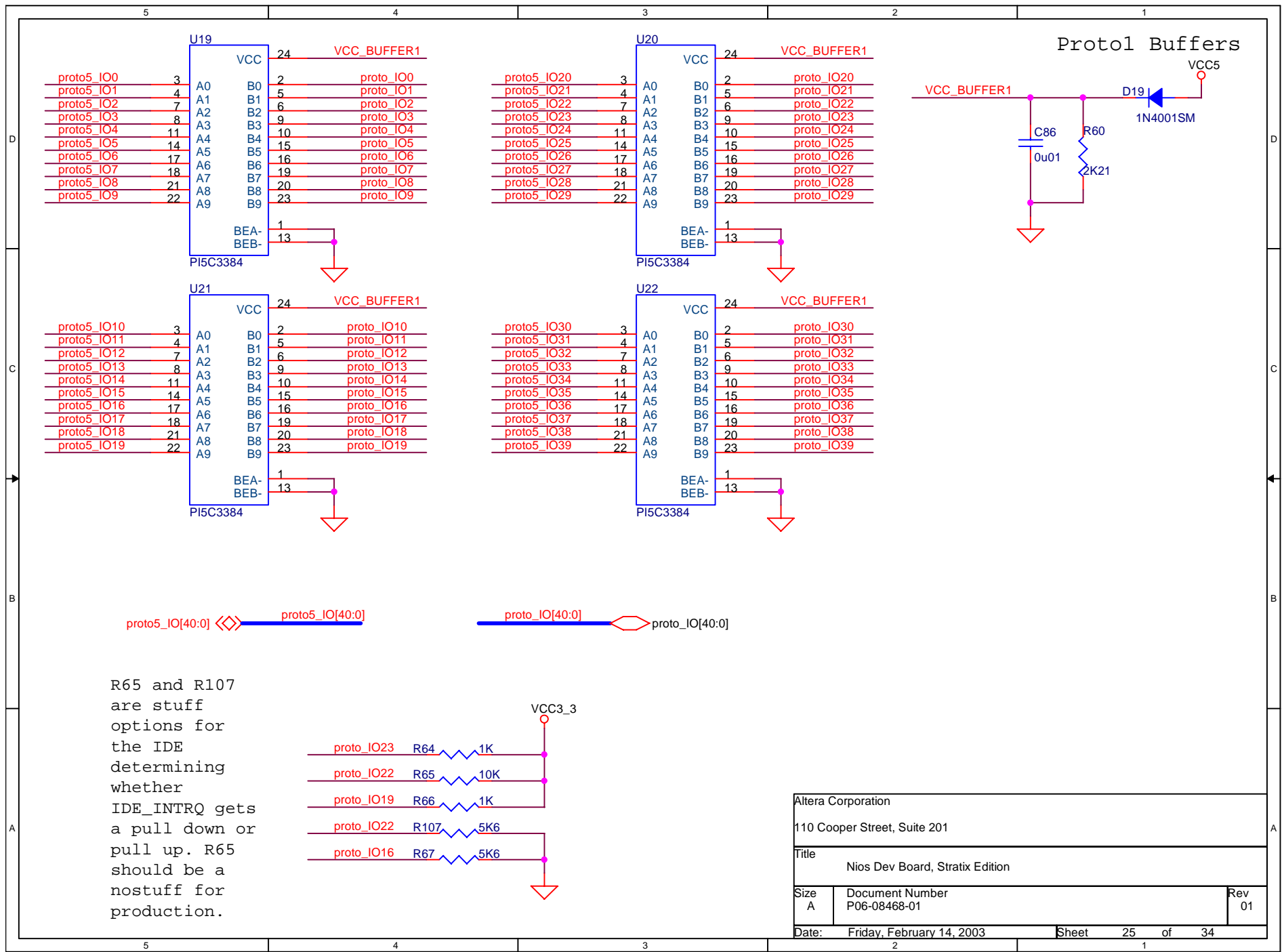
Label this button very clearly with the words. POWER ON RESET and put a box around the button and text.



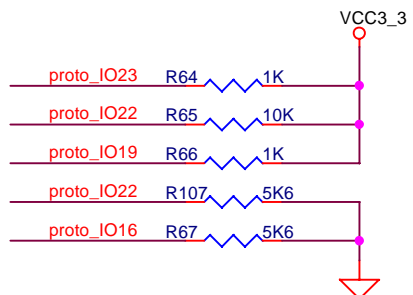
FM1 Board FAB Vermont Board

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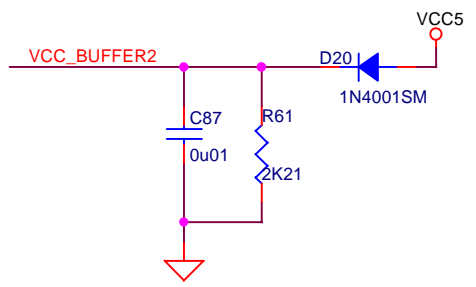
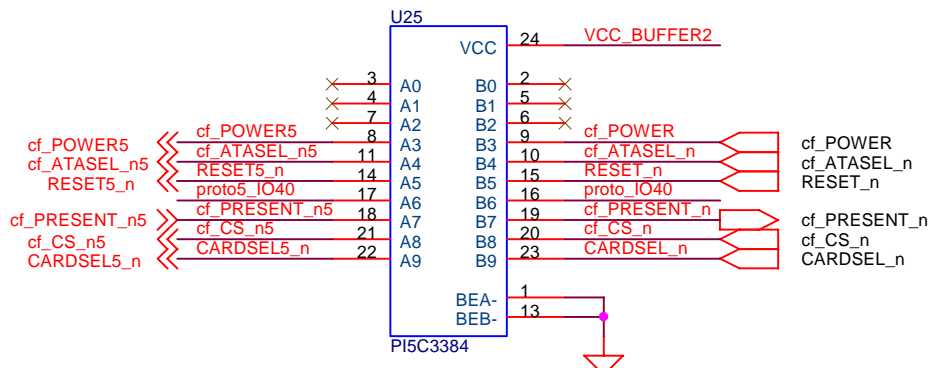


R65 and R107 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R65 should be a nostuff for production.



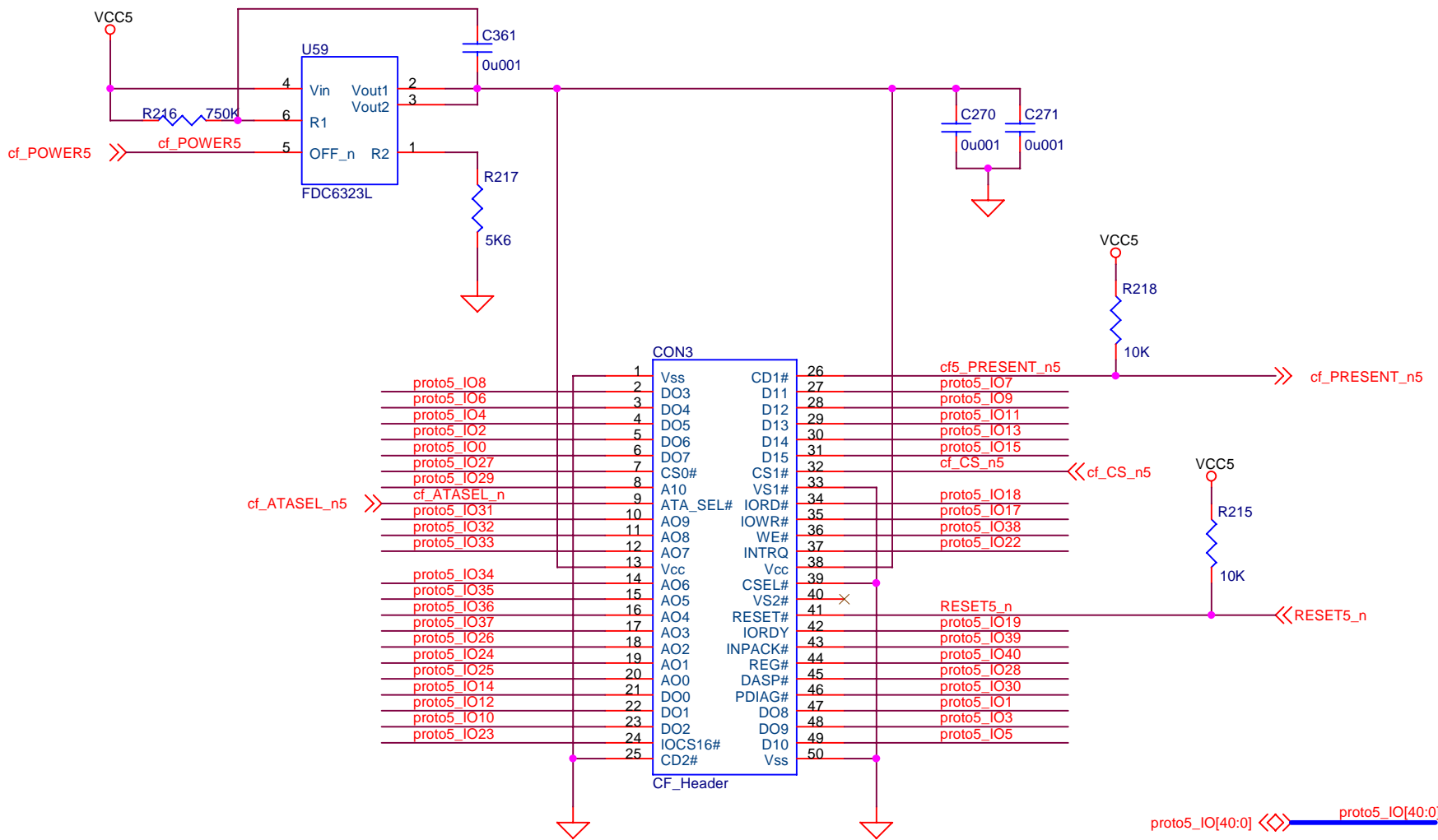
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Protol Buffers



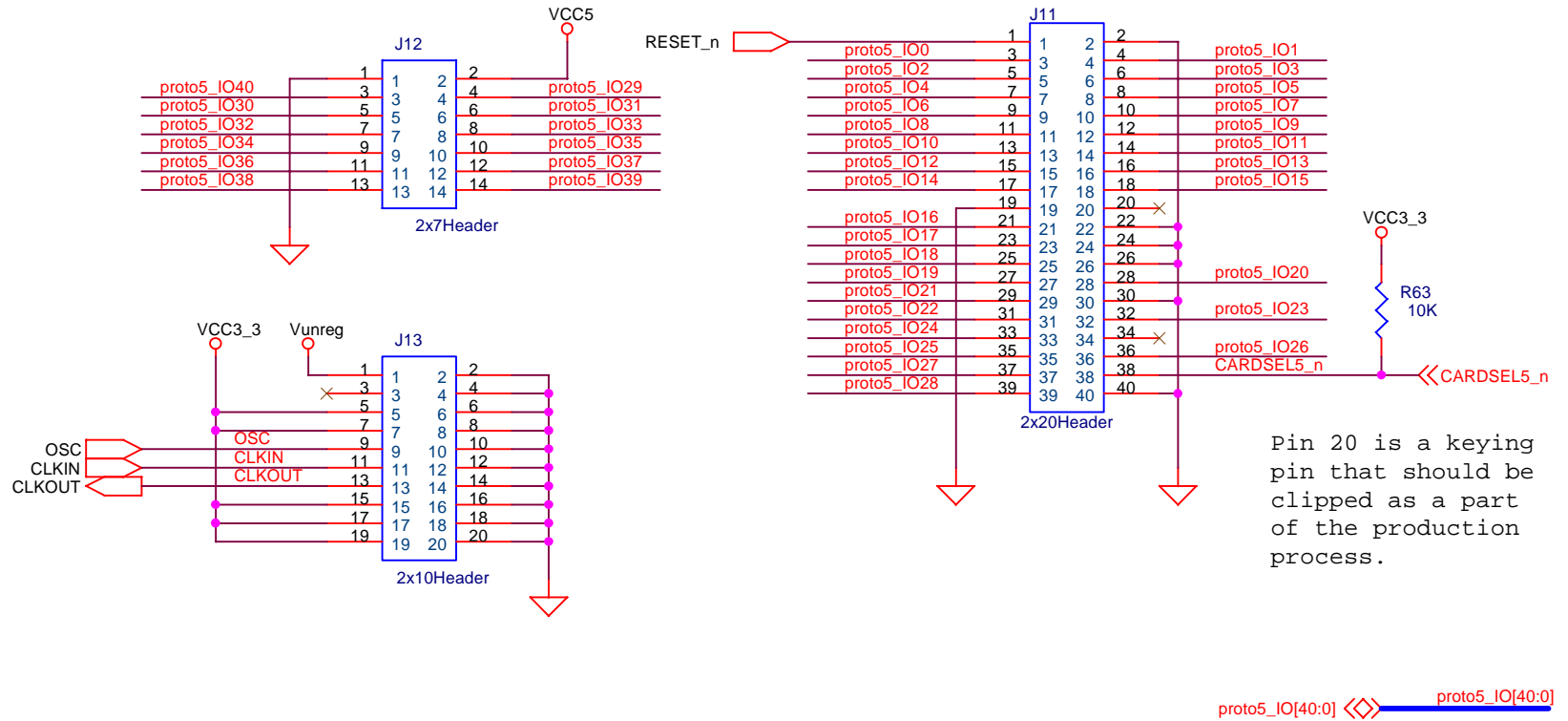
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Compaq Flash Socket

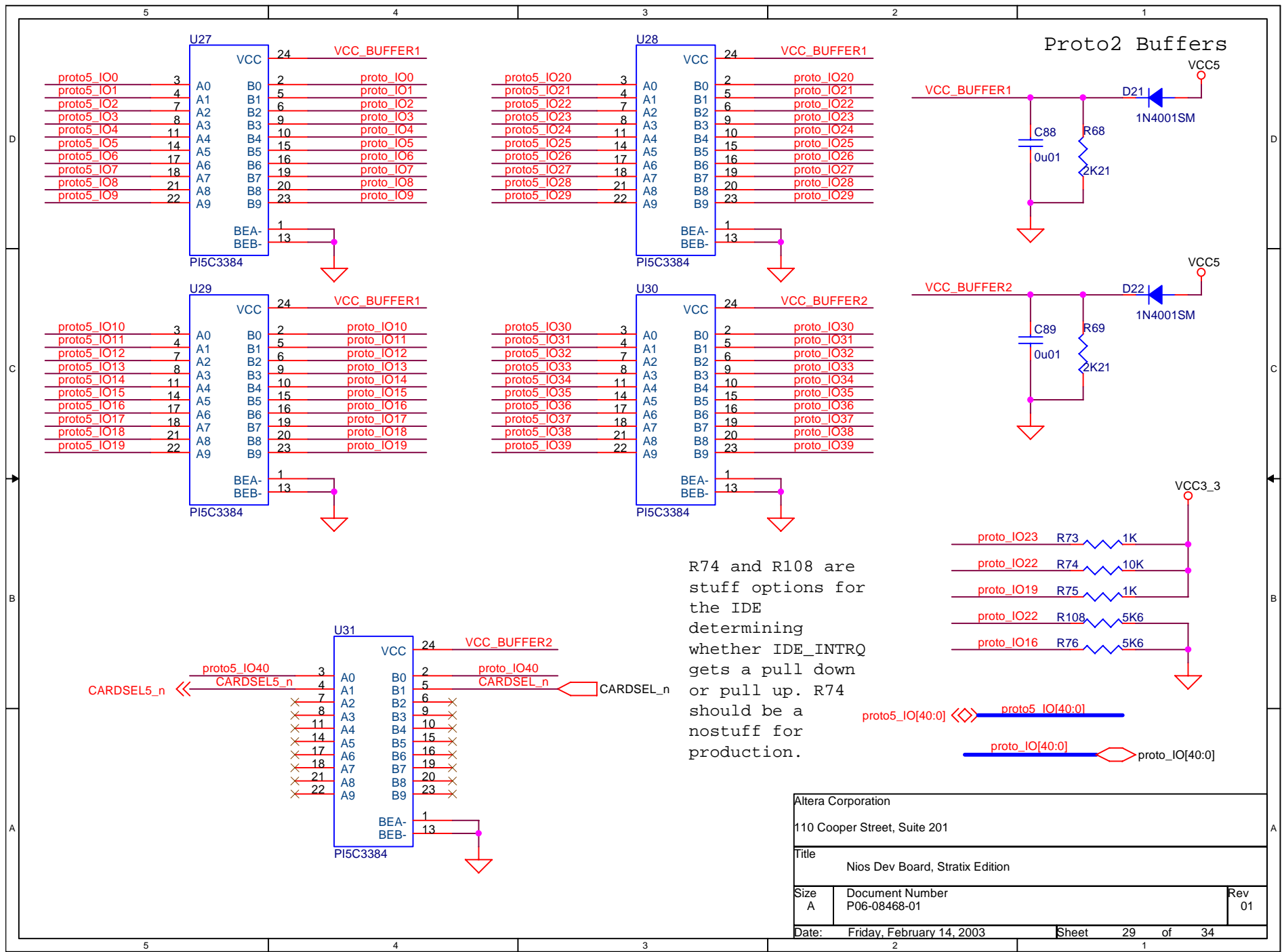


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Protocard 1

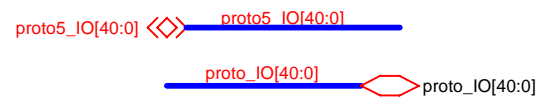


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Proto2 Buffers

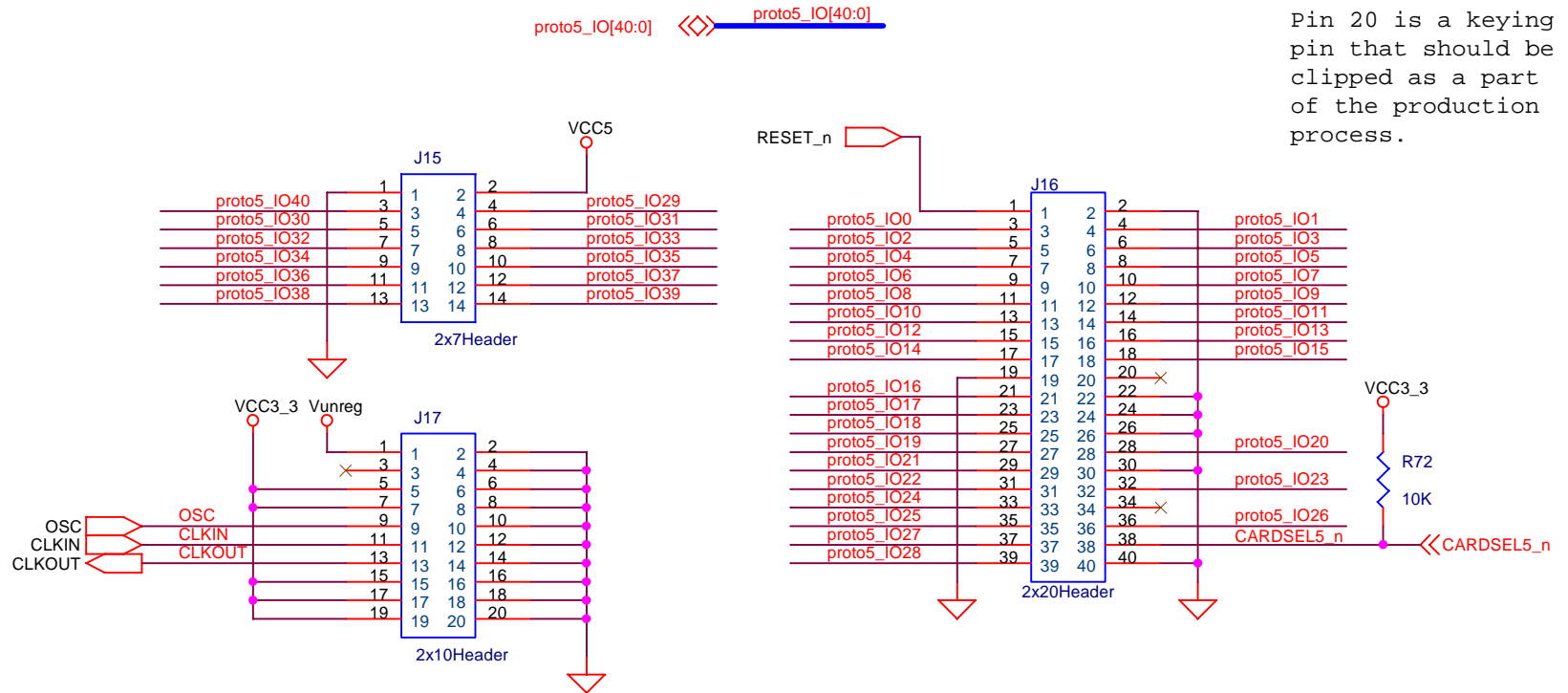
R74 and R108 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R74 should be a nostuff for production.



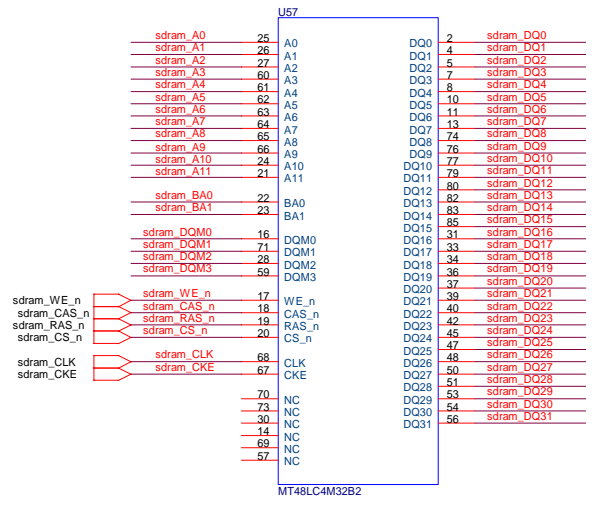
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Proto2 Headers

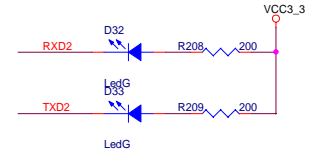
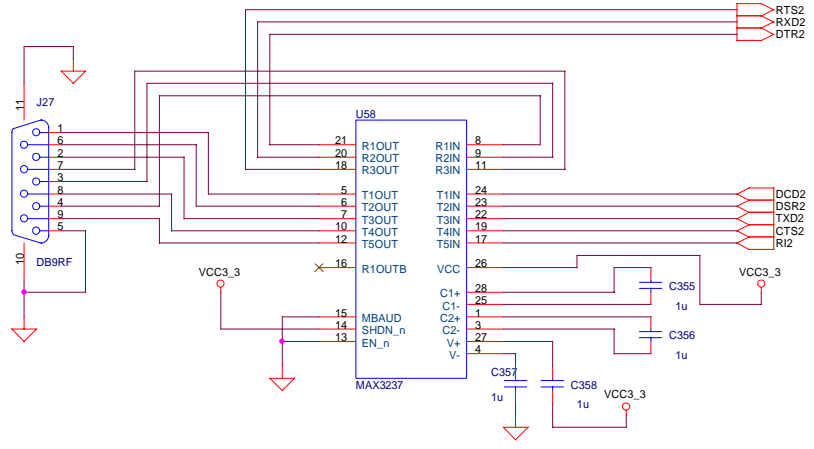
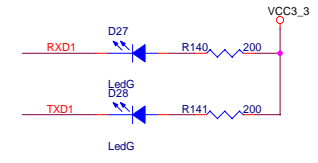
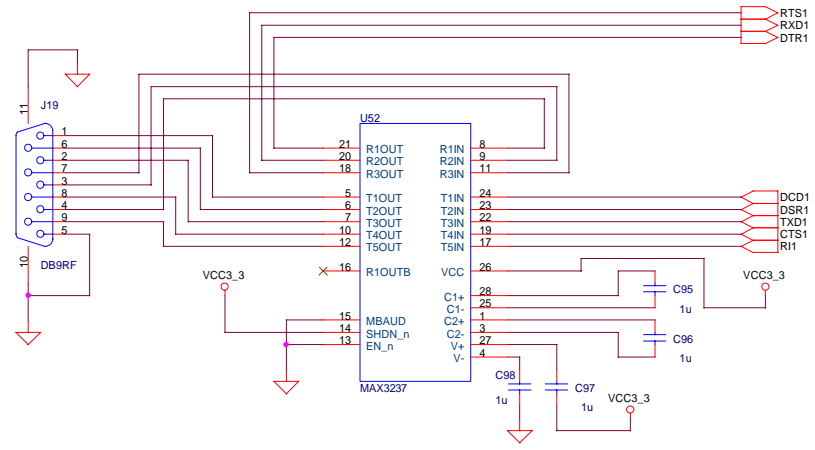
Pin 20 is a keying pin that should be clipped as a part of the production process.



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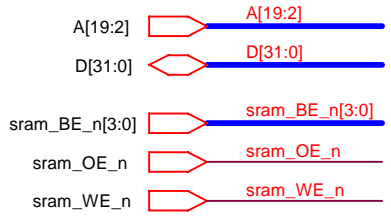
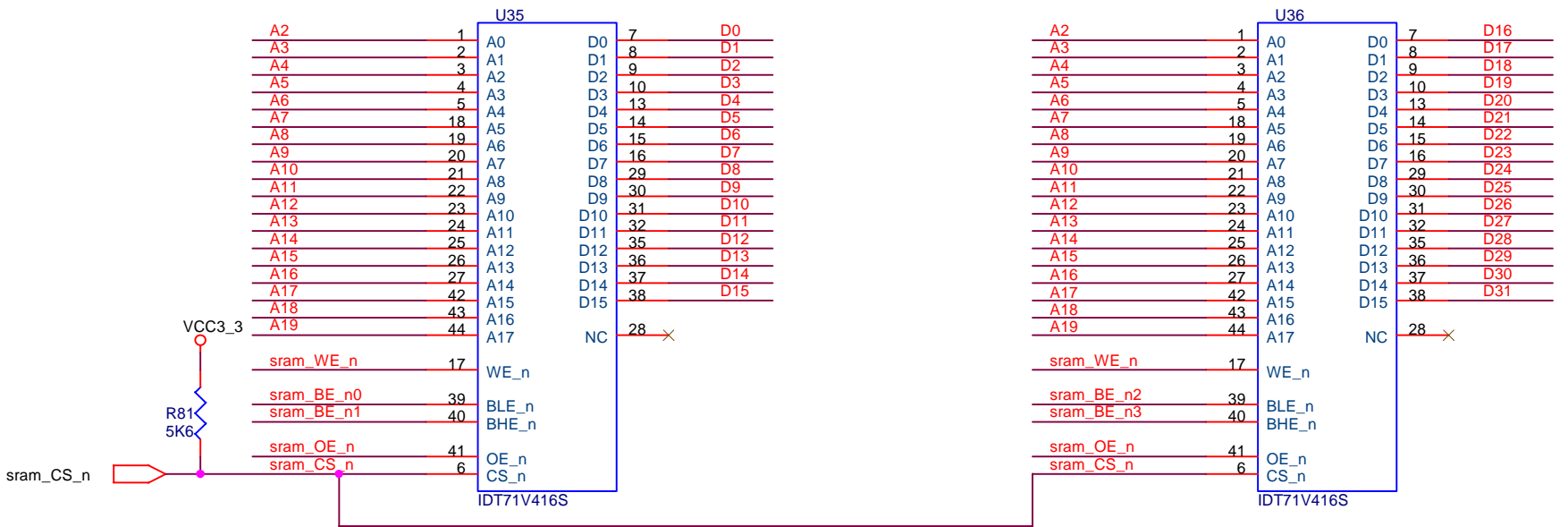


Serial Ports



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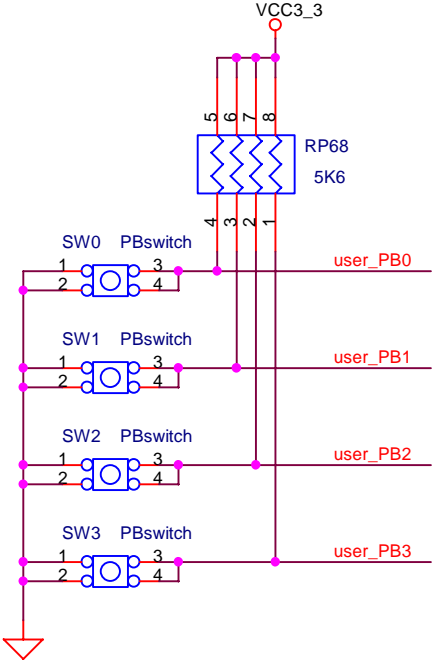
SRAM



One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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Switches Buttons



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