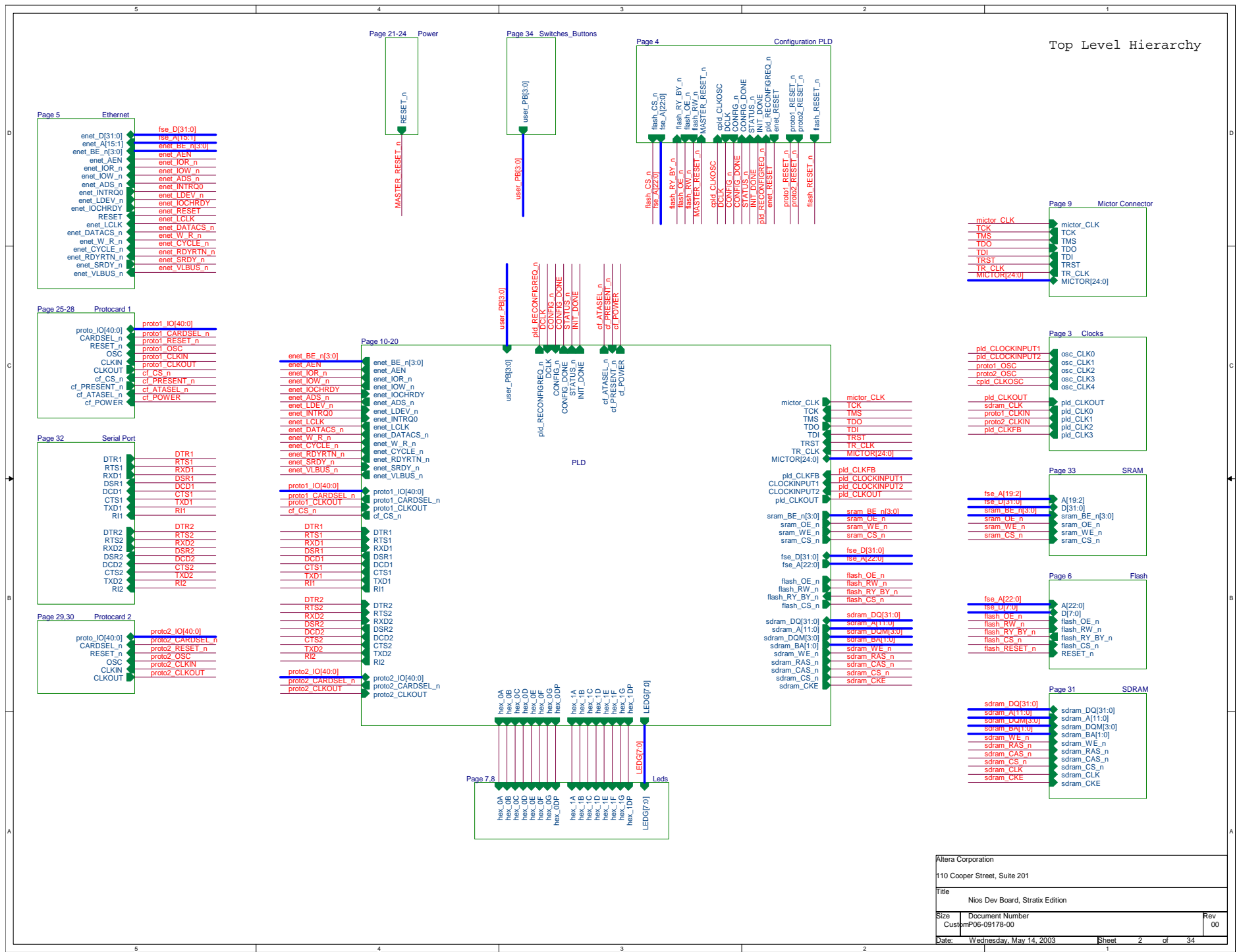


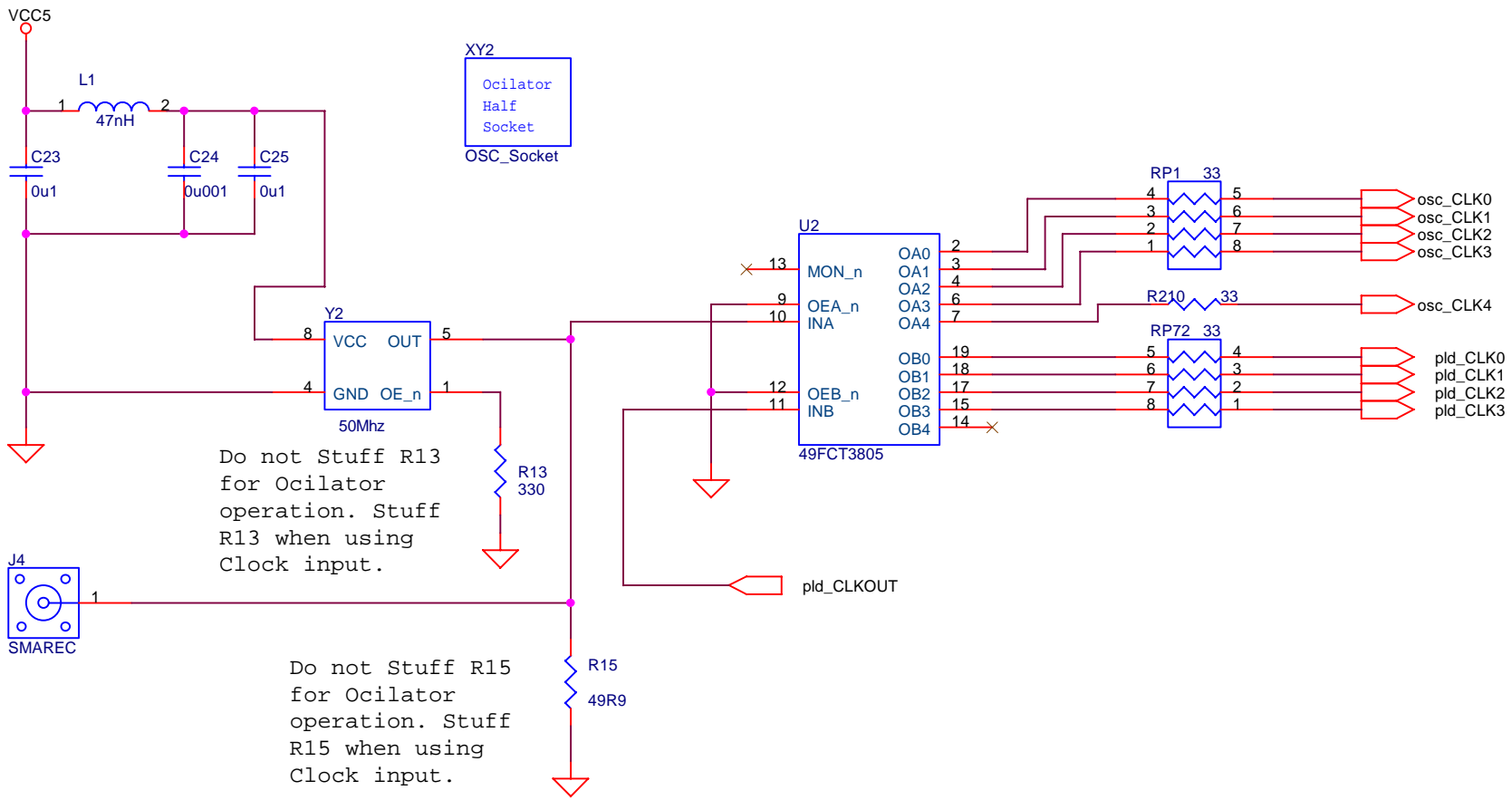
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# Top Level Hierarchy



# Clocks

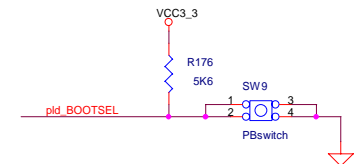
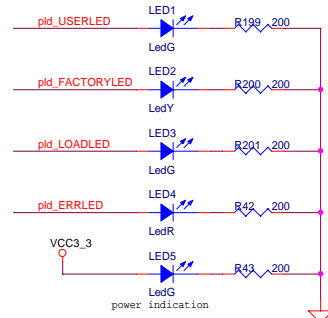
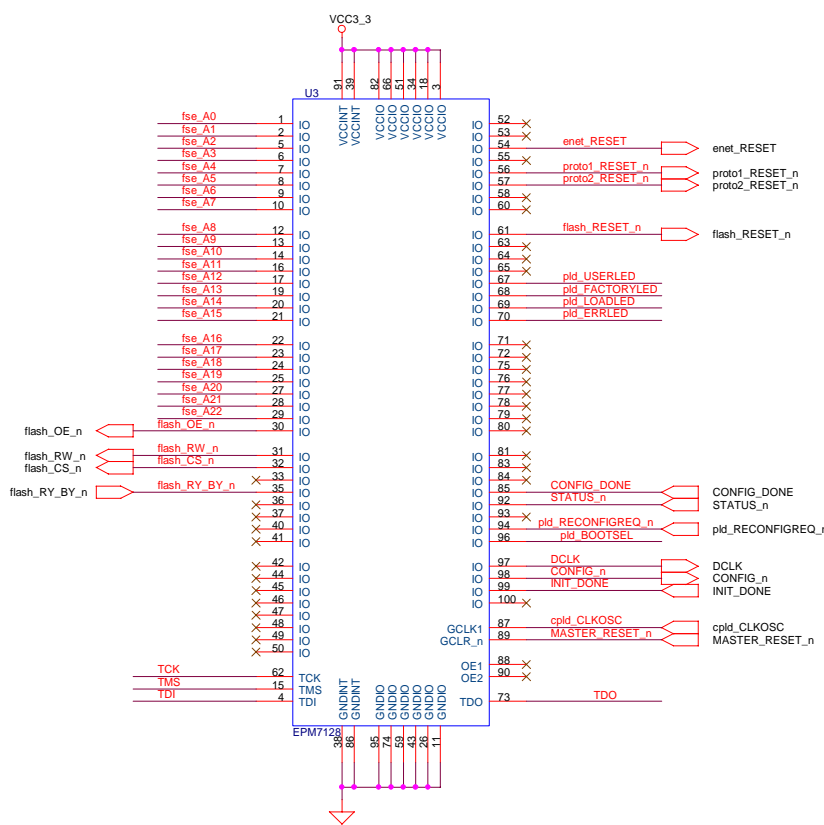


Do not Stuff R13 for Ocilator operation. Stuff R13 when using Clock input.

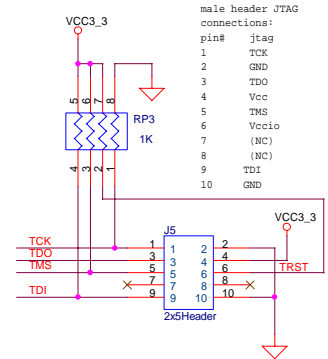
Do not Stuff R15 for Ocilator operation. Stuff R15 when using Clock input.

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fse\_A[22:0] ← fse\_A[22:0]

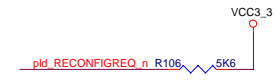


pld\_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.

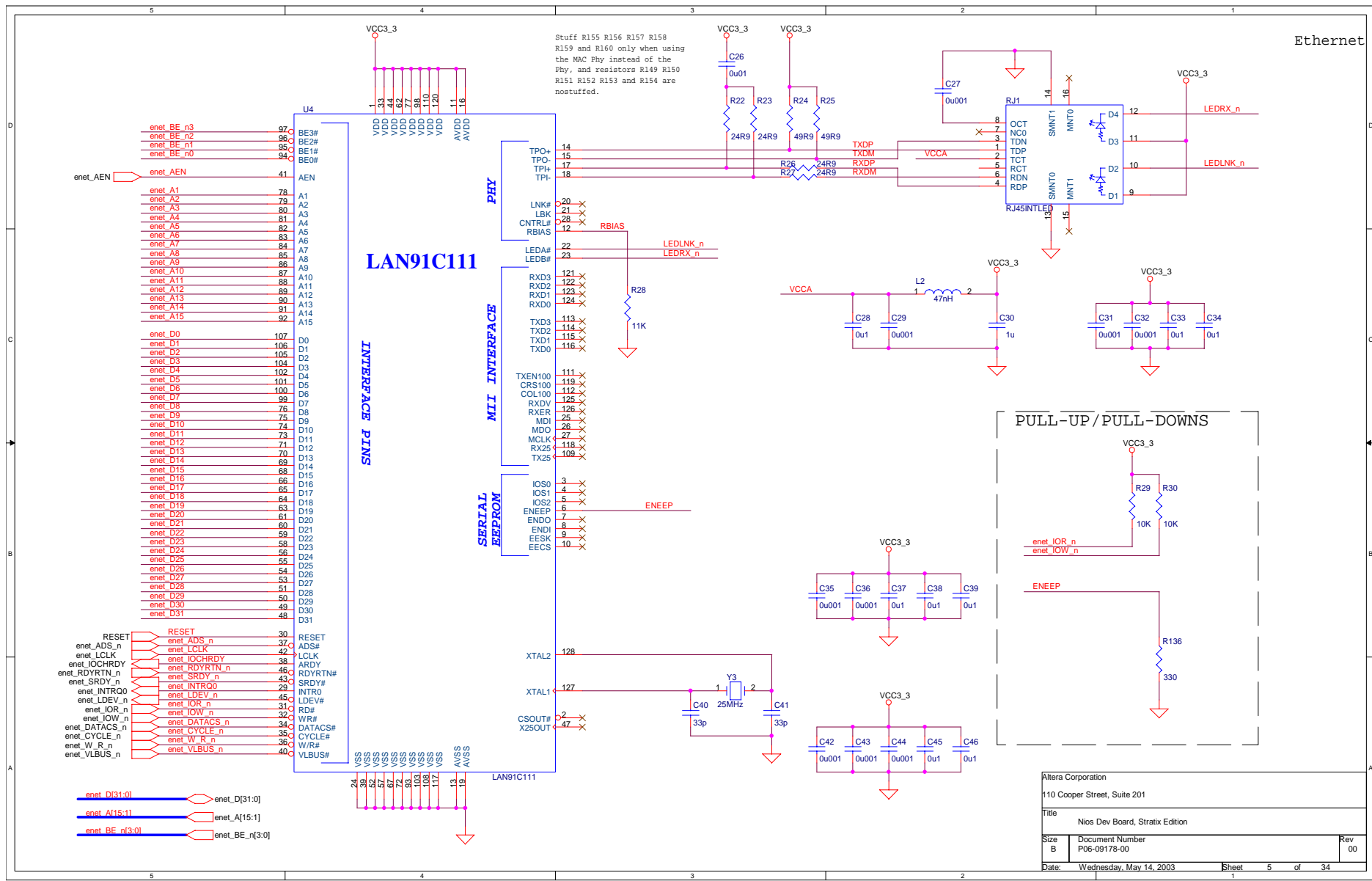


male header JTAG connections:

pin#	jtag
1	TCK
2	GND
3	TDO
4	Vcc
5	TMS
6	Vccio
7	(NC)
8	(NC)
9	TDI
10	GND



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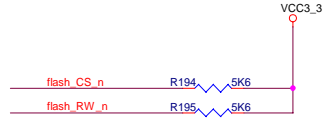
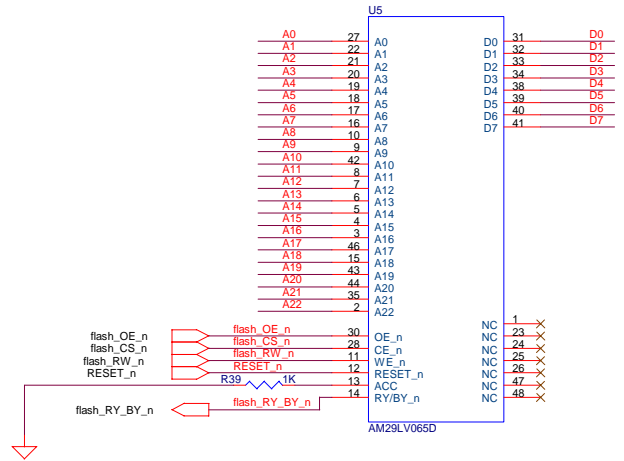
- enet\_BE\_n3 97 BE3#
- enet\_BE\_n2 96 BE2#
- enet\_BE\_n1 95 BE1#
- enet\_BE\_n0 94 BE0#
- enet\_AEN 41 AEN
- enet\_A1 78 A1
- enet\_A2 79 A2
- enet\_A3 80 A3
- enet\_A4 81 A4
- enet\_A5 82 A5
- enet\_A6 83 A6
- enet\_A7 84 A7
- enet\_A8 85 A8
- enet\_A9 86 A9
- enet\_A10 87 A10
- enet\_A11 88 A11
- enet\_A12 89 A12
- enet\_A13 90 A13
- enet\_A14 91 A14
- enet\_A15 92 A15
- enet\_D0 107 D0
- enet\_D1 106 D1
- enet\_D2 105 D2
- enet\_D3 104 D3
- enet\_D4 102 D4
- enet\_D5 101 D5
- enet\_D6 100 D6
- enet\_D7 99 D7
- enet\_D8 76 D8
- enet\_D9 75 D9
- enet\_D10 74 D10
- enet\_D11 73 D11
- enet\_D12 71 D12
- enet\_D13 70 D13
- enet\_D14 69 D14
- enet\_D15 68 D15
- enet\_D16 66 D16
- enet\_D17 65 D17
- enet\_D18 64 D18
- enet\_D19 63 D19
- enet\_D20 61 D20
- enet\_D21 60 D21
- enet\_D22 59 D22
- enet\_D23 58 D23
- enet\_D24 56 D24
- enet\_D25 55 D25
- enet\_D26 54 D26
- enet\_D27 53 D27
- enet\_D28 51 D28
- enet\_D29 50 D29
- enet\_D30 49 D30
- enet\_D31 48 D31
- RESET 30 RESET
- enet\_ADS\_n 37 ADS#
- enet\_LCLK 42 LCLK
- enet\_IOCHRDY 38 ARDY
- enet\_RDYRTN\_n 46 RDYRTN#
- enet\_SRDY\_n 43 SRDY#
- enet\_INTRQ0 29 INTRQ
- enet\_LDEV\_n 45 LDEV#
- enet\_IOR\_n 31 RD#
- enet\_IOW\_n 32 WR#
- enet\_DATACS\_n 34 DATACS#
- enet\_CYCLE\_n 35 CYCLE#
- enet\_W\_R\_n 36 W/R#
- enet\_VLBUS\_n 40 VLBUS#

- enet\_D[31:0] enet\_D[31:0]
- enet\_A[15:1] enet\_A[15:1]
- enet\_BE\_n[3:0] enet\_BE\_n[3:0]

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A[22:0]

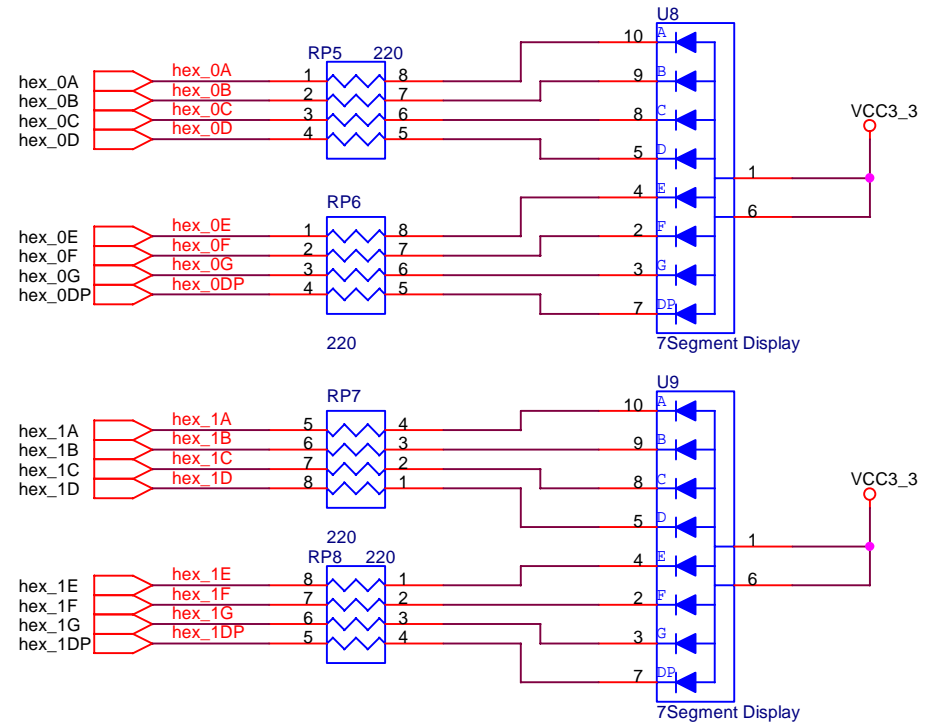
D[7:0]



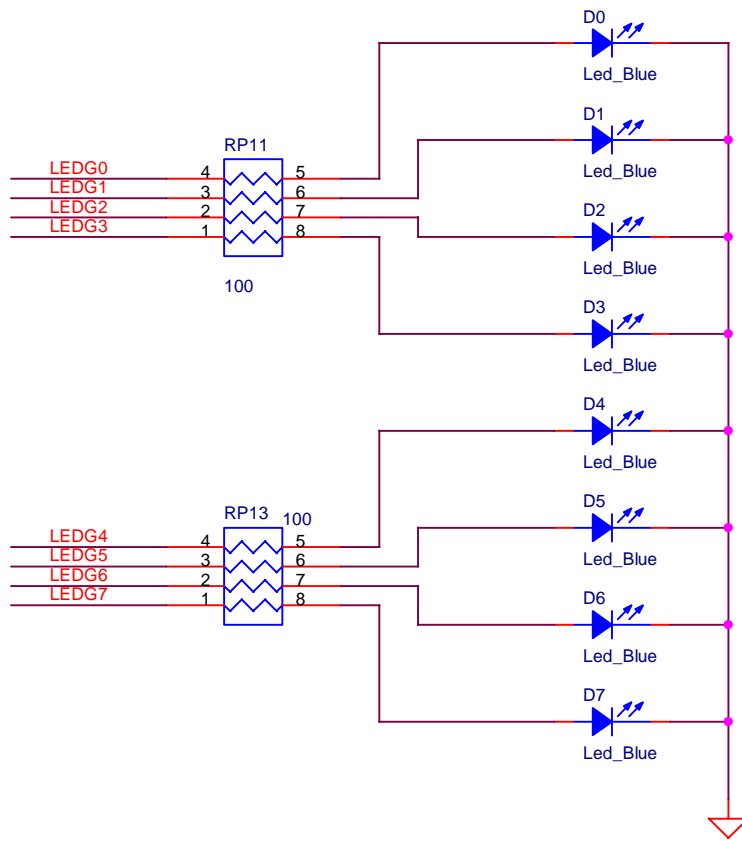
Flash chip is 8M x 8 for 8Mbytes of flash

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# Hex Display



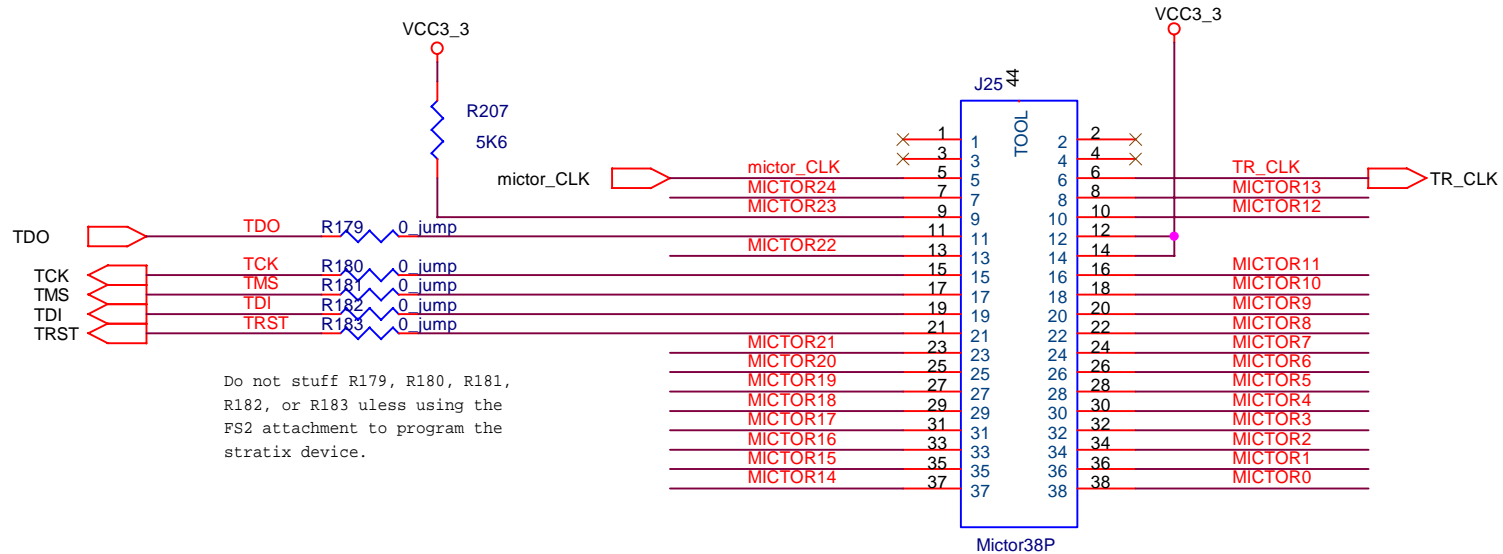
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LEDG[7:0] LEDG[7:0]

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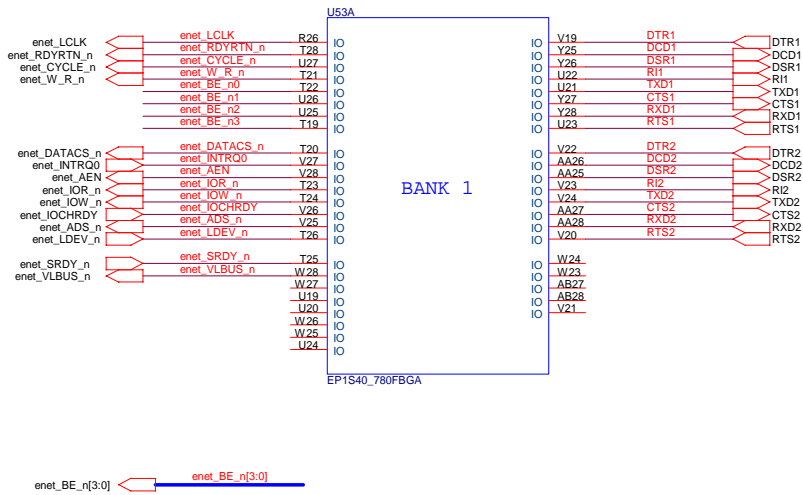




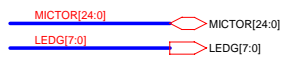
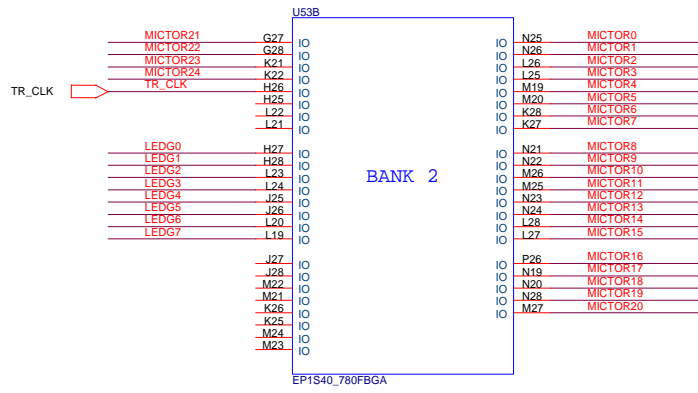
MICTOR[24:0] MICTOR[24:0]

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PLD Bank 1

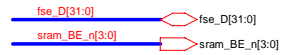
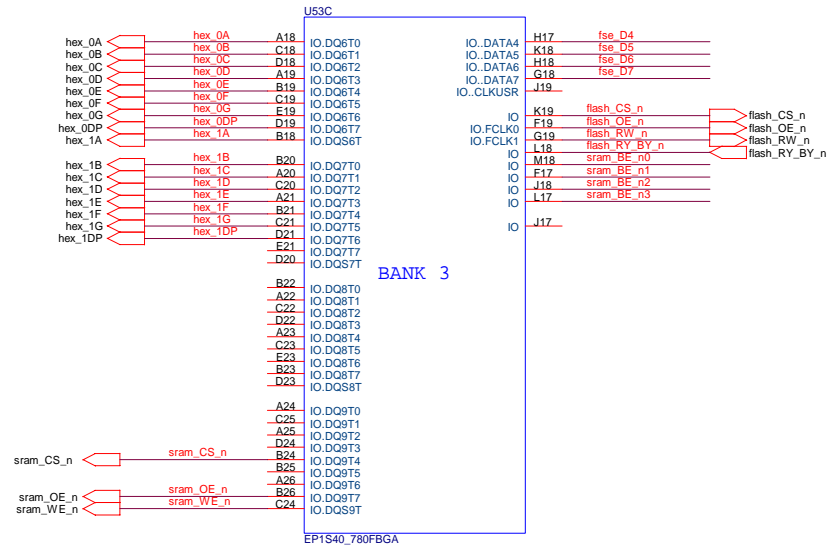


PLD Bank 2

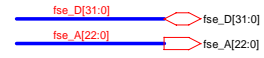
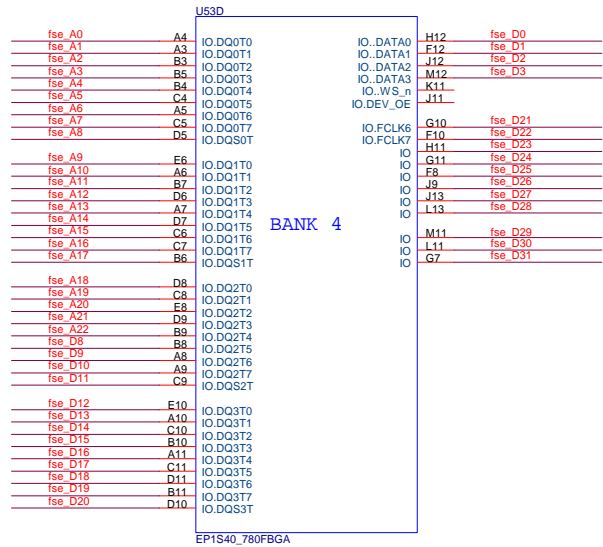


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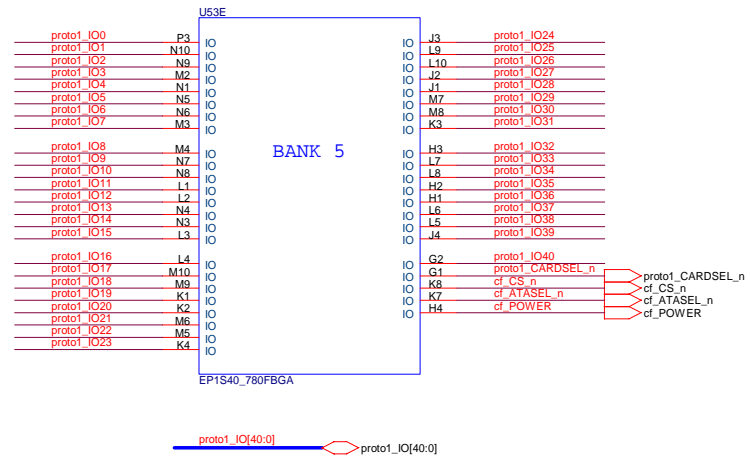
PLD Bank 3

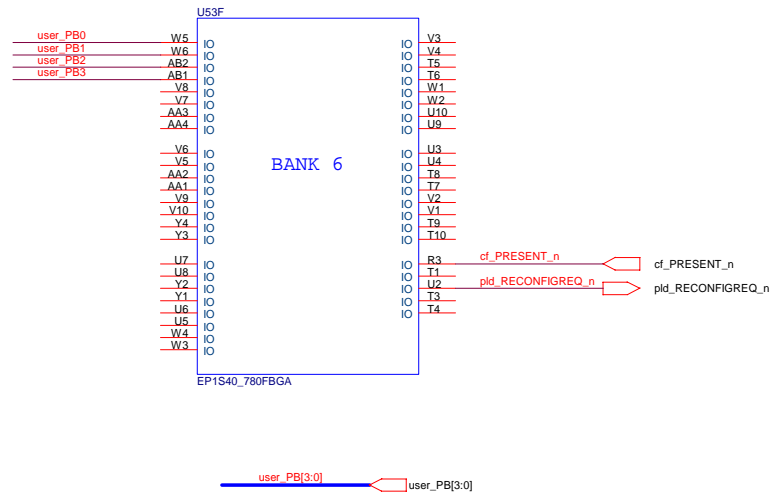


PLD Bank 4

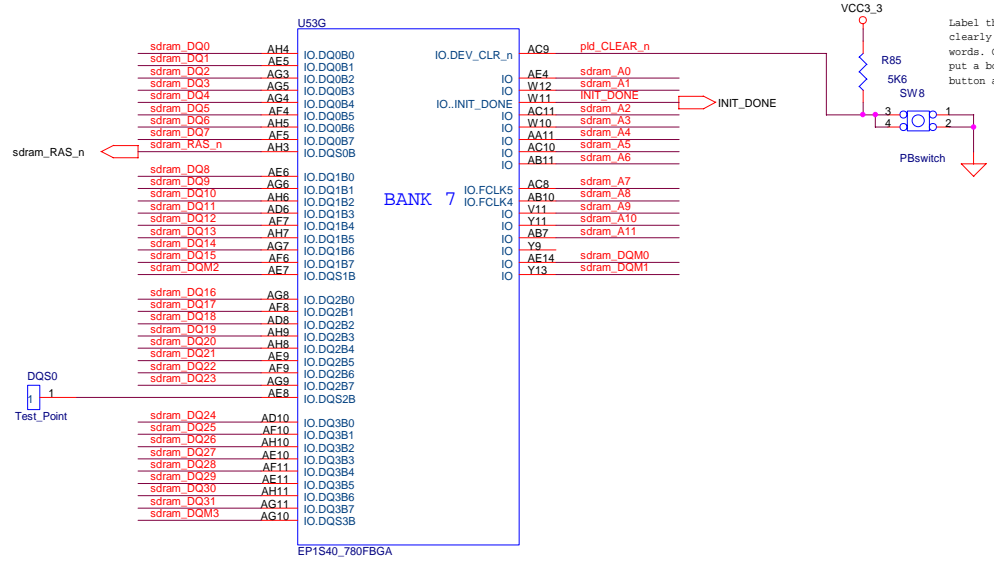


PLD Bank 5



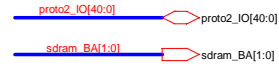
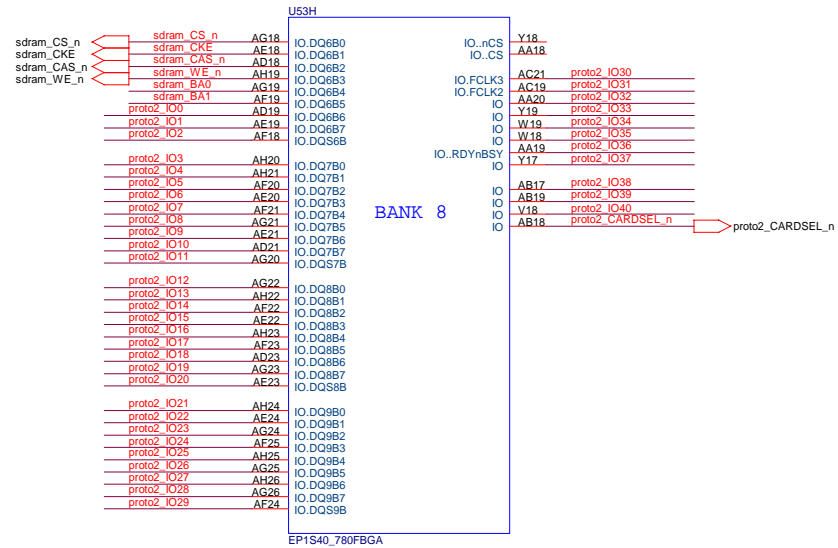


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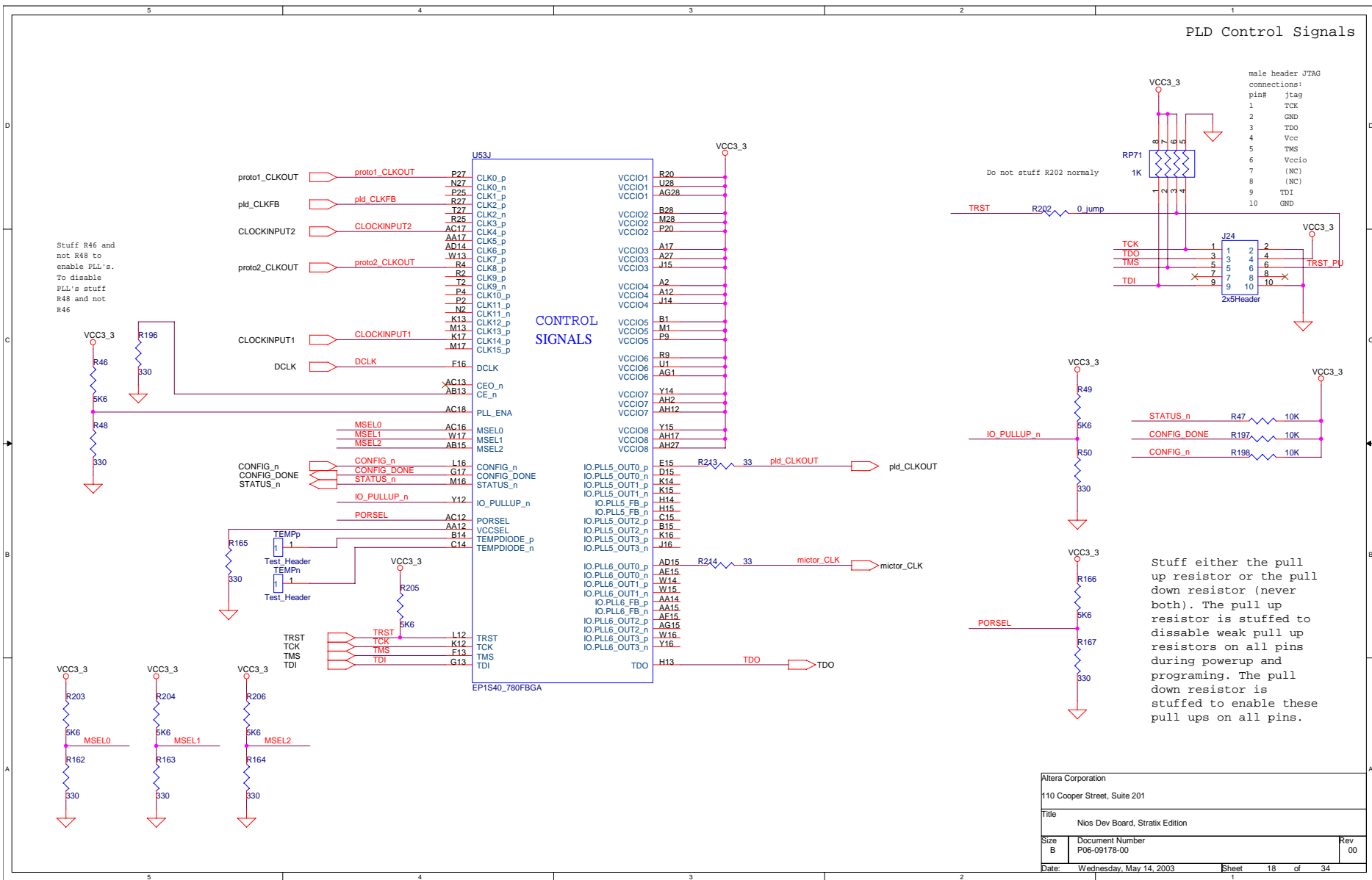




PLD Bank 8



# PLD Control Signals

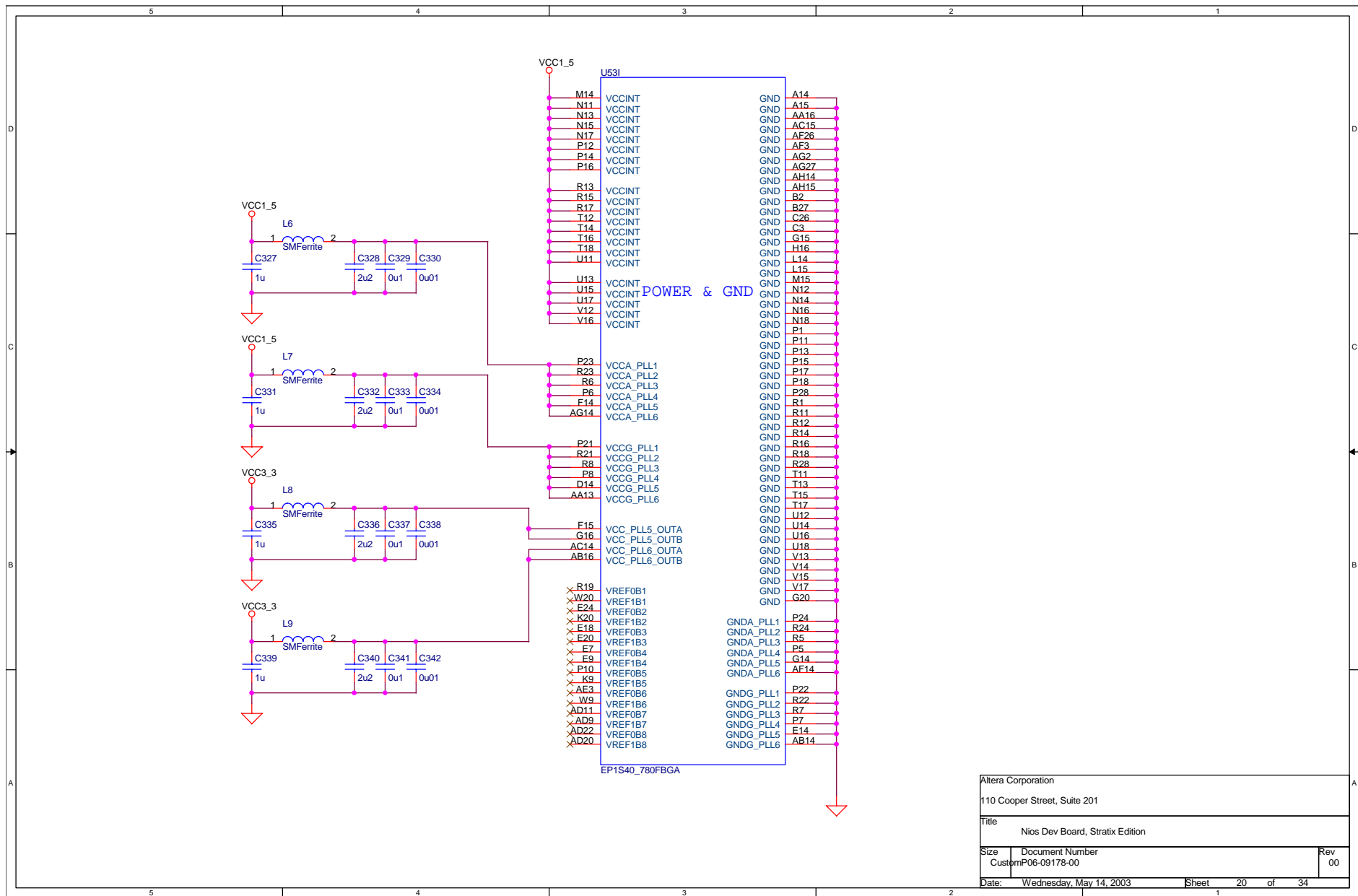


U53K

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<del>A16</del>	NC	NC	AF28
AA10	NC	NC	AG12
AA21	NC	NC	AG13
AA22	NC	NC	AG16
AA23	NC	NC	AG17
AA24	NC	NC	AH13
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<del>AA8</del>	NC	NC	B13
<del>AA9</del>	NC	NC	B16
AB12	NC	NC	B17
AB20	NC	NC	C1
AB21	NC	NC	C12
AB22	NC	NC	C13
AB23	NC	NC	C16
AB24	NC	NC	C17
AB25	NC	NC	C2
AB26	NC	NC	C27
<del>AB3</del>	NC	NC	C28
<del>AB4</del>	NC	NC	D1
<del>AB5</del>	NC	NC	D12
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<del>AB9</del>	NC	NC	D17
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AC20	NC	NC	D26
AC22	NC	NC	D27
AC23	NC	NC	D28
AC24	NC	NC	D3
AC25	NC	NC	D4
AC26	NC	NC	E1
AC27	NC	NC	E11
AC28	NC	NC	E12
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<del>AC7</del>	NC	NC	F1
AD1	NC	NC	F11
AD12	NC	NC	F18
AD13	NC	NC	F2
AD16	NC	NC	F20
AD17	NC	NC	F21
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AD24	NC	NC	F23
AD25	NC	NC	F24
AD26	NC	NC	F25
AD27	NC	NC	F26
AD28	NC	NC	F27
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<del>AD4</del>	NC	NC	F3
<del>AD5</del>	NC	NC	F4
<del>AD7</del>	NC	NC	F5
<del>AF2</del>	NC	NC	F6
AF17	NC	NC	F7
AF16	NC	NC	F9
AF13	NC	NC	G12
AF12	NC	NC	G21
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AE28	NC	NC	G23
AE27	NC	NC	G24
AE26	NC	NC	G25
AE25	NC	NC	G26
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AE17	NC	NC	G4
AE16	NC	NC	G5
AE13	NC	NC	G6
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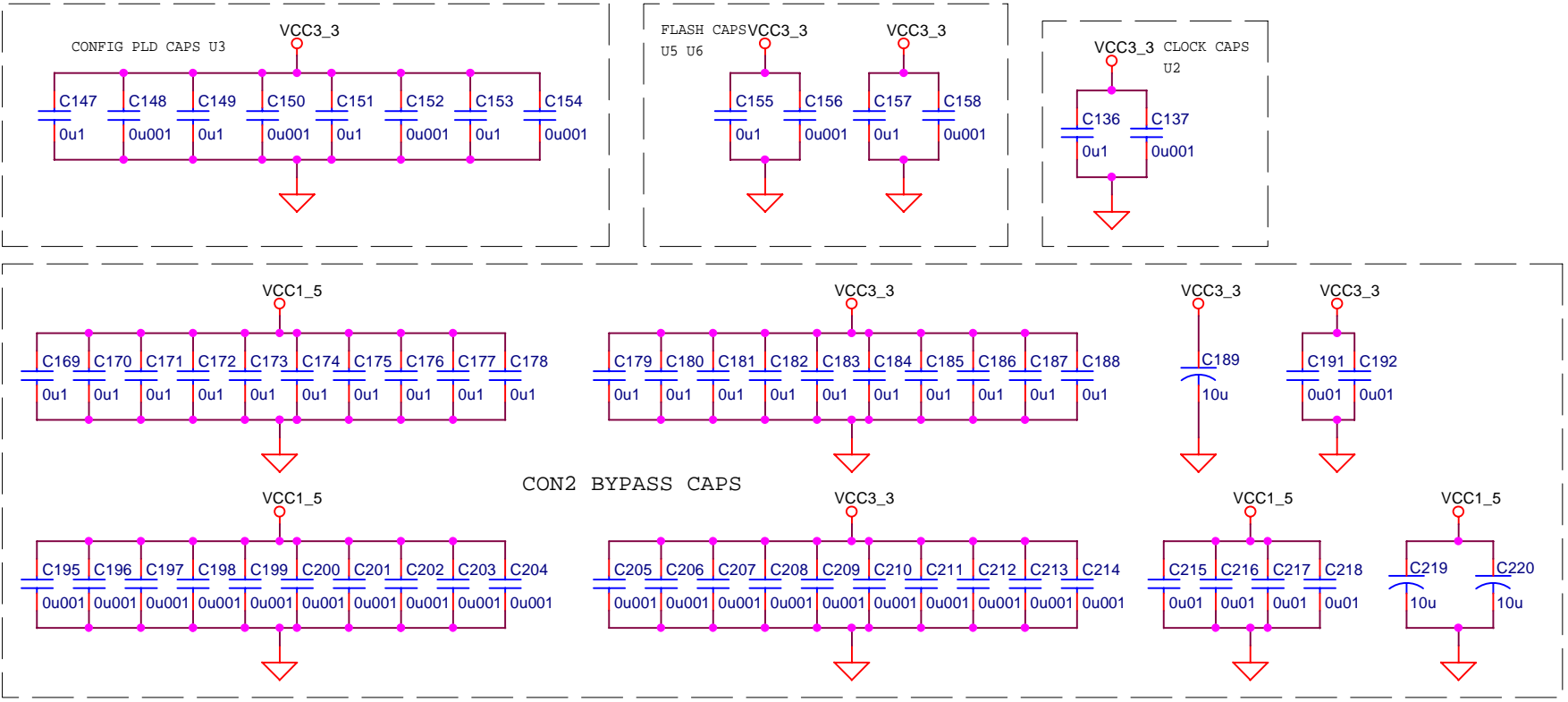
EP1S40\_780FBGA

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# Bypass CAPS



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5 4 3 2 1

D

D

C

C

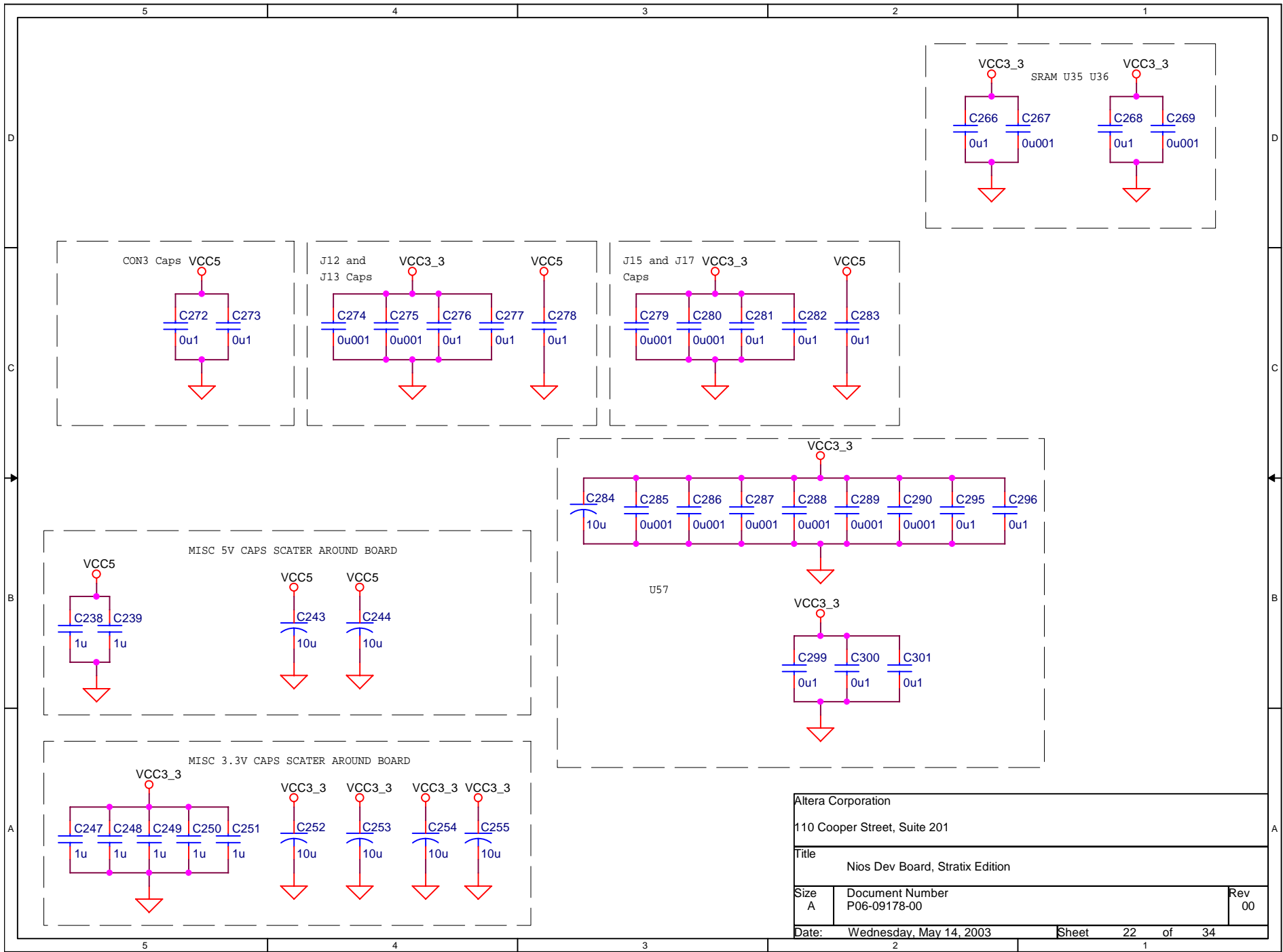
B

B

A

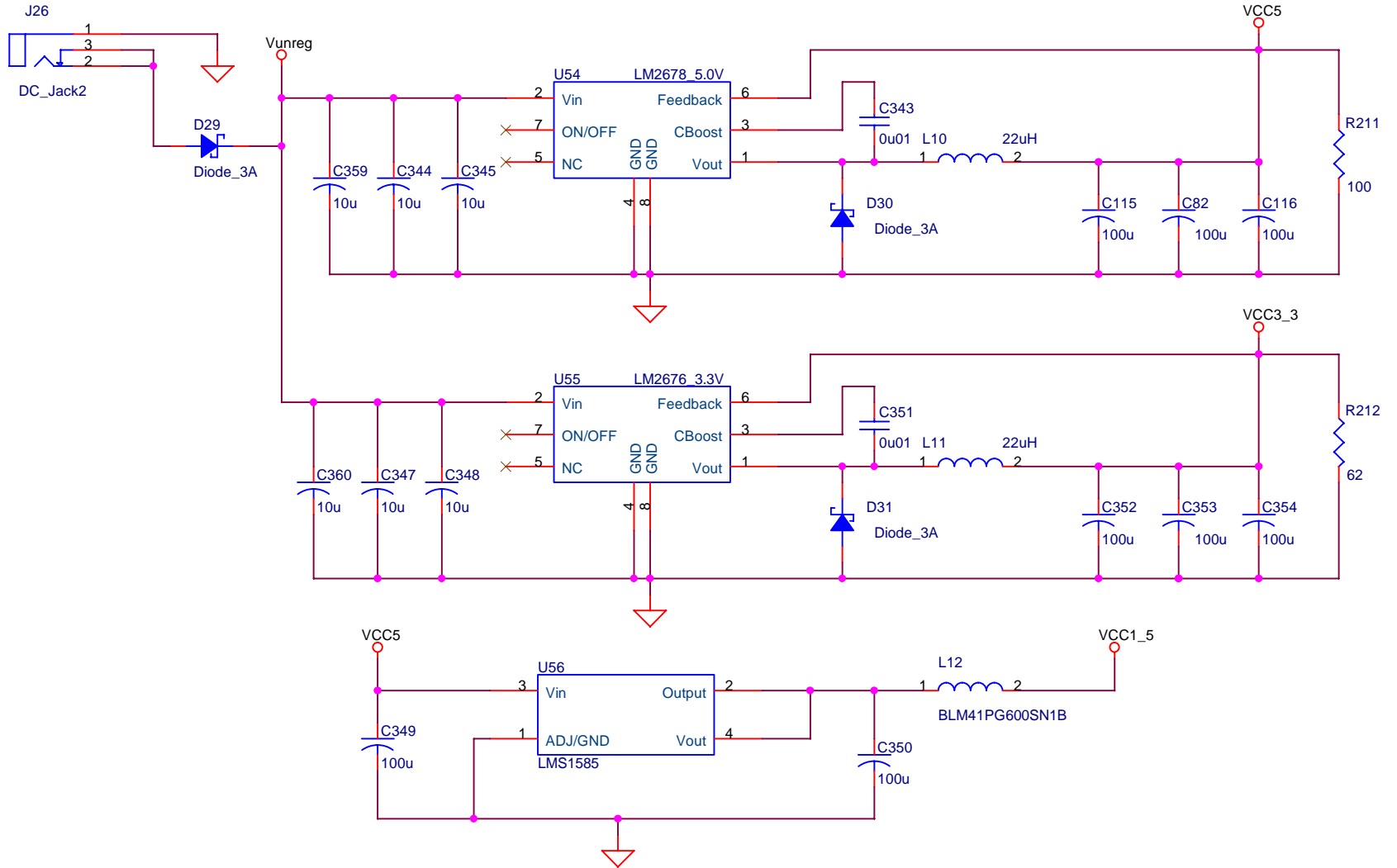
A

5 4 3 2 1



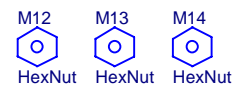
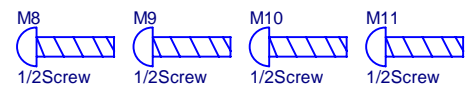
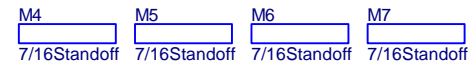
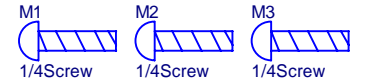
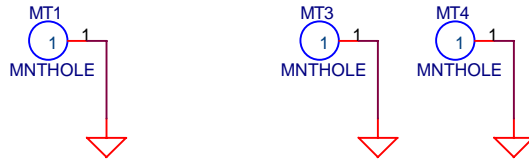
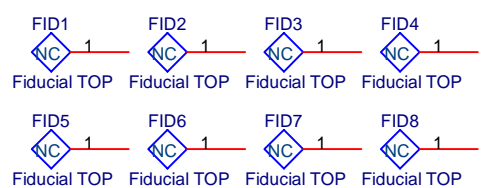
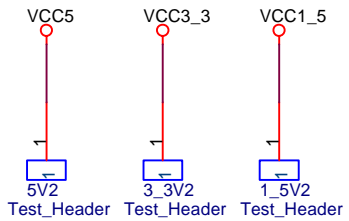
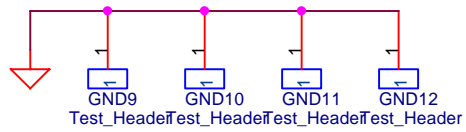
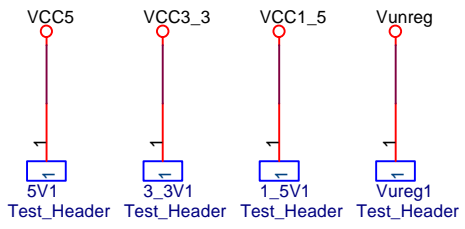
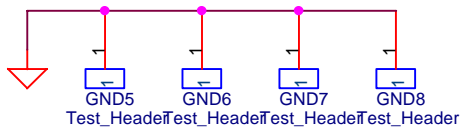
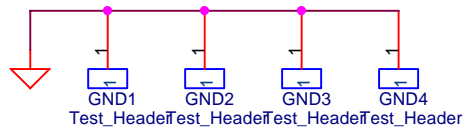
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Power Connector

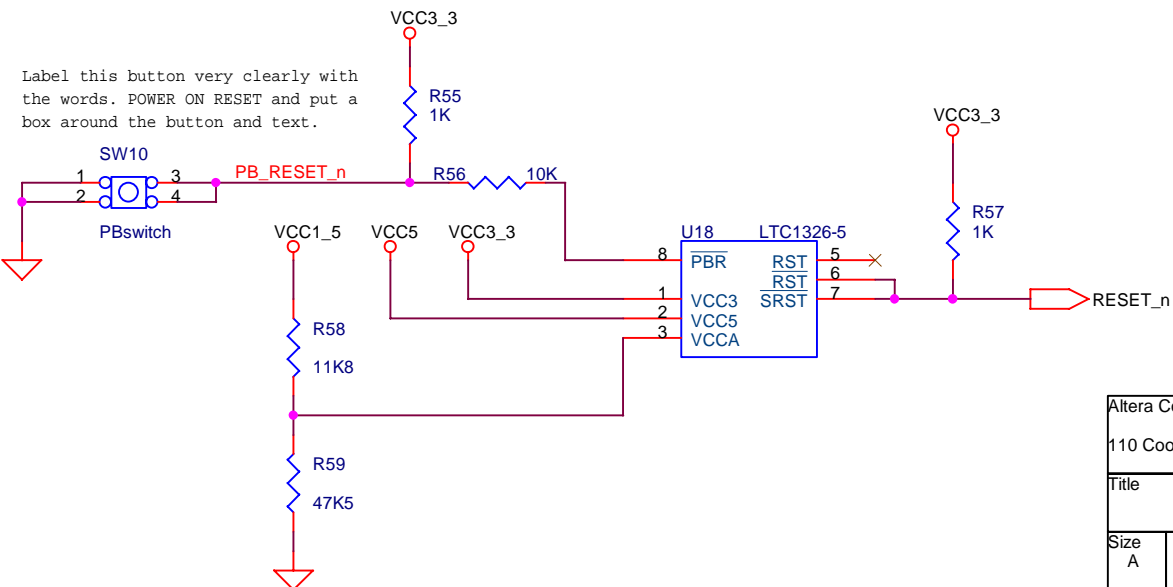


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# Reset and Test headers

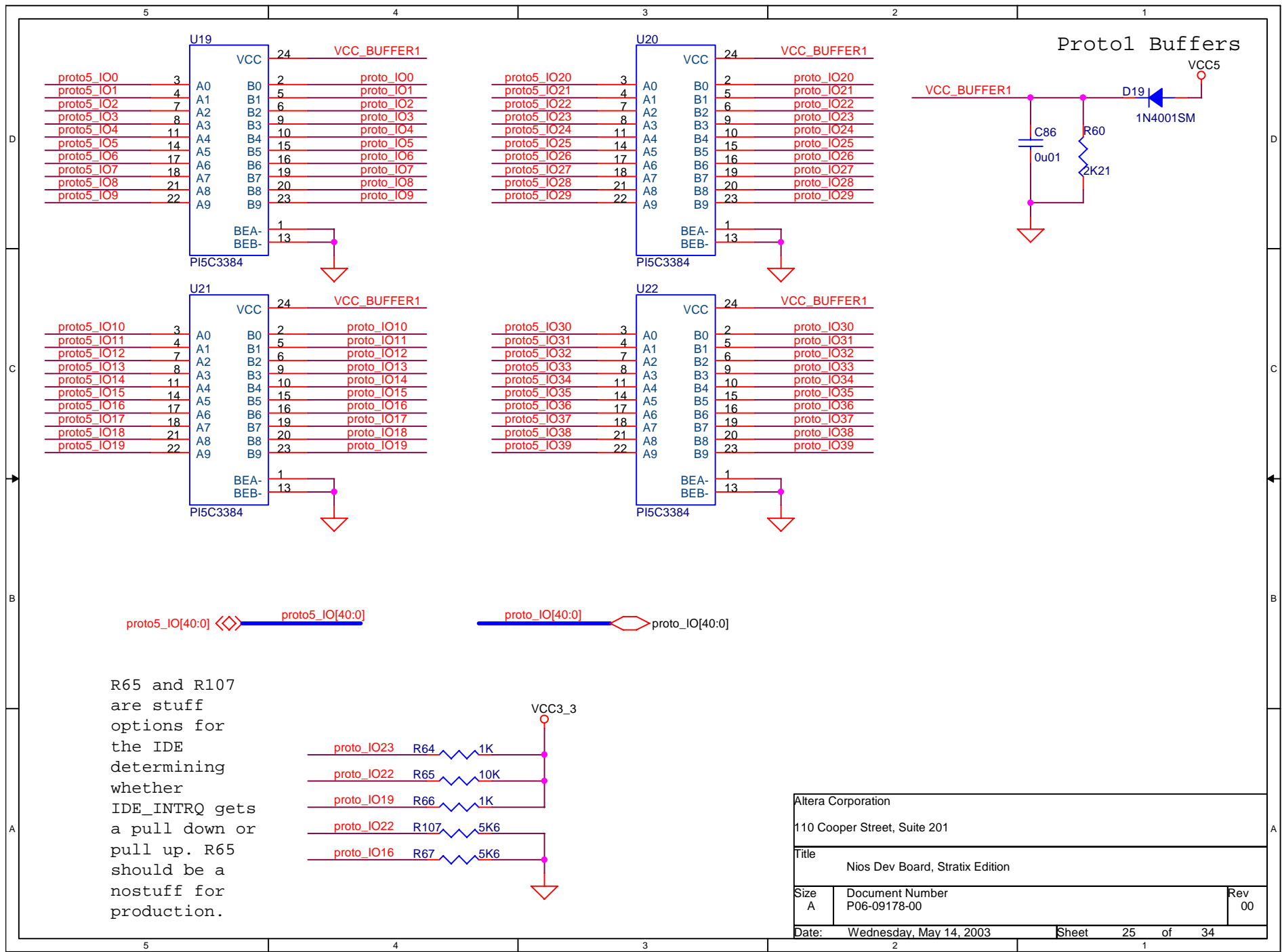


Label this button very clearly with the words. POWER ON RESET and put a box around the button and text.

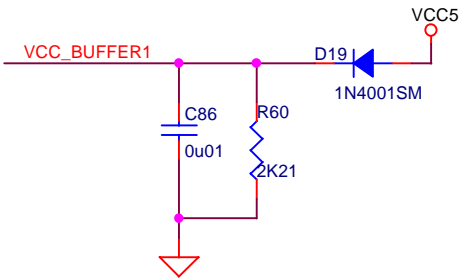


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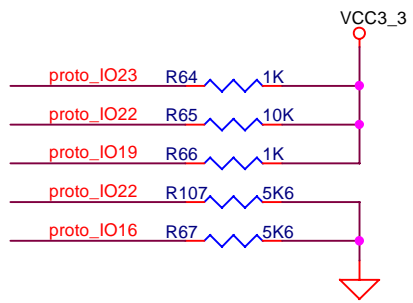




### Protol Buffers

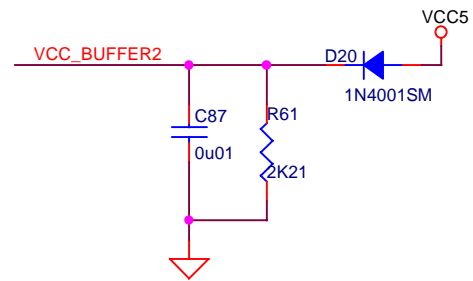
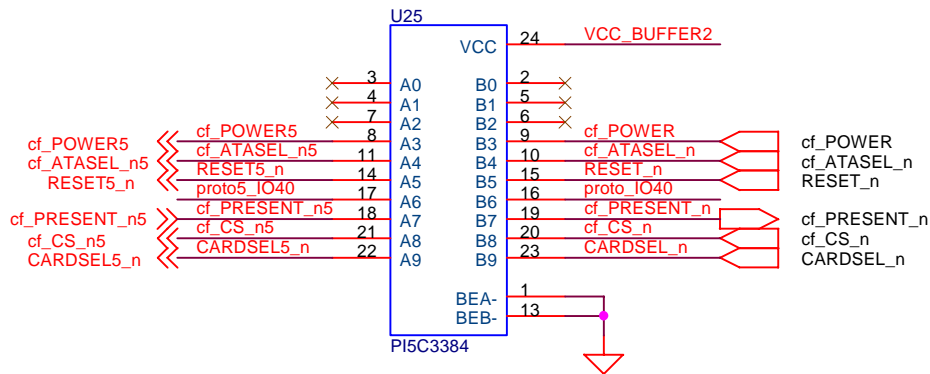


R65 and R107 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R65 should be a nostuff for production.



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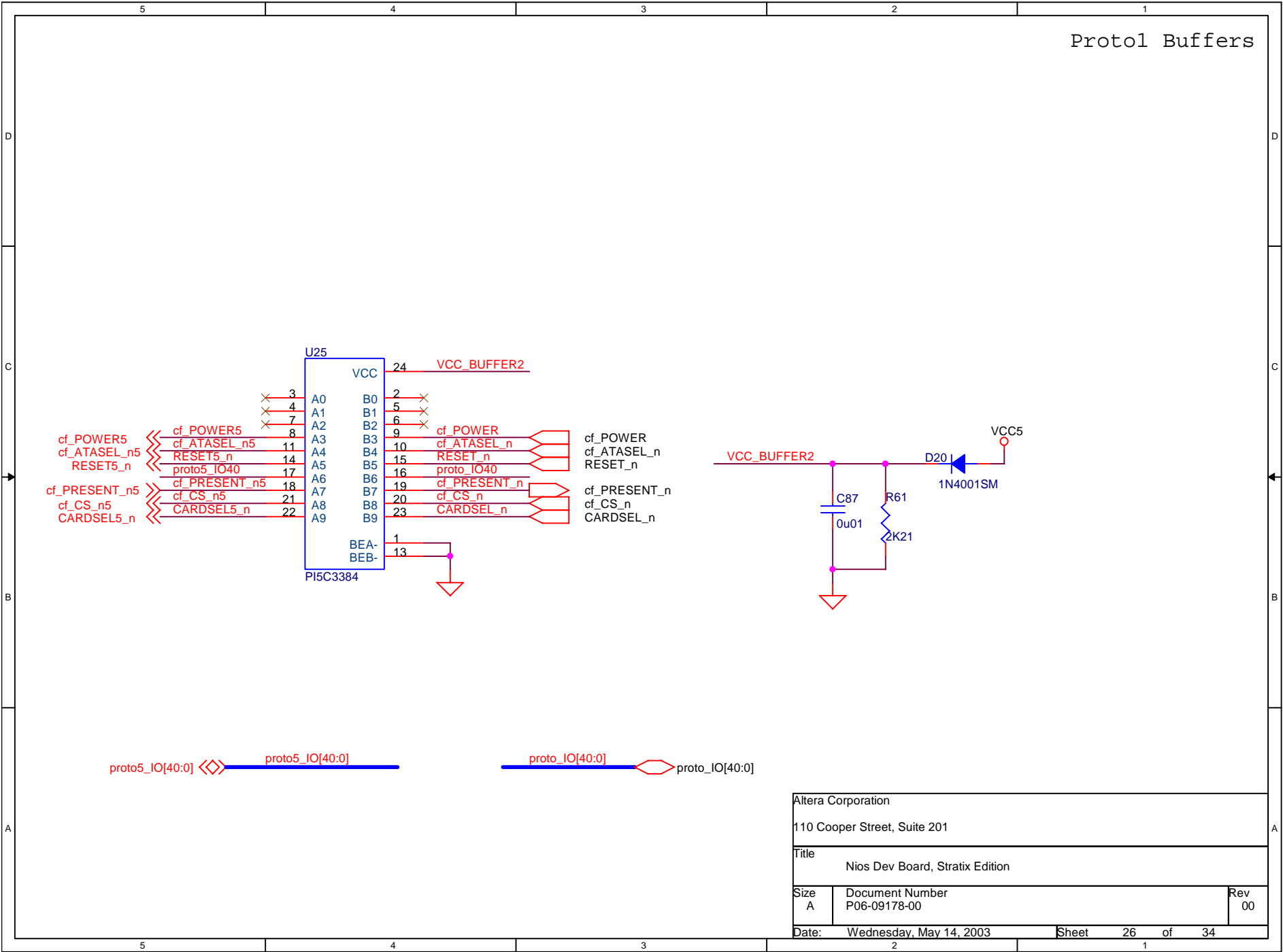
# Protol Buffers



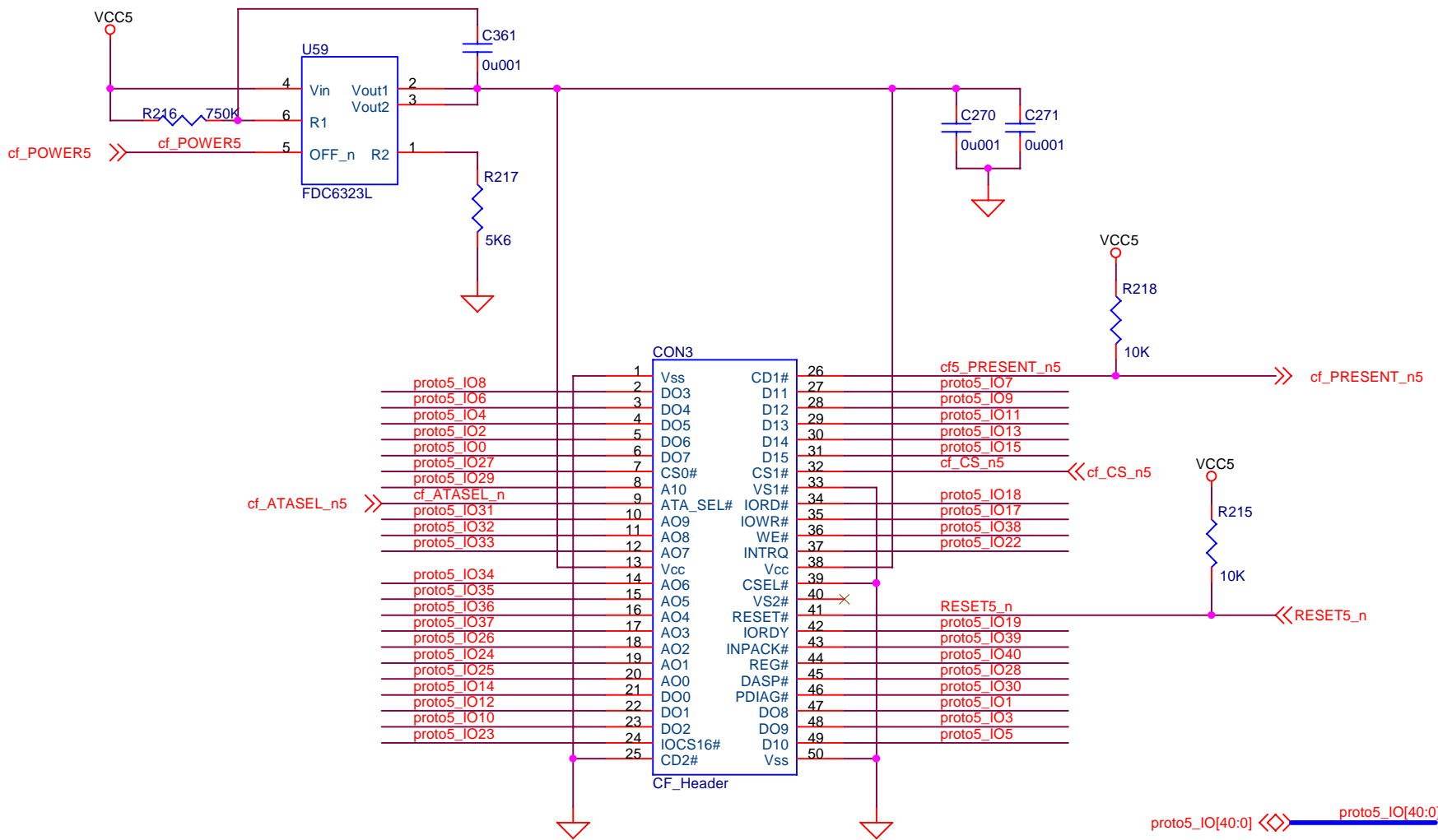
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proto\_IO[40:0] <<> proto\_IO[40:0]

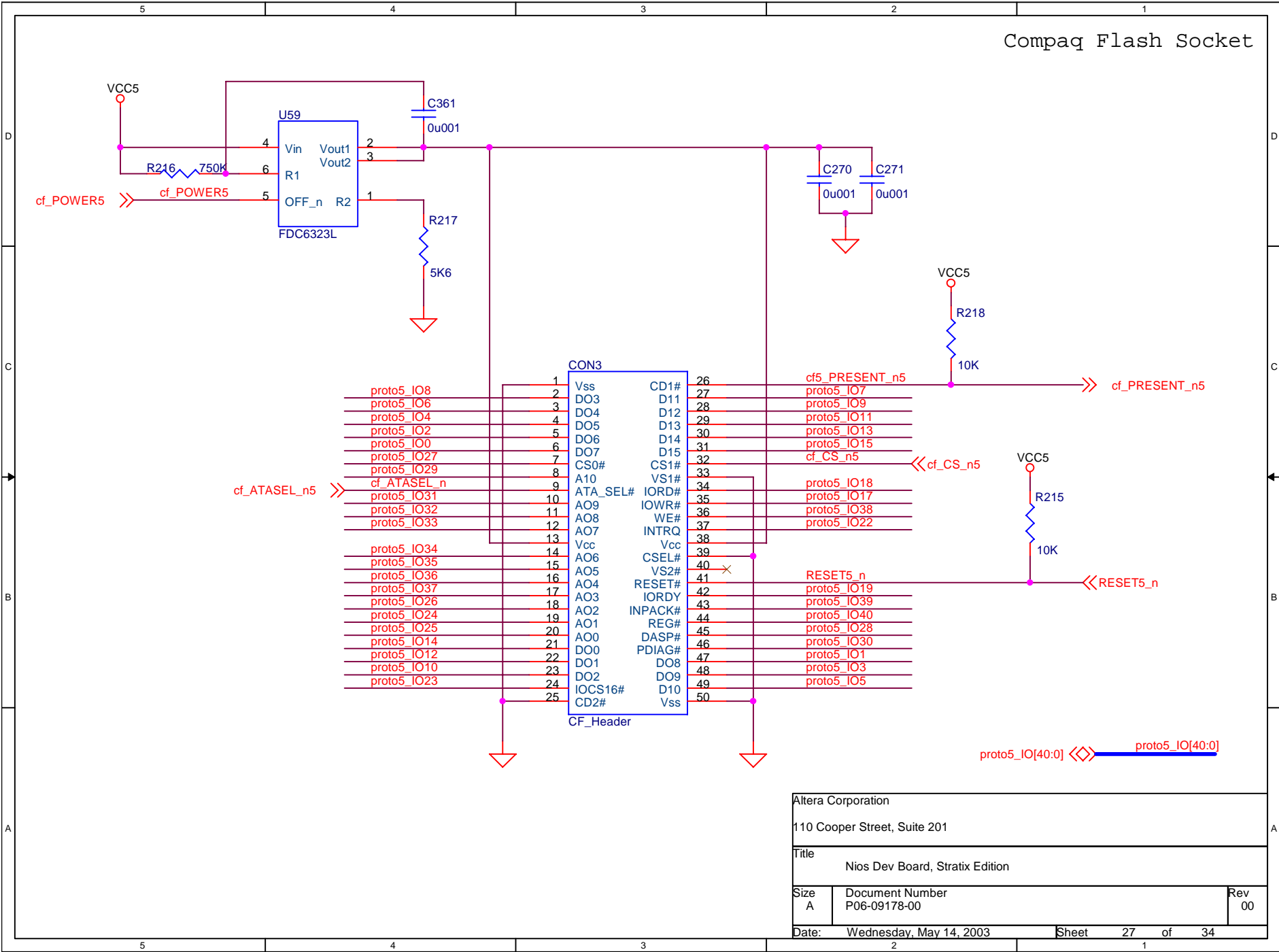
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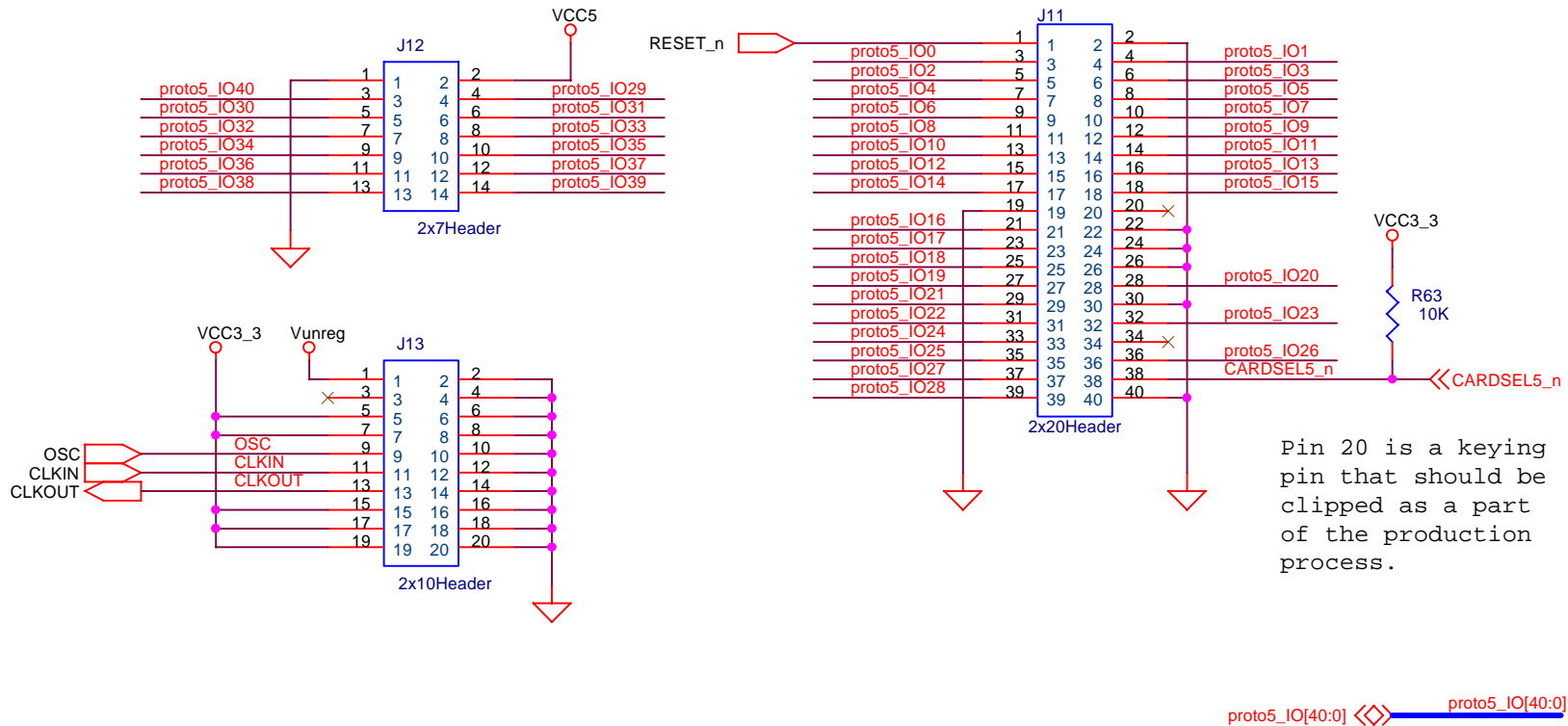
# Compaq Flash Socket



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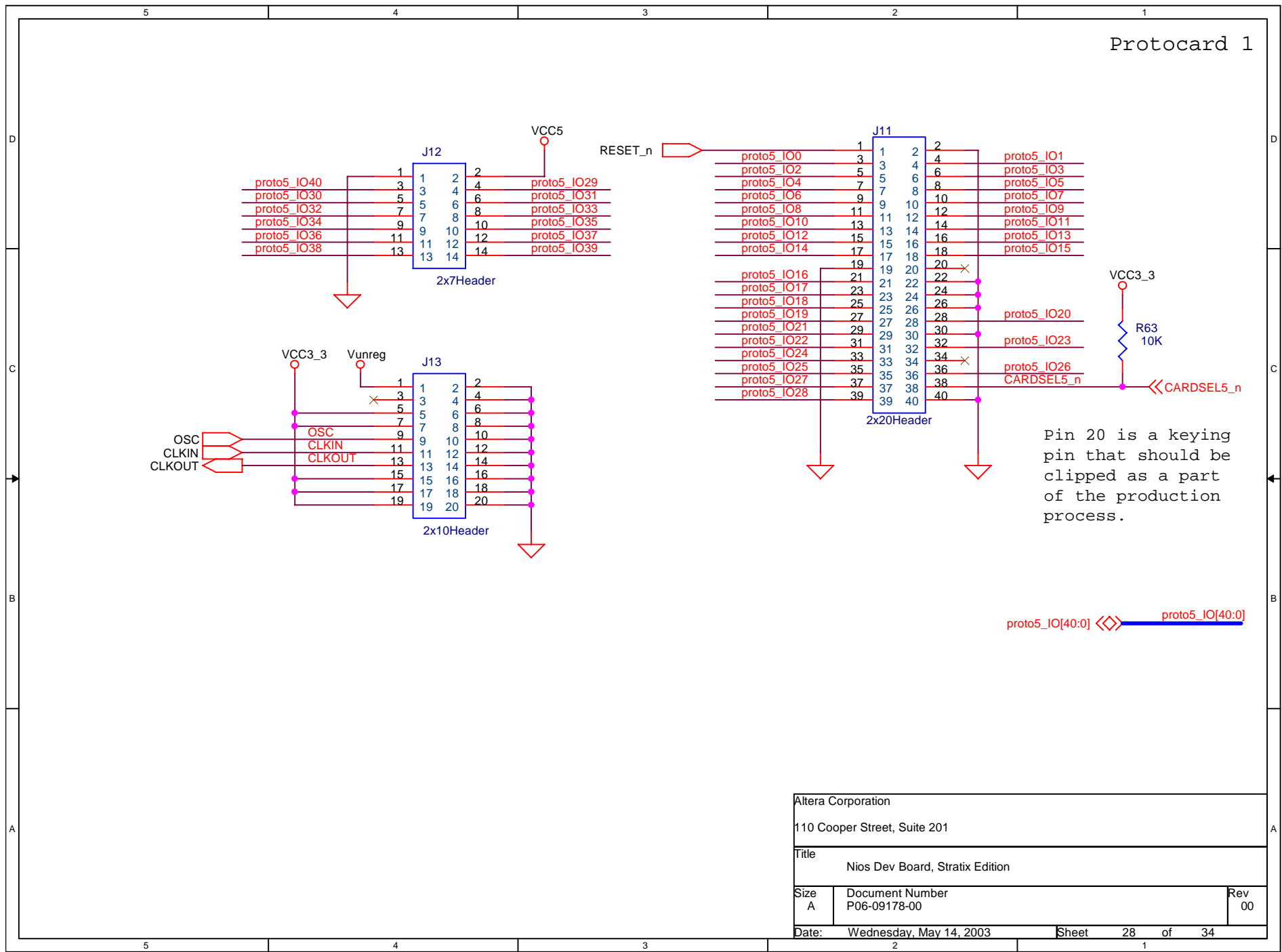


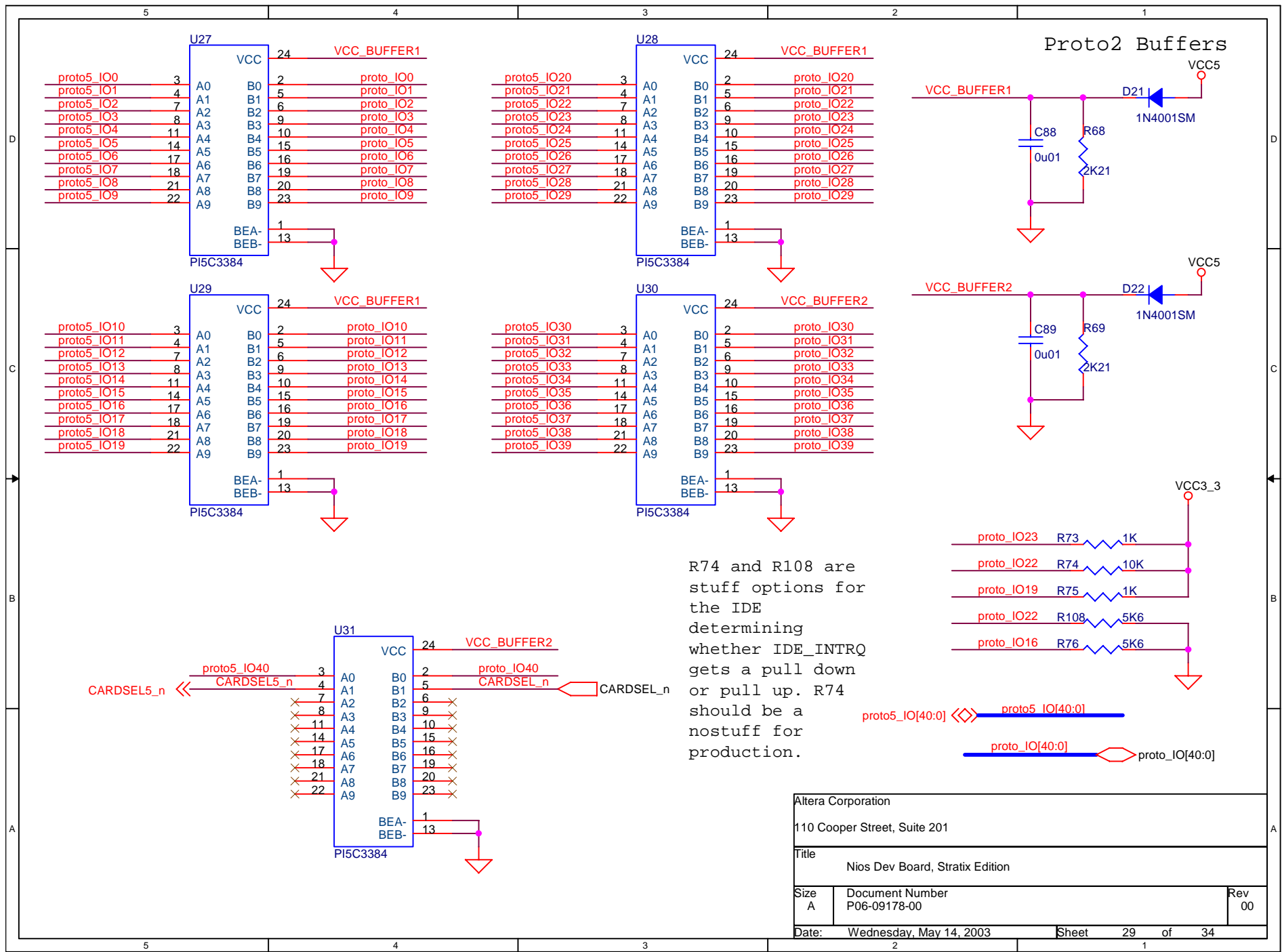
# Protocard 1



Pin 20 is a keying pin that should be clipped as a part of the production process.

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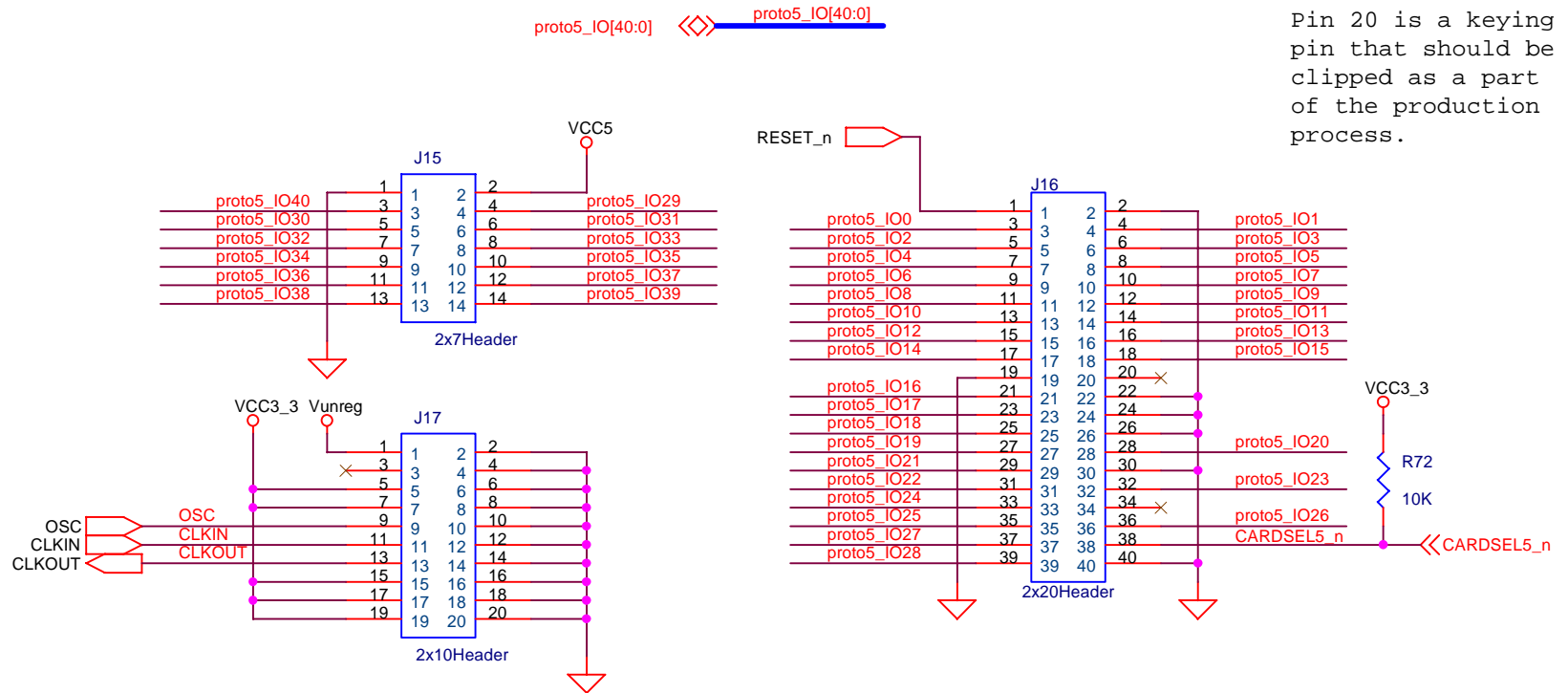


R74 and R108 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R74 should be a nostuff for production.

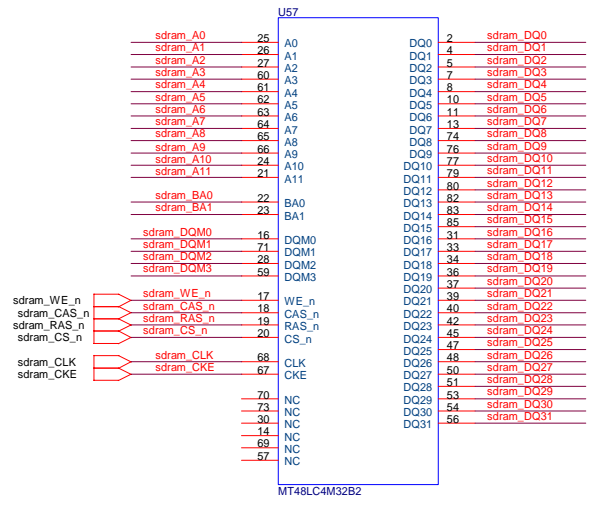
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# Proto2 Headers

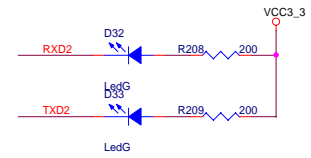
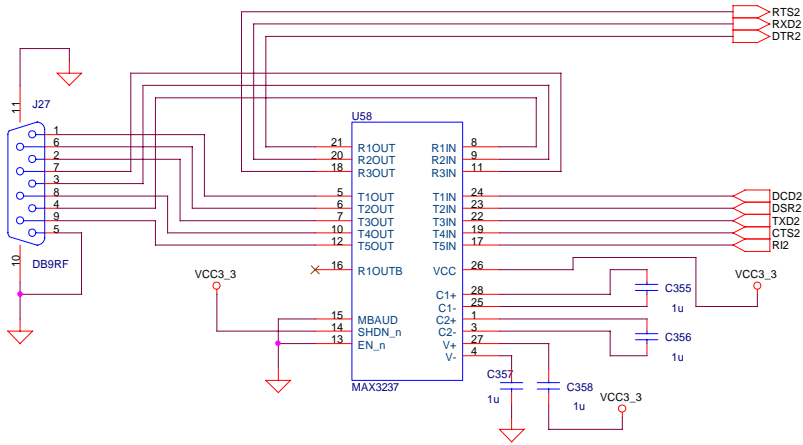
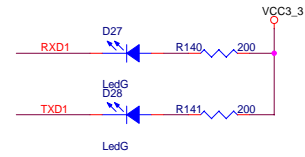
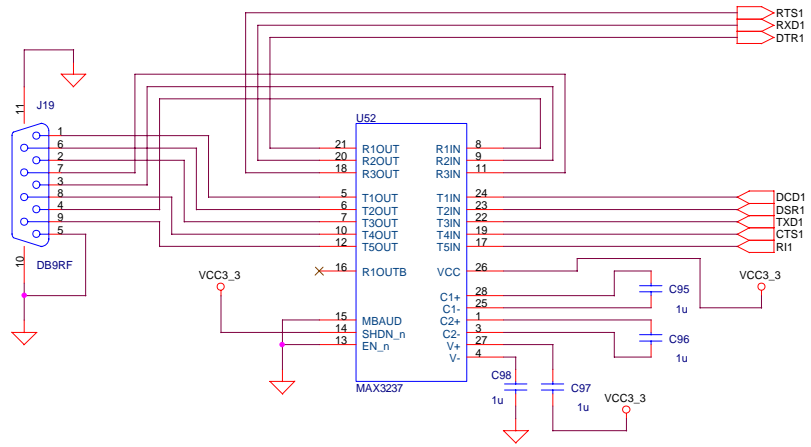
Pin 20 is a keying pin that should be clipped as a part of the production process.



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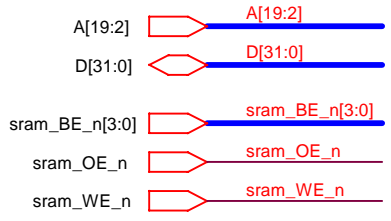
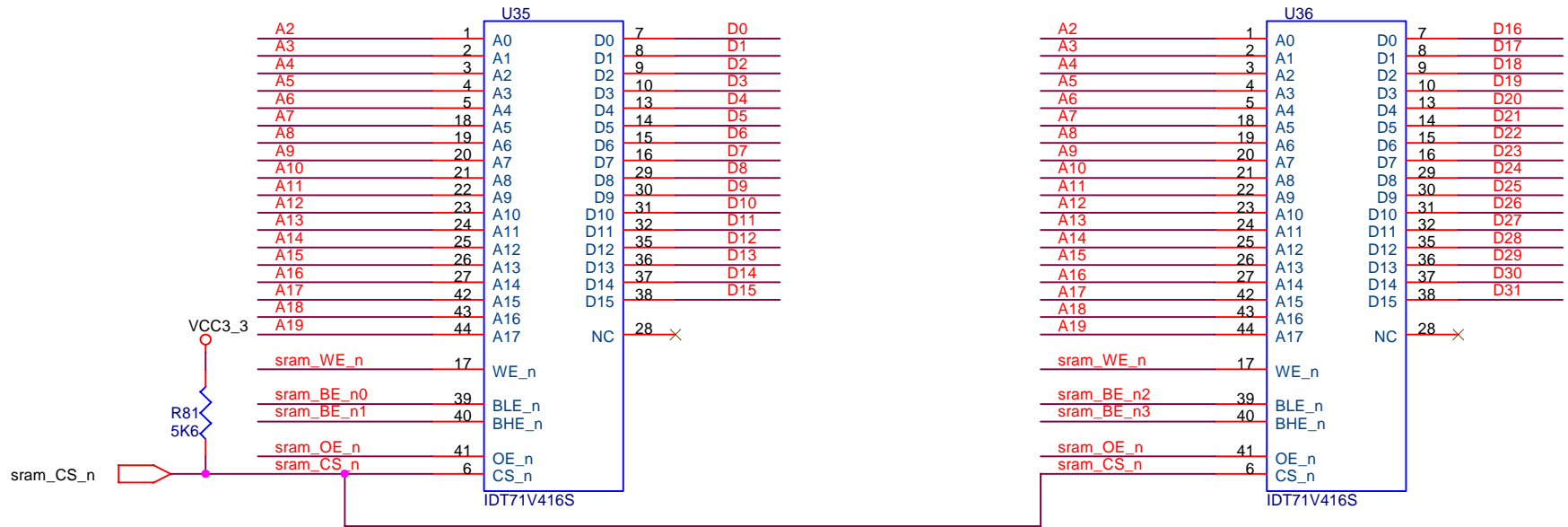
# Serial Ports



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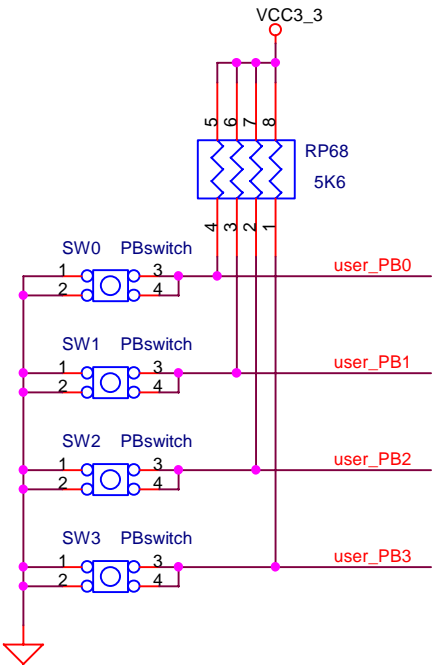
SRAM



One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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Switches Buttons



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