Nios Development Board
Stratix Edition
Rev 00

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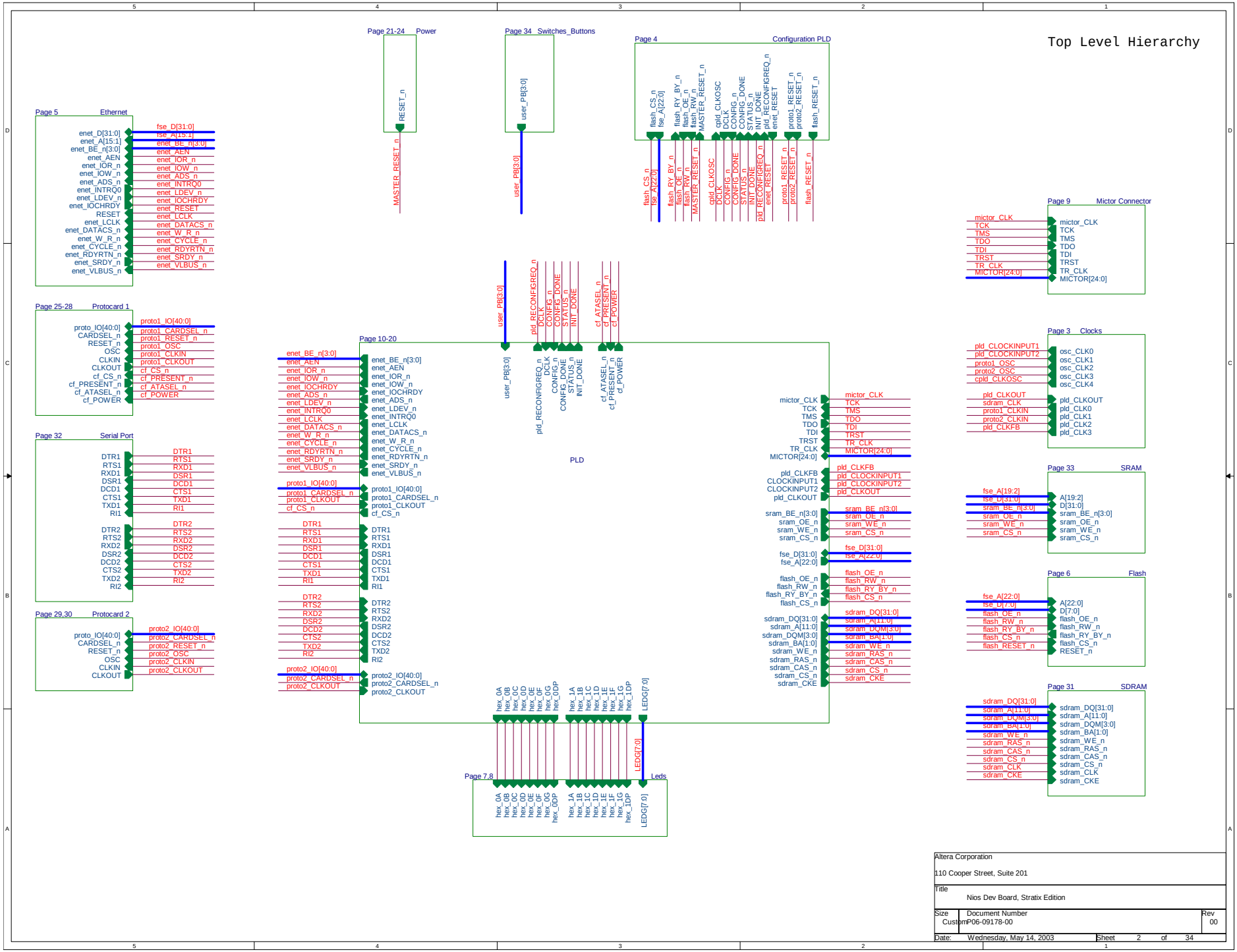

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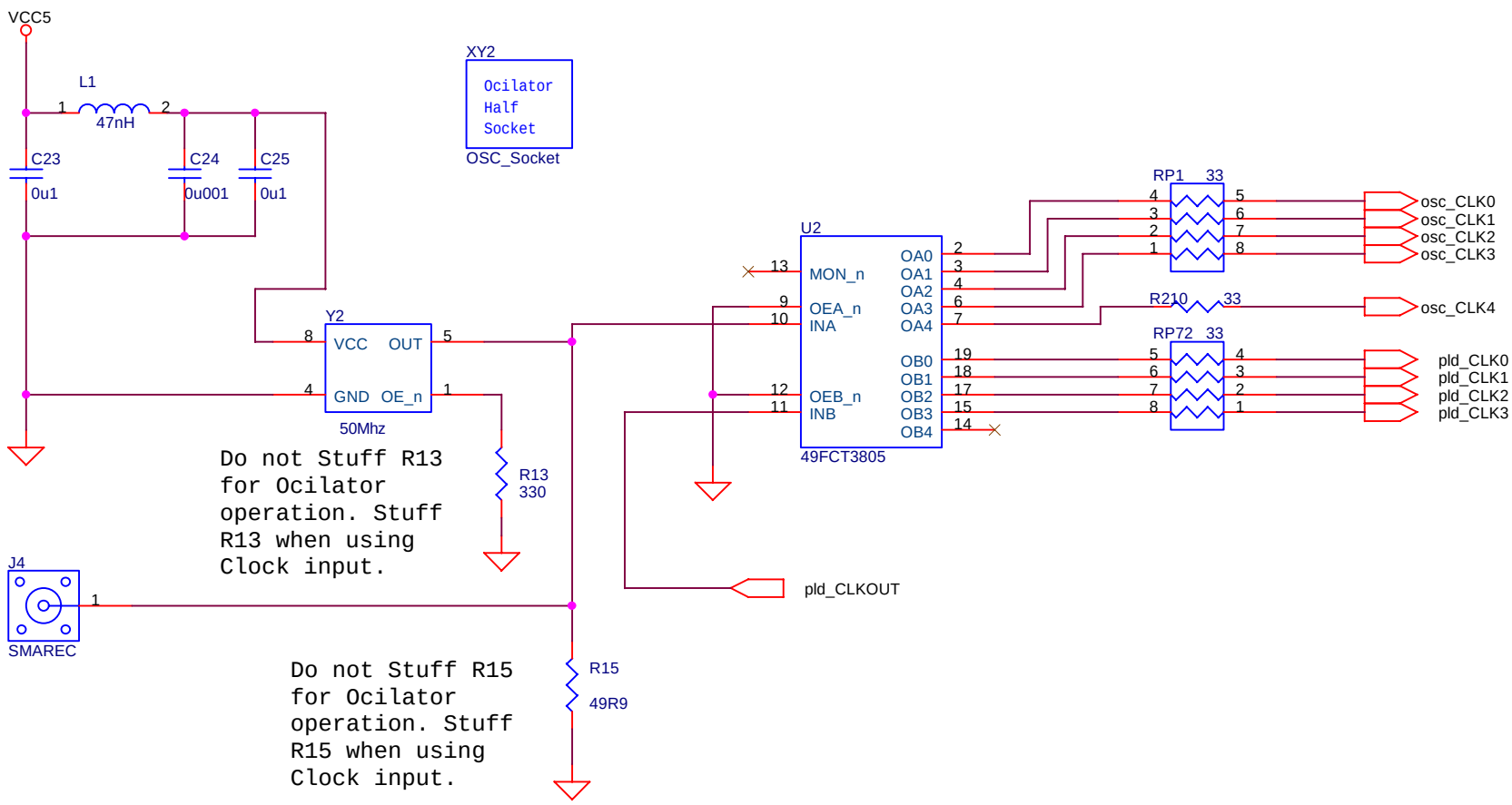
Clocks



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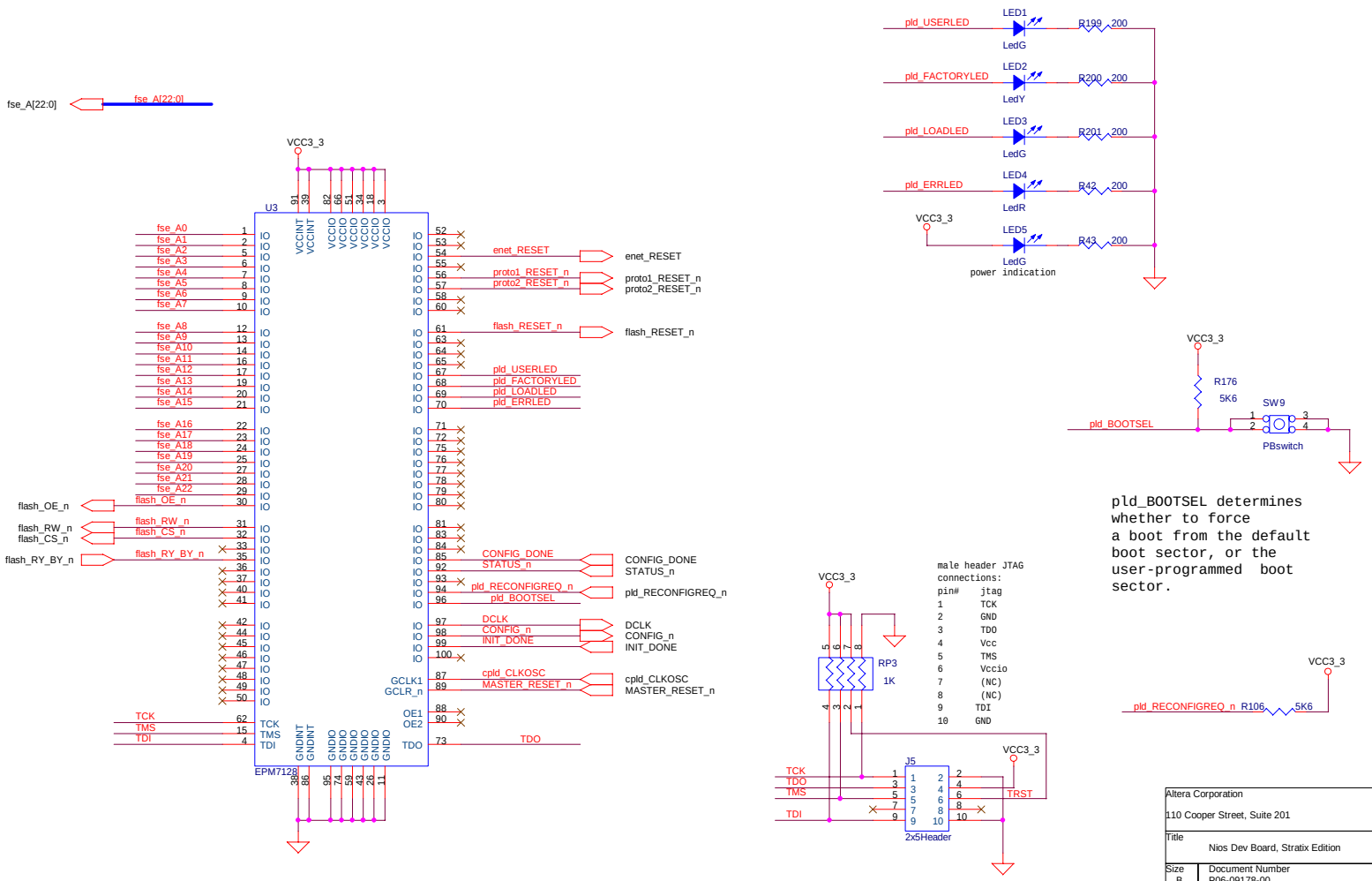
Configuration PLD



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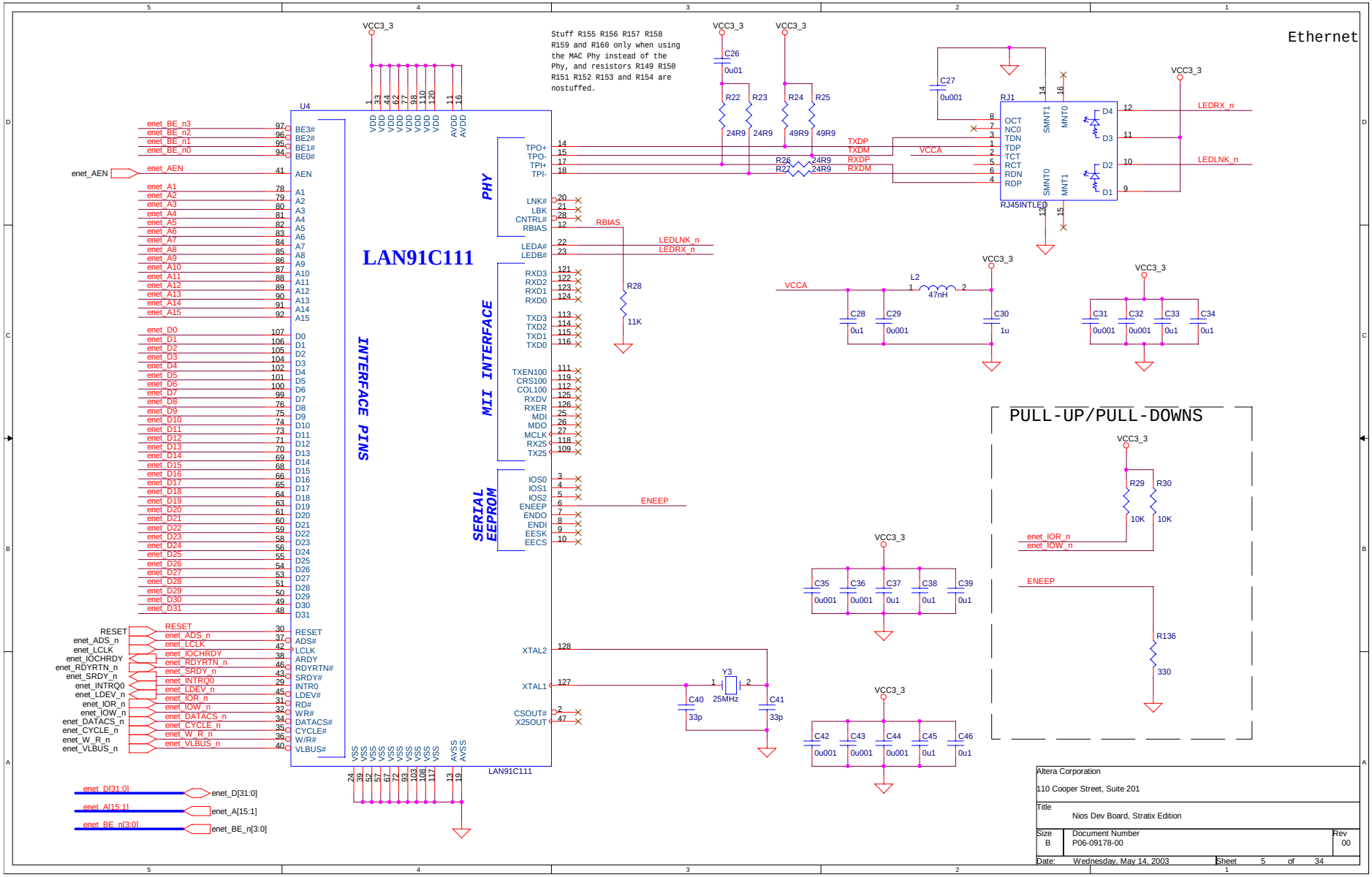
Ethernet
Stuff R155 R156 R157 R158 R159 and R160 only when using the MAC Phy instead of the Phy, and resistors R149 R150 R151 R152 R153 and R154 are nostuffed.
LAN91C111
PHY
MII INTERFACE
SERIAL EEPROM
INTERFACE PINS
PULL-UP/PULL-DOWNS
RJ45INTLED
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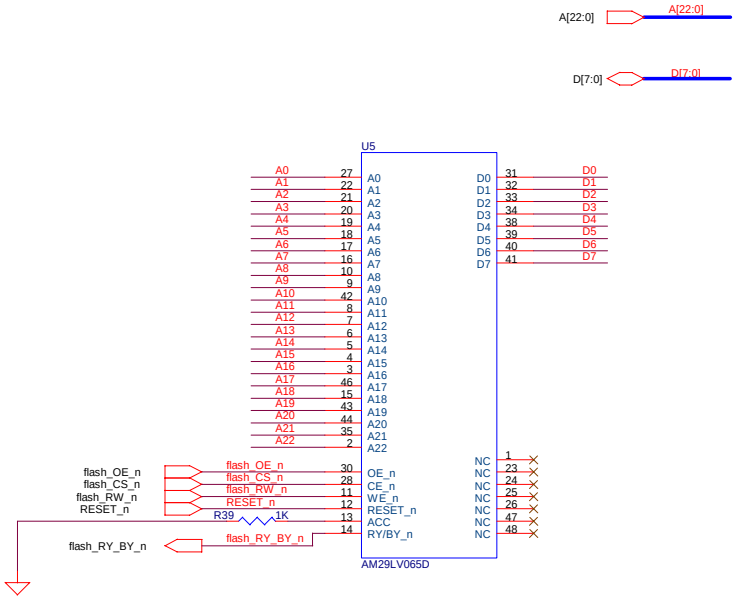
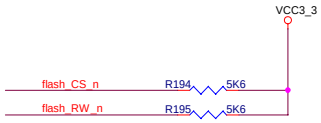
Flash





Flash chip is 8M x 8 for
8Mbytes of flash

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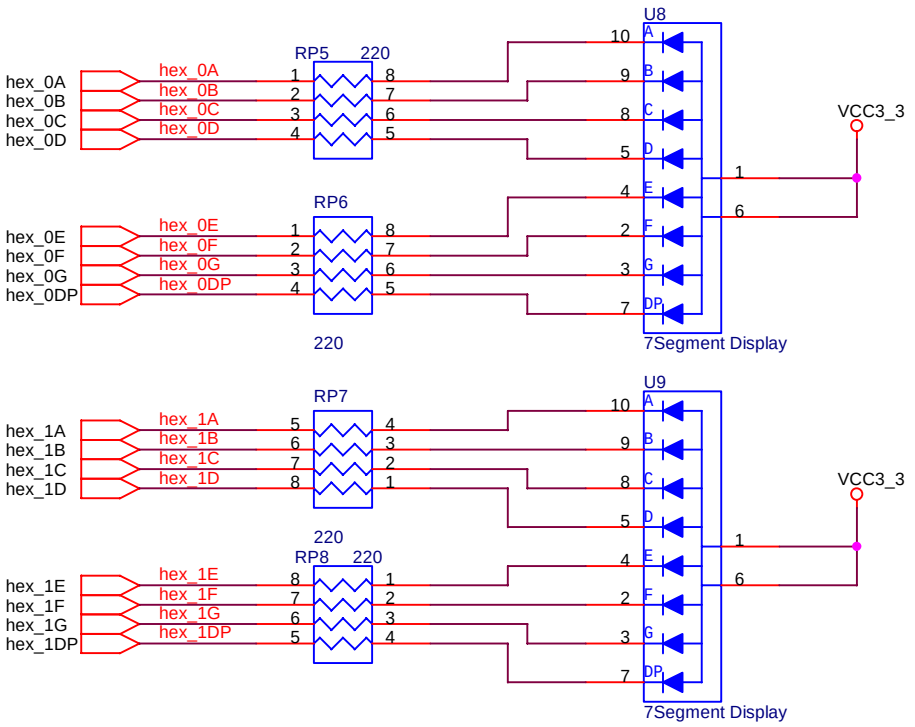
Hex Display



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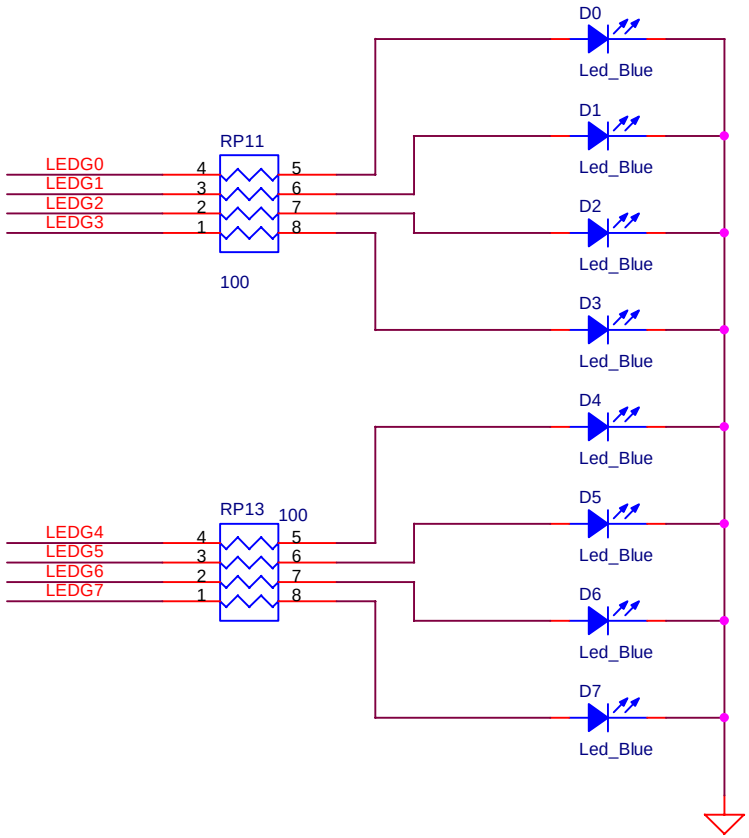
Leds



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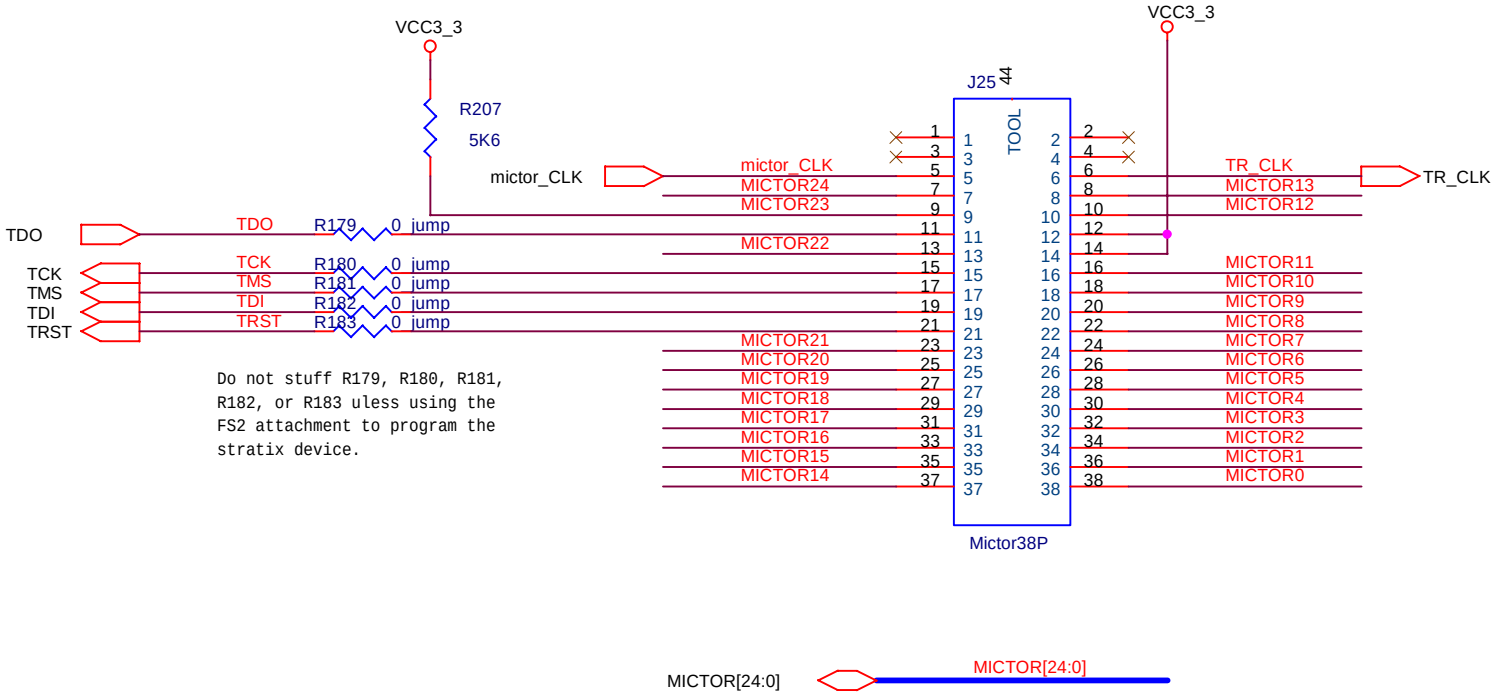

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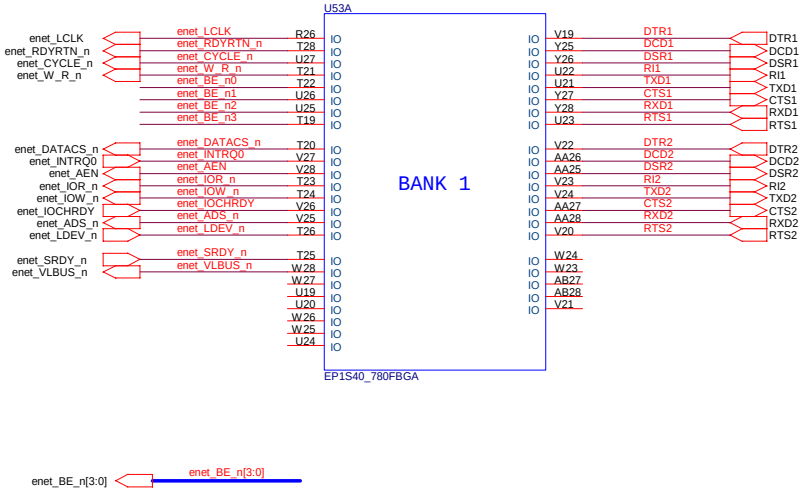
PLD Bank 1



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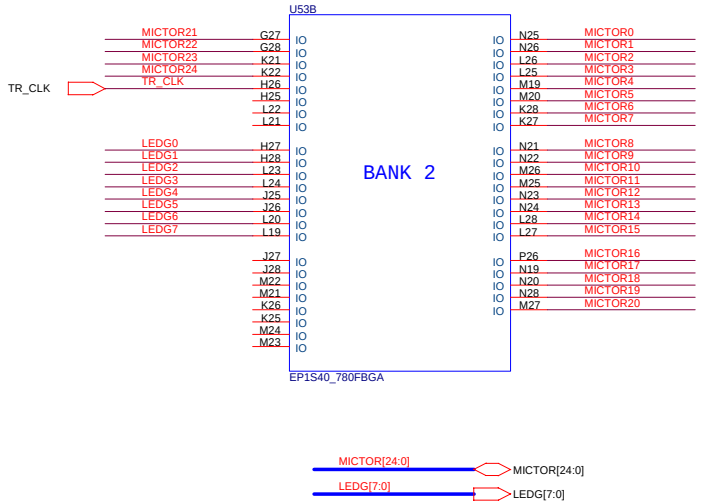
PLD Bank 2



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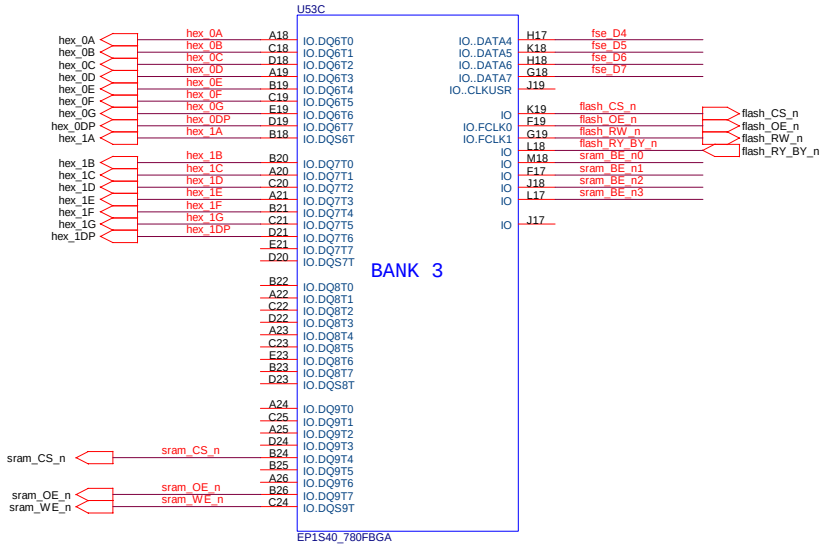
PLD Bank 3



fse_D[31:0] → fse_D[31:0]

sram_BE_n[3:0] → sram_BE_n[3:0]

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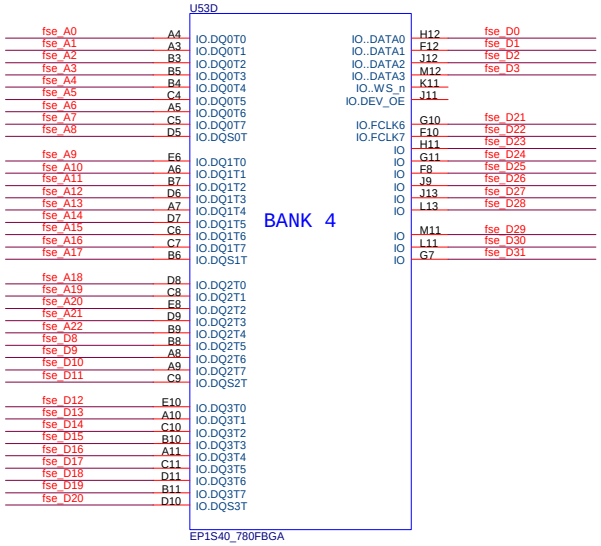
PLD Bank 4



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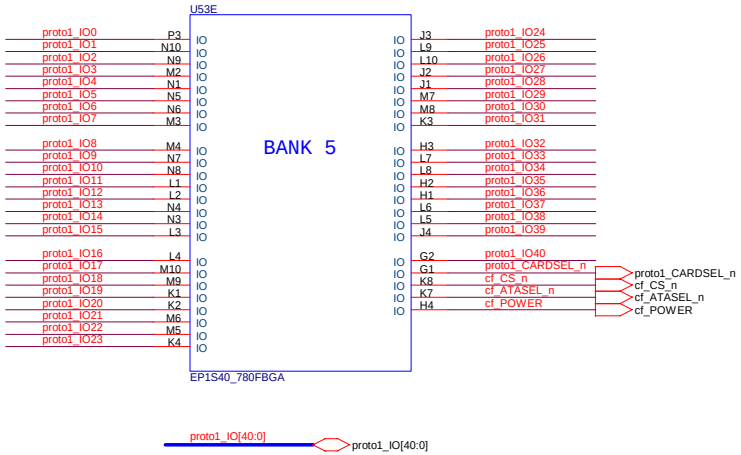
PLD Bank 5



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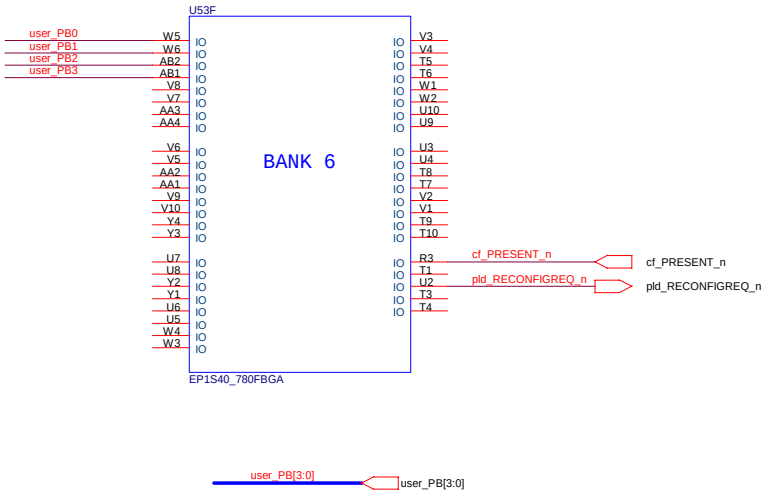
PLD Bank 6



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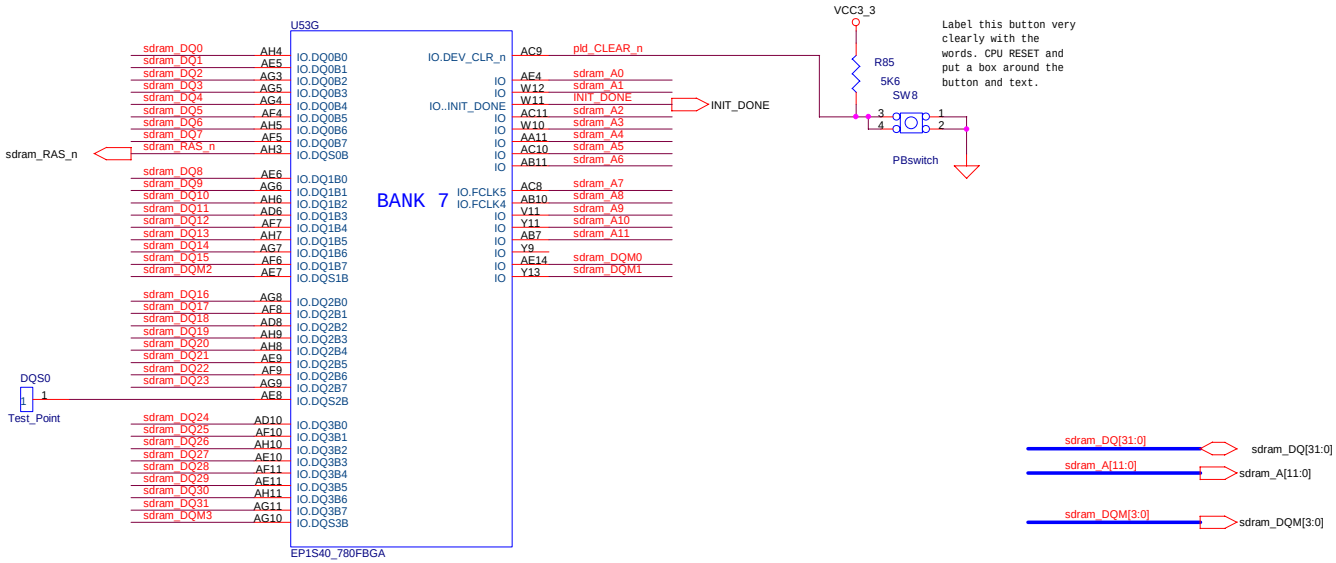
PLD Bank 7



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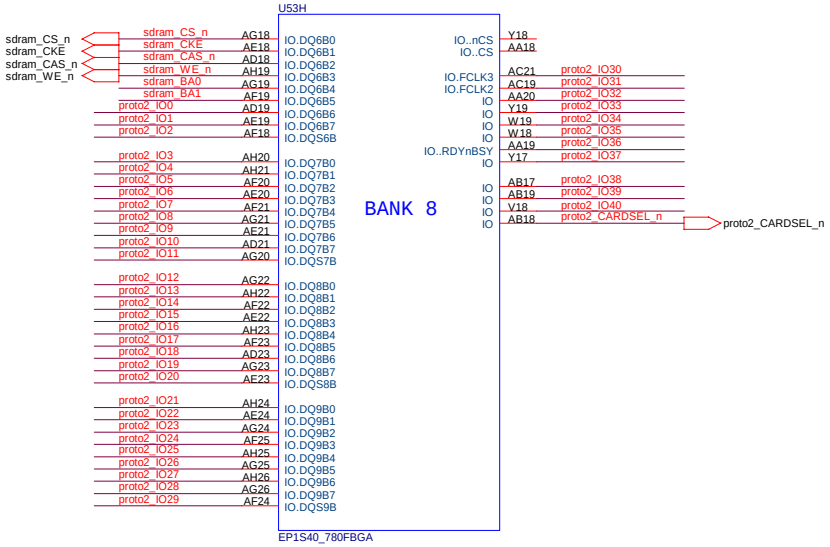
PLD Bank 8



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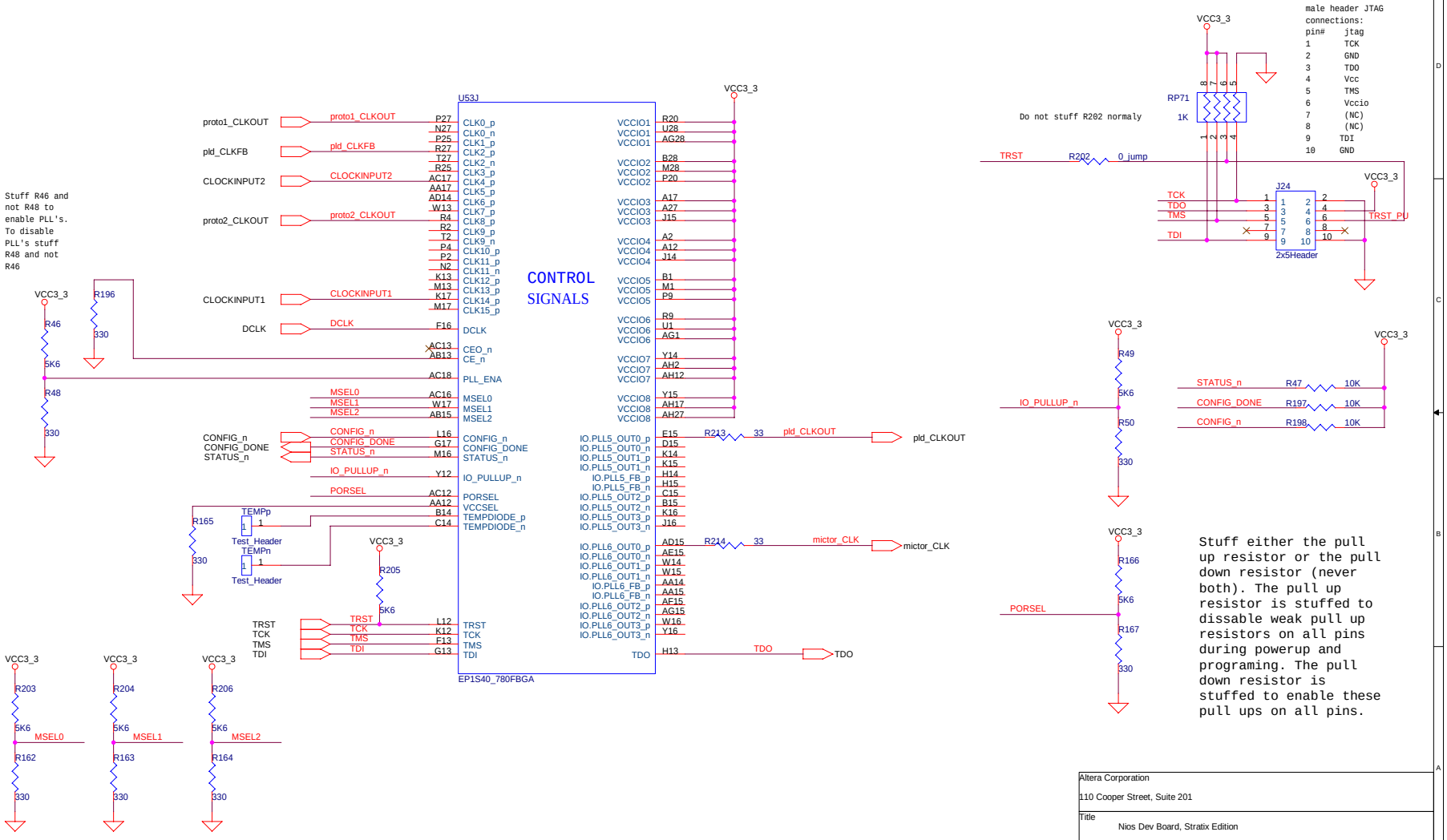
PLD Control Signals



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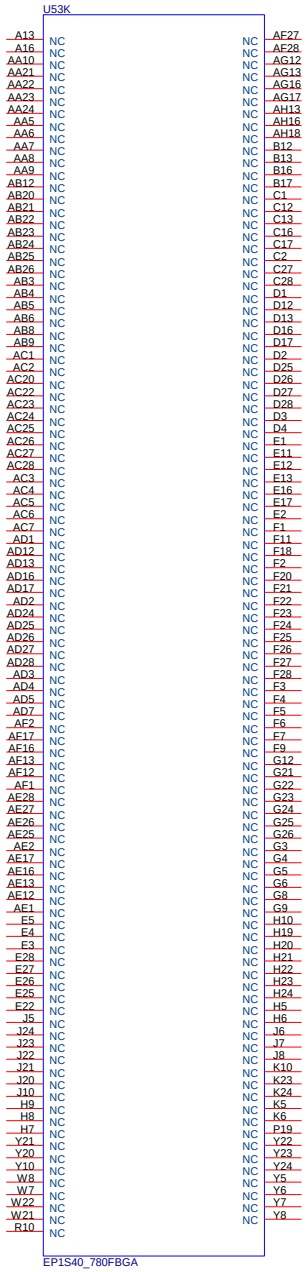
PLD NC



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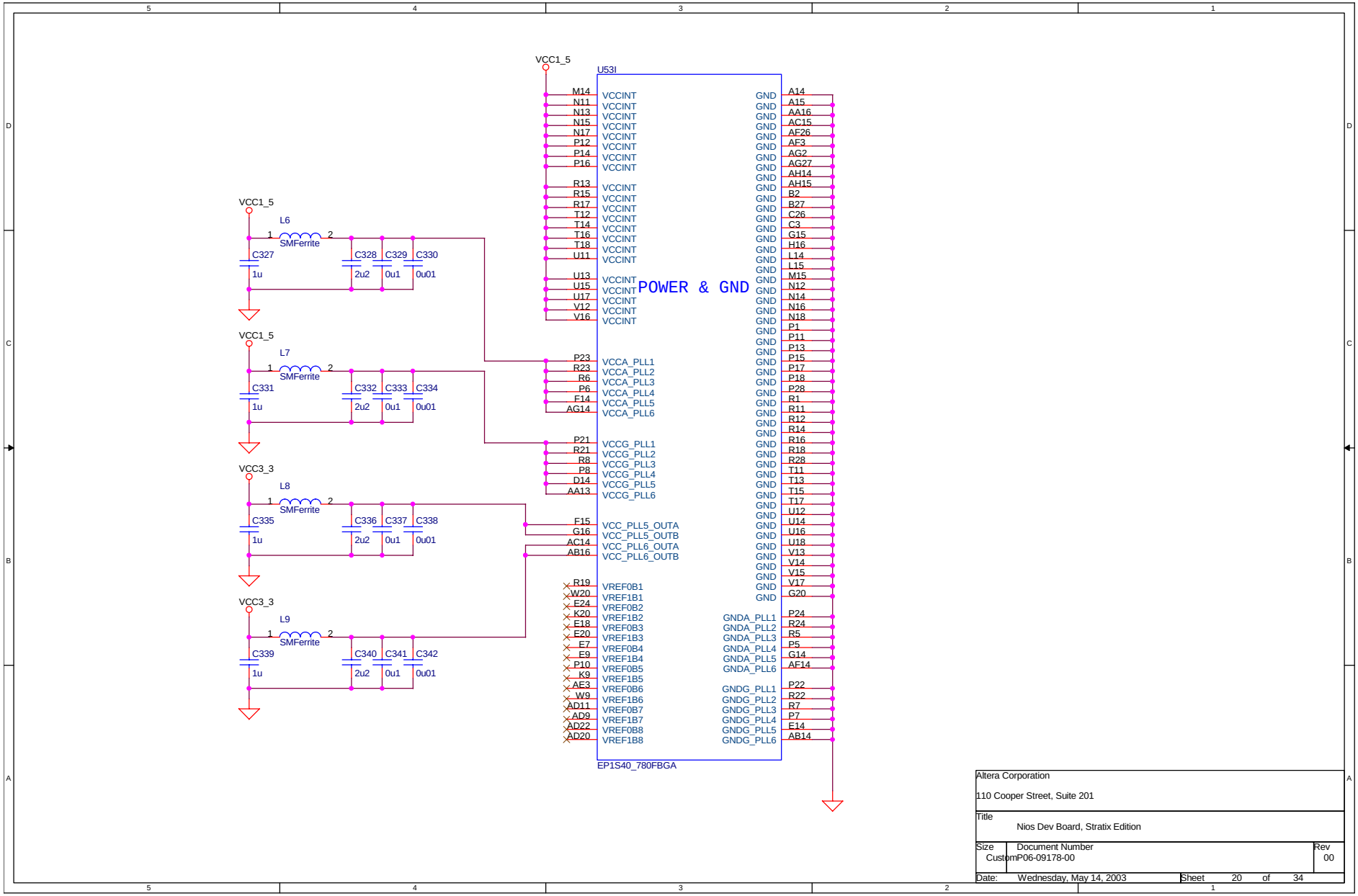

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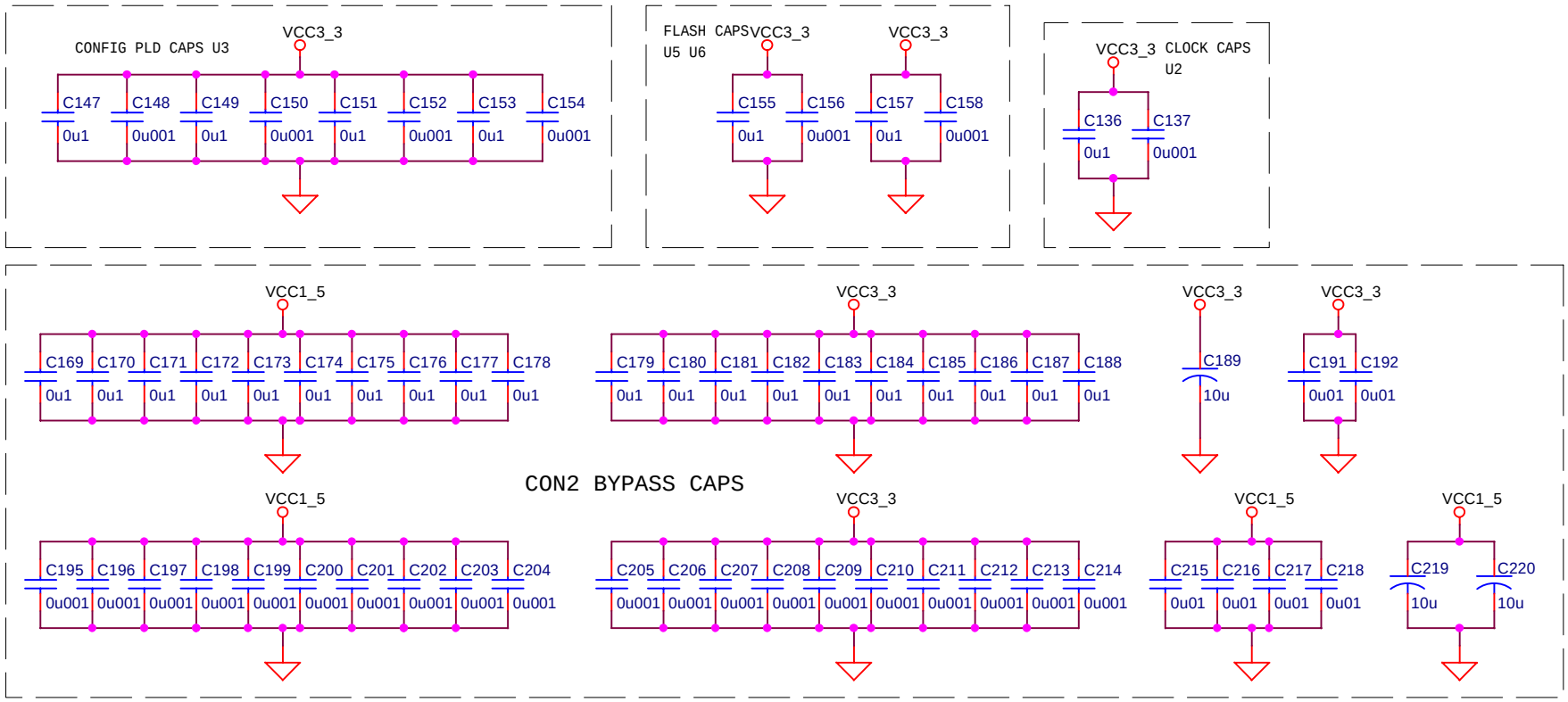
Bypass CAPS



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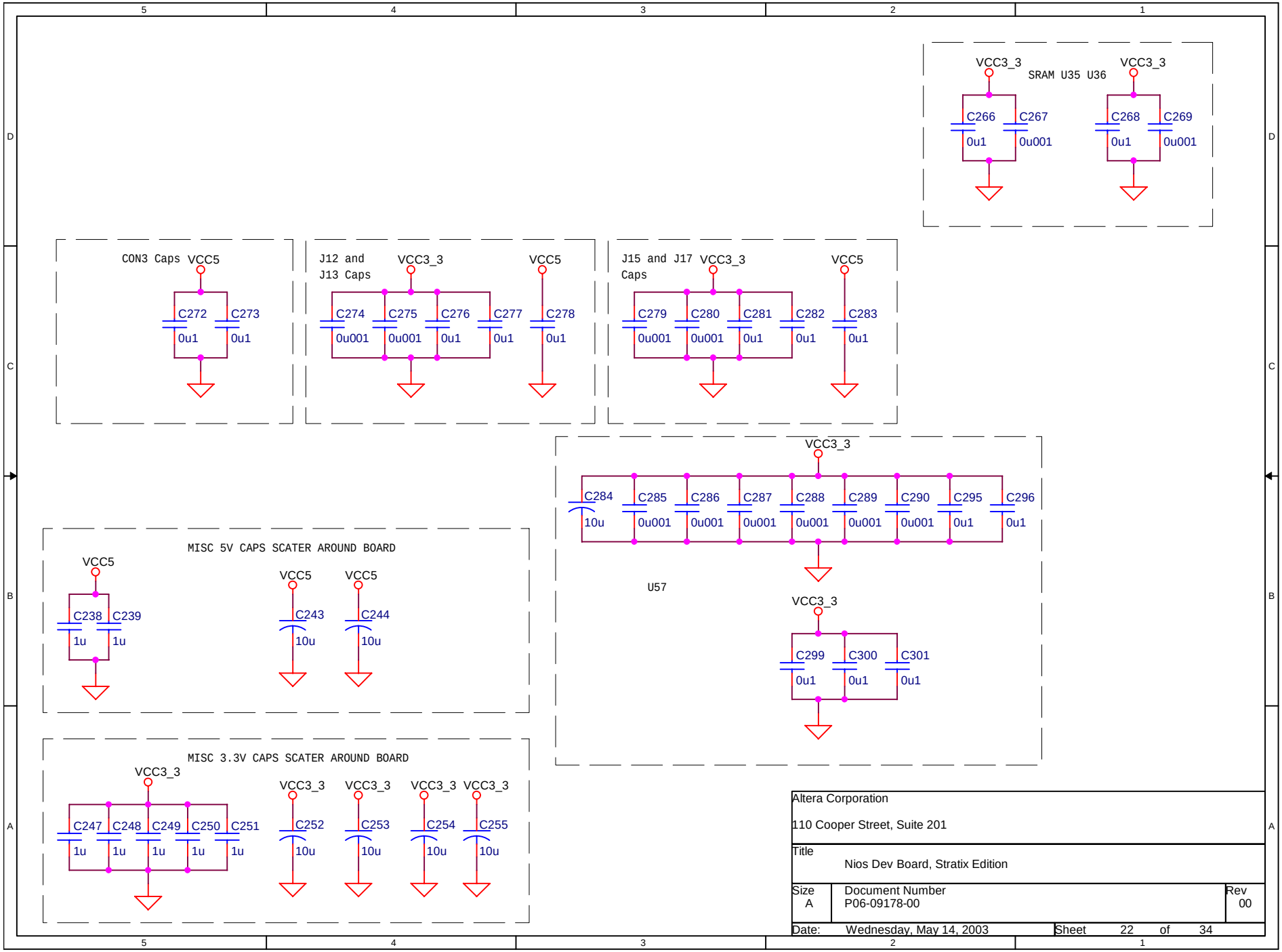
SRAM U35 U36
VCC3_3
C266
C267
0u1
0u001
VCC3_3
C268
C269
0u1
0u001
CON3 Caps
VCC5
C272
C273
0u1
0u1
J12 and
J13 Caps
VCC3_3
C274
C275
C276
C277
0u001
0u001
0u1
0u1
VCC5
C278
0u1
J15 and J17
Caps
VCC3_3
C279
C280
C281
C282
0u001
0u001
0u1
0u1
VCC5
C283
0u1
VCC3_3
C284
C285
C286
C287
C288
C289
C290
C295
C296
10u
0u001
0u001
0u001
0u001
0u001
0u001
0u1
0u1
U57
VCC3_3
C299
C300
C301
0u1
0u1
0u1
MISC 5V CAPS SCATER AROUND BOARD
VCC5
C238
C239
1u
1u
VCC5
C243
10u
VCC5
C244
10u
MISC 3.3V CAPS SCATER AROUND BOARD
VCC3_3
C247
C248
C249
C250
C251
1u
1u
1u
1u
1u
VCC3_3
C252
10u
VCC3_3
C253
10u
VCC3_3
C254
10u
VCC3_3
C255
10u
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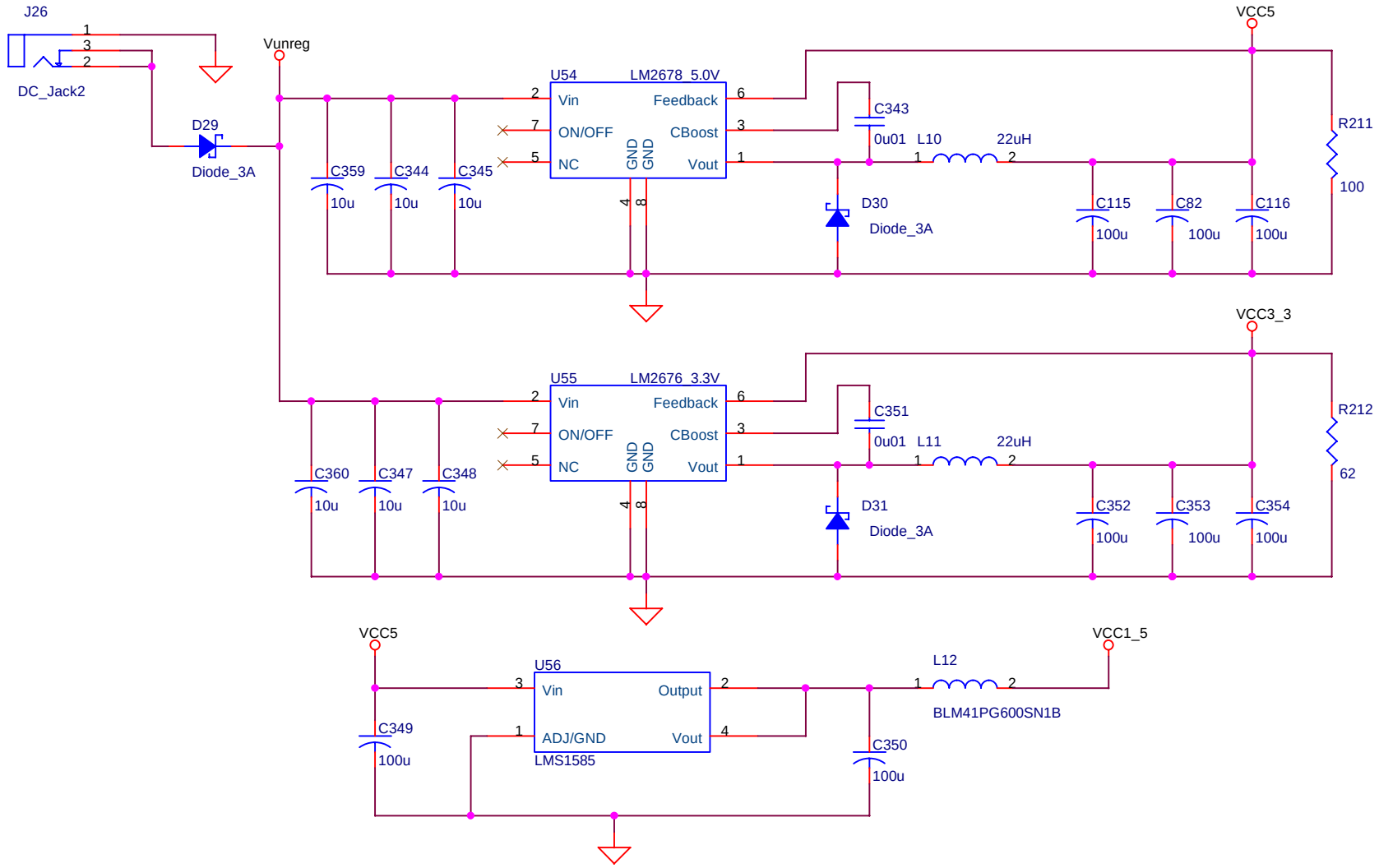
Power Connector



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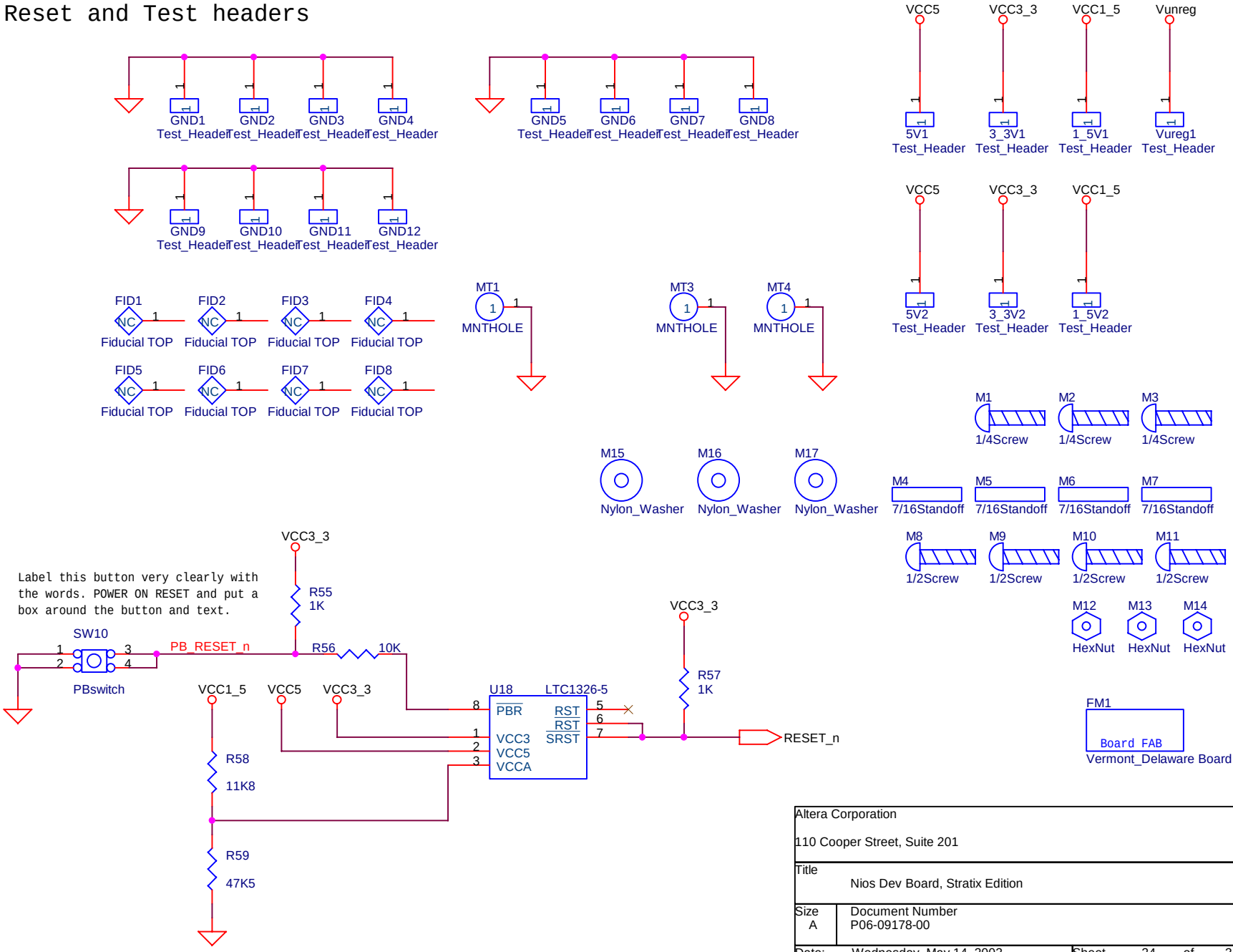
Reset and Test headers



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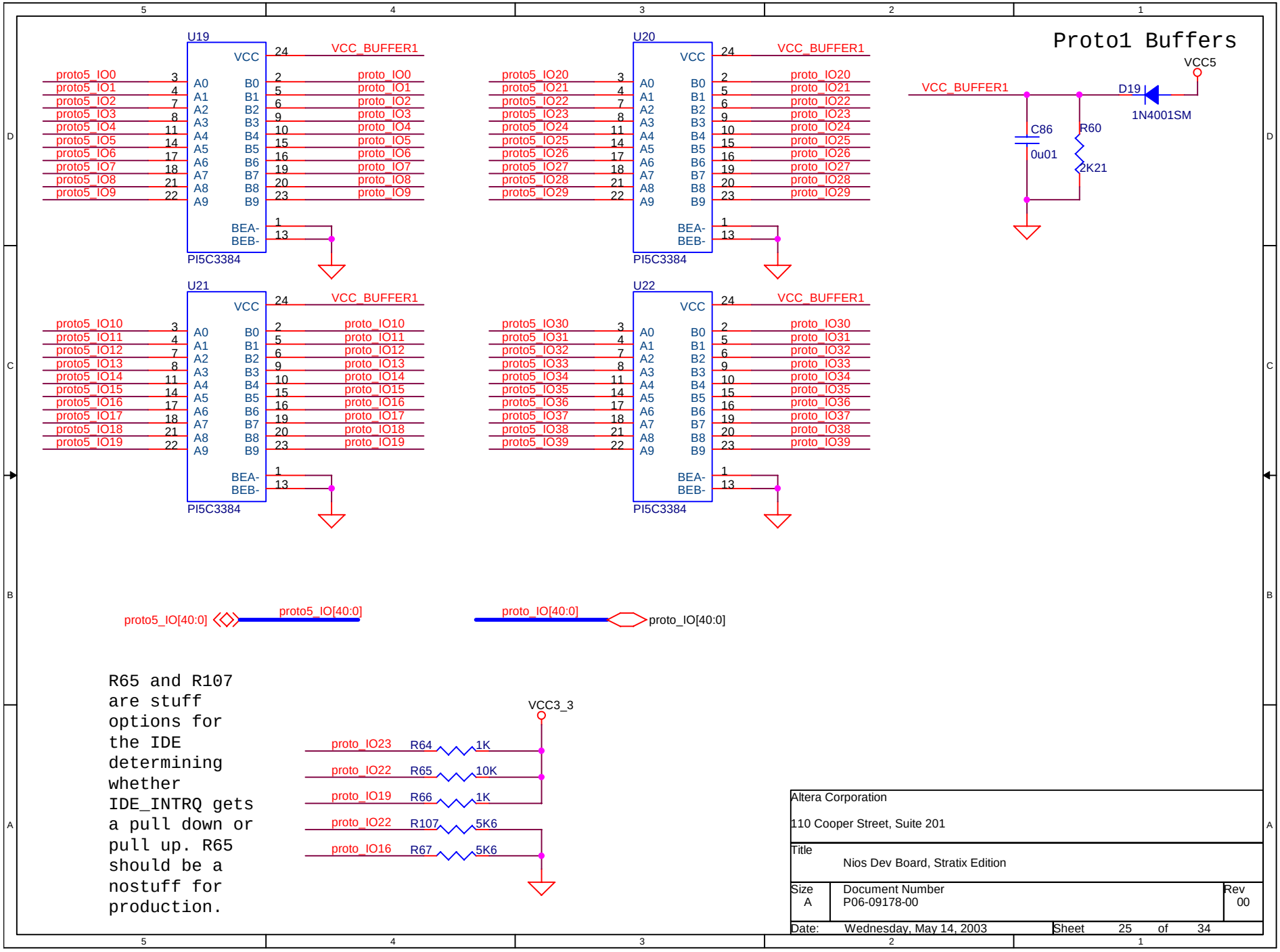
Proto1 Buffers
U19
U20
U21
U22
PI5C3384
VCC
VCC_BUFFER1
BEA-
BEB-
proto5_IO[40:0]
proto_IO[40:0]
VCC5
D19
1N4001SM
C86
0u01
R60
2K21
VCC3_3
proto_IO23 R64 1K
proto_IO22 R65 10K
proto_IO19 R66 1K
proto_IO22 R107 5K6
proto_IO16 R67 5K6
R65 and R107 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R65 should be a nostuff for production.
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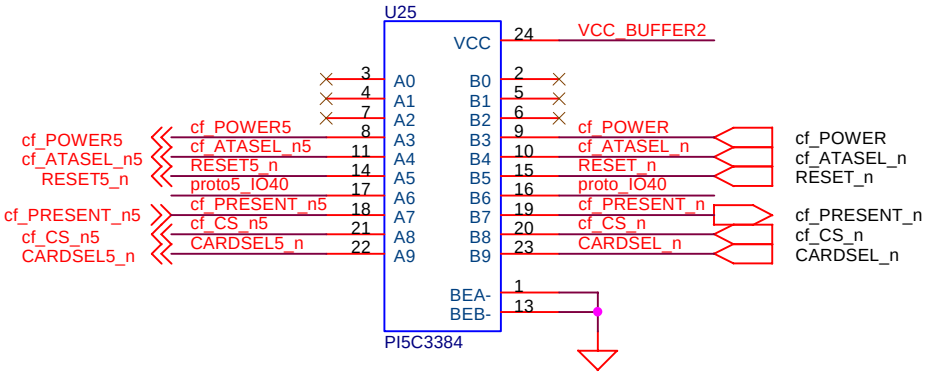
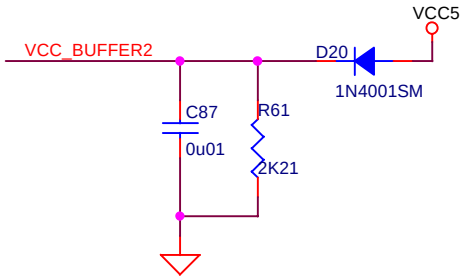
Proto1 Buffers





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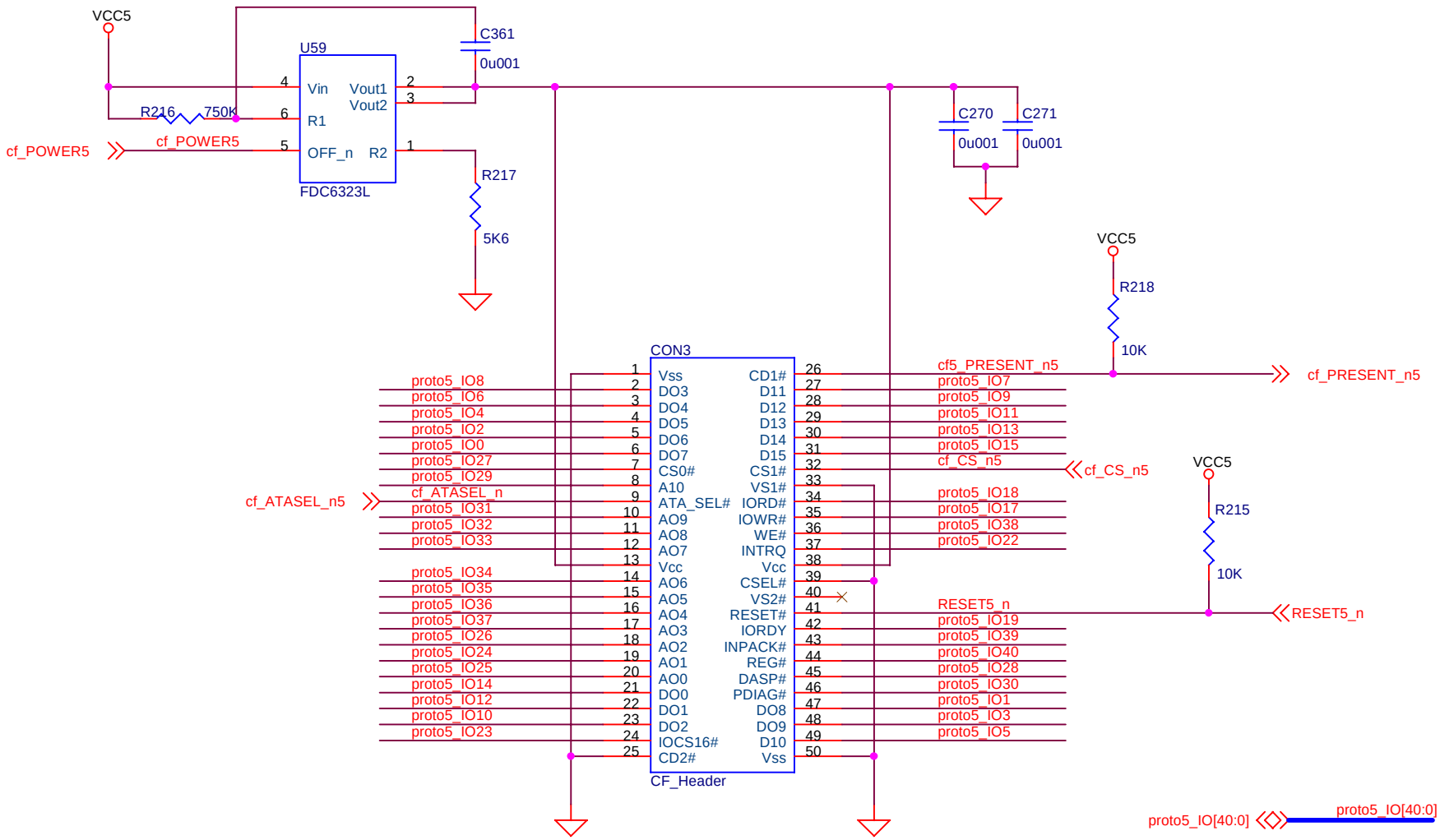
Compaq Flash Socket



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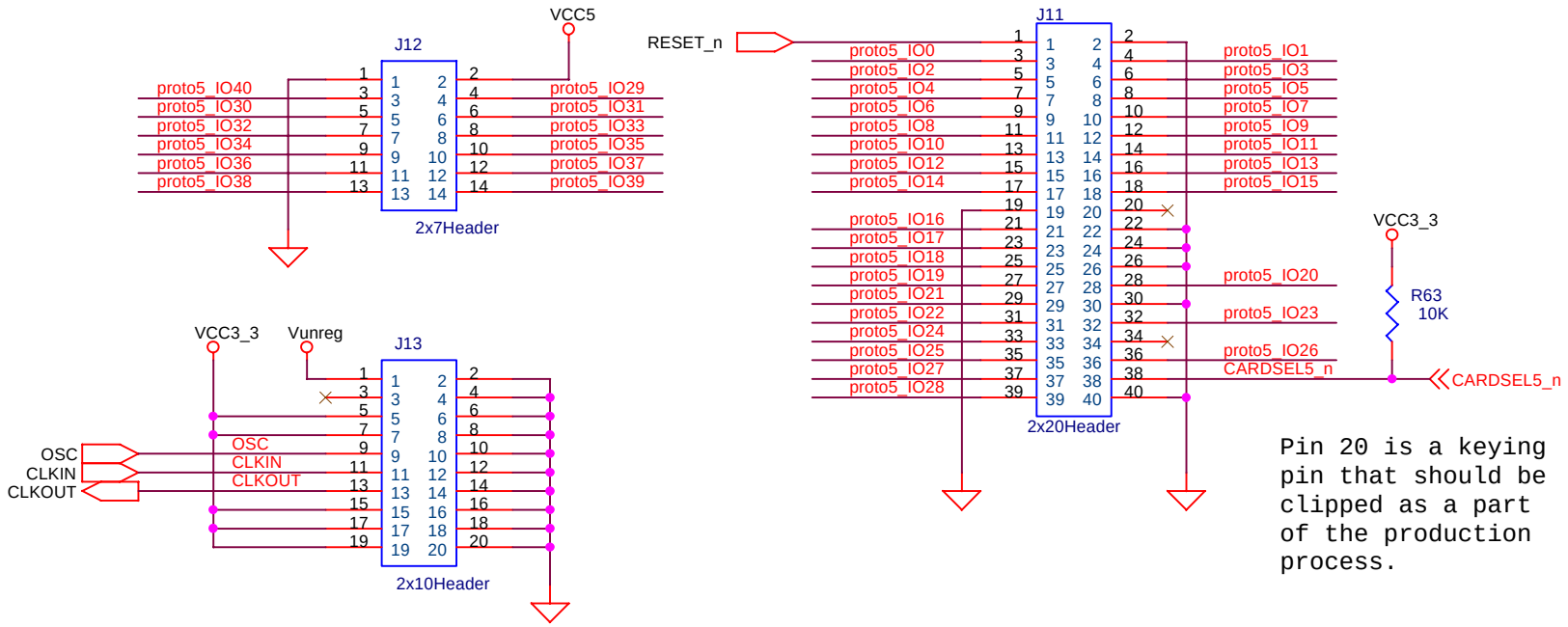
Protocard 1



Pin 20 is a keying pin that should be clipped as a part of the production process.

proto5_IO[40:0] proto5_IO[40:0]

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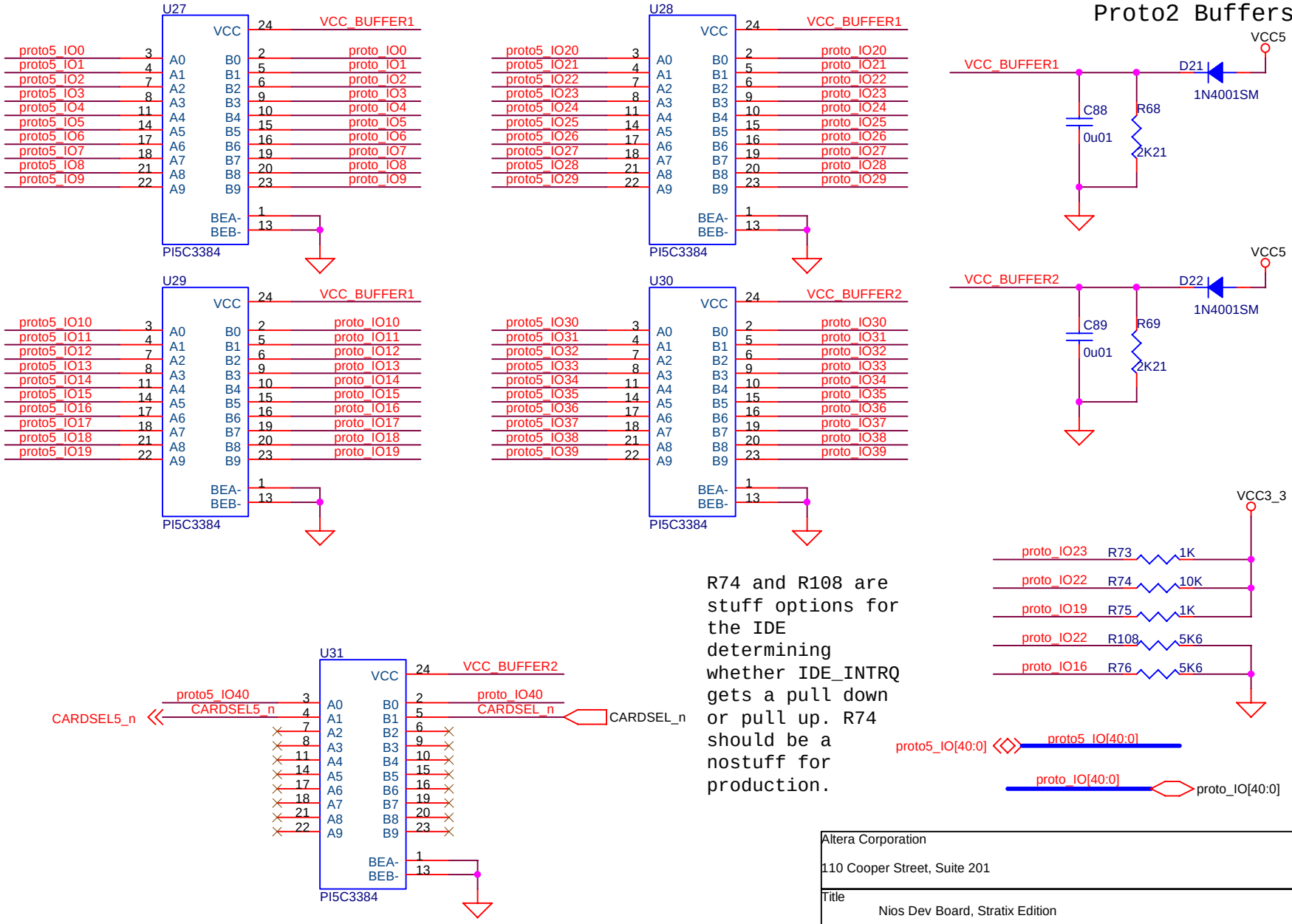
Proto2 Buffers



R74 and R108 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or pull up. R74 should be a nostuff for production.

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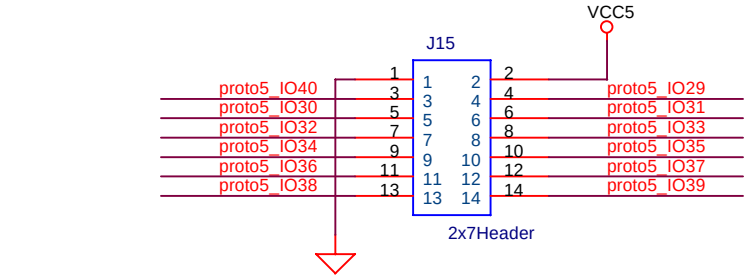
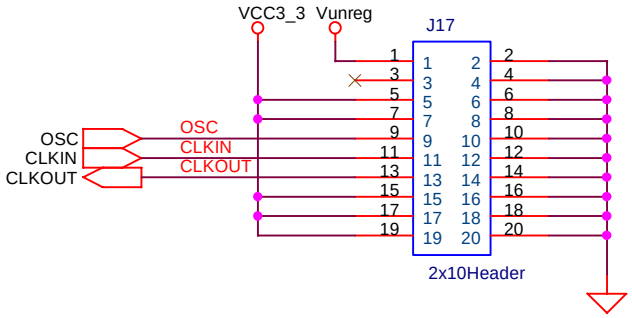
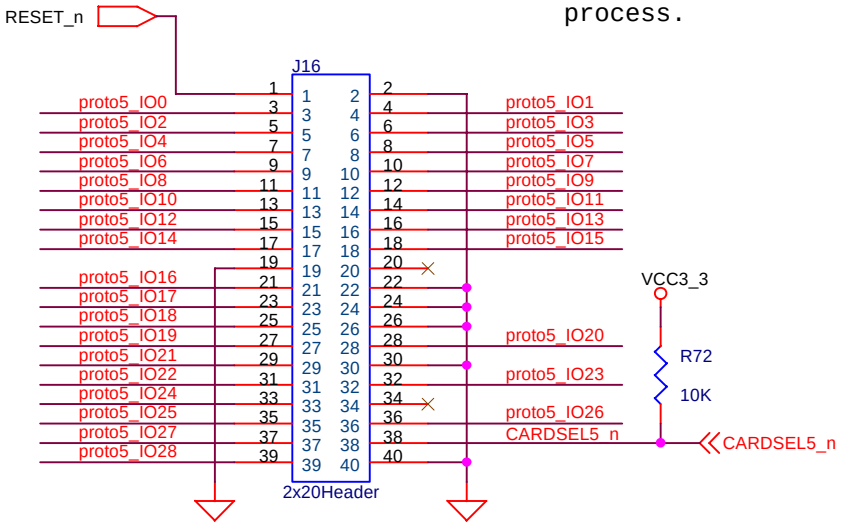
Proto2 Headers

proto5_IO[40:0] proto5_IO[40:0]

Pin 20 is a keying pin that should be clipped as a part of the production process.







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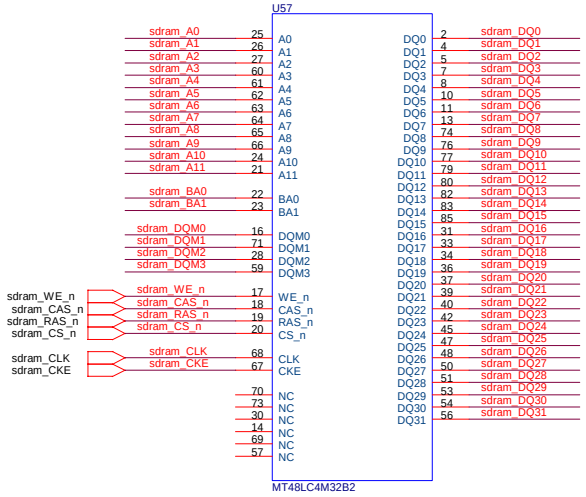
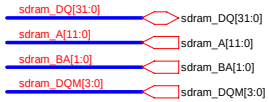
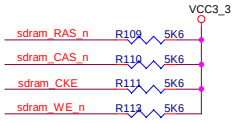
SDRAM







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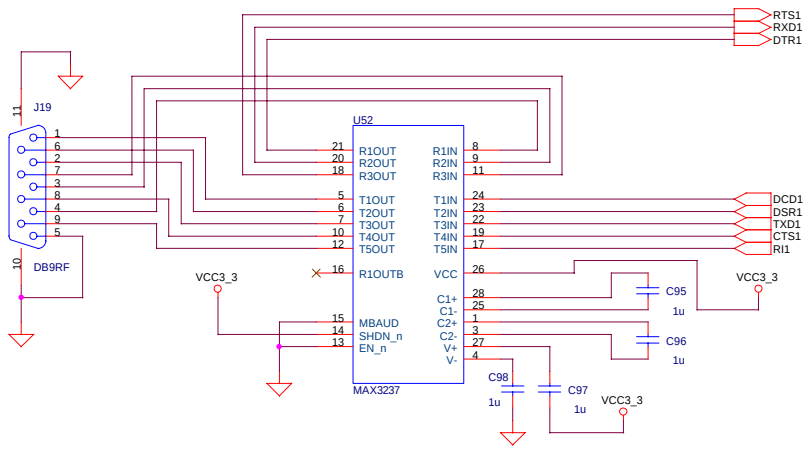
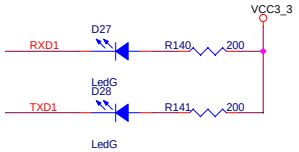
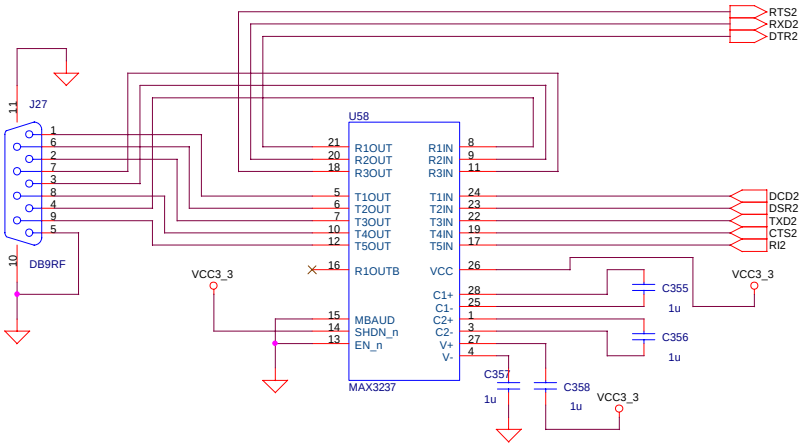
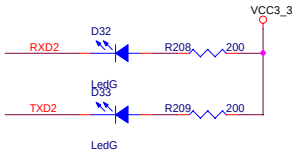
Serial Ports









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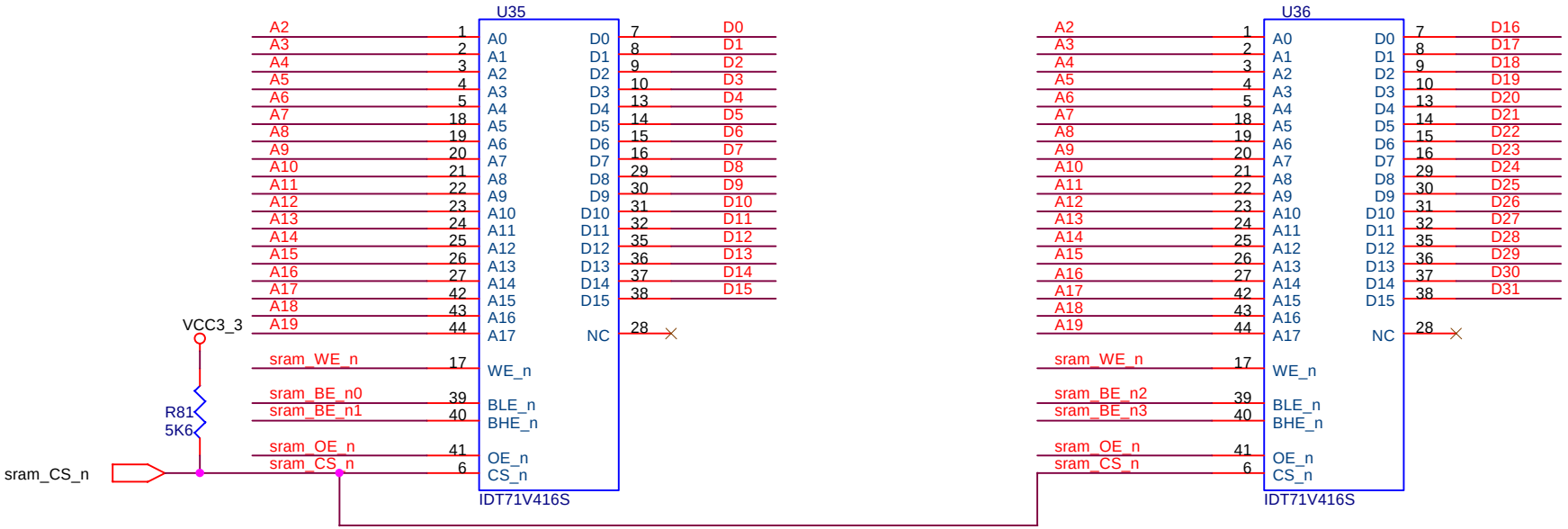
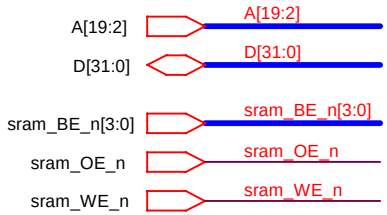
SRAM





One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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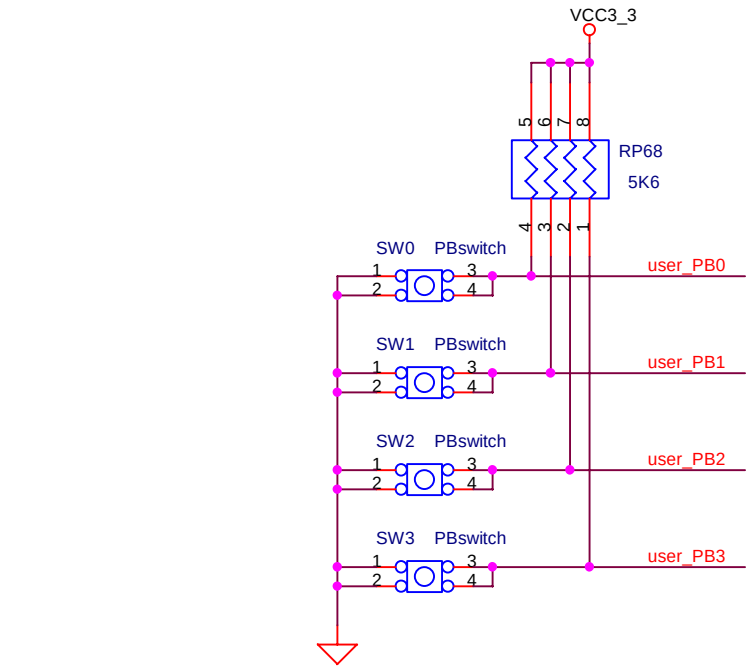
Switches Buttons



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