

Nios Development Board Cyclone II Edition

Rev 01

Revision History

Date	Change Description	Rev
10/19/04	Started design	00
3/24/05	Started Rev01 of design to move the pmc_reset line and the correct the RAS and CAS lines as well as the SSRAM address lines.	00

<Variant Name>

Altera Corp.

110 Cooper Street, Suite 201, Santa Cruz, CA 95060

Title

Nios II Cyclone II Board (Texas)

Size

A

Document Number

P06-XXXXX

Rev

00

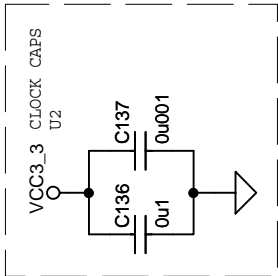
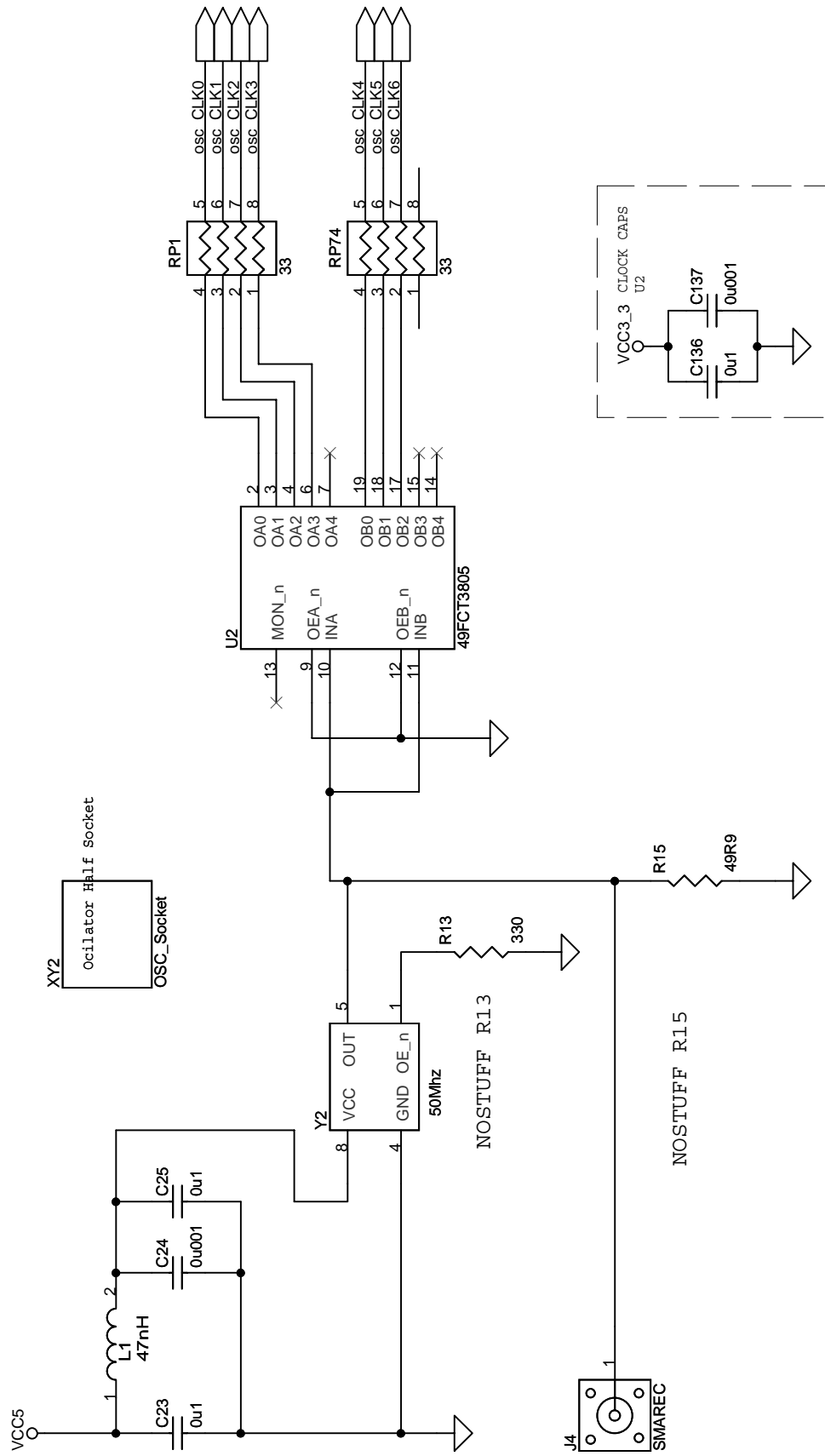
Date:

Thursday, March 24, 2005

Sheet

1 of 32

Clocks



<Variant Name>

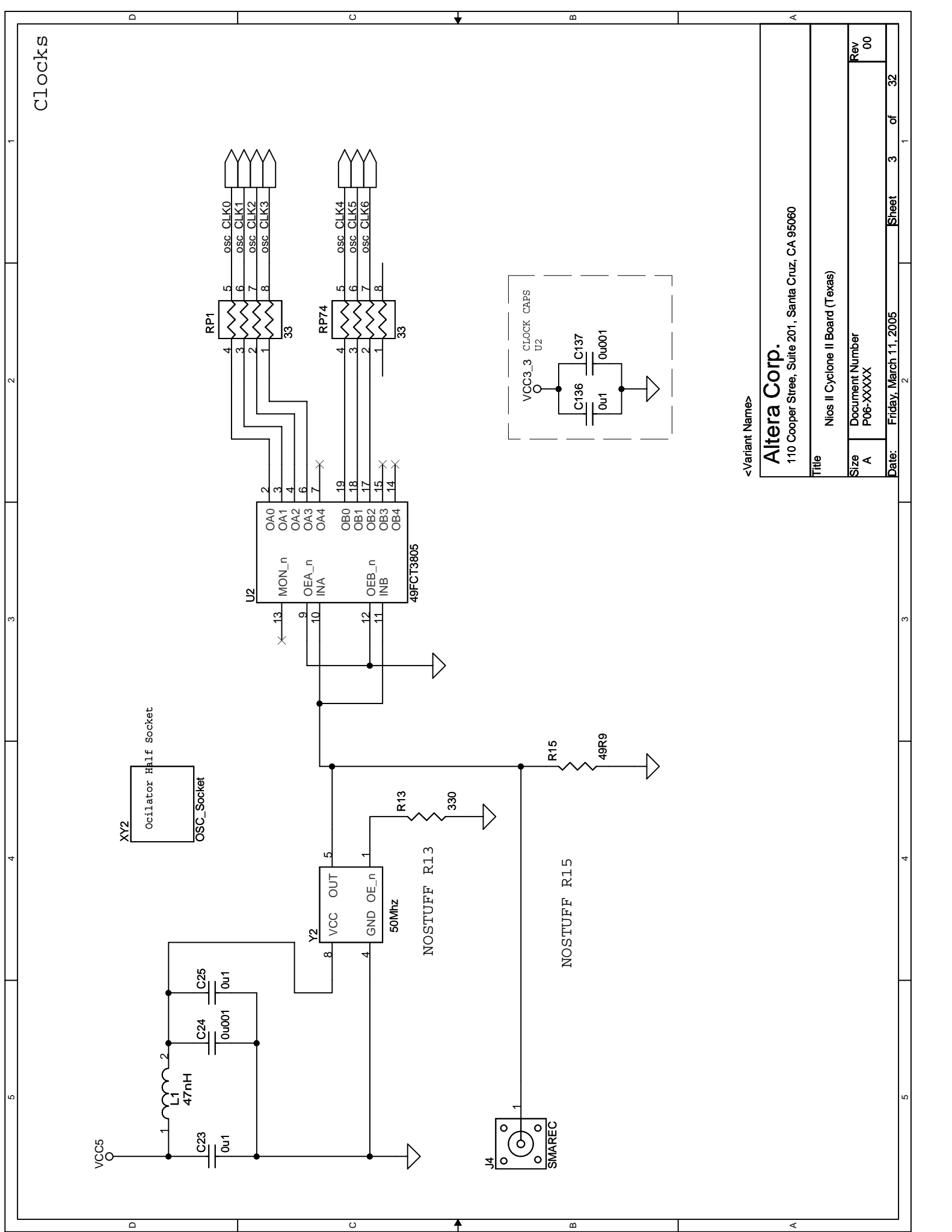
Altera Corp.

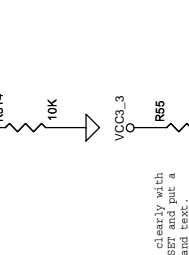
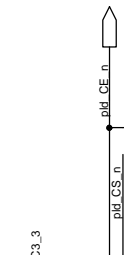
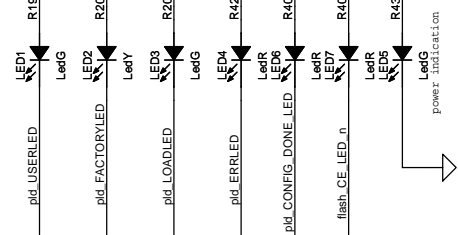
110 Cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Nios II Cyclone II Board (Texas)

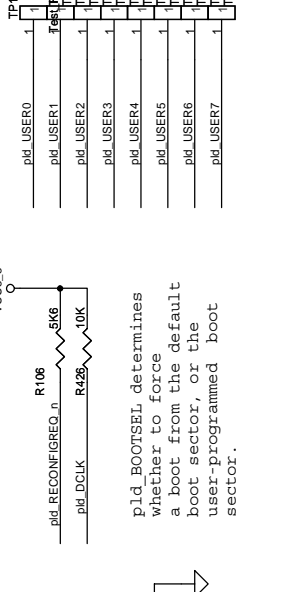
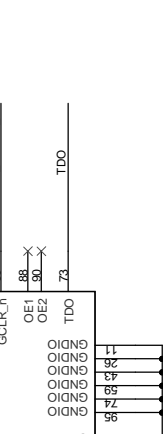
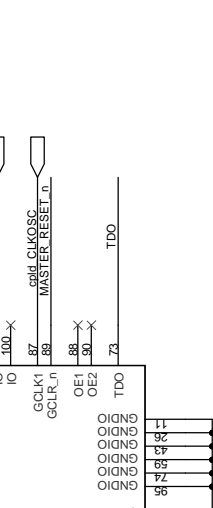
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Document Number: P06-XXXXX

Date: Friday, March 11, 2005 Sheet 3 of 32

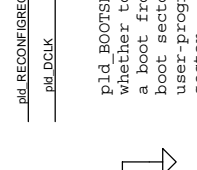




Label this button very clearly with the words, POWER ON RESET and put a box around the button and text.



male header JTAG
 pin#
 1 TCK
 2 GND
 3 TMS
 4 VCC
 5 Verccio
 6 TRST
 7 TDI
 8 GND
 9 TDO
 10 GND



pid_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.

NO CHANGE

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

VCC3_3

enet_BE_n3
enet_BE_n2
enet_BE_n1
enet_BE_n0
enet_AEN

enet_A1
enet_A2
enet_A3
enet_A4
enet_A5
enet_A6
enet_A7
enet_A8
enet_A9
enet_A10
enet_A11
enet_A12
enet_A13
enet_A14
enet_A15

enet_D0
enet_D1
enet_D2
enet_D3
enet_D4
enet_D5
enet_D6
enet_D7
enet_D8
enet_D9
enet_D10
enet_D11
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enet_D24
enet_D25
enet_D26
enet_D27
enet_D28
enet_D29
enet_D30
enet_D31

enet_RESET
enet_ADS_n
enet_CLK
enet_RDY
enet_RDYRTN_n
enet_SRDY_n
enet_INTRO
enet_LDEV_n
enet_IOR_n
enet_DATACS_n
enet_WLR_n
enet_VLBUS_n

enet_IOS0
enet_IOS1
enet_IOS2
enet_ENEP
enet_ENDI
enet_EESK
enet_EECS

enet_IOR_n
enet_IOW_n
enet_RESET
enet_AEN
enet_ADS_n
enet_ENEEP

enet_IOR_n
enet_IOW_n
enet_RESET
enet_AEN
enet_ADS_n
enet_ENEEP

enet_IOR_n
enet_IOW_n
enet_RESET
enet_AEN
enet_ADS_n
enet_ENEEP

enet_IOR_n
enet_IOW_n
enet_RESET
enet_AEN
enet_ADS_n
enet_ENEEP

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enet_IOW_n
enet_RESET
enet_AEN
enet_ADS_n
enet_ENEEP

enet_IOR_n
enet_IOW_n
enet_RESET
enet_AEN
enet_ADS_n
enet_ENEEP

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enet_IOW_n
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enet_AEN
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enet_ENEEP

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enet_AEN
enet_ADS_n
enet_ENEEP

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enet_RESET
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enet_ADS_n
enet_ENEEP

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enet_AEN
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enet_ADS_n
enet_ENEEP

enet_IOR_n
enet_IOW_n
enet_RESET
enet_AEN
enet_ADS_n
enet_ENEEP

PHY

MI INTERFACE

SERIAL

EEPROM

LAN91C111

INTERFACE PINS

LAN91C111

ETHERNET

PULL-UP / PULL-DOWNS

Variant Names

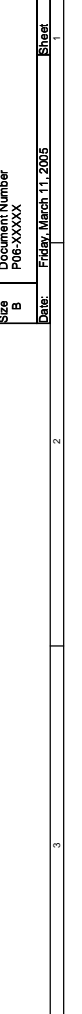
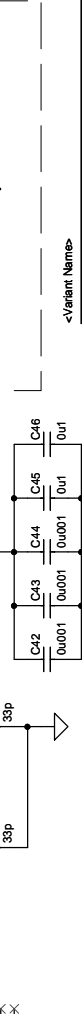
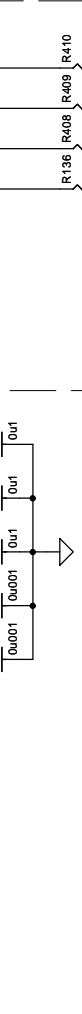
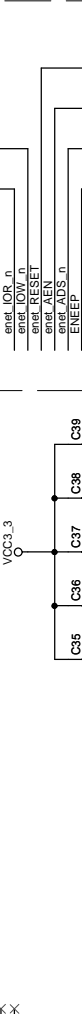
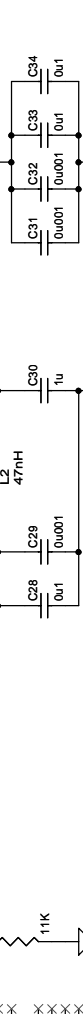
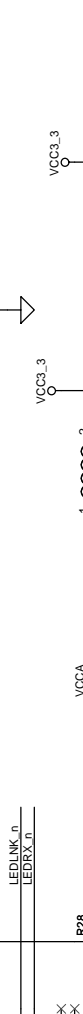
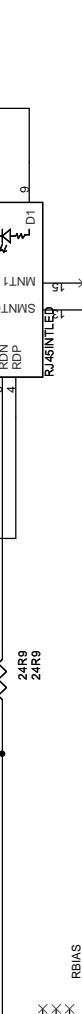
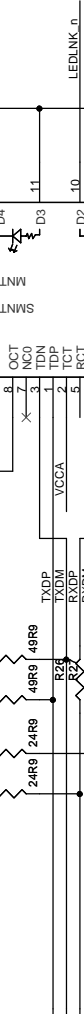
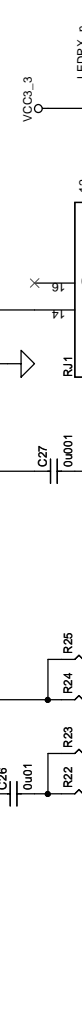
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Title Nios II Cyclone II Board (Teosae)

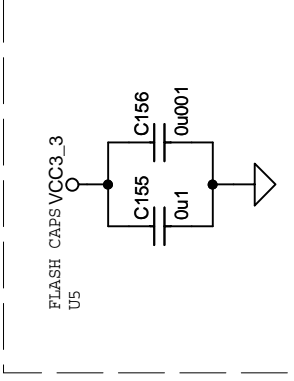
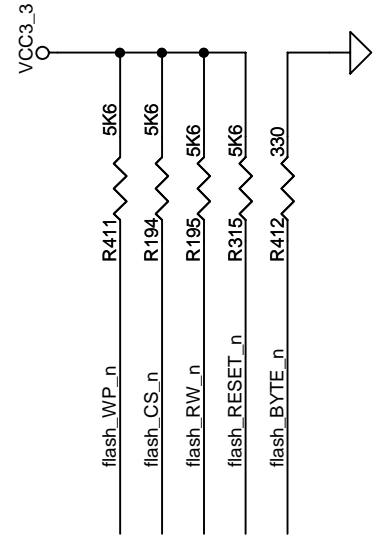
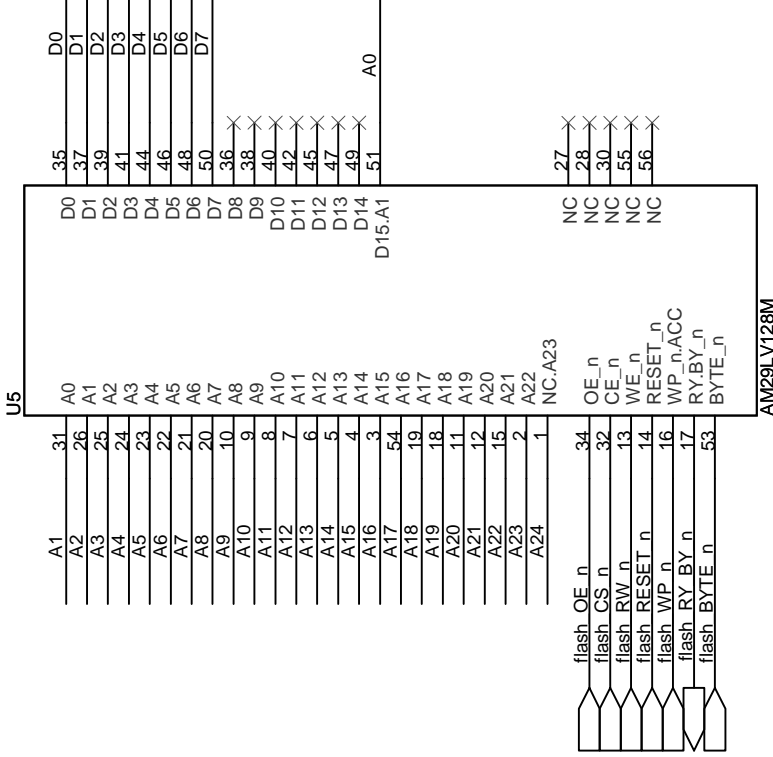
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Date: Friday, March 11, 2005 Sheet 5 of 32



Flash

Flash chip is 16M x 8 for 16Mbytes of flash



<Variant Name>

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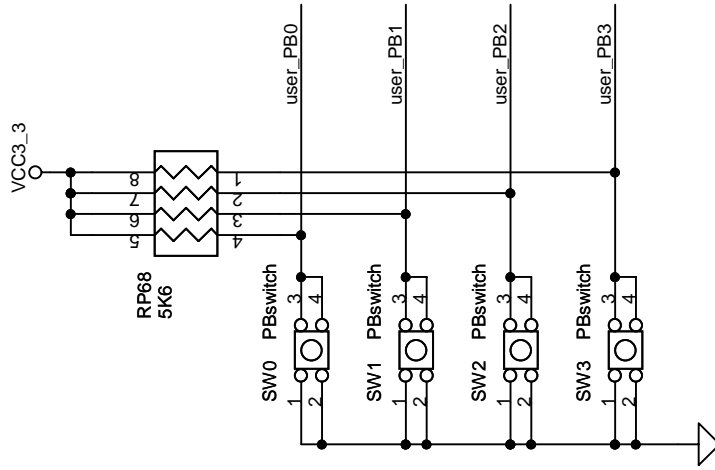
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Nios II Cyclone II Board (Texas)

Title			
Size	A	Document Number	P06-XXXXX
Rev			00

NO CHANGE

Buttons



user_PB[3:0]

<Variant Name>

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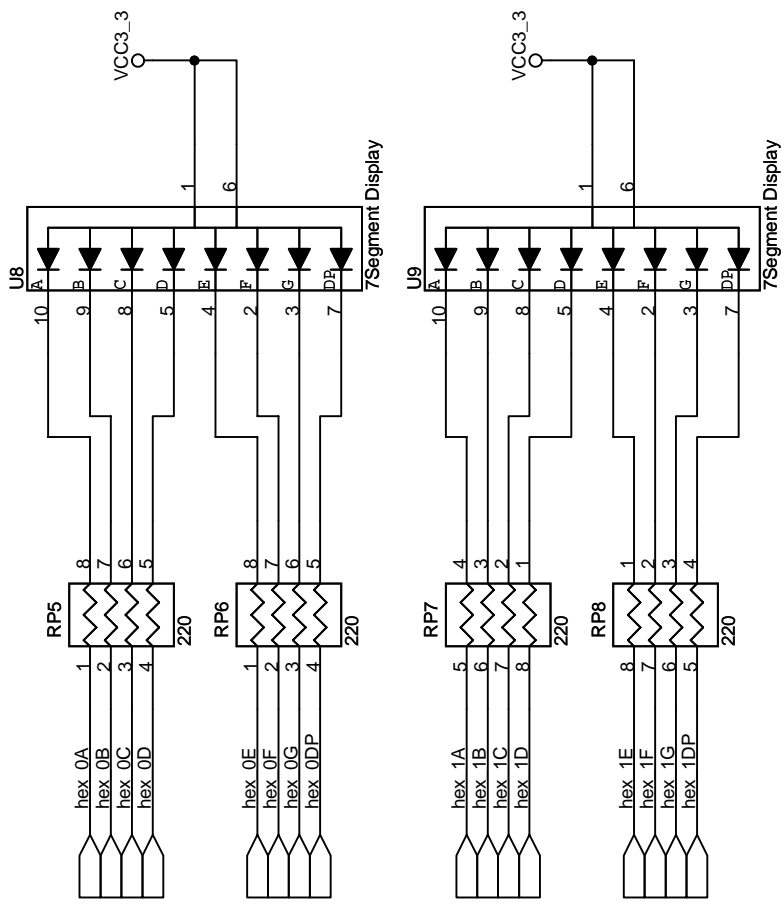
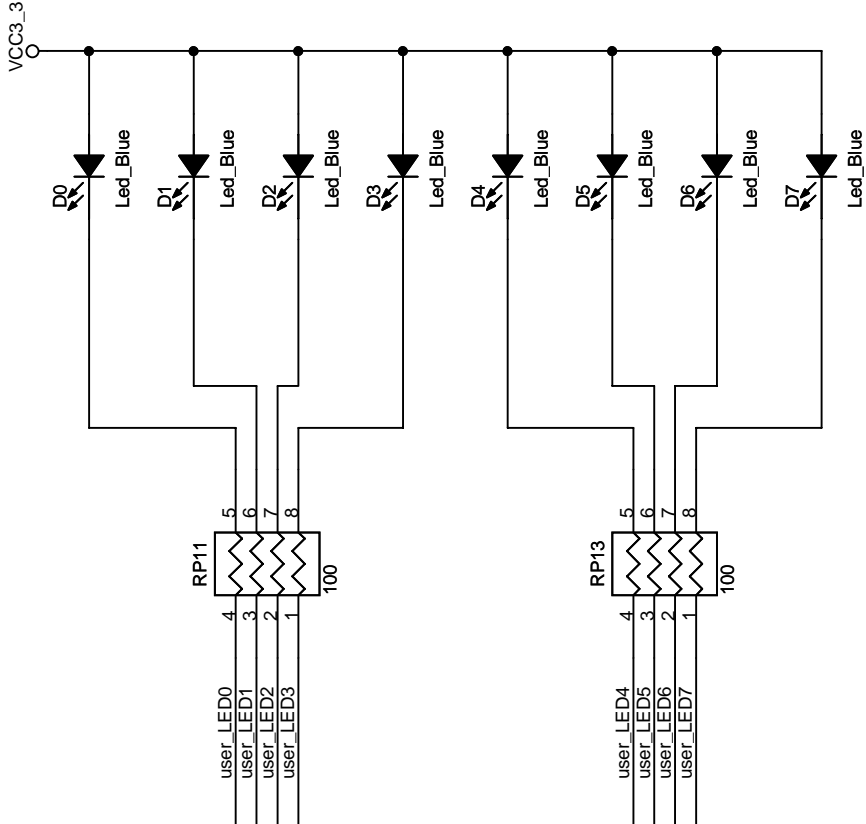
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Size: A
Document Number: P06-XXXXX

Rev: 00

Date: Thursday, December 23, 2004 Sheet 7 of 32

Leds and Hex Display



<Variant Name>

Altera Corp.

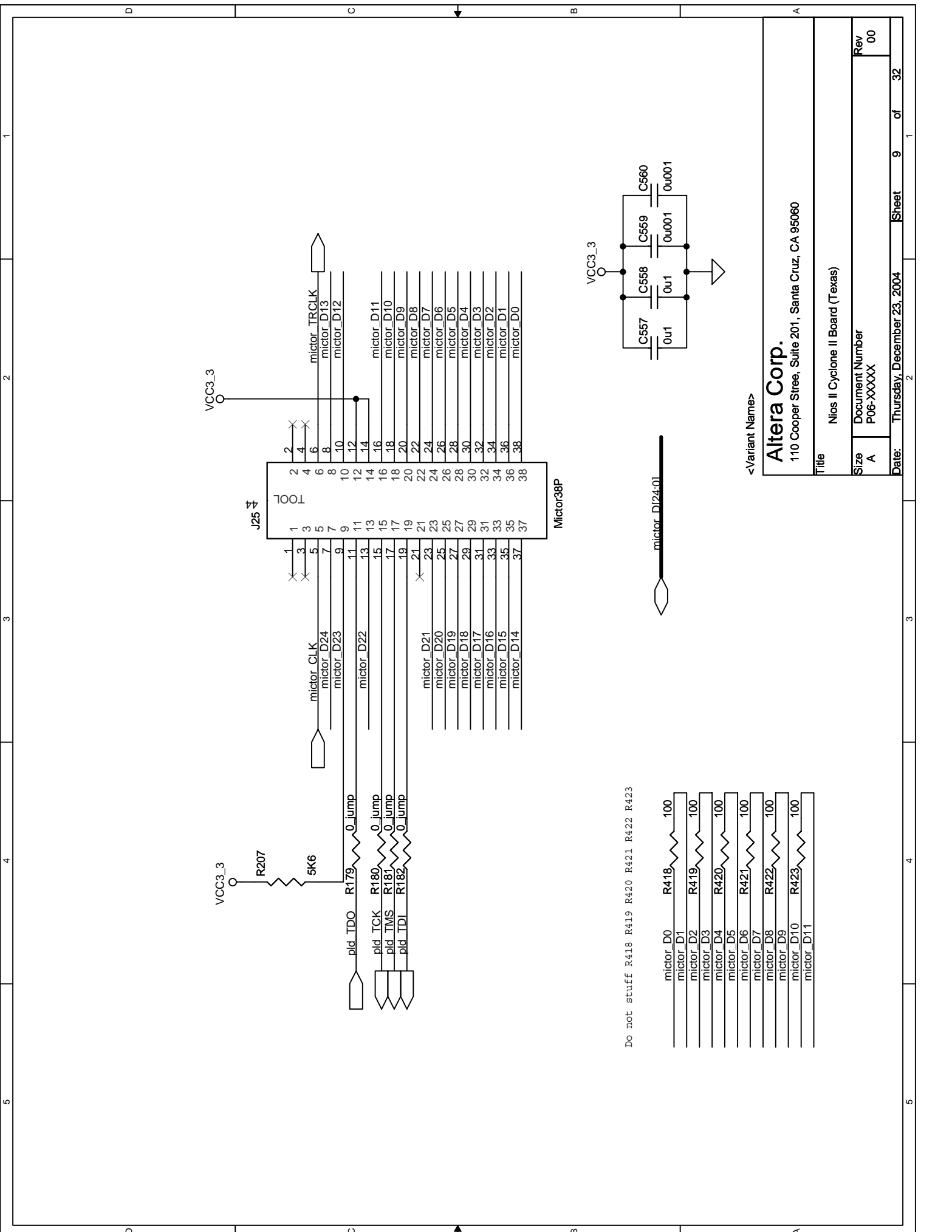
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Title: Nios II Cyclone II Board (Texas)

Size: Document Number
A: P06-XXXXX

Rev: 00

Date: Thursday, December 23, 2004 Sheet 8 of 32



Do not stuff R418 R419 R420 R421 R422 R423

micror_D0	R418	100
micror_D1		
micror_D2	R419	100
micror_D3		
micror_D4	R420	100
micror_D5		
micror_D6	R421	100
micror_D7		
micror_D8	R422	100
micror_D9		
micror_D10	R423	100
micror_D11		

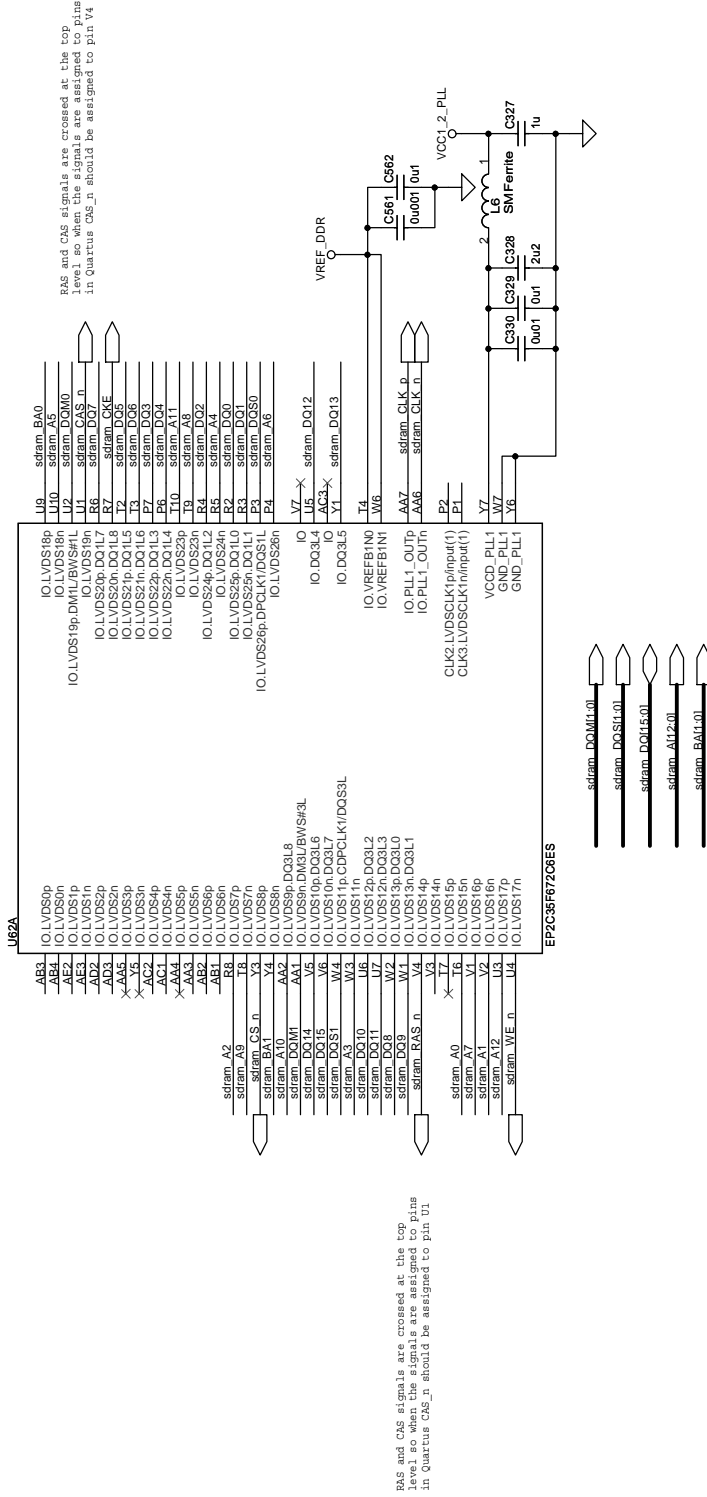
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Altera Corp.

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Title	
Nios II Cyclone II Board (Texas)	
Size	Document Number
A	P06-XXXXX
Date:	Thursday, December 23, 2004
Sheet	9 of 32
Rev	00

PLD Bank 1



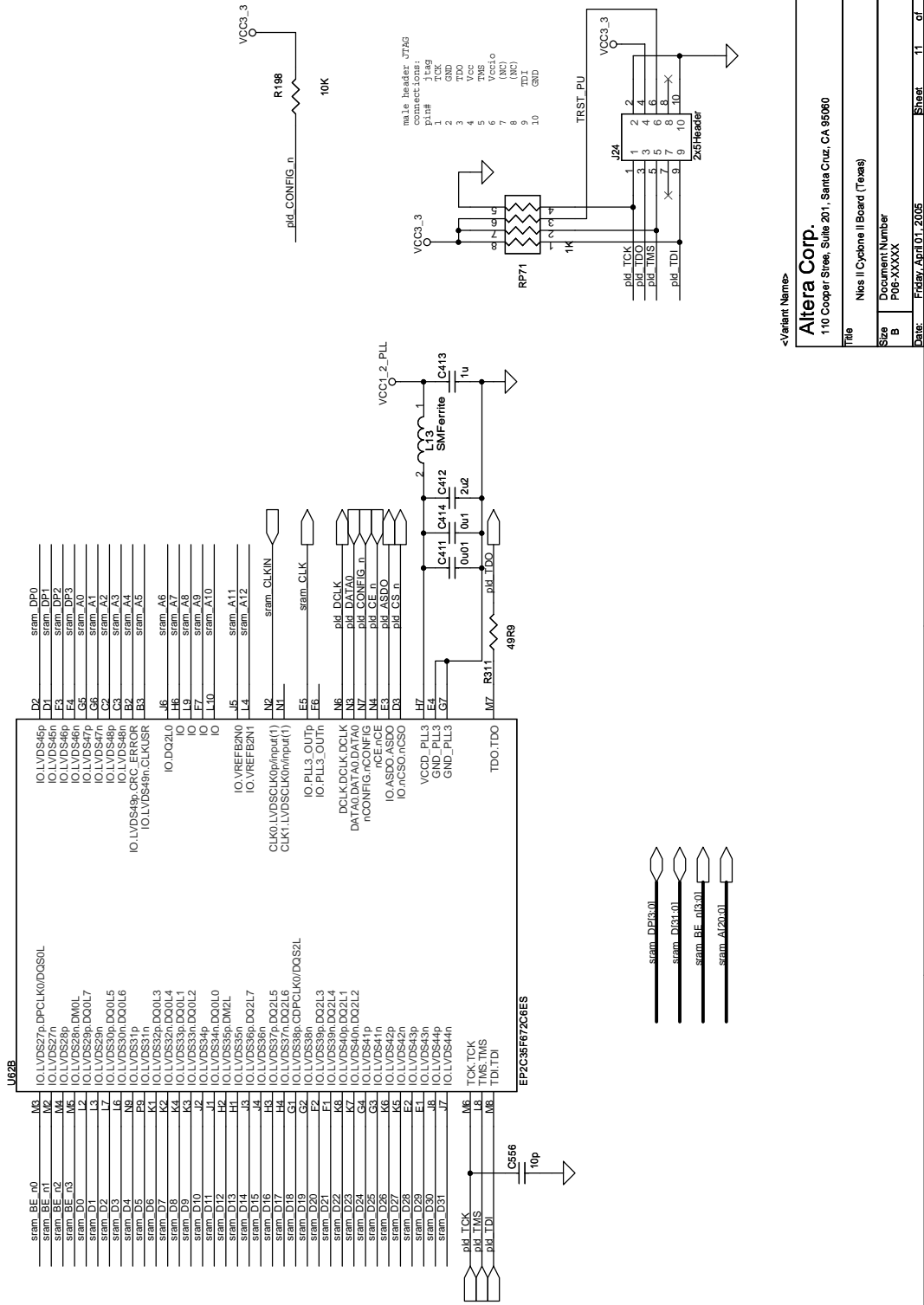
RAS and CAS signals are crossed at the top level so when the signals are assigned to pins in Quartus CAS_n should be assigned to pin V4

<Variant Name>

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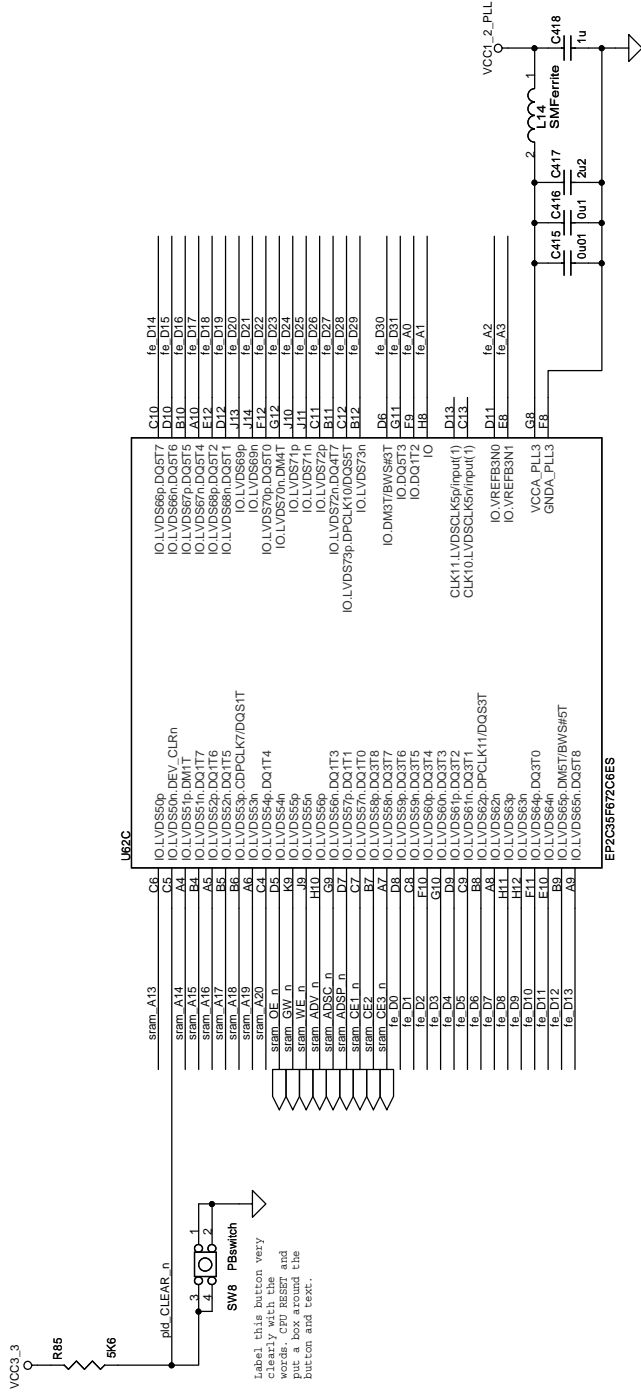
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Size	Document Number
Rev	P06-XXXX
Date	Friday, April 01, 2005
Sheet	10 of 32

PLD Bank 2



<Variant Name>
Altera Corp.
 110 Cooper Street, Suite 201, Santa Cruz, CA 95060
 Title: Nios II Cyclone II Board (Teos) |
 Size: B | Document Number: P06-XXXXX |
 Date: Friday, April 01, 2005 | Sheet: 11 of 32

PLD Bank 3



<Variant Name>

Altera Corp.

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Title: Nios II Cyclone II Board (Teesa)

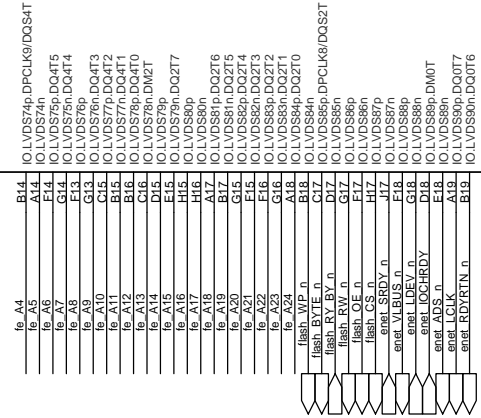
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Rev: P06-XXXXX

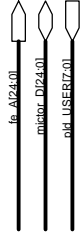
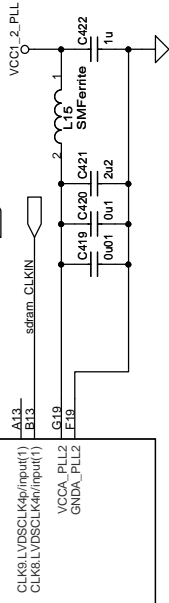
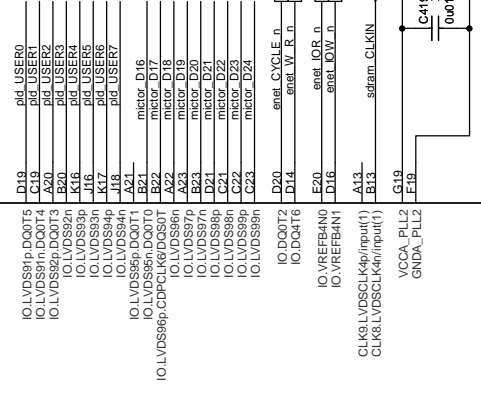
Date: Friday, April 01, 2005

Sheet: 12 of 32

U62D



EP2K3F67Z06ES



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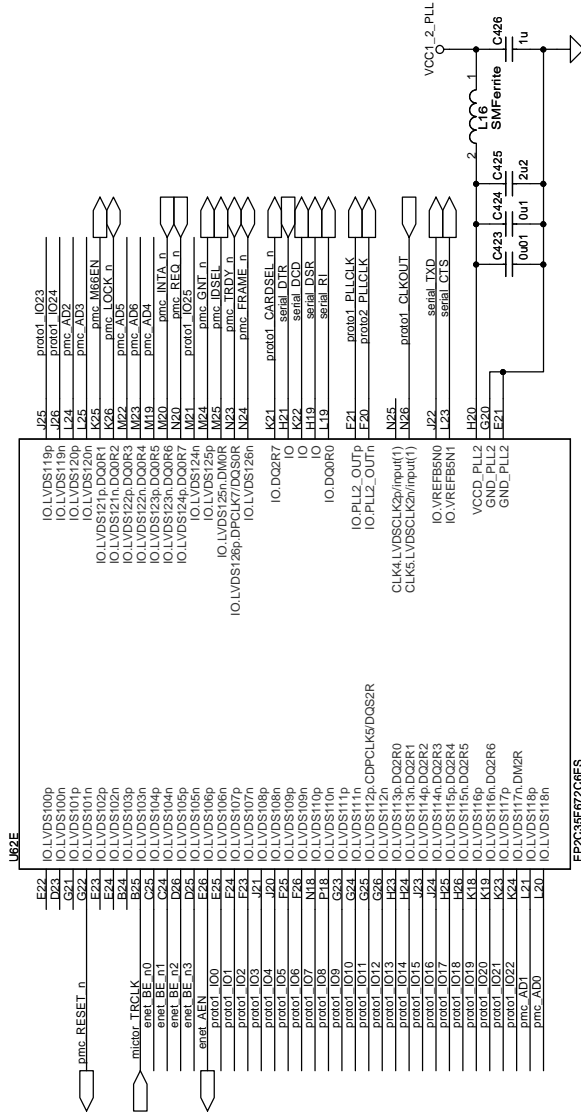
110 Cooper Street, Suite 201, Santa Cruz, CA 95060

Title: Nios II Cyclone II Board (Texas)

Size	Document Number	Rev
B	P06-XXXX	00

Date: Friday, April 01, 2005 Sheet 13 of 32

PLD Bank 5

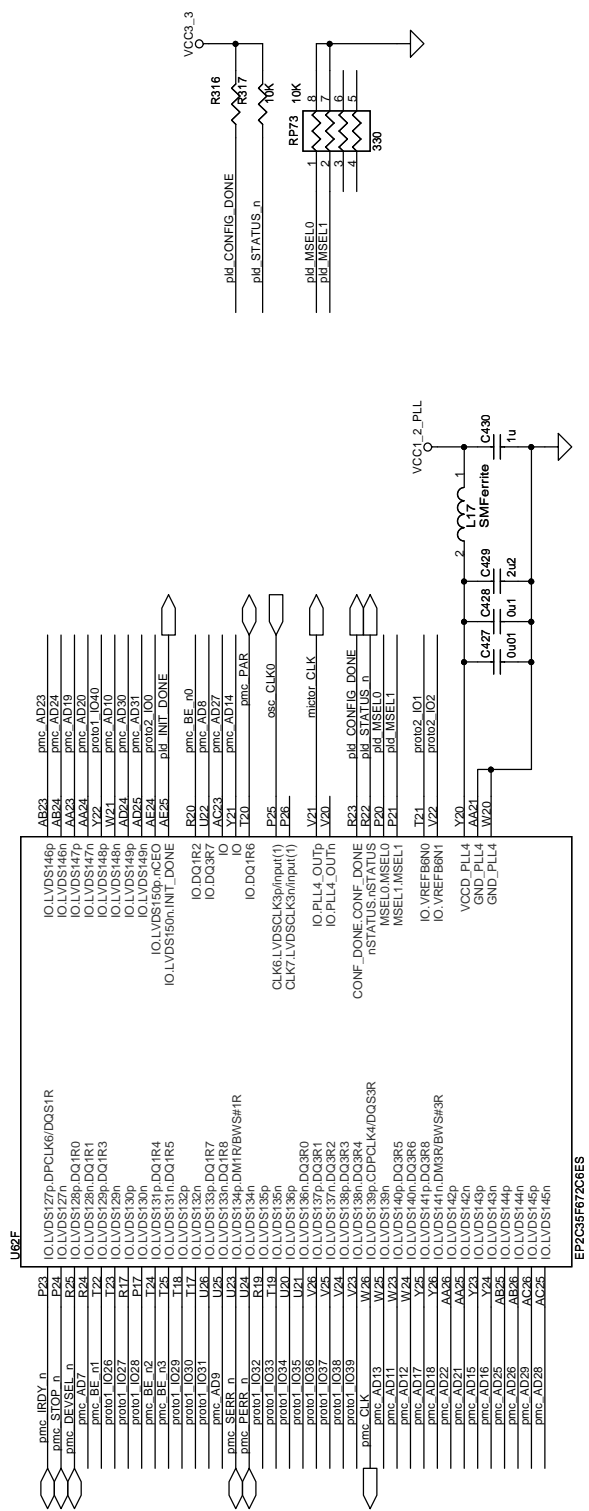


- emul_BE_n[0:0]
- miolcl_D124[0]
- pmc_AD131[0]
- pmi01_IO610[0]

<Variant Name>
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Title	Nios II Cyclone II Board (Teos)		
Size	B	Document Number	P06-XXXX
Rev	00	Sheet	14 of 32

Date: Friday, April 01, 2005



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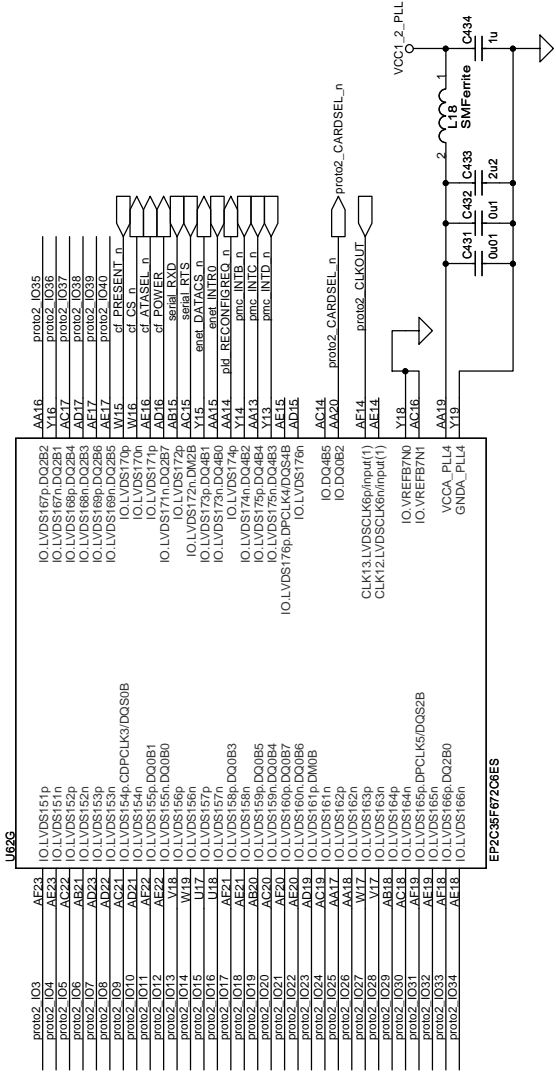
Altera Corp.
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Title: Nios II Cyclone II Board (Tweaks)

Size: Document Number P06-XXXXX

Date: Friday, April 01, 2005 Sheet 15 of 32

Rev 00

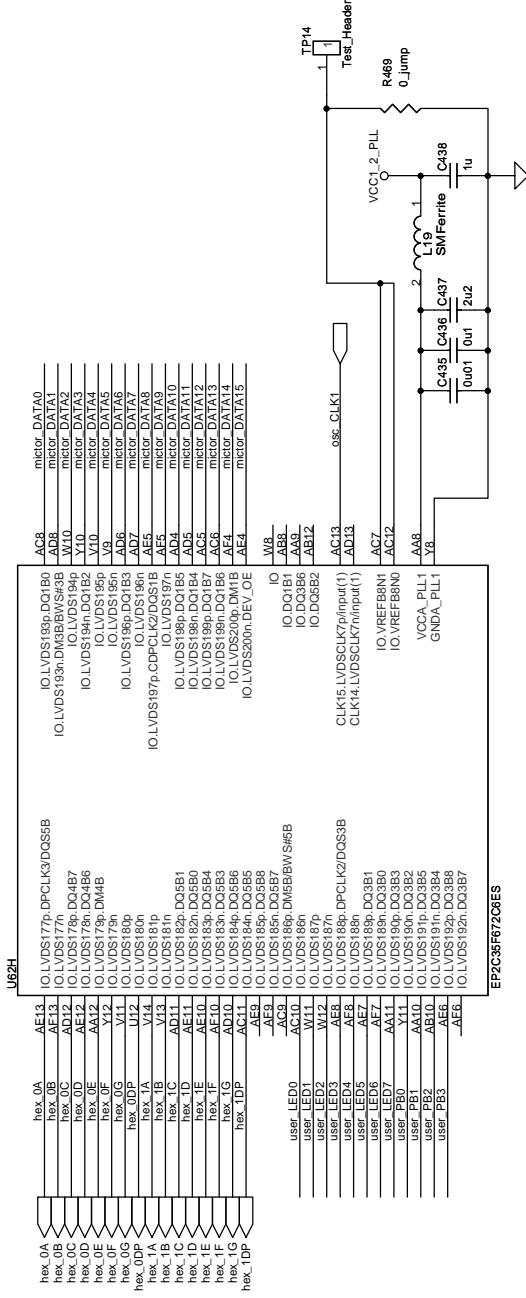


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Title	Nics II Cyclone II Board (Texas)		
Size	Document Number	Rev	00
B	P06-XXXX		
Date:	Friday, April 01, 2005	Sheet	16 of 32

PLD Bank 8

- micror_DATA0 R446 ~ 0_jump micror_D0 R446 ~ 0_jump
- micror_DATA1 R447 ~ 0_jump micror_D1 R447 ~ 0_jump
- micror_DATA2 R448 ~ 0_jump micror_D2 R448 ~ 0_jump
- micror_DATA3 R449 ~ 0_jump micror_D3 R449 ~ 0_jump
- micror_DATA4 R451 ~ 0_jump micror_D4 R451 ~ 0_jump
- micror_DATA5 R453 ~ 0_jump micror_D5 R453 ~ 0_jump
- micror_DATA6 R454 ~ 0_jump micror_D6 R454 ~ 0_jump
- micror_DATA7 R456 ~ 0_jump micror_D7 R456 ~ 0_jump
- micror_DATA8 R457 ~ 0_jump micror_D8 R457 ~ 0_jump
- micror_DATA9 R459 ~ 0_jump micror_D9 R459 ~ 0_jump
- micror_DATA10 R460 ~ 0_jump micror_D10 R460 ~ 0_jump
- micror_DATA11 R462 ~ 0_jump micror_D11 R462 ~ 0_jump
- micror_DATA12 R463 ~ 0_jump micror_D12 R463 ~ 0_jump
- micror_DATA13 R465 ~ 0_jump micror_D13 R465 ~ 0_jump
- micror_DATA14 R466 ~ 0_jump micror_D14 R466 ~ 0_jump
- micror_DATA15 R468 ~ 0_jump micror_D15 R468 ~ 0_jump



<Variant Name>

Altera Corp.

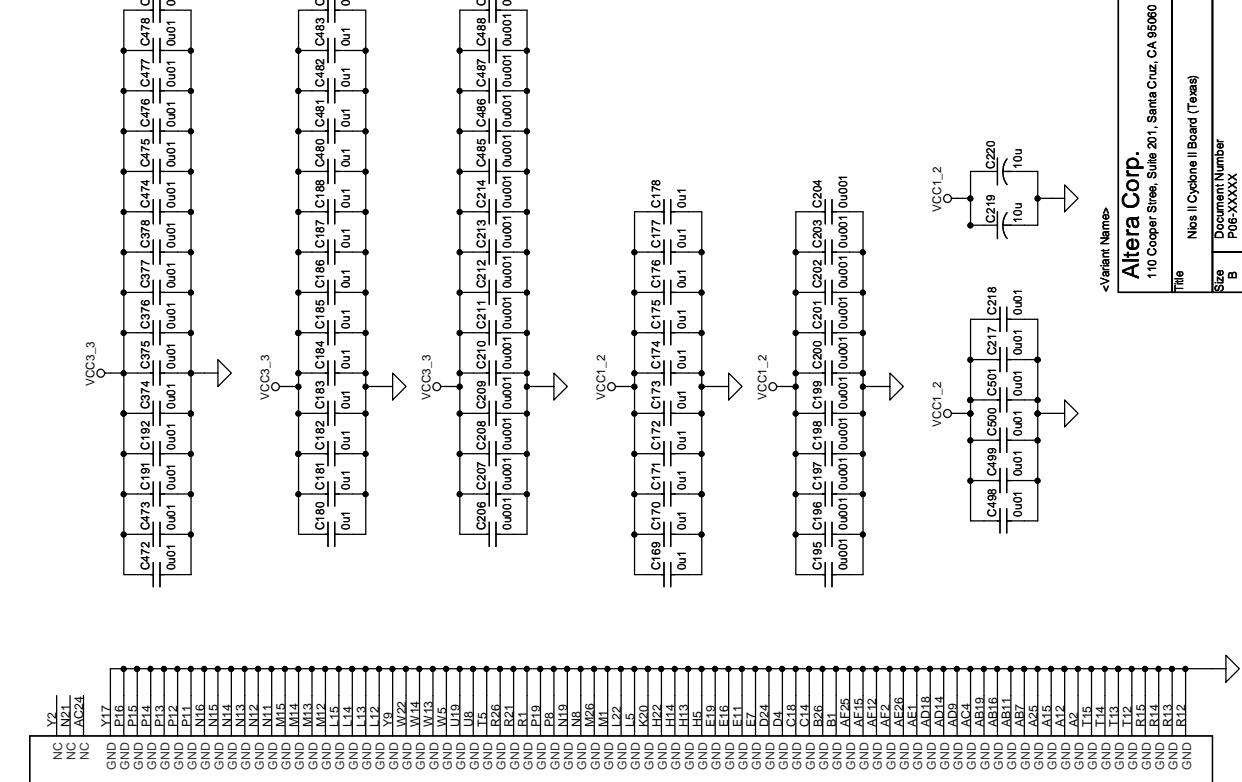
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Title: Nios II Cyclone II Board (Teos)

Size: B Document Number: P06-XXXXX Rev: 00

Date: Friday, April 01, 2005 Sheet: 17 of 32

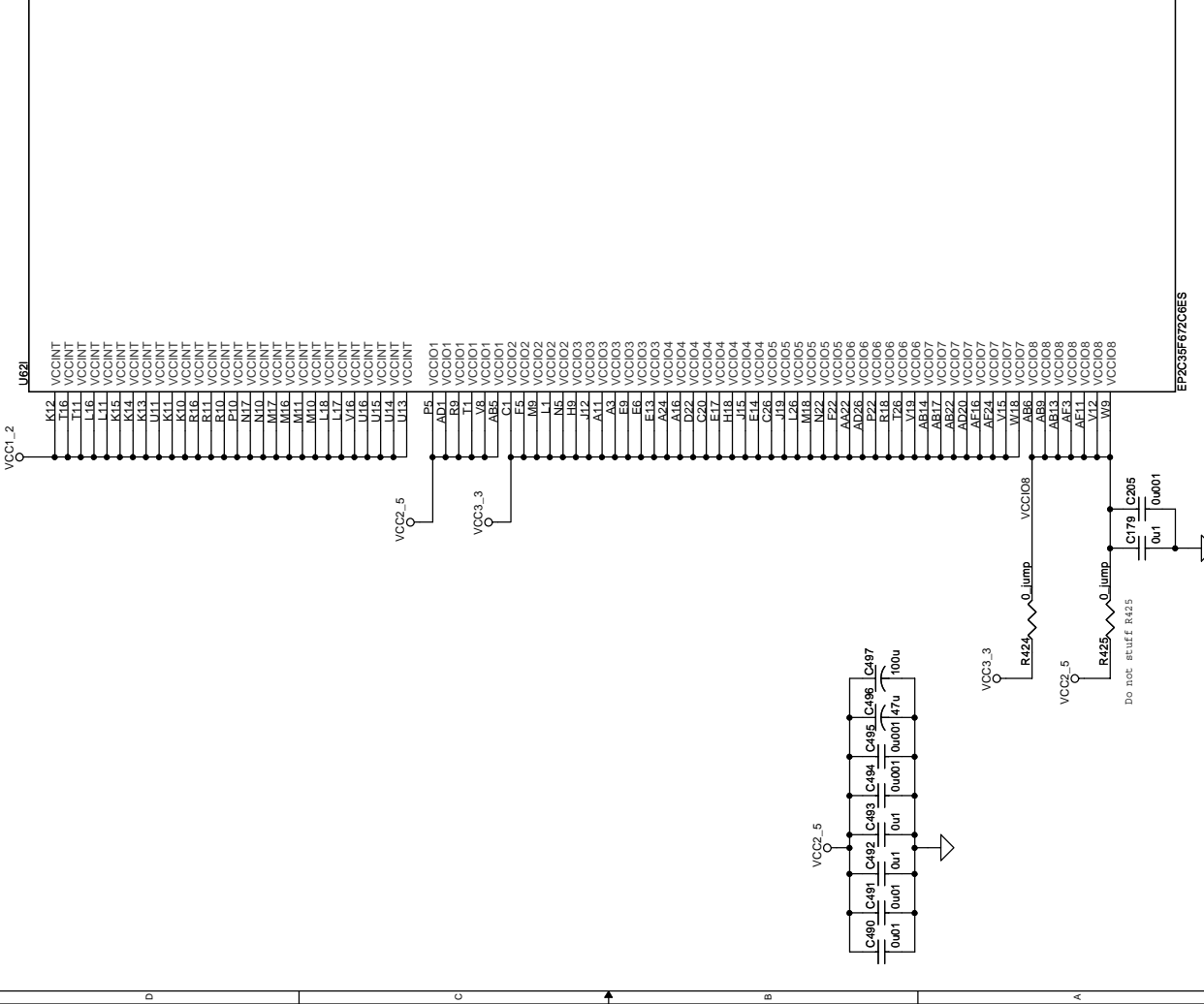
PLD Power



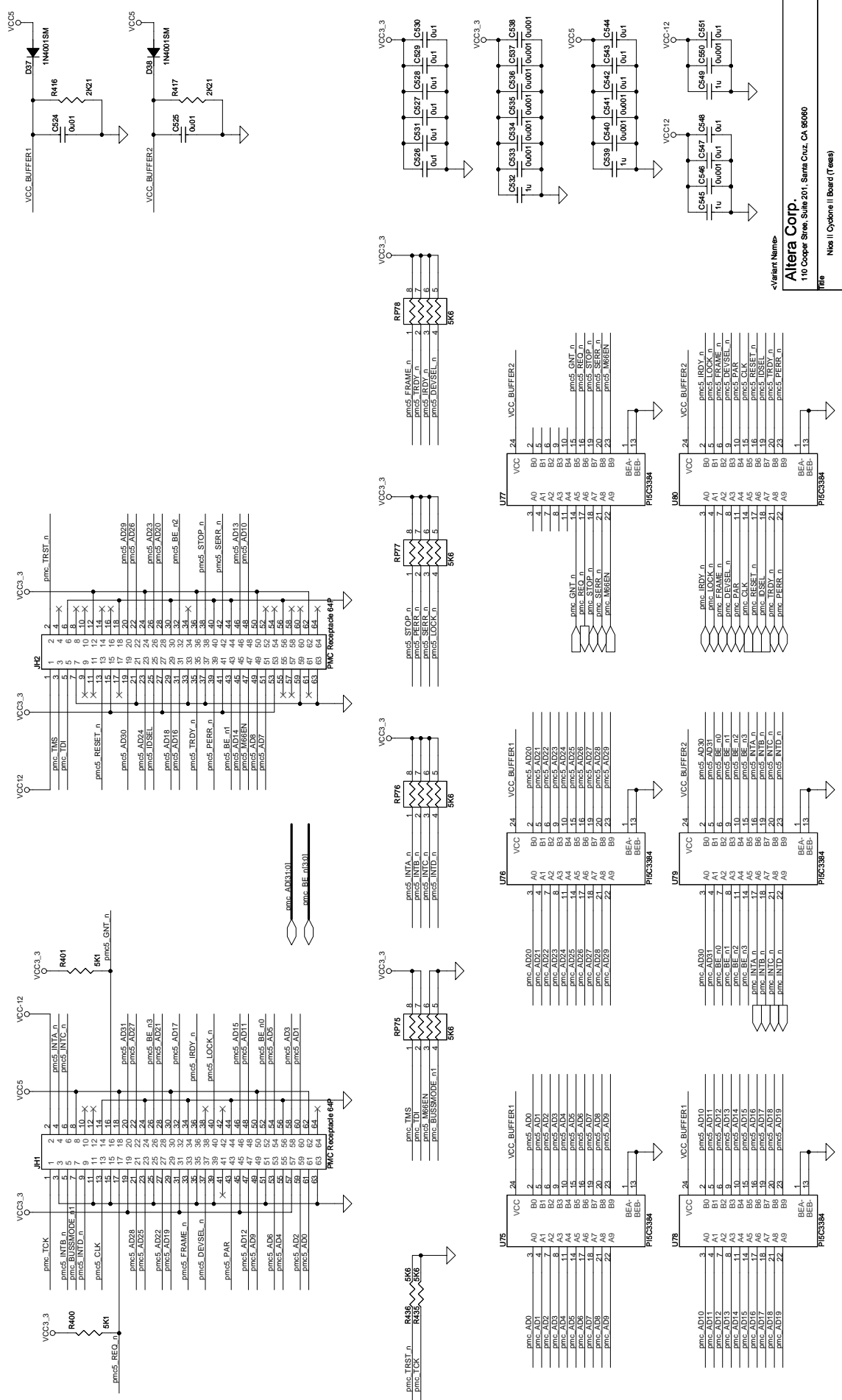
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Altera Corp.
110 Cooper Street, Suite 201, Santa Cruz, CA 95060

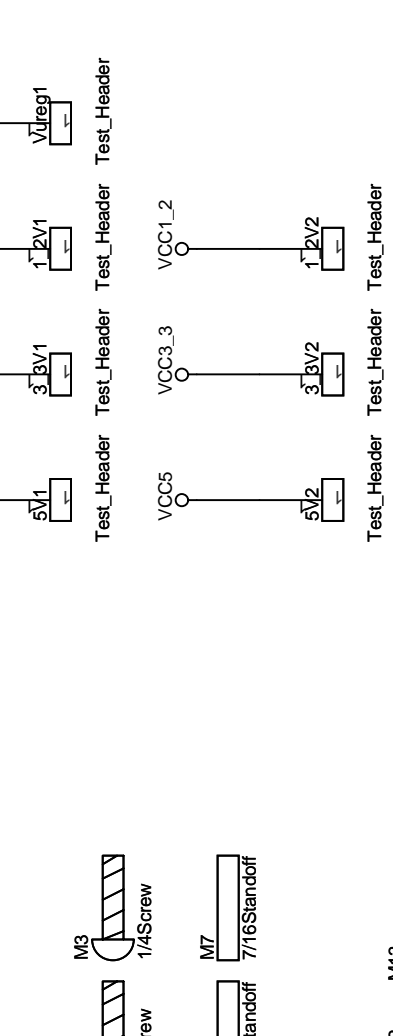
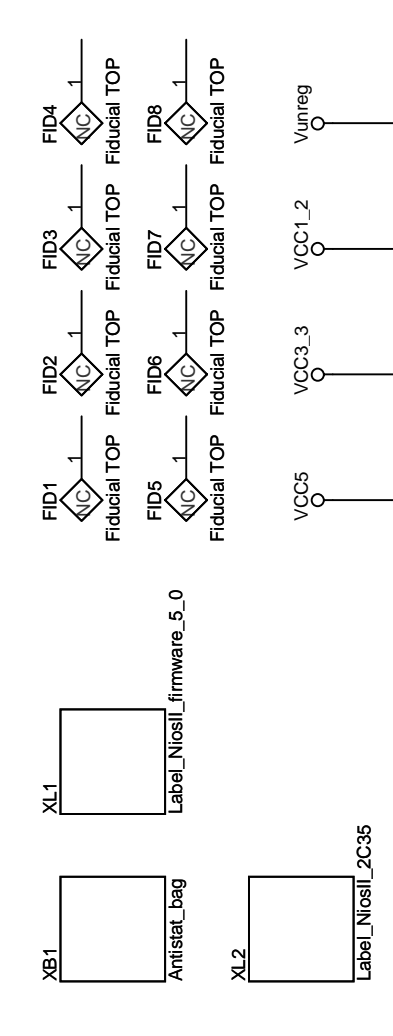
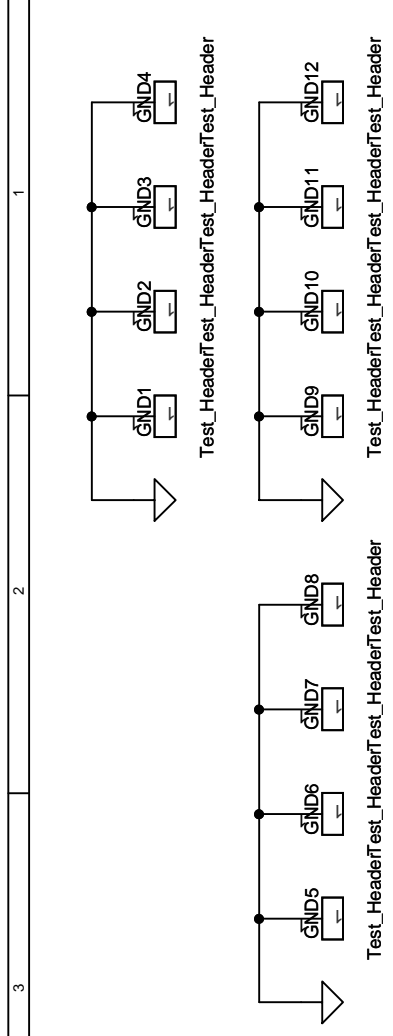
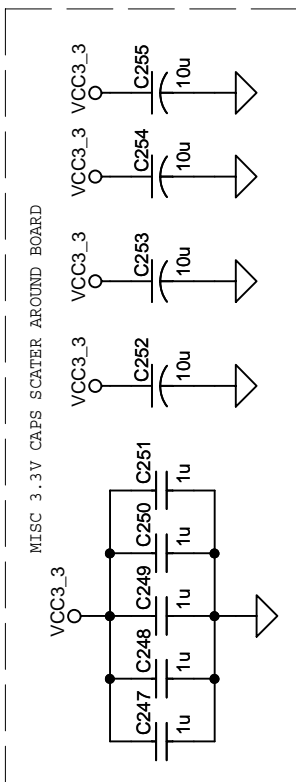
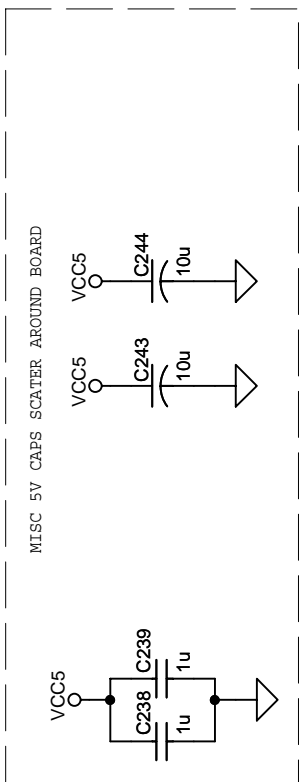
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Size	Document Number
B	P06-XXXXX
Date:	Friday, April 01, 2005
Sheet	18 of 32
Rev	00



Do not attach R425



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 Title: Nics II Cyclone II Board (Teess)
 S&T: 85526511 Number
 CushmanP06-XXXX
 Date: Friday, January 14, 2005 Sheet 19 of 32

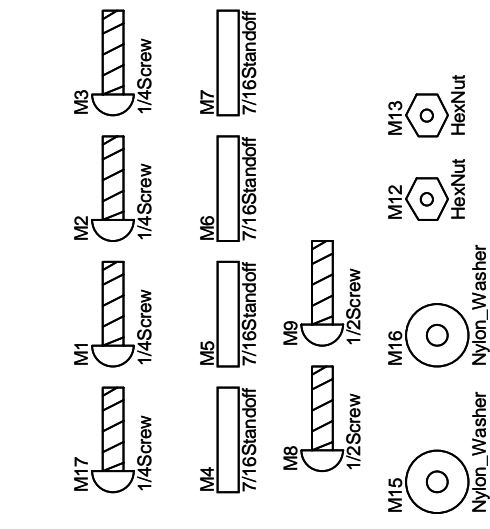
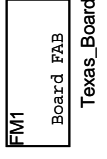


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Altera Corp.

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Title		Nios II Cyclone II Board (Texas)	
Size	Document Number	Rev	
A	P06-XXXXX	00	
Date:	Friday, April 01, 2005	Sheet	20 of 32



Power Connector

Label "5V Input"

J28 BANNANA_JACK_RED

VCC5

F1 Fuse_Block_7AMP

5A @ 5V

R211

C552

0.1

C563

0.1

C343

0.1

L10

22uH

C115

100u

C82

100u

D30

Diode_3A

Label "3.3V Input"

J29 BANNANA_JACK_RED

VCC3_3

F2 Fuse_Block_7AMP

5A @ 3.3V

R212

C554

0.1

C555

0.1

C351

0.1

L11

22uH

C352

100u

C353

100u

D31

Diode_3A

Label "GND"

J33 BANNANA_JACK_BLK

Vinreg

U54 LM2678 5.0V

U55 LM2678 3.3V

Label "1.2V Input"

J30 BANNANA_JACK_RED

VCC1_2

1.0A @ 1.2V

F3 Fuse_Block_7AMP

R221

C382

47u

C379

0.1

C380

0.1

Q1

FDS9680A

Q2

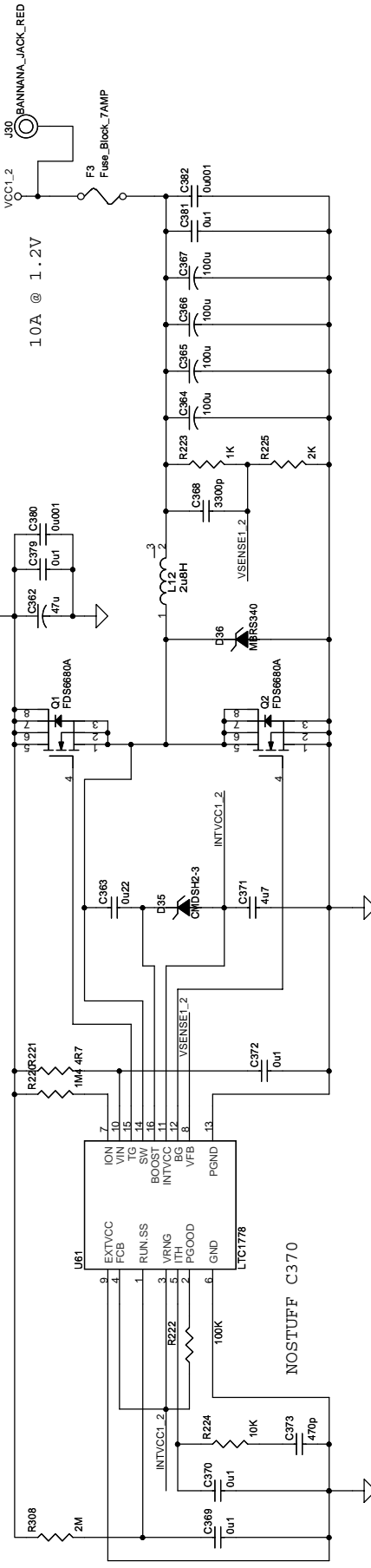
FDS9680A

C388

3300p

D36

MPRS340



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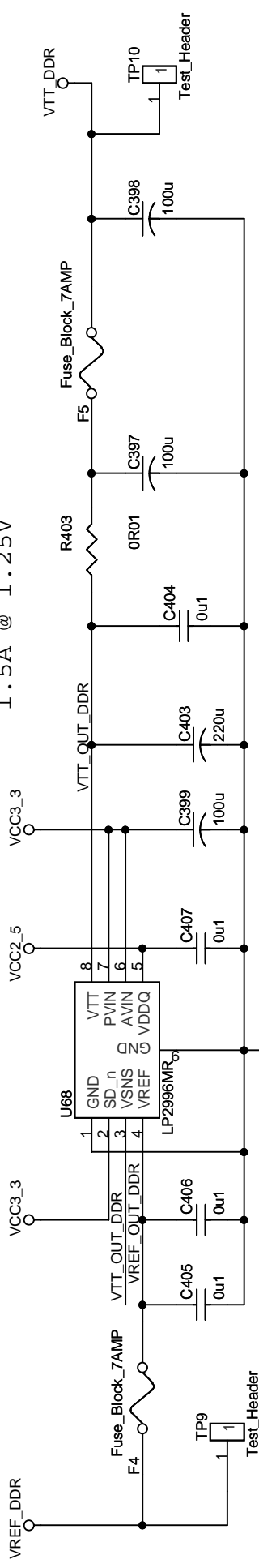
Title Nios II Cyclone II Board (Teaos)

Size B Document Number P06-XXXXX

Date: Friday, March 11, 2005 Sheet 21 of 32

Reset and Test headers

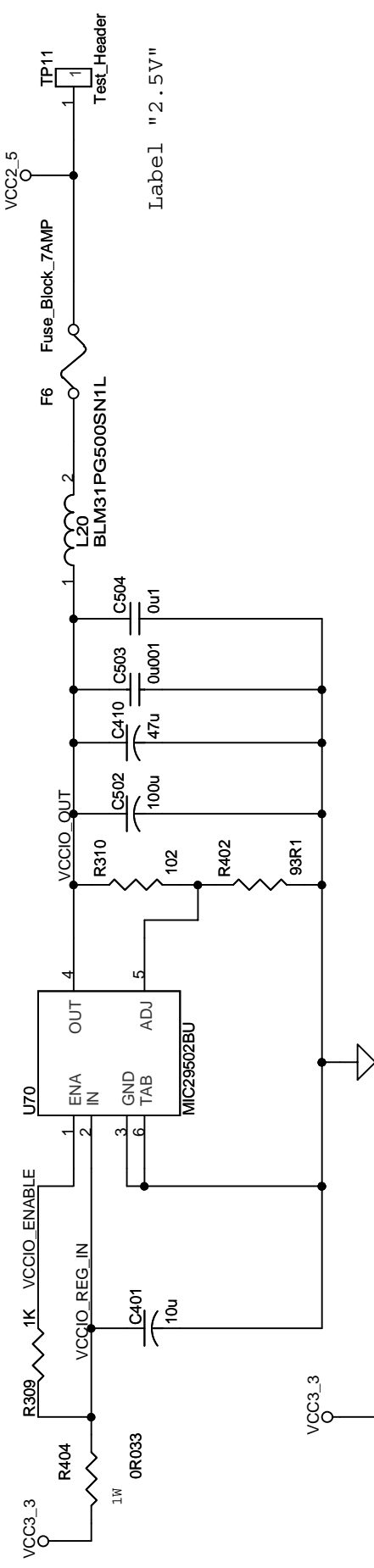
1.5A @ 1.25V



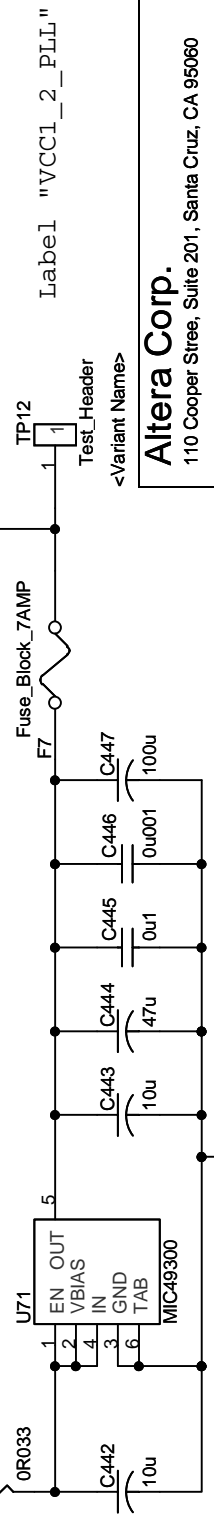
Label "VREF_DDR"

Label "VTT_DDR"

5A @ 2.5V



3A @ 1.2V



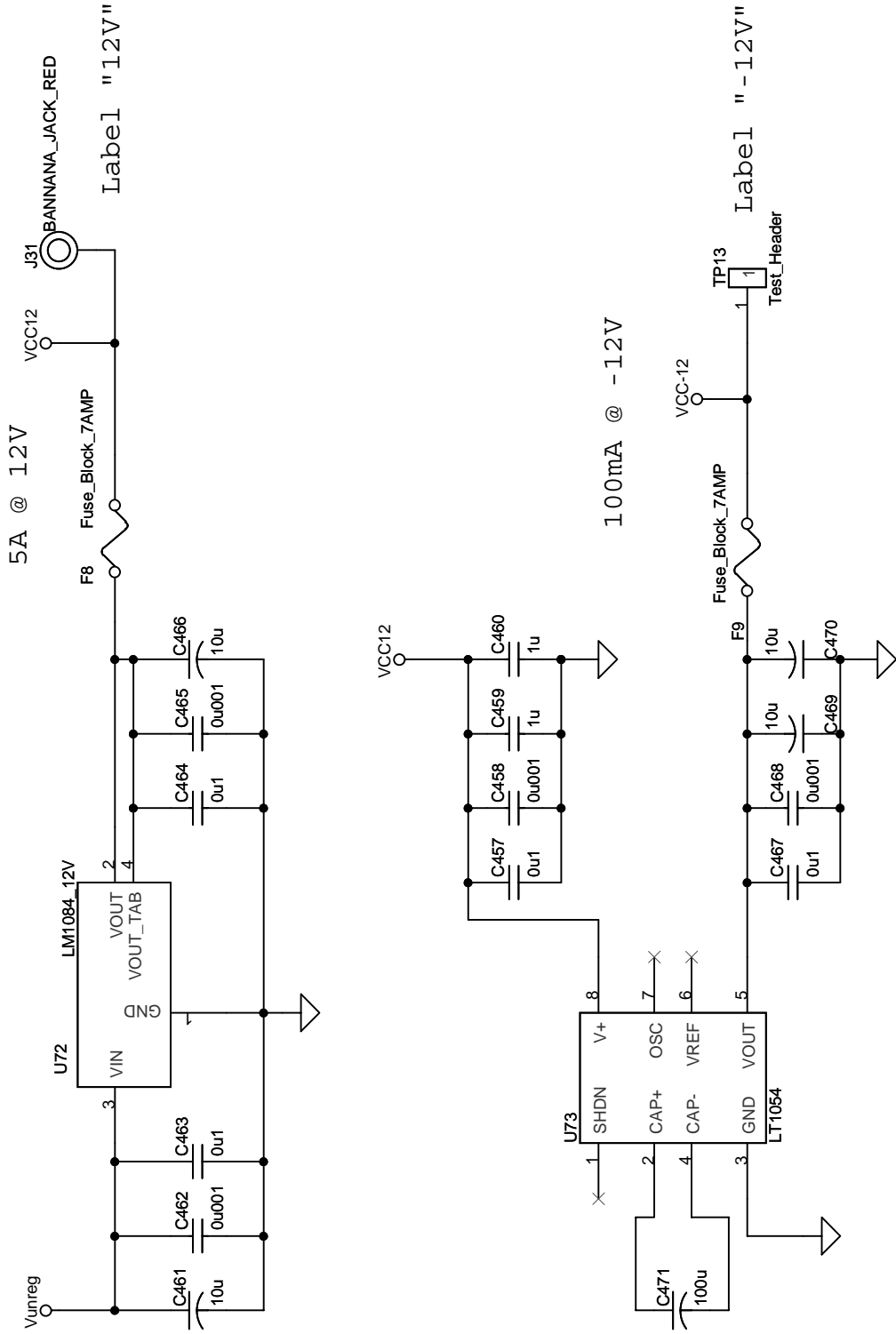
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Title: Nios II Cyclone II Board (Texas)

Size	Document Number	Rev
A	P06-XXXXX	00

Date: Friday, March 11, 2005 Sheet 22 of 32



<Variant Name>

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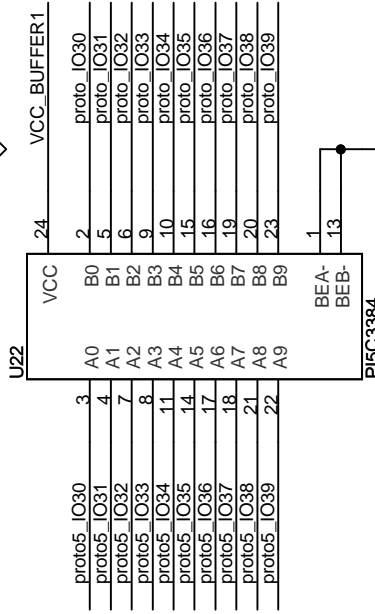
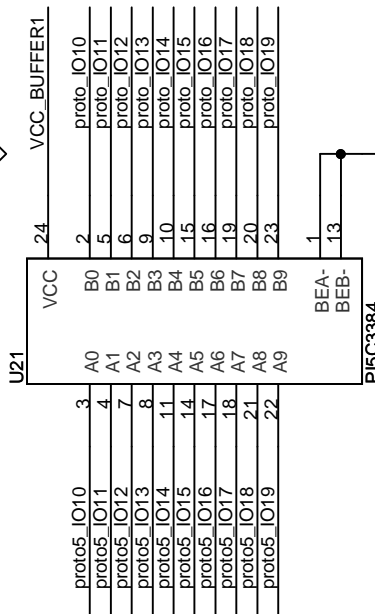
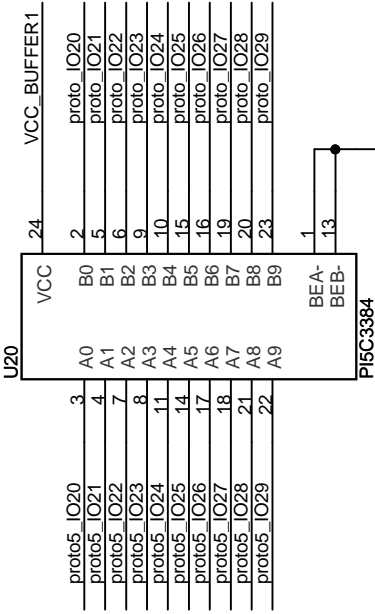
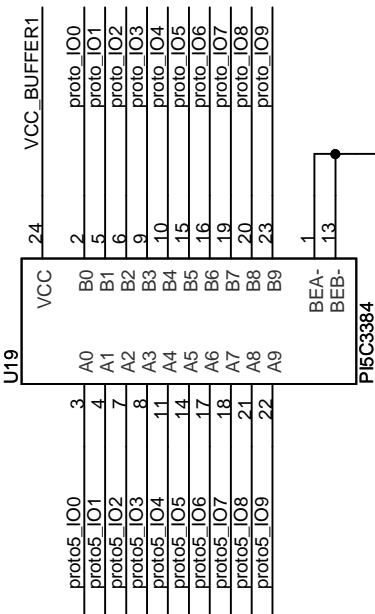
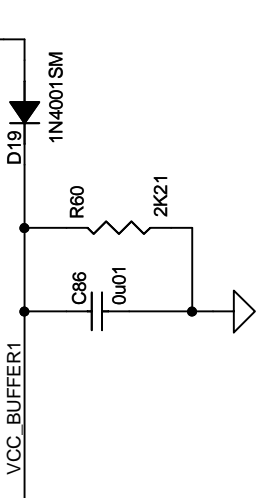
Title: Nios II Cyclone II Board (Texas)

Size: A
Document Number: P06-XXXXX

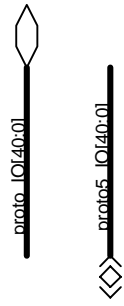
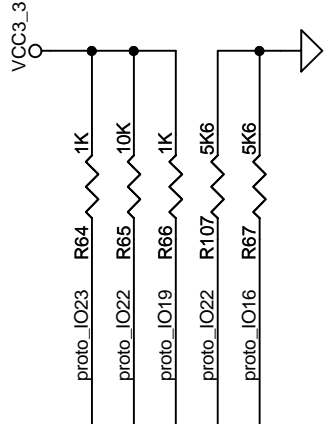
Rev: 00

NO CHANGE

Proto1 Buffers



R65 and R107 are stuff options for the IDE determining whether IDE_INTRQ gets a pull down or should be a nostuff for production.



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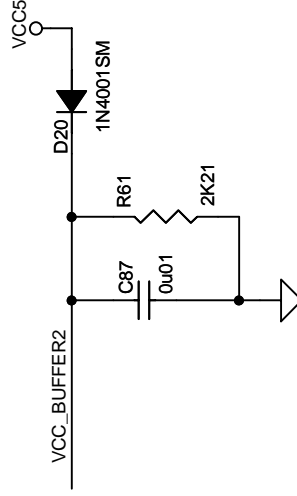
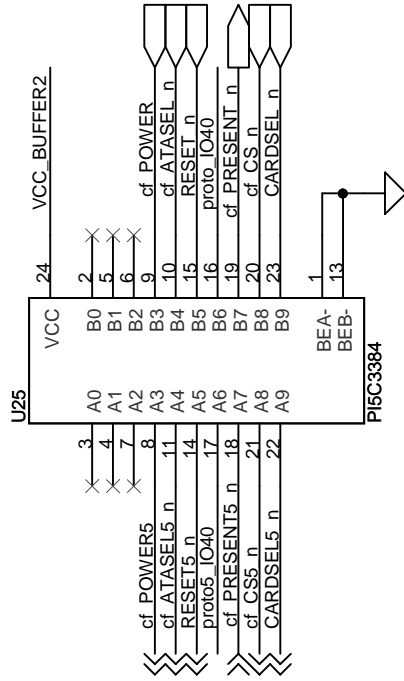
Title: Nios II Cyclone II Board (Texas)

Size: A
Document Number: P06-XXXXX

Date: Thursday, December 23, 2004

NO CHANGE

Proto1 Buffers



proto5_IO140:01

proto_IO140:01

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Size A Document Number P06-XXXXX

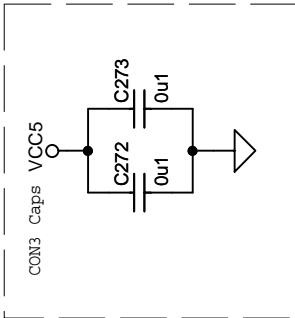
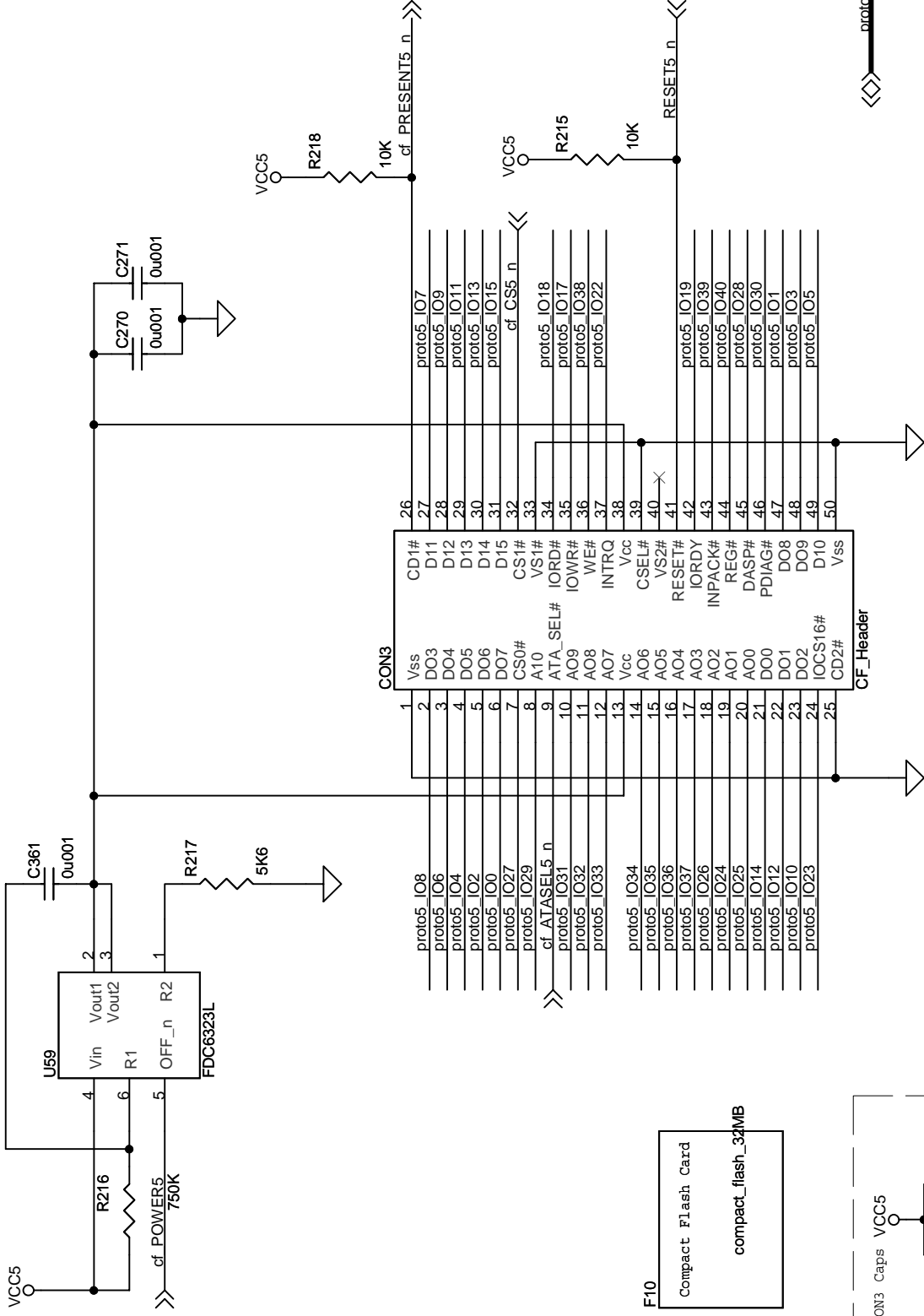
Rev 00

Date: Thursday, December 23, 2004

Sheet 25 of 32

NO CHANGE

Compact Flash Socket



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Title Nios II Cyclone II Board (Texas)

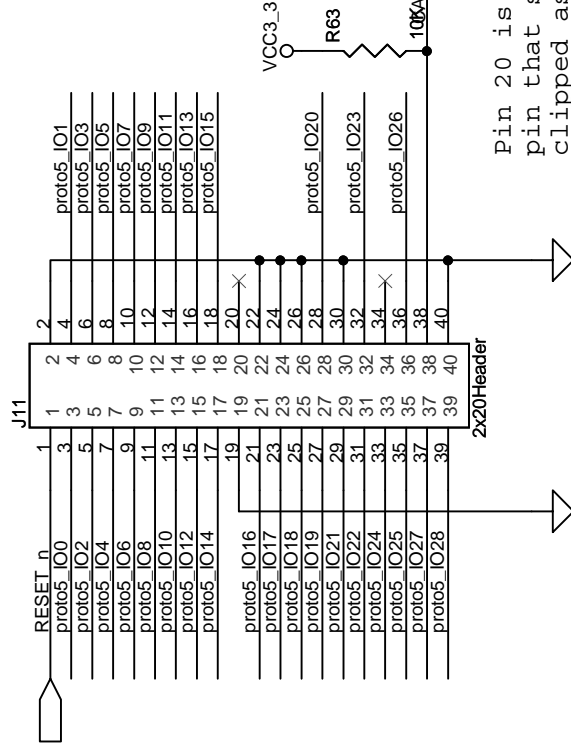
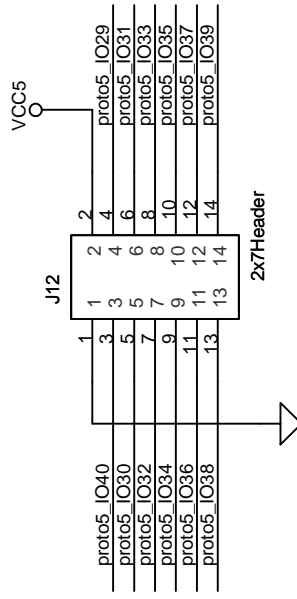
Size A Document Number P06-XXXXX

Rev 00

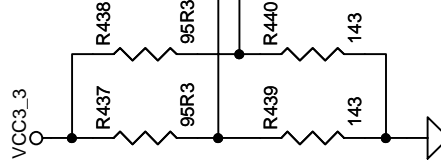
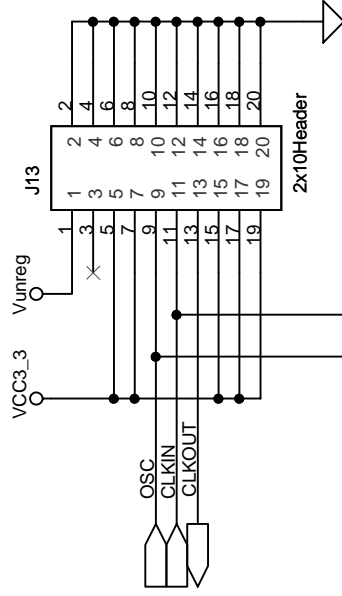
Date: Thursday, March 24, 2005 Sheet 26 of 32

NO CHANGE

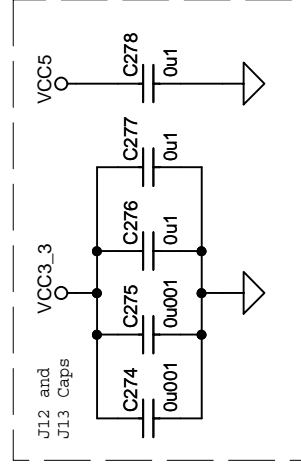
Protocard 1



Pin 20 is a keying pin that should be clipped as a part of the production process.



<<< proto5_IO140:01



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Title

Nios II Cyclone II Board (Texas)

Size

A Document Number

P06-XXXXX

Rev

00

Date:

Friday, January 14, 2005

Sheet

27 of 32

2

1

5

4

3

2

1

D

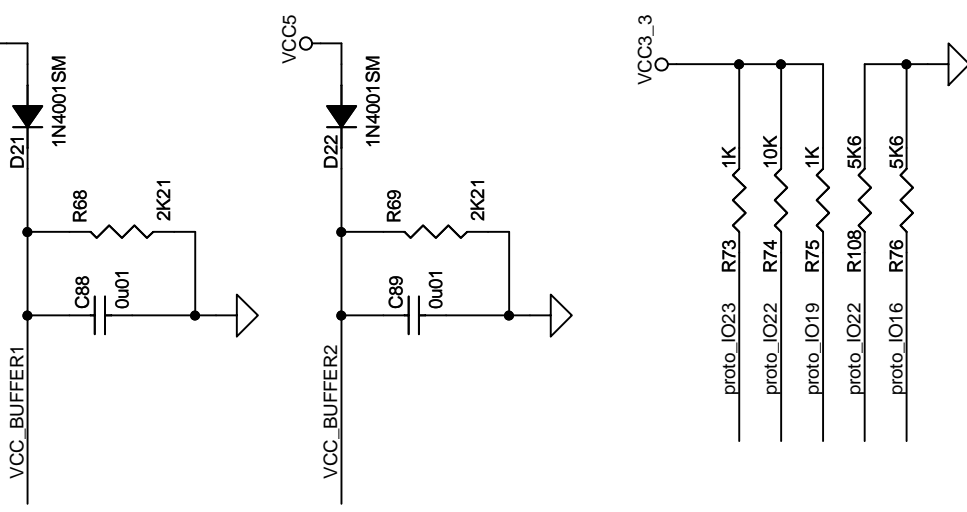
C

B

A

NO CHANGE

Proto2 Buffers

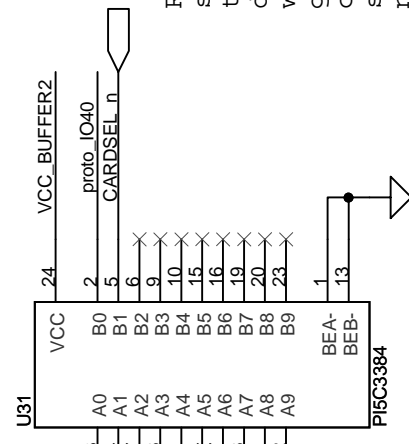


3	proto5_IO20
4	proto5_IO21
7	proto5_IO22
8	proto5_IO23
11	proto5_IO24
14	proto5_IO25
17	proto5_IO26
18	proto5_IO27
21	proto5_IO28
22	proto5_IO29
24	VCC_BUFFER1

3	proto5_IO30
4	proto5_IO31
7	proto5_IO32
8	proto5_IO33
11	proto5_IO34
14	proto5_IO35
17	proto5_IO36
18	proto5_IO37
21	proto5_IO38
22	proto5_IO39
24	VCC_BUFFER2

3	proto5_IO0
4	proto5_IO1
7	proto5_IO2
8	proto5_IO3
11	proto5_IO4
14	proto5_IO5
17	proto5_IO6
18	proto5_IO7
21	proto5_IO8
22	proto5_IO9
24	VCC_BUFFER1

3	proto5_IO10
4	proto5_IO11
7	proto5_IO12
8	proto5_IO13
11	proto5_IO14
14	proto5_IO15
17	proto5_IO16
18	proto5_IO17
21	proto5_IO18
22	proto5_IO19
24	VCC_BUFFER1



3	proto5_IO40
4	proto5_IO41
7	proto5_IO42
8	proto5_IO43
11	proto5_IO44
14	proto5_IO45
17	proto5_IO46
18	proto5_IO47
21	proto5_IO48
22	proto5_IO49
24	VCC_BUFFER2

R74 and R108 are stuff options for the IDE determining whether IDE_INTRQ gets a pull_down or pull up. R74 should be a nostuff for production.

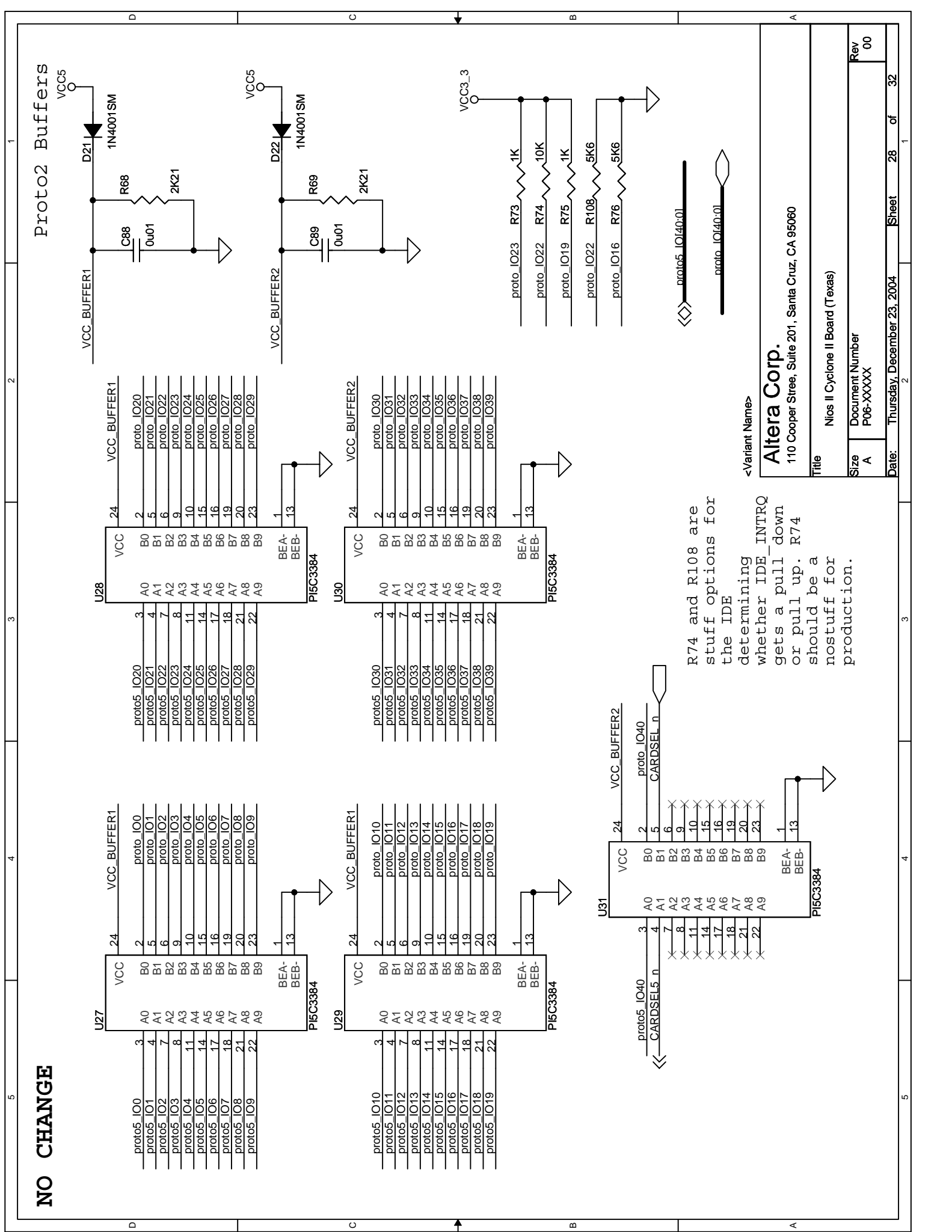
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Title: Nios II Cyclone II Board (Texas)

Size: A
 Document Number: P06-XXXXX
 Rev: 00

Date: Thursday, December 23, 2004
 Sheet: 28 of 32

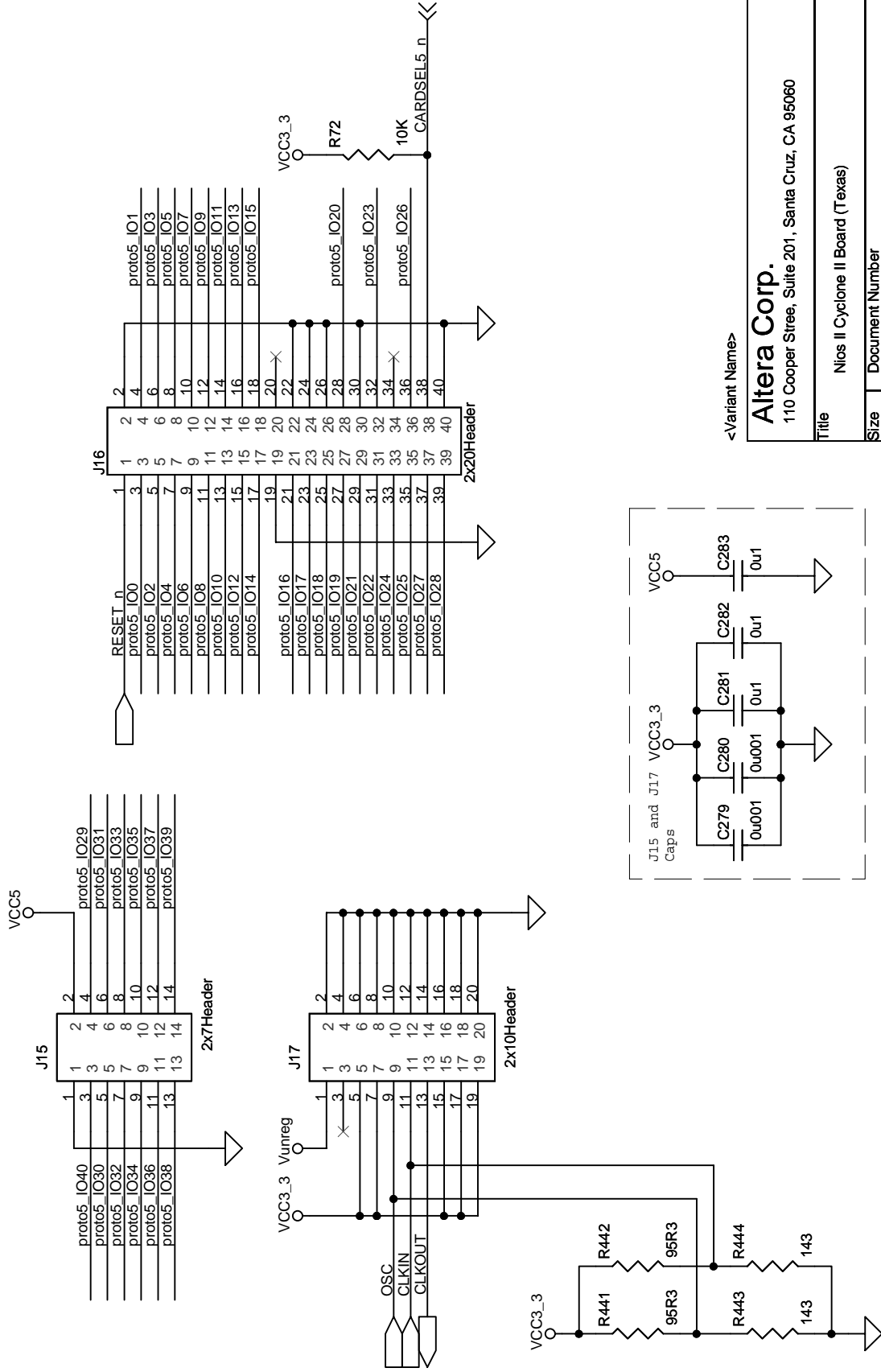


NO CHANGE

Proto2 Headers

Pin 20 is a keying pin that should be clipped as a part of the production process.

◀◀ proto5_IO[40:0] ▶▶



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Title: Nios II Cyclone II Board (Texas)

Size: A
Document Number: P06-XXXXX

Rev: 00

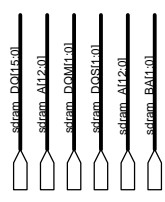
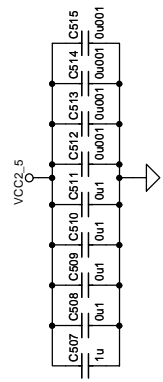
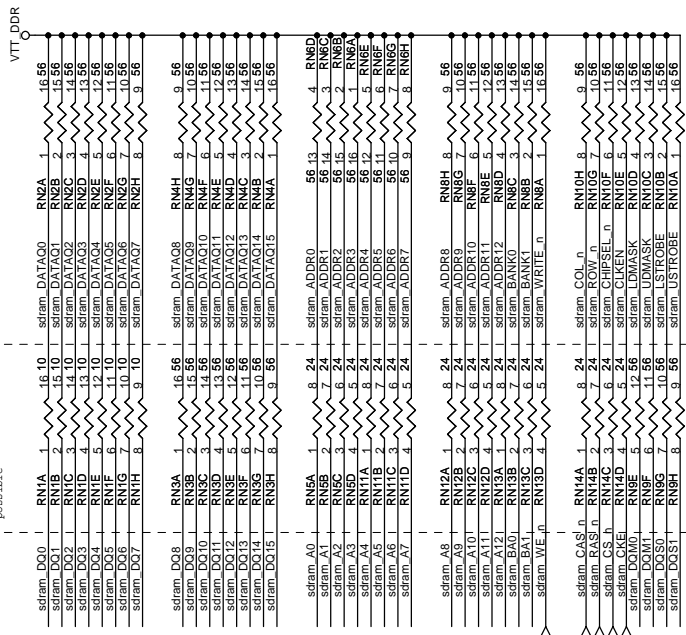
Date: Friday, January 14, 2005 Sheet 29 of 32

Place the pull up resistors just past U63 so that each trace tag the pin that it is going through the resistor to VTT_DDR

Place these resistors as close to the PAD U62 as possible

Place R321 just past the pins on U63. The net to R321 is terminated.

Place R319 and R320 as close to P1D as possible



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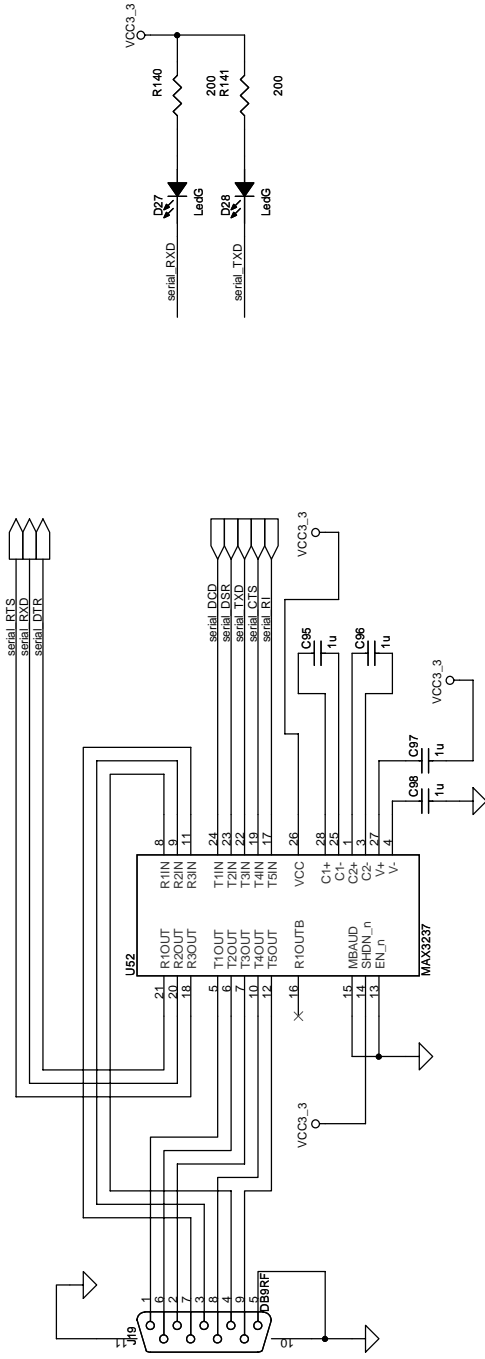
Size: B
Document Number: P06-XXXXX

Date: Monday, March 28, 2005

Sheet: 30 of 32

Rev: 00

Serial Ports



<Variant Name>

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Title: Nios II Cyclone II Board (Teras)

Size: B

Document Number: P06-XXXXX

Rev: 00

Date: Thursday, December 23, 2004

Sheet: 31

of: 32

