

# Nios Development Board

## Stratix II Edition

### Rev 03

Revision History		
Date	Change Description	Rev
10/21/03	Started design	01
7/22/04	Rev 02 of design is made to fix the bus alignment problem with the flash.	02
8/27/04	Rev 03 is done to add the pull up resistor to the Run/SS pin of the 1.2V supply in order to prevent power up problem.	03

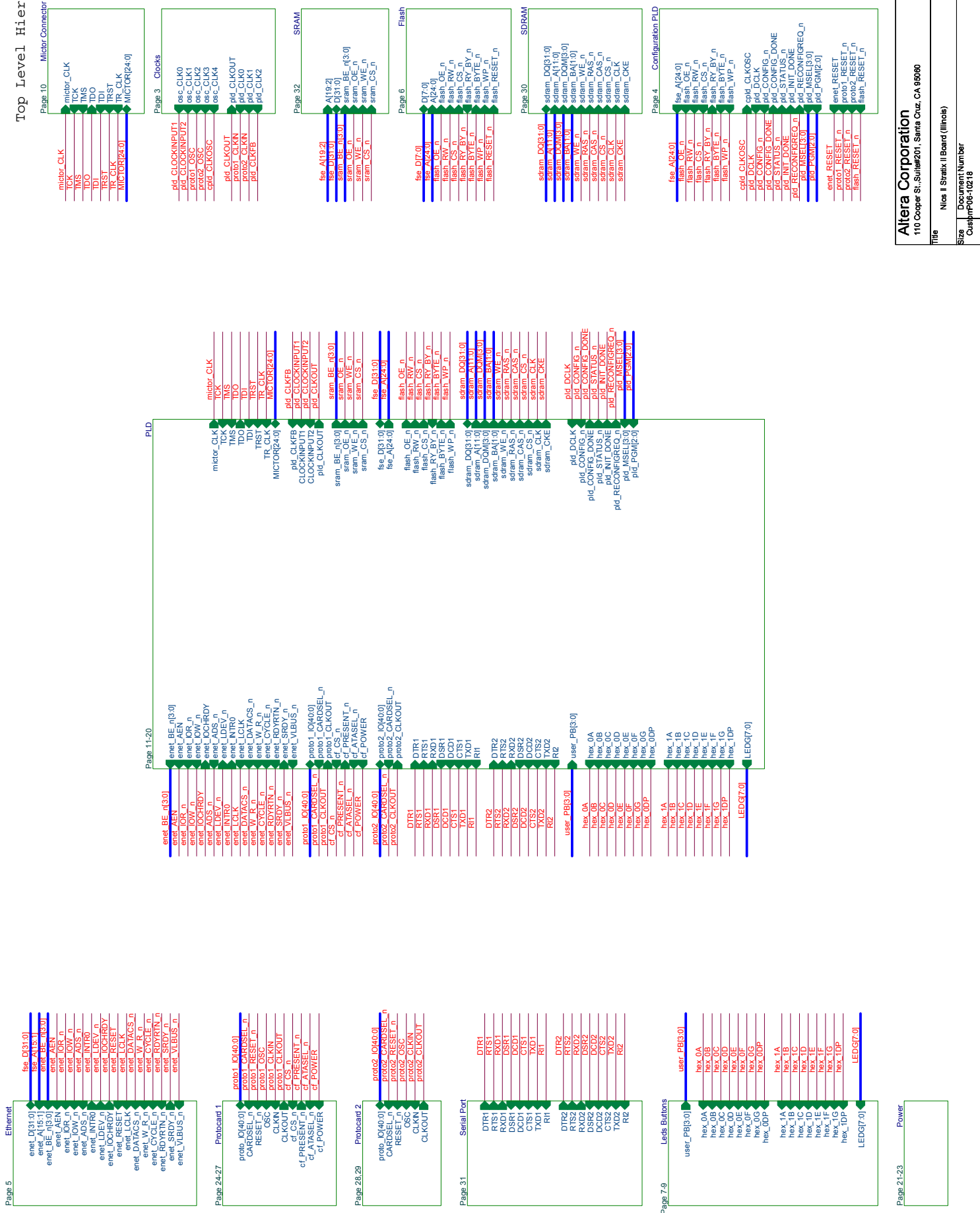
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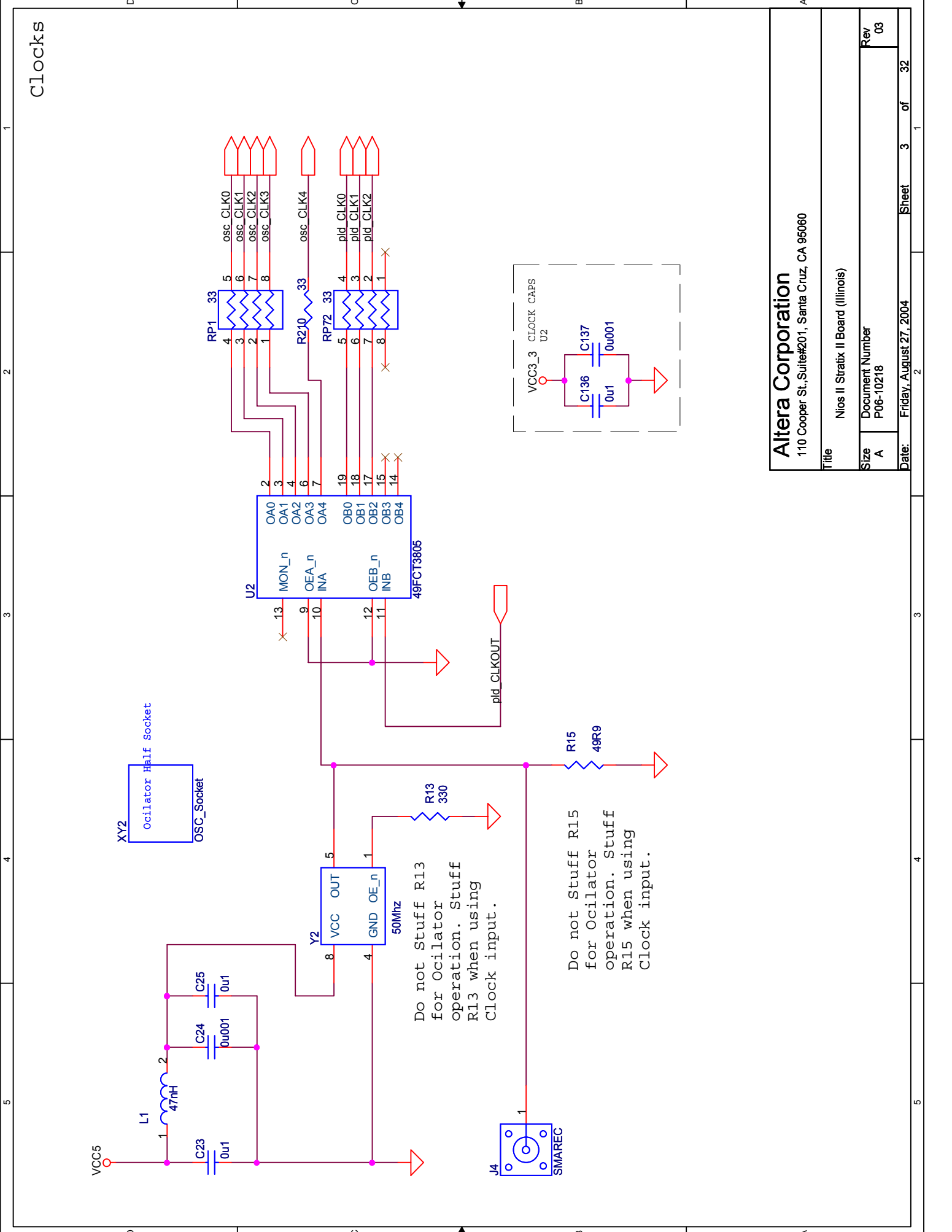
Title: Nios II Stratix II Board (Illinois)

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# Top Level Hierarchy





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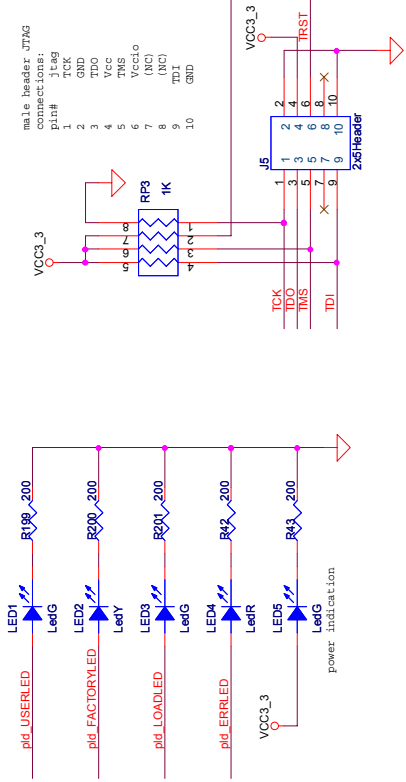
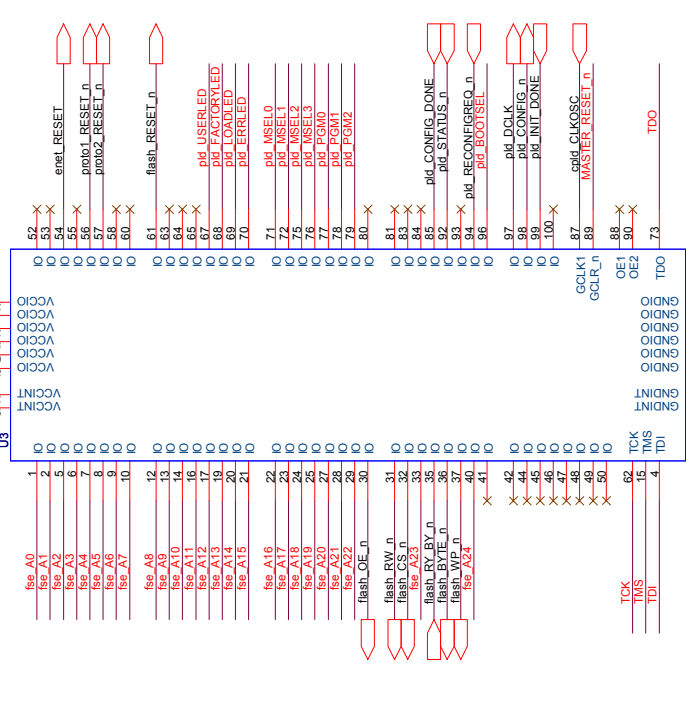
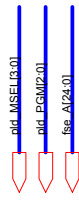
Title Nios II Stratix II Board (Illinois)

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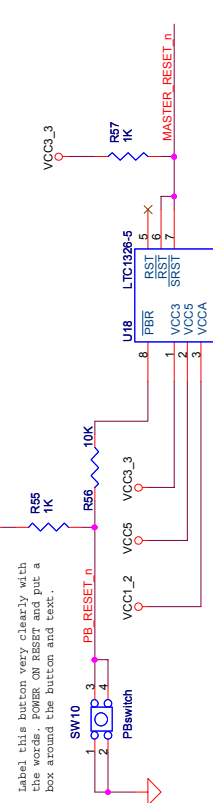
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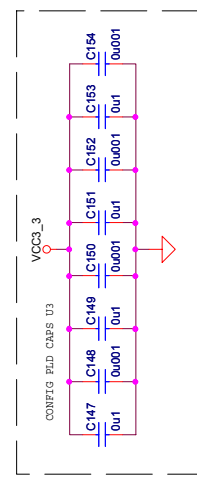
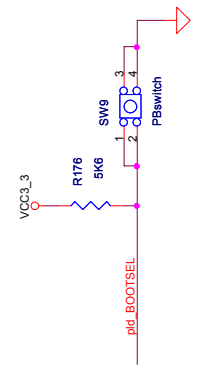
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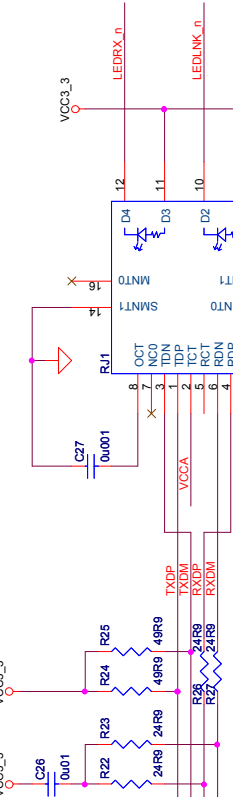


Label this button every clearly with the words POWER ON RESET and put a box around the button and text.

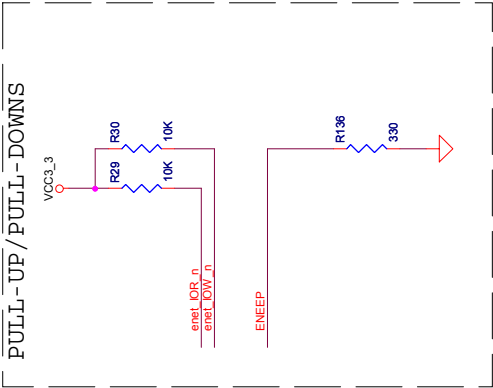
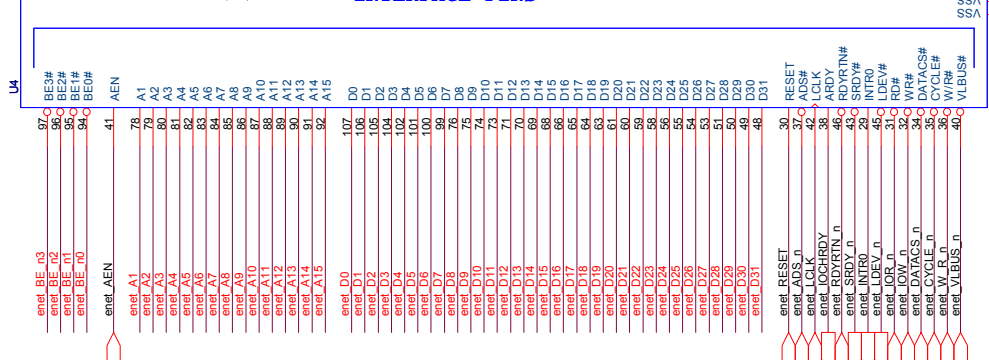
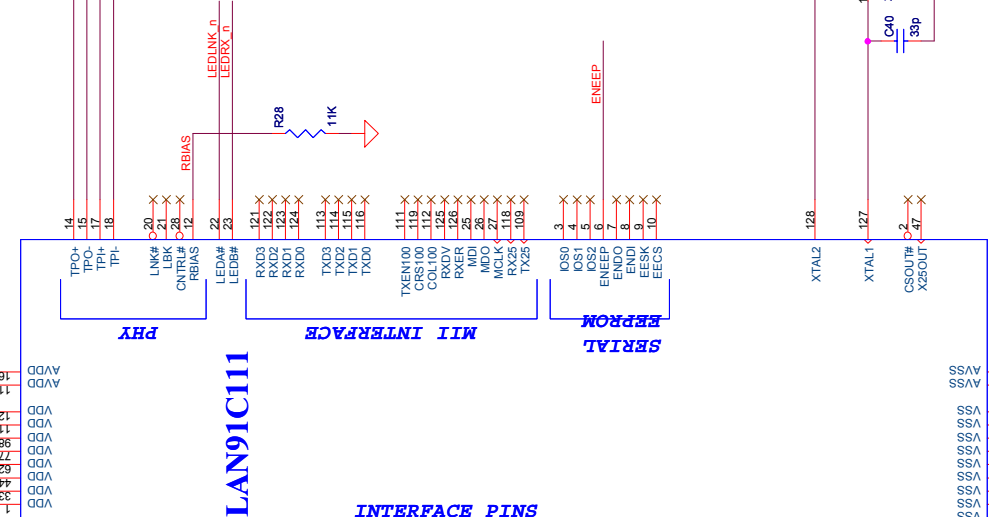


pld\_BOOTSEL determines whether to force a boot from the default boot sector, or the user-programmed boot sector.





8ch1F, R155, R156, R157, R158, R159 and R160 only when using the MAC PHY integrated in the LAN91C111. R151, R152, R153 and R154 are non-routable.



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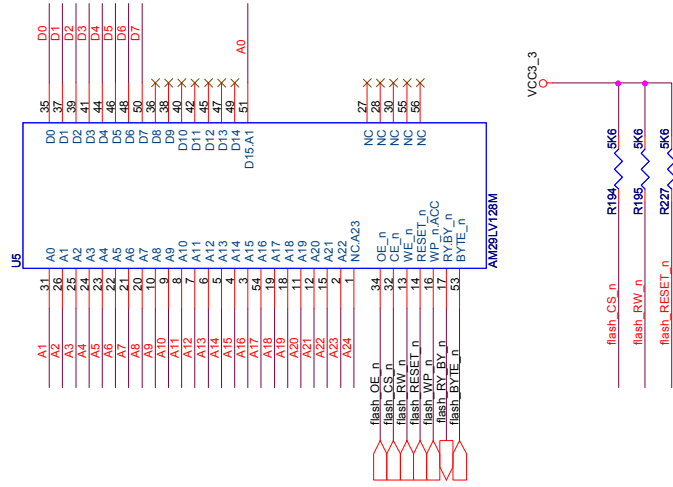
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Flash chip is 16M x 8 for 16Mbytes of flash

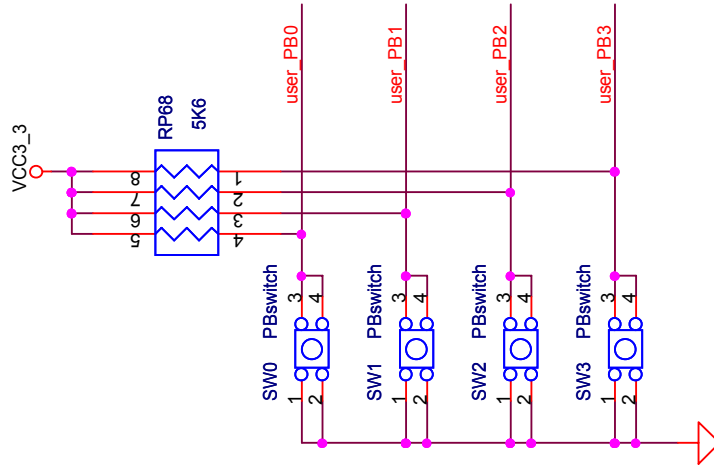
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# Buttons



user\_PB[3:0]

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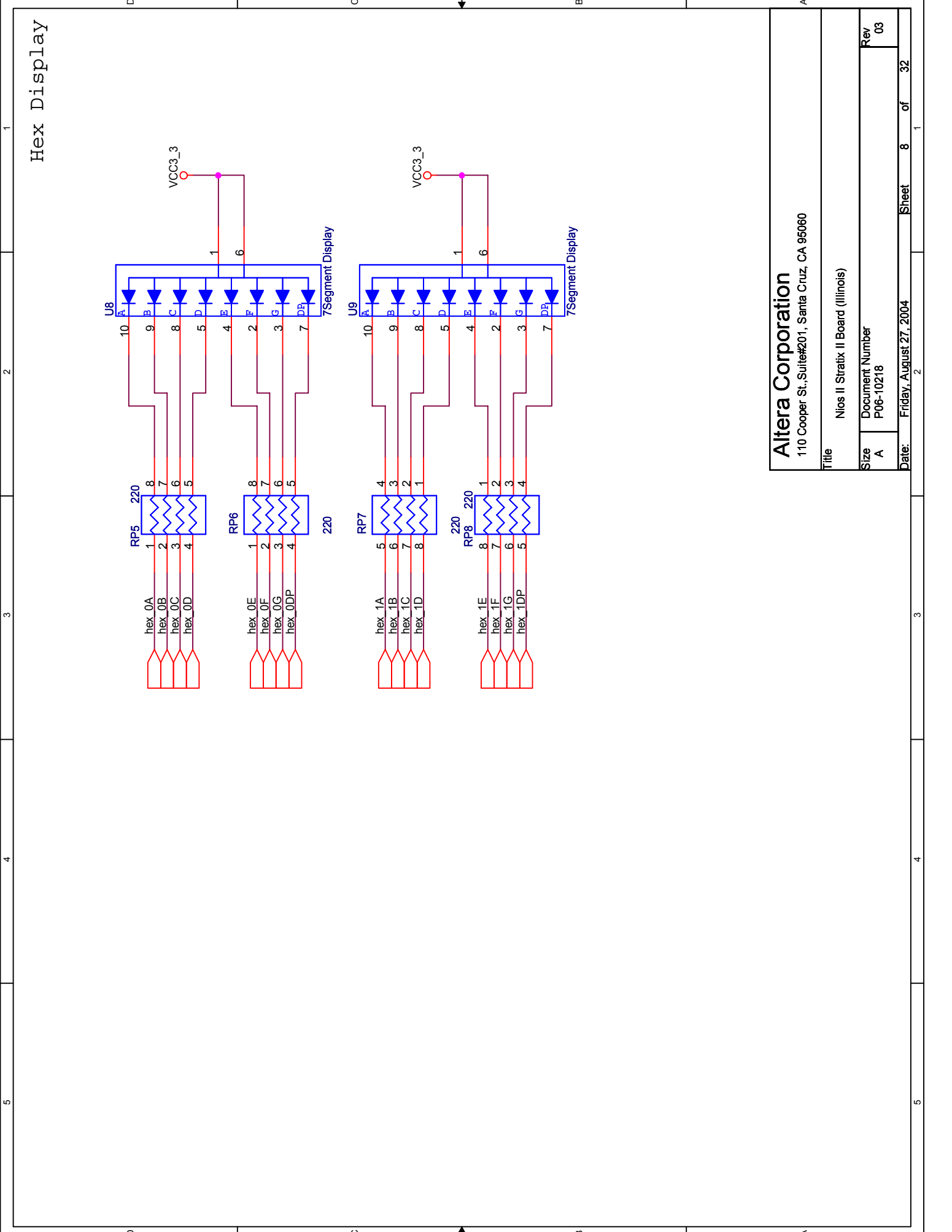
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# Hex Display

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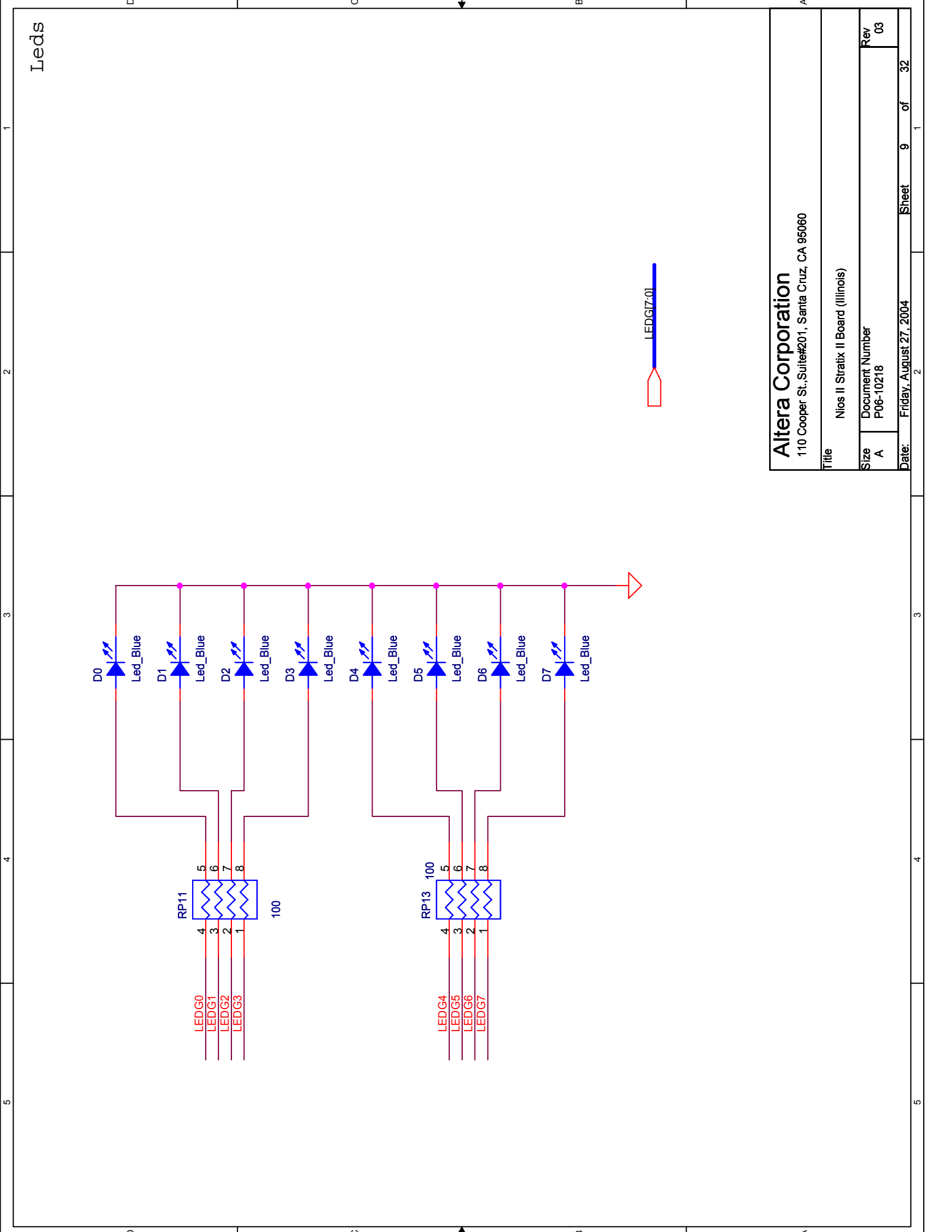
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LEDGIZ.01

Leds

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1

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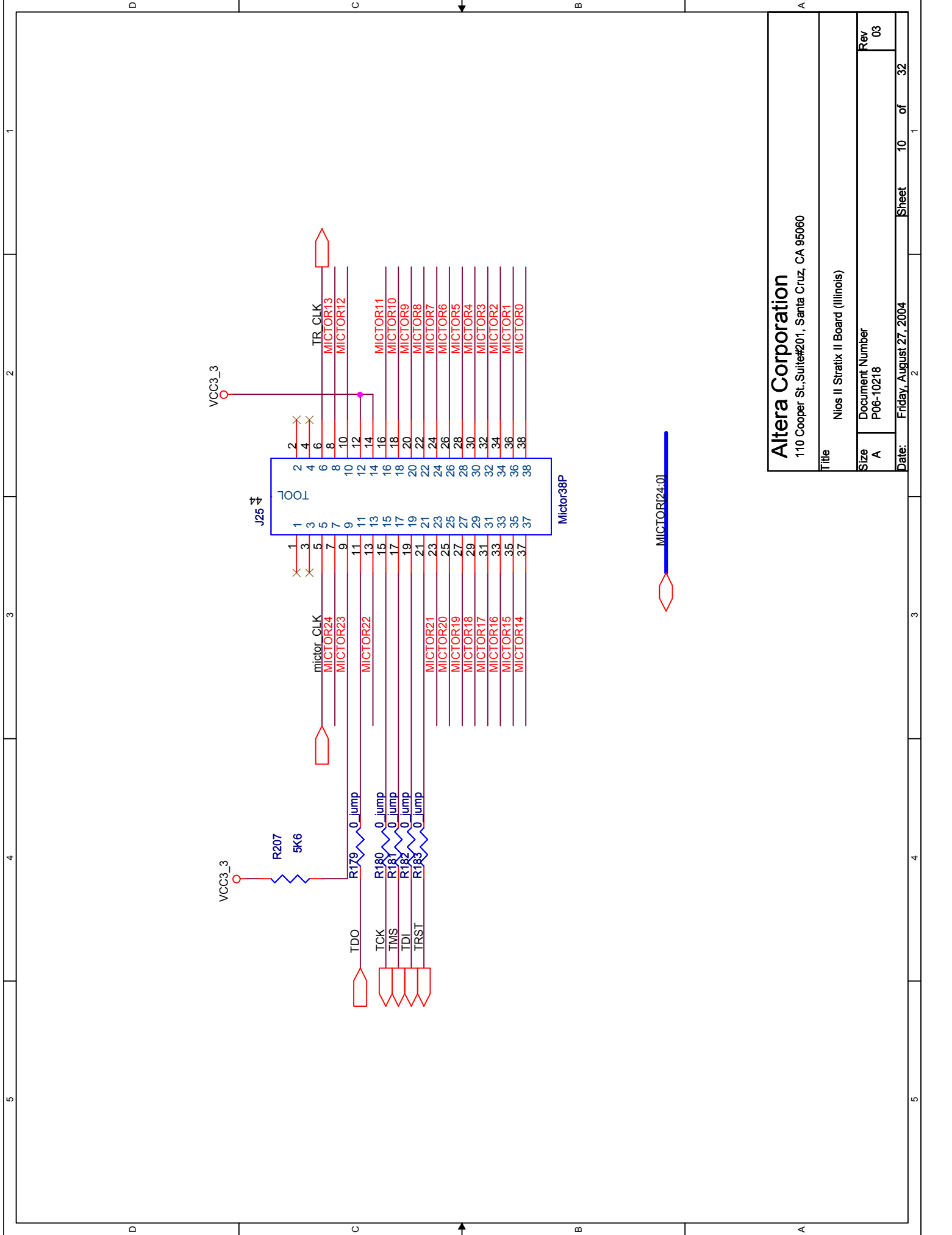
1

2

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4

5



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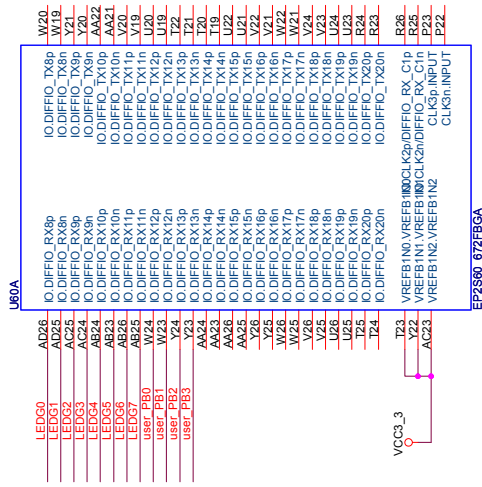
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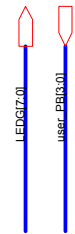
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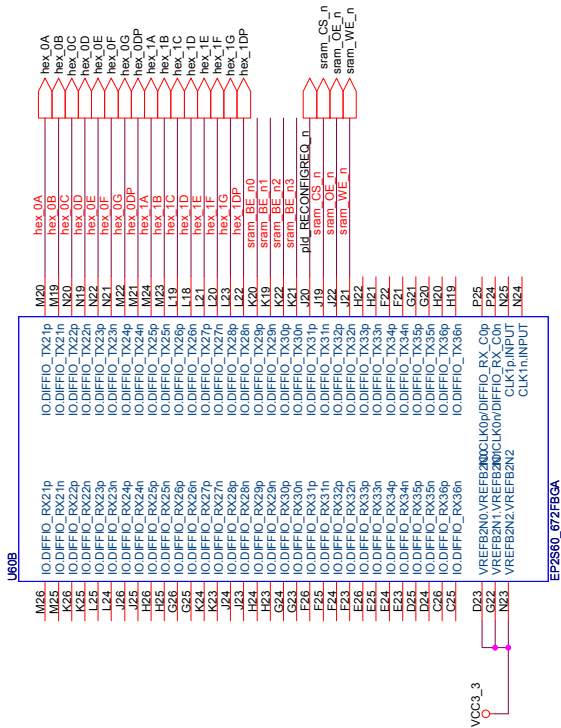
PLD Bank 1



EP2S60\_67F6CA



PLD Bank 2



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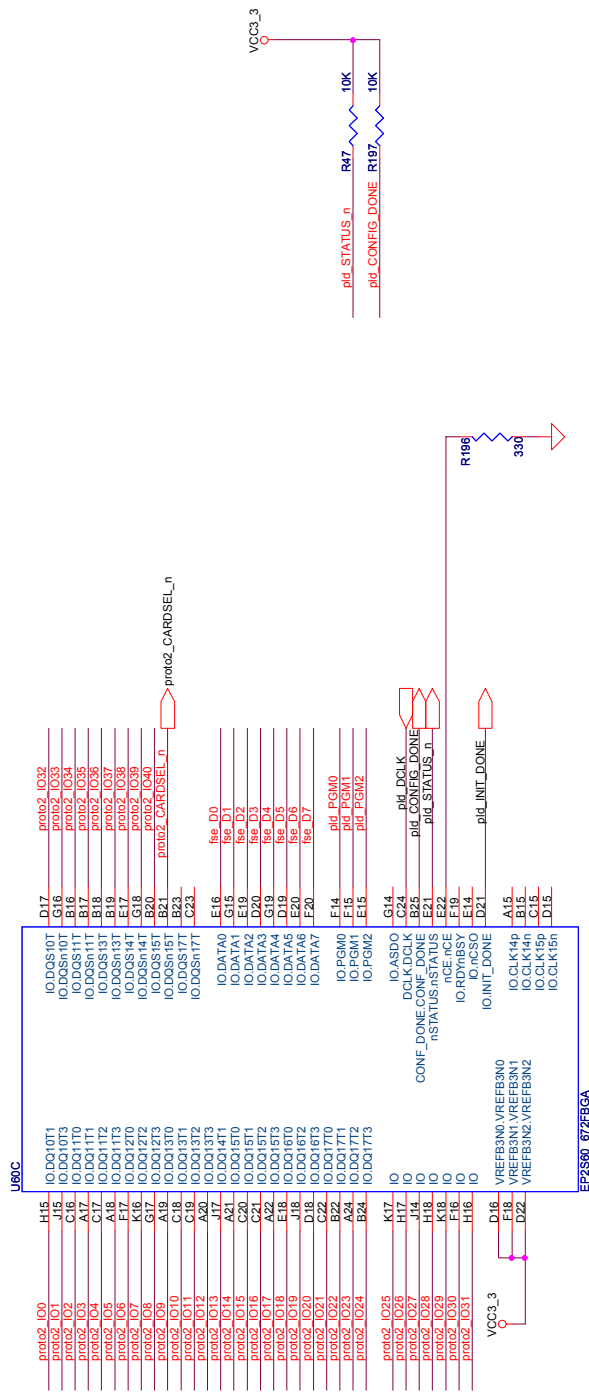
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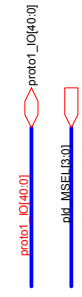
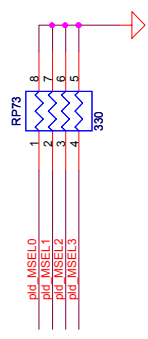
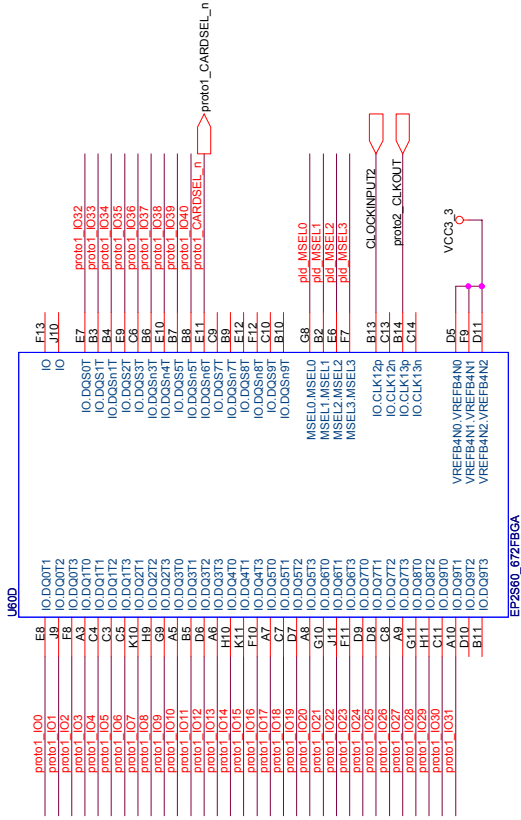
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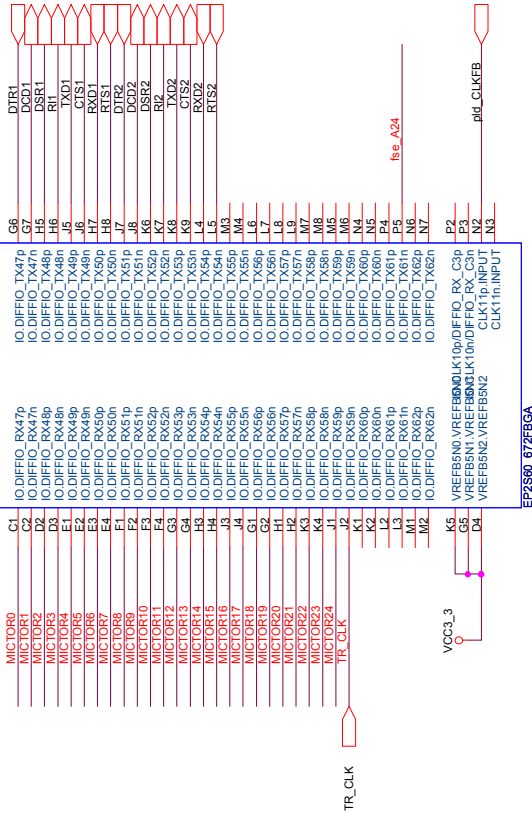
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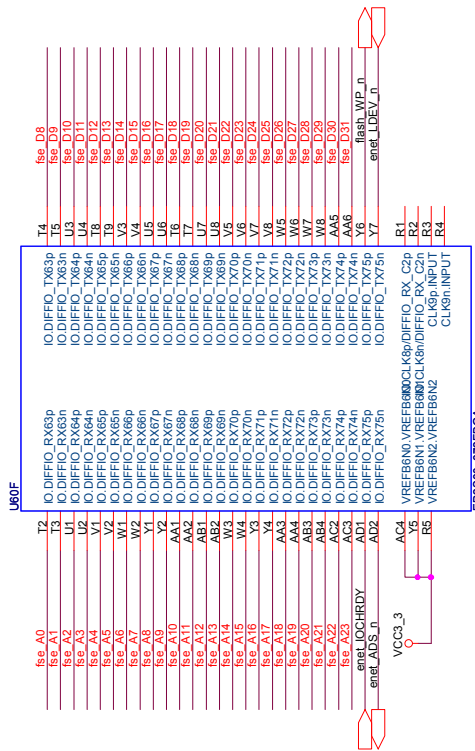
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EP2K10\_67FBGA

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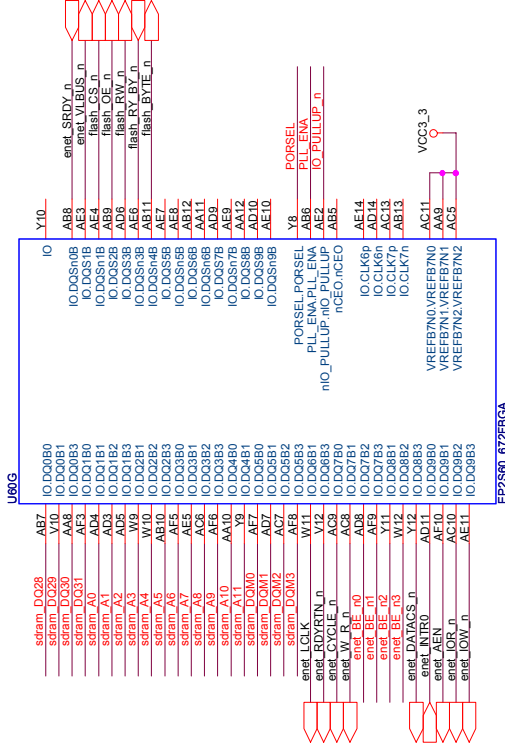
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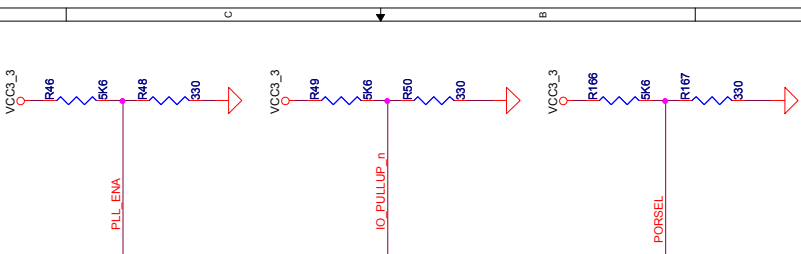
PLD Bank 7



Stuff R46 and not R48 Co enable PLL's.

Stuff R50 and not R49 to enable weak pull up resistors on the configuration pins.

Stuff R167 and not R166 to select the 100m wait after power up.



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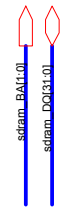
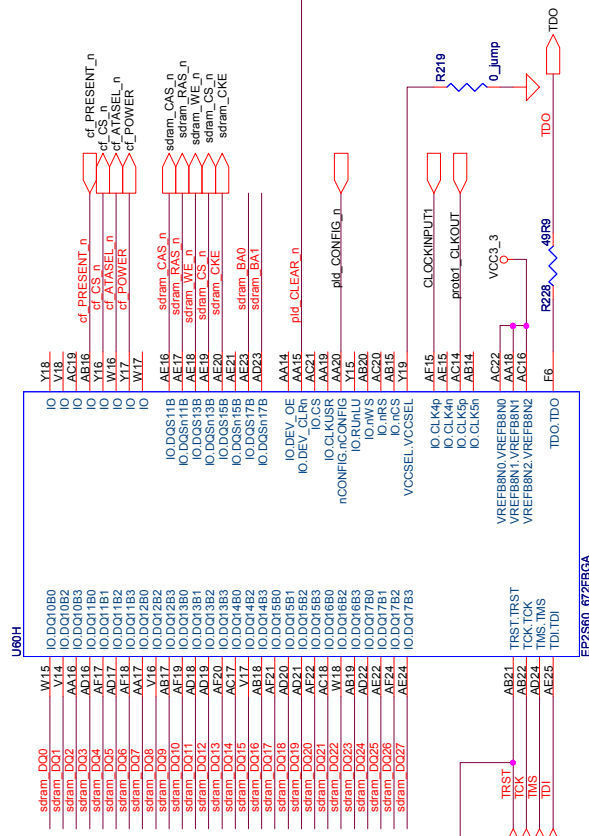
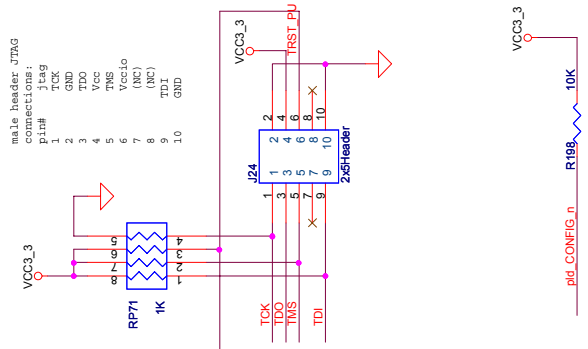
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male header JTAG connections:  
 pin# Jtag  
 1 TRST  
 2 TCK  
 3 TMS  
 4 TDI  
 5 Vcc  
 6 Vccio  
 7 (NC)  
 8 (NC)  
 9 TDI  
 10 GND

Do not stuff  
 R202 normally

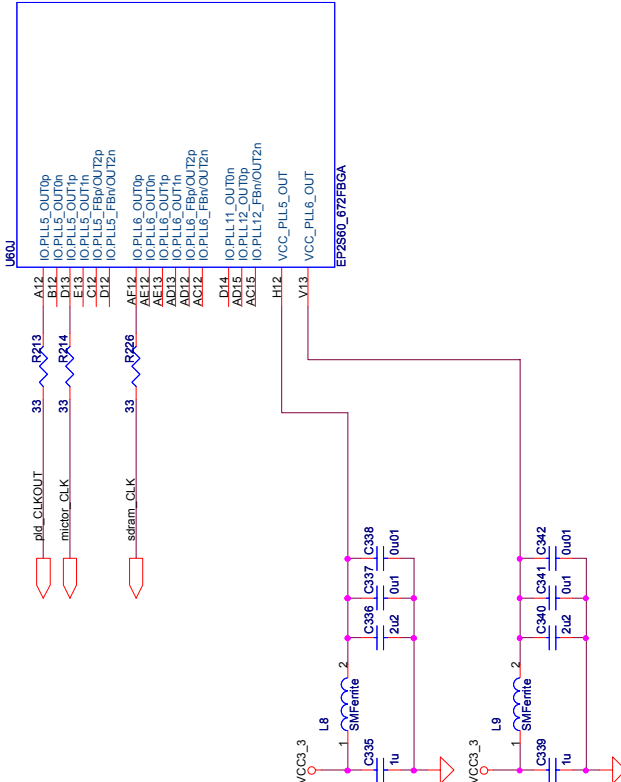
Label this button very  
 clearly with the  
 words "CPU RESET" and  
 put a box around the  
 button and text.



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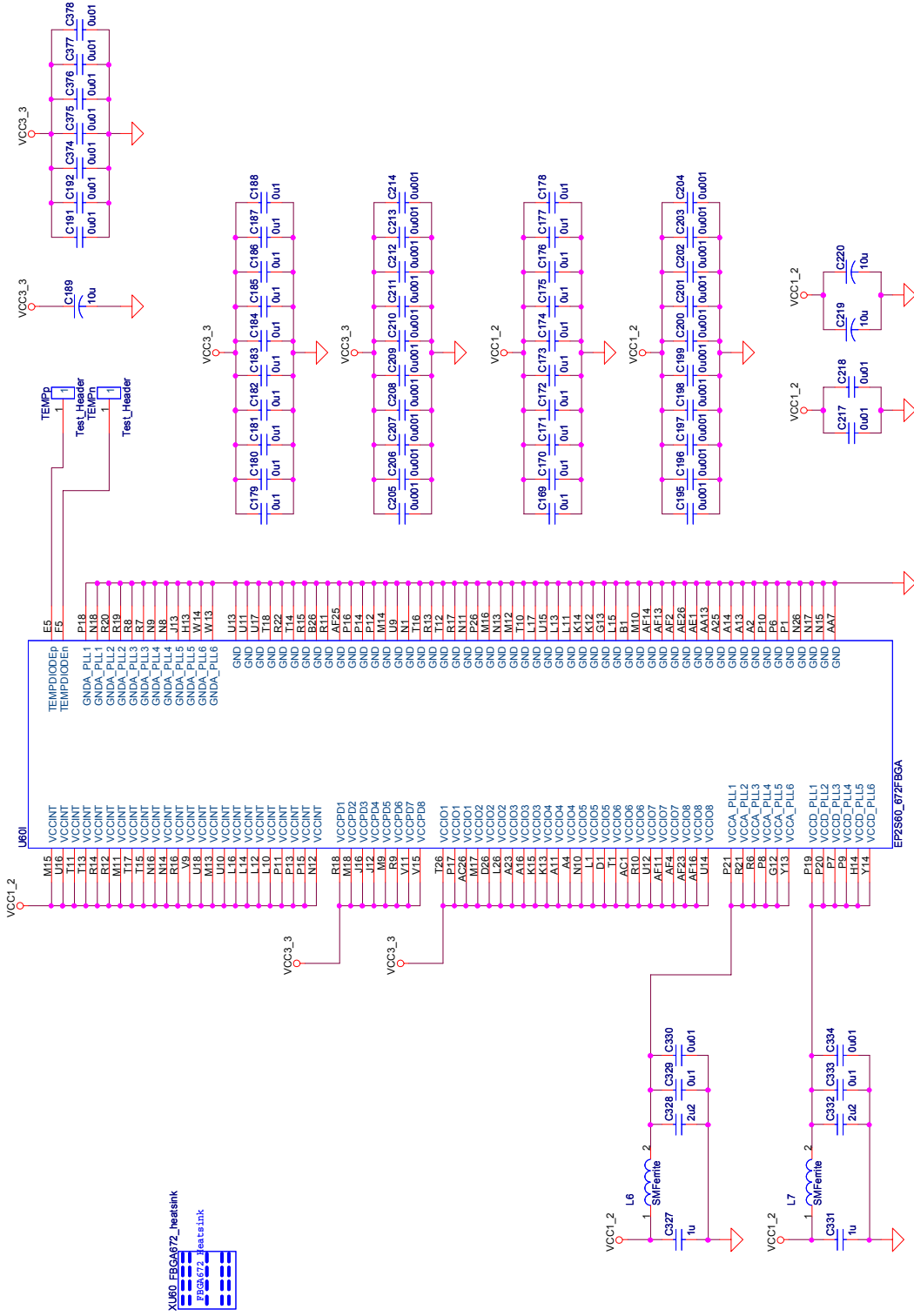
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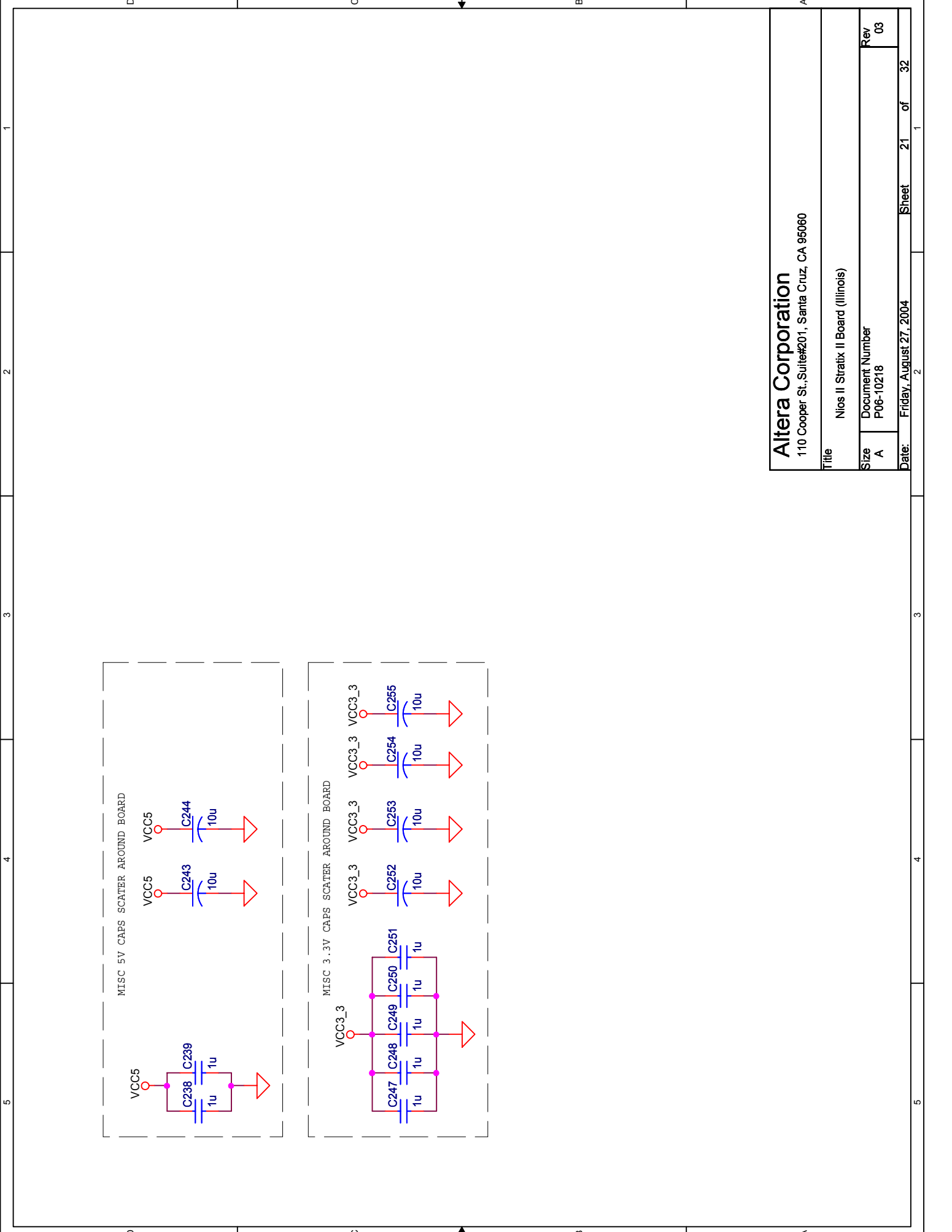
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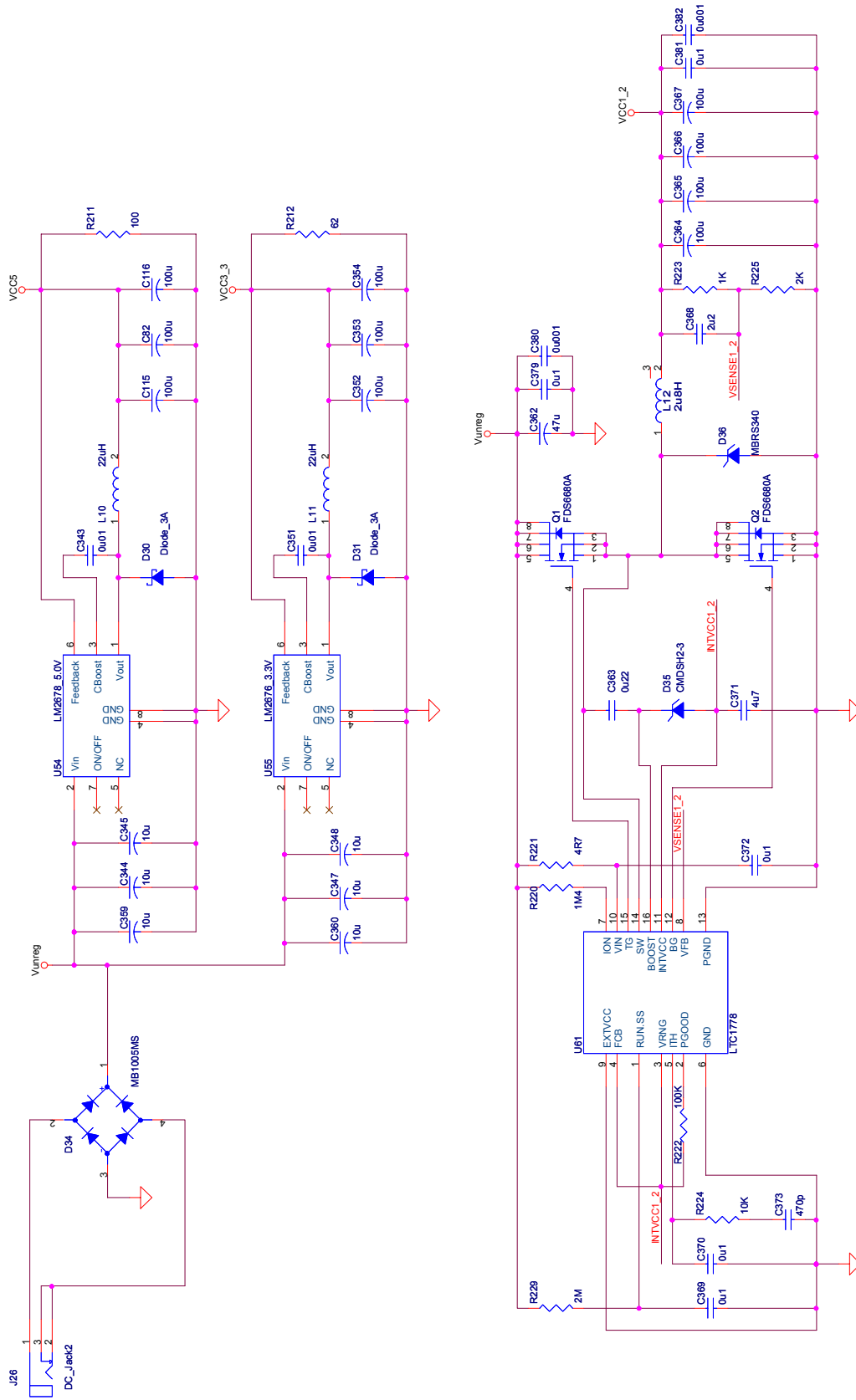
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Power Connector



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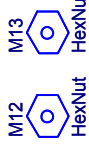
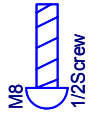
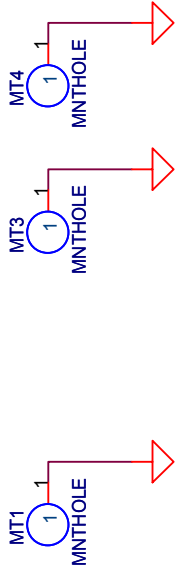
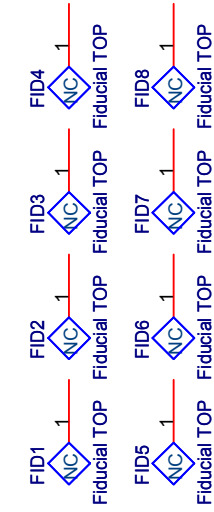
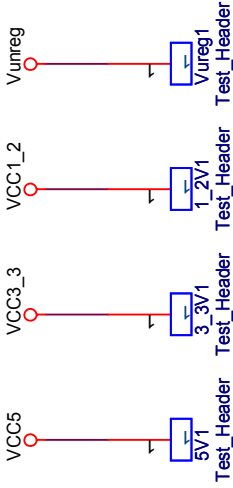
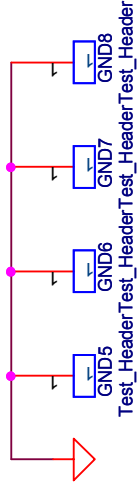
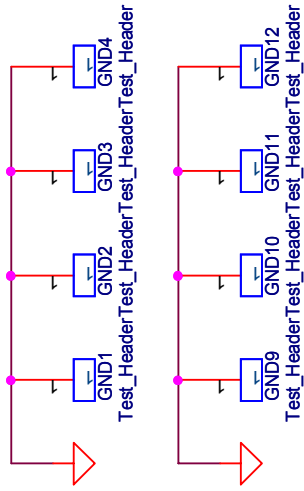
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# Reset and Test headers



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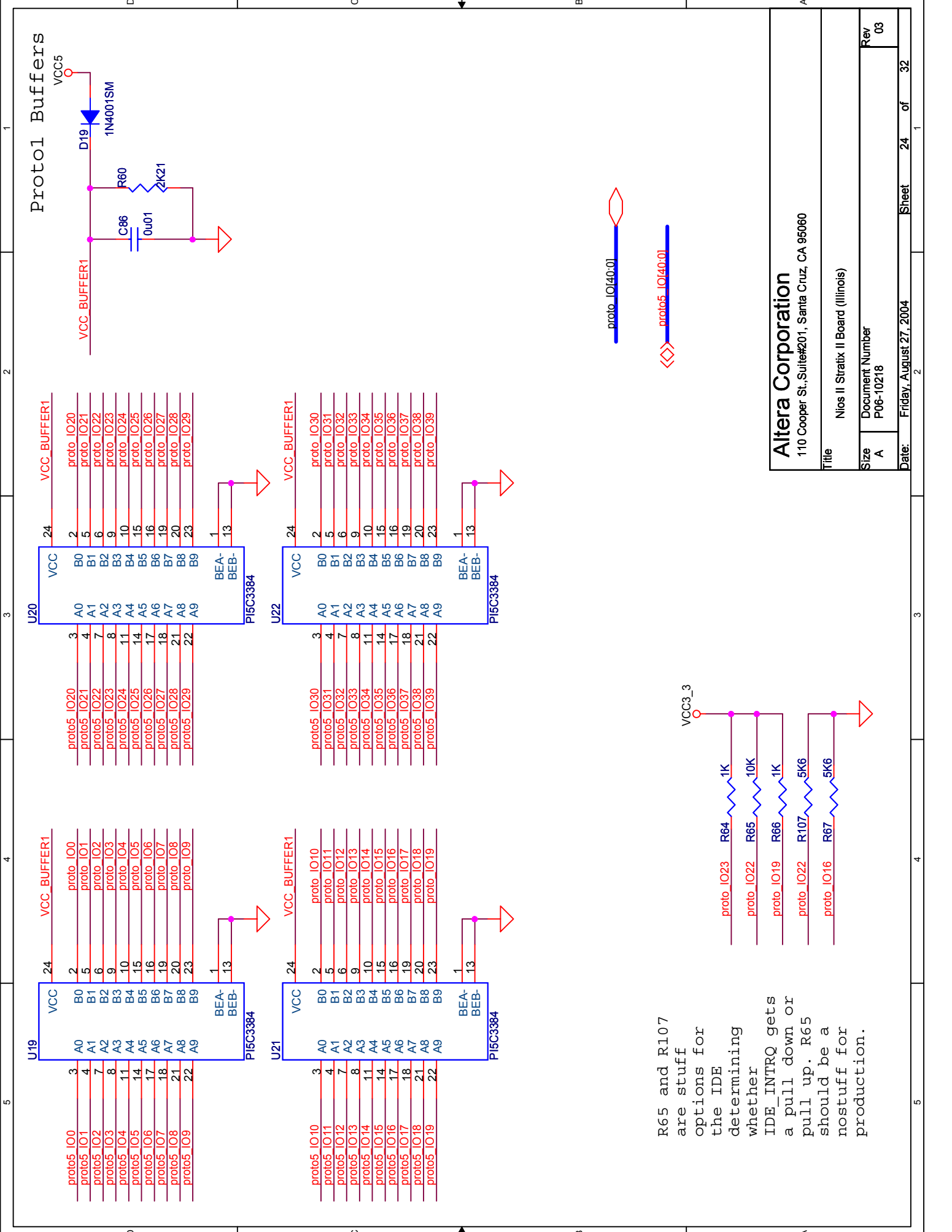
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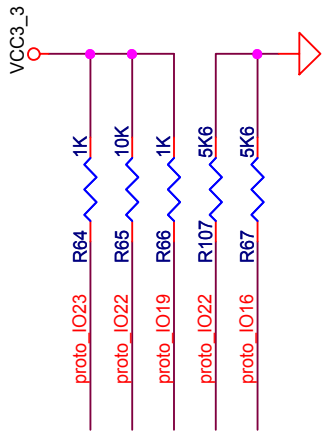
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R65 and R107 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R65 should be a nostuff for production.



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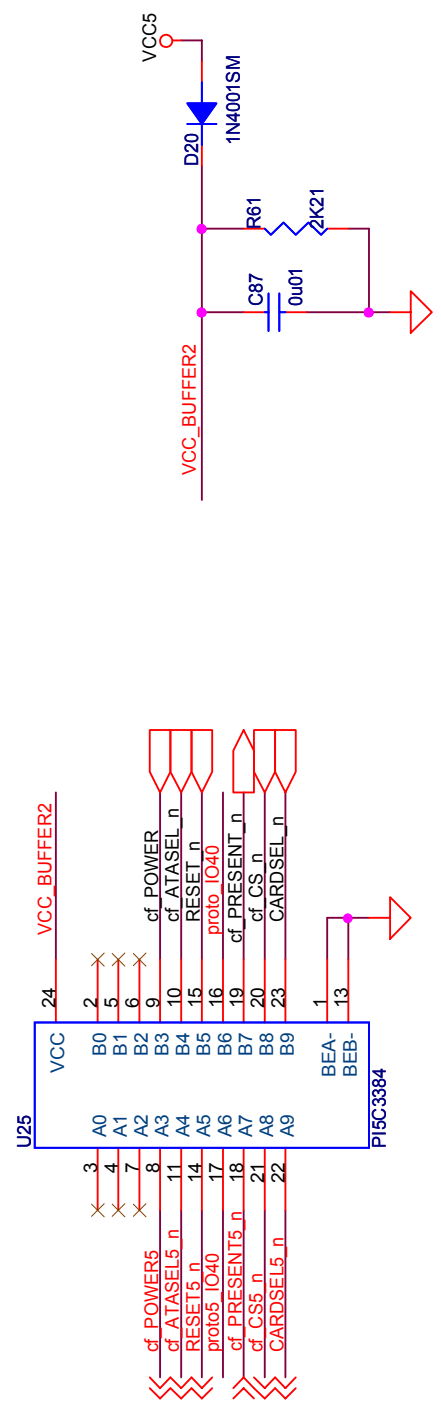
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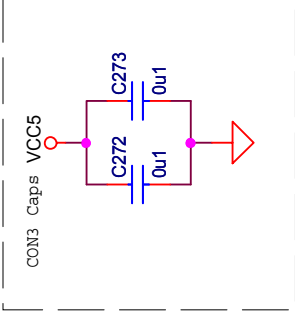
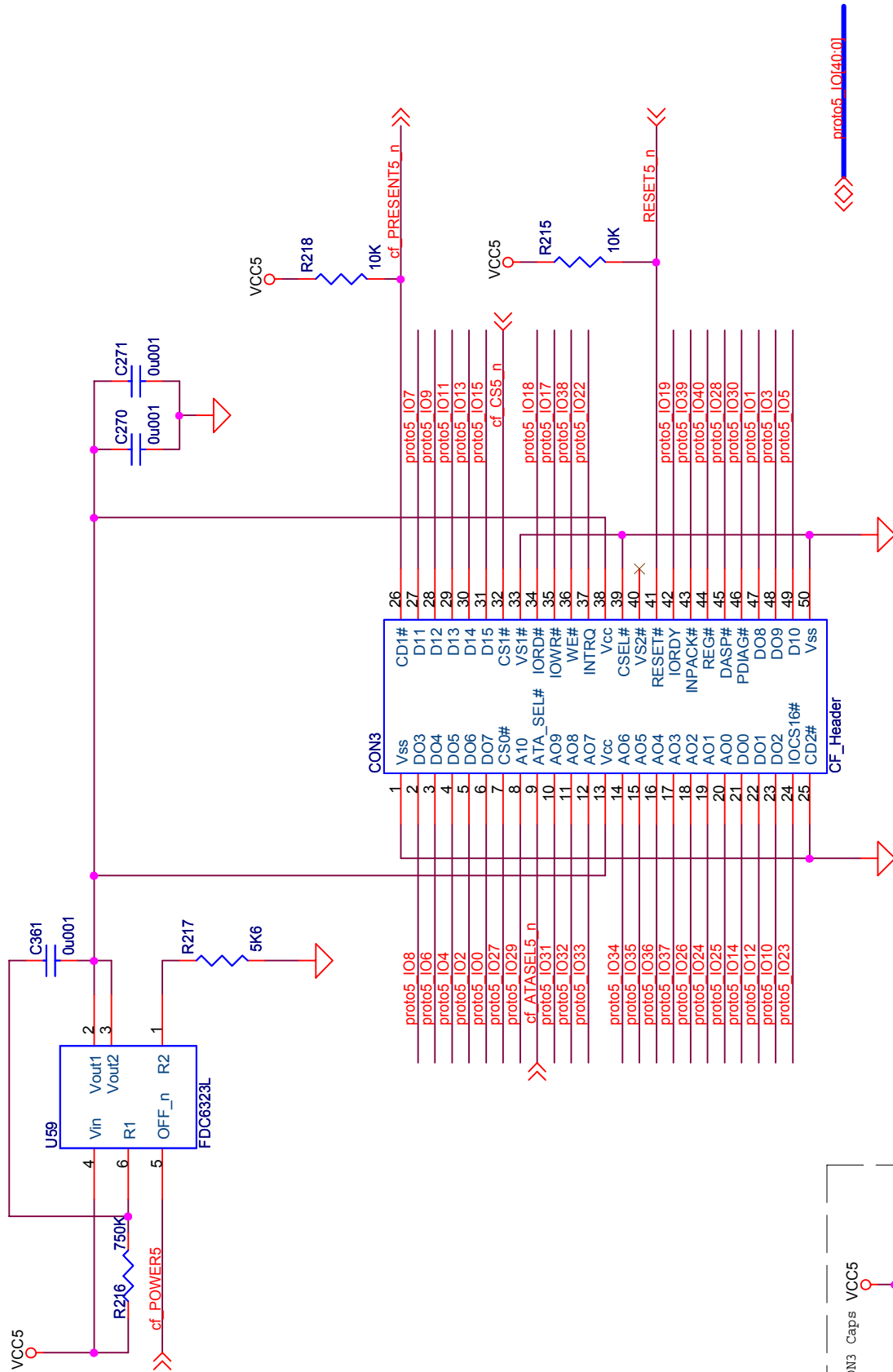
Proto1 Buffers



proto5\_IO[40:0]      proto\_IO[40:0]

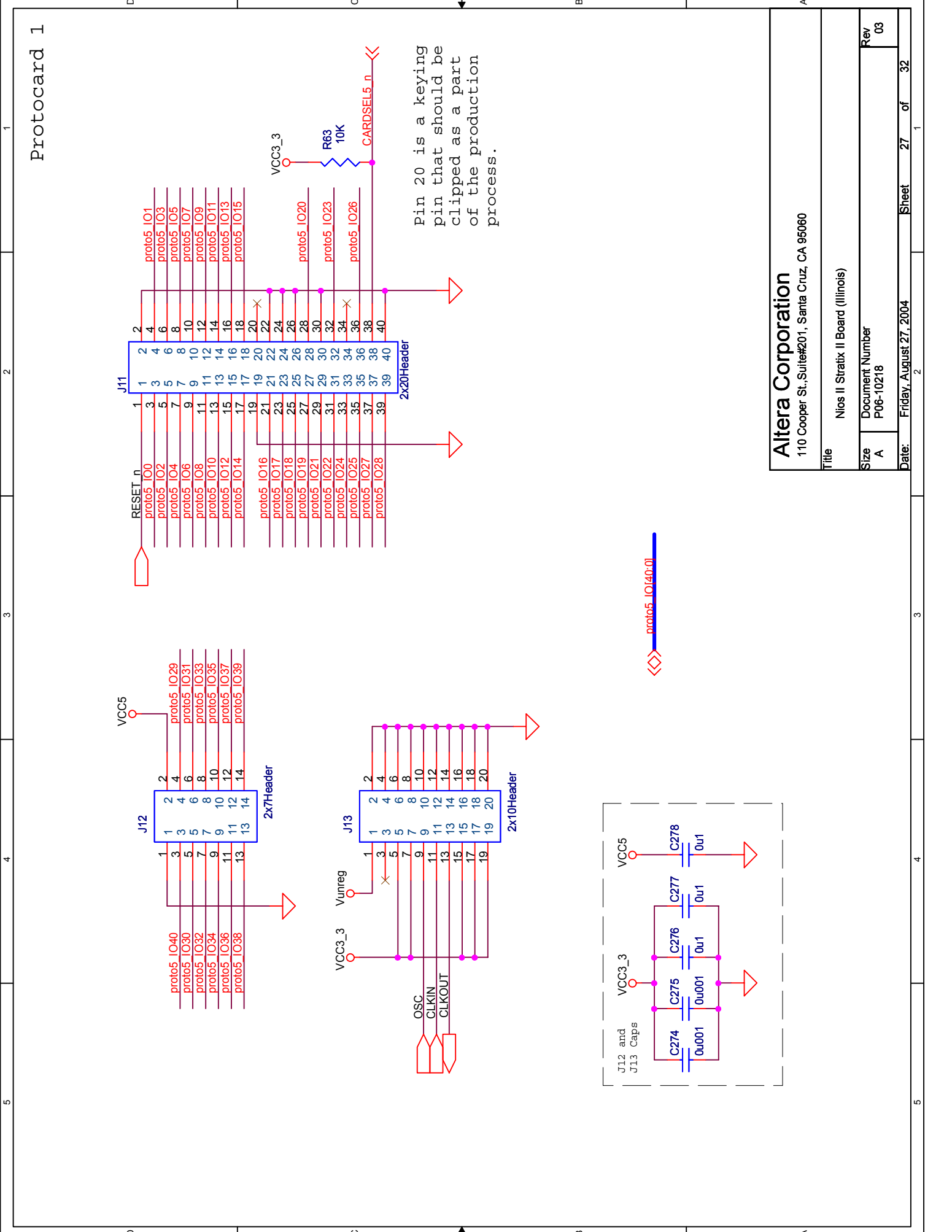
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# Compag Flash Socket



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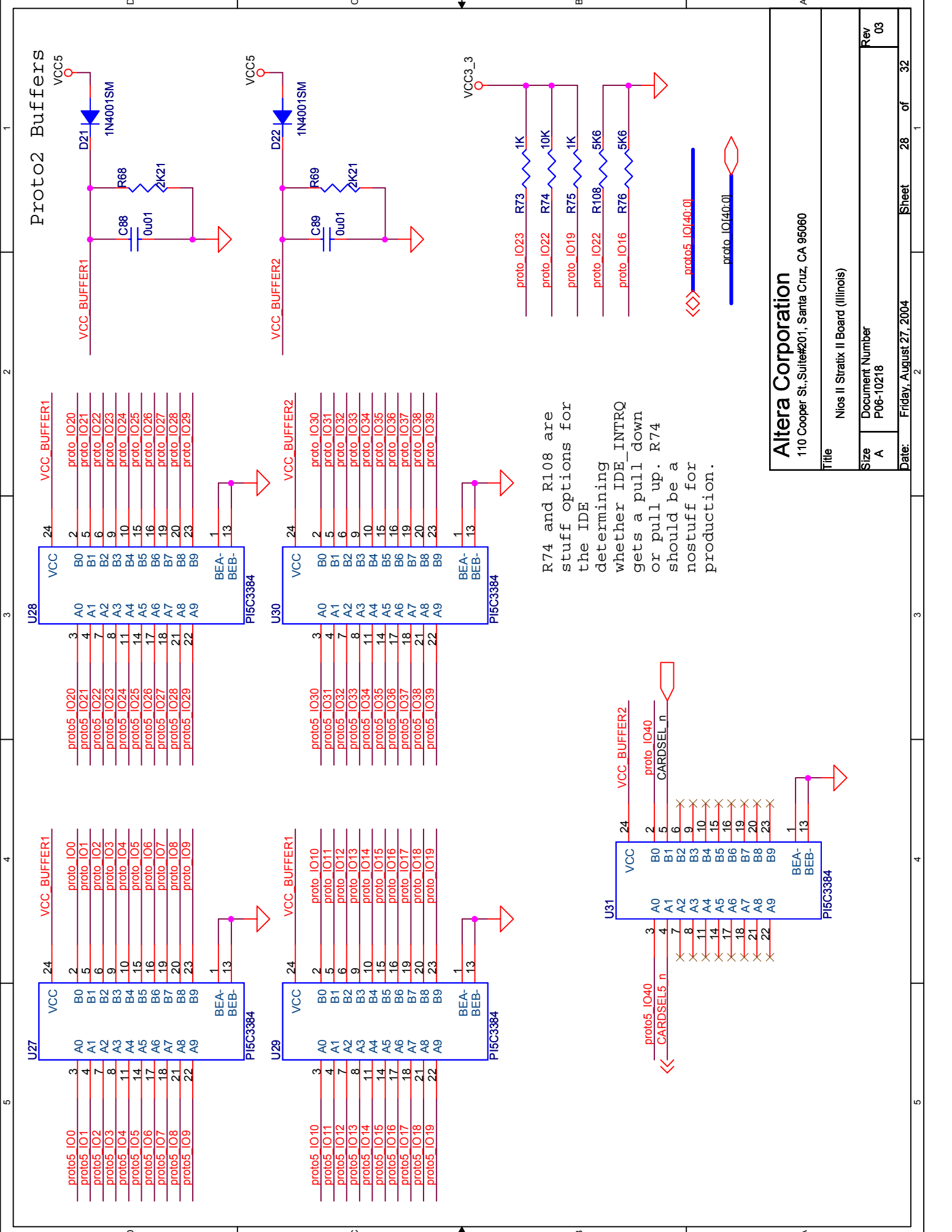


# Protocard 1

Pin 20 is a keying pin that should be clipped as a part of the production process.

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R74 and R108 are stuff options for the IDE determining whether IDE\_INTRQ gets a pull down or pull up. R74 should be a nostuff for production.

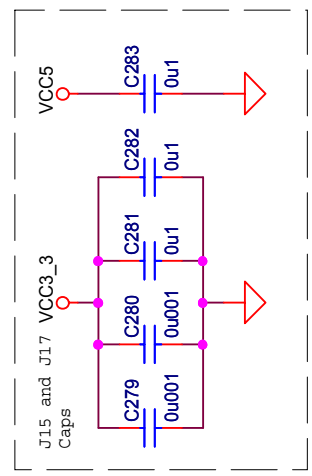
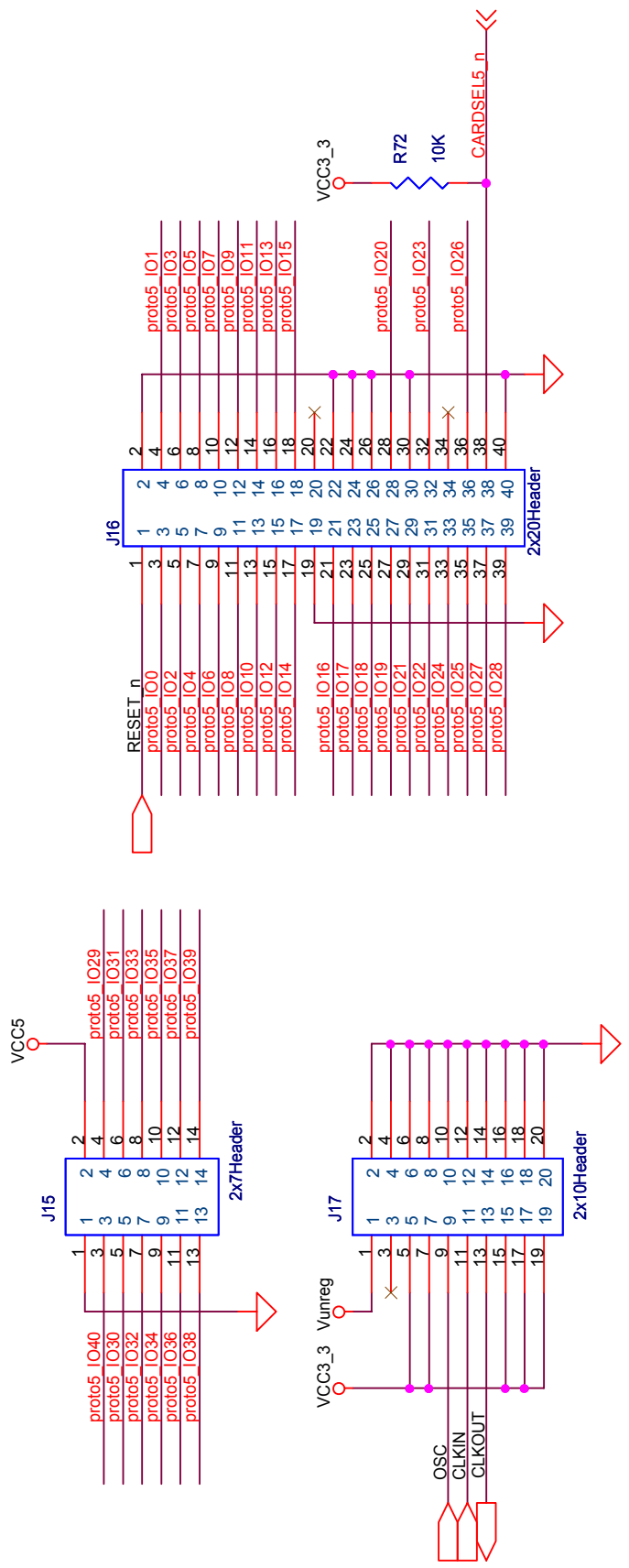
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# Proto2 Headers

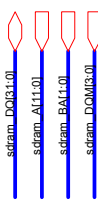
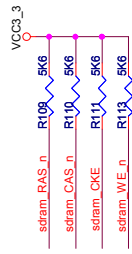
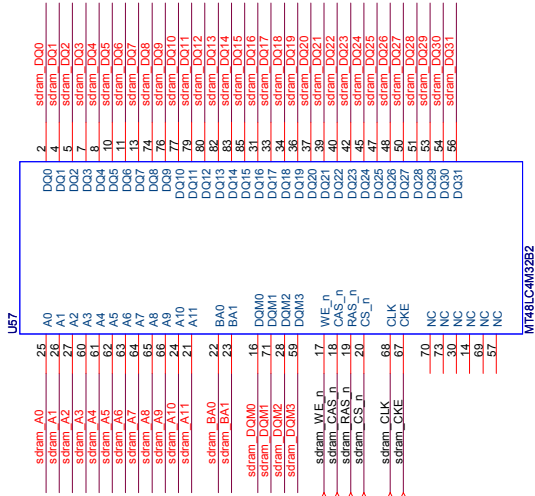
Pin 20 is a keying pin that should be clipped as a part of the production process.

proto5\_IO140\_01



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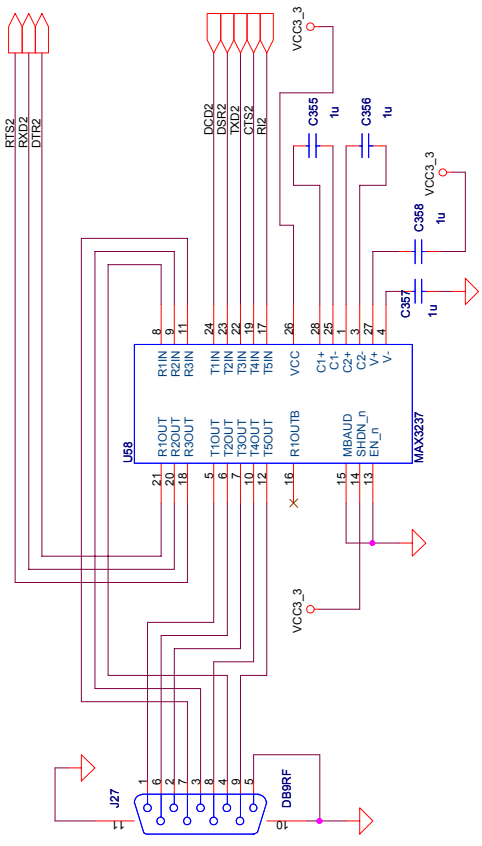
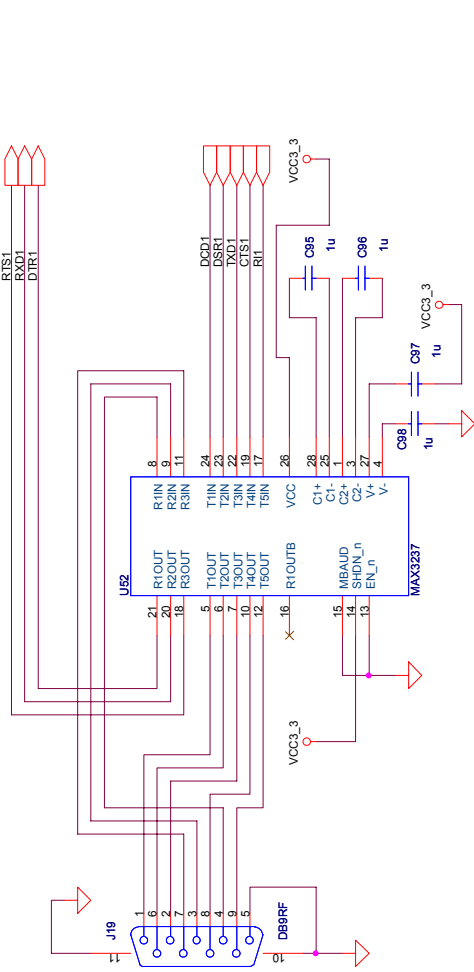
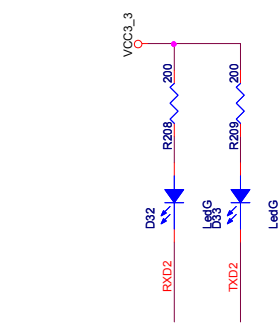
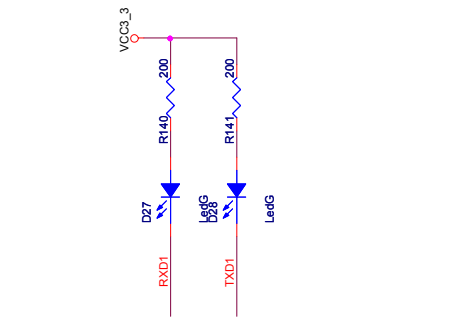
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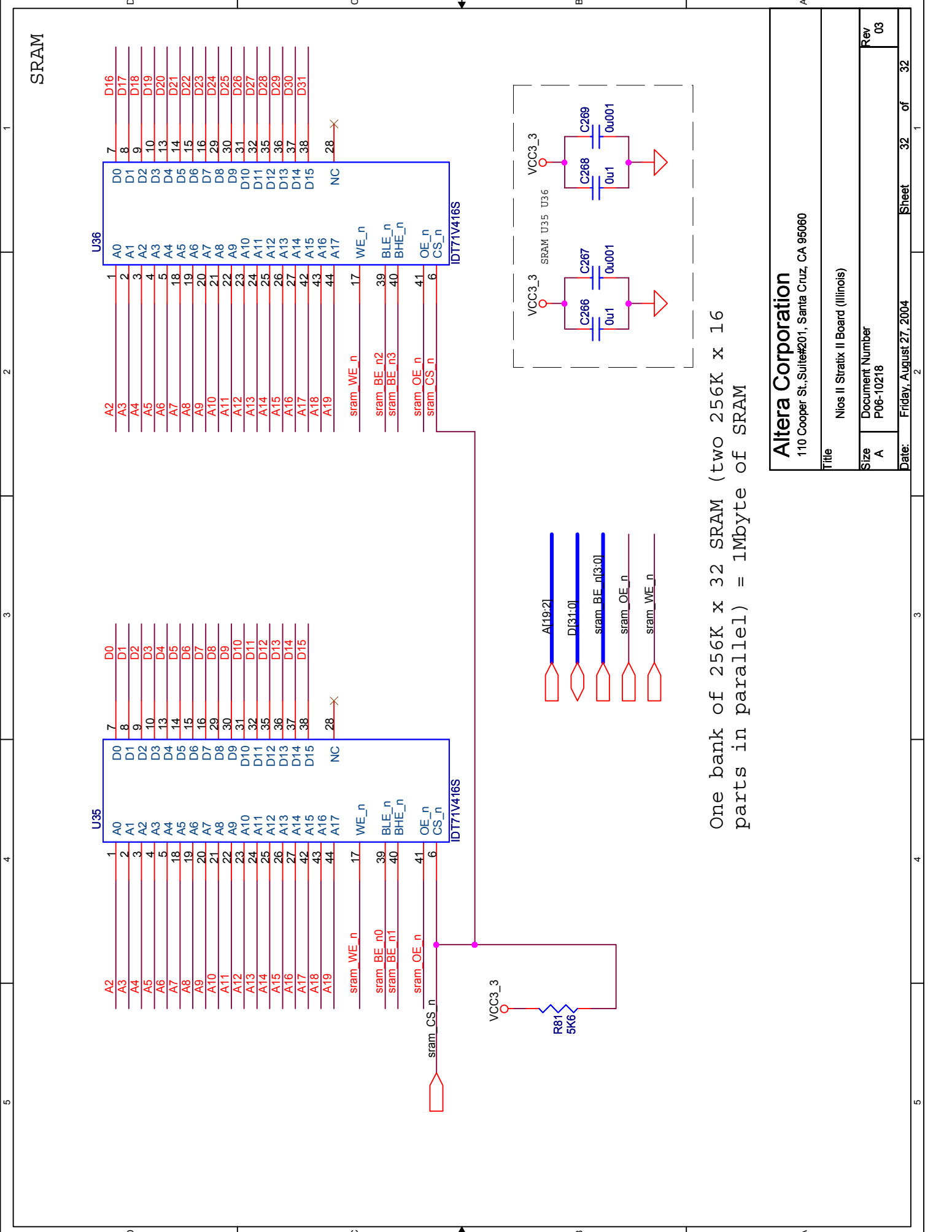
Serial Ports



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One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

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