News & Views
First Quarter, February 2000
Newsletter for Altera Customers

Altera Provides World-Class HDL Synthesis & Simulation Tools

Altera has entered into agreements with Synopsys, Inc., and Mentor Graphics Corporation that enable Altera's entire customer base to access premier programmable logic development tools. Under terms of the agreements, Altera® customers receive a full-featured version of either Synopsys' FPGA *Express*™ software or Mentor Graphics' LeonardoSpectrum™ software, and Mentor Graphic's Model*Sim*™ simulation software with their Altera software subscriptions. These third-party tools are included at no additional charge to the standard software subscription price. Now, Altera customers have access to a leading hardware description language (HDL) simulator and a choice of two performance-enhancing synthesis tools.

These agreements allow Altera to provide all active subscribers with world-class synthesis tools and enhanced behavioral simulation tools, continuing Altera's goal to deliver optimal performance and an enhanced design methodology through third-party software. With the release of the Quartus™ development system in 1999, Altera offered NativeLink™ functionality to link third-party synthesis and simulation with Quartus fitting and compilation algorithms; this integration provides efficient performance optimization and faster debugging.

Better synthesis directly equates to better performance. Altera designers now have a choice of either Synopsys' FPGA *Express* or Mentor Graphics' LeonardoSpectrum for synthesis. FPGA *Express* is a powerful VHDL and Verilog HDL synthesis tool with a simple, push-button user interface designed for high-density programmable logic. LeonardoSpectrum combines a push-button interface with the powerful control and optimization features associated with workstation-based ASIC tools.

As designers use programmable logic devices (PLDs) with increasing density, behavioral simulation tools become more important. Altera now provides the Model*Sim* behavioral simulation tool to complement the existing timing simulation tools in the Quartus and MAX+PLUS® II development systems. Designers can easily adopt a system-on-a-programmable-chip (SOPC) design methodology using Model*Sim* features such as behavioral simulation capability, test bench support, and Tcl scripting functionality.

The agreements with Synopsys and Mentor Graphics provide a cost-effective opportunity for Altera customers to use world-class synthesis and simulation tools. These third-party tools are included with each Altera software subscription; designers with current subscriptions will receive these third-party tools with a future Quartus and MAX+PLUS II upgrade. For more information on this offer, or to purchase an Altera software subscription, contact your Altera sales representative. North American customers can also purchase subscriptions from the Programmable eStore on the Altera web site (**http://www.altera.com**).

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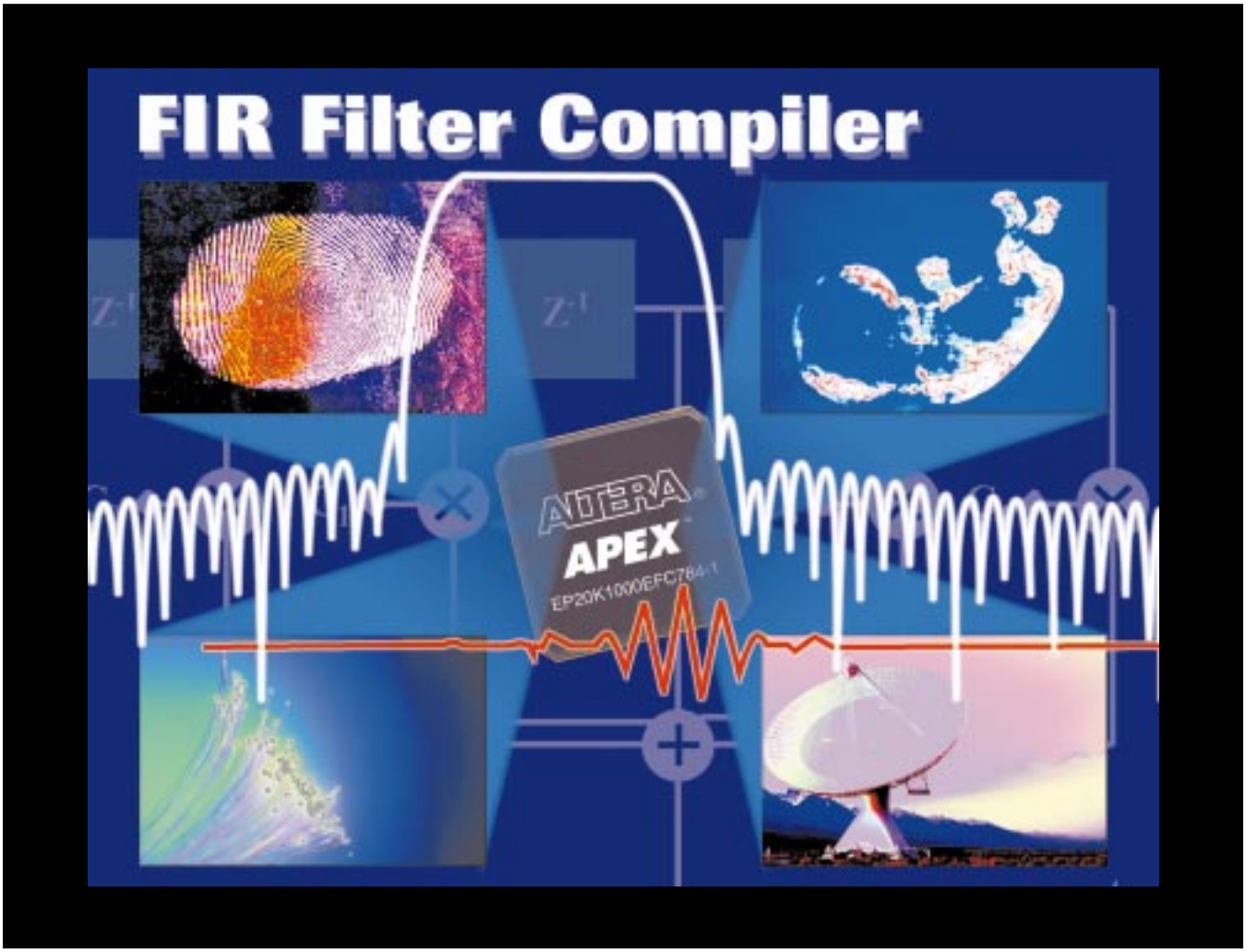
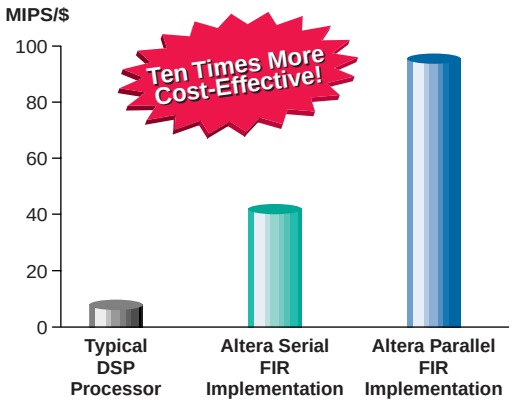
Inside This Issue:



Using Programmable Logic for DSP Solutions Saves Time,

The Altera® Finite Impulse Response (FIR) Compiler MegaCore™ function reduces the design time of your high-performance FIR filters from **six weeks to less than one day**.



This benchmark is for a symmetric FIR filter (50 taps, 8-bit data, 12-bit coefficient resolution) targeting an Altera EP20K100 APEX™ device and a TI TMS320C54x (50 MHz) DSP processor.

Reduces Cost,

Using the FIR Compiler is ten times more cost-effective than using a standard DSP processor.

and Makes the Job Easier!

This flexible, easy-to-use graphical compiler allows you to specify the data width, data type, number of taps, and the interpolation or decimation factor you need for your design. It supports third-party system-level DSP tools such as MATLAB or Simulink, and simulation tools such as VHDL and Verilog HDL.

Test-Drive the Altera FIR Filter Compiler for Free

You can test-drive the Altera FIR Compiler for free by downloading it from the IP MegaStore™ site at **http://www.altera.com/IPmegastore**. Discover for yourself how easily you can reduce your design time and cut your design costs.

ALTERA®

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Table of *Contents*

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System-on-a-Programmable-Chip Development Board Speeds Verification

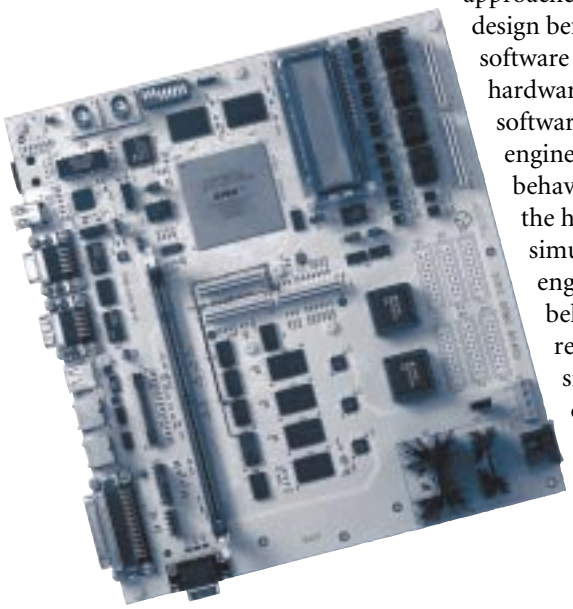
The System-on-a-Programmable-Chip Development Board supports many different applications by incorporating PMCs (allowing daughter-card expansion), programmable logic, memory, debug facilities, and several different interface resources.

As system-on-a-programmable-chip designs gain broad acceptance, the need for cost-effective, efficient design verification and implementation increases. The established methods of software-based simulation and hardware emulation are extremely time-consuming and pose significant limitations such as high cost and low performance in system-level verification. Because of these limitations, designers must find alternative approaches to these verification dilemmas. The most common verification approach is to develop a custom-prototyping board, which could cost tens of thousands of dollars and take many months to create.

The ideal verification environment can run system software on a hardware platform in real time. Altera's new System-on-a-Programmable-Chip Development Board helps to move products through the design cycle quickly by providing a more effective alternative to the traditional system verification using expensive hardware-emulation systems.

The Past

Before the System-on-a-Programmable-Chip Development Board, there were only two approaches for verifying your design before manufacturing: software simulation and hardware emulation. In software simulation, an engineer implements a behavioral model to simulate the hardware. If the simulation reveals a bug, the engineer must correct the behavioral model and resimulate. However, simulation is time-consuming and lacks the real-world accuracy necessary for comprehensive system verification. Verifying a design in a software simulator is more time-consuming than running the design in the actual hardware. For example, a complex design may require several days of software simulation to get final results. Even if a design runs in a simulator without errors, it may, in fact, have functional or timing bugs when the real hardware is implemented and presented with unexpected conditions. This process results in another time-consuming design iteration cycle.



The second approach to design verification is hardware emulation. However, significant drawbacks hinder this approach as well. The emulation system is expensive; a box with a capacity of only 500,000 gates can cost as much as $400,000. A typical emulation box can only run at hundreds-of-kHz speeds—much slower than actual device speeds. Additionally, emulation boxes only provide a hardware model to test your design. You can often encounter additional problems once you implement the design and operate the system software and hardware in a real-time environment.

The Present

The Altera® System-on-a-Programmable-Chip Development Board offers a more accurate and economical solution to design development and verification. The System-on-a-Programmable-Chip Development Board supports many different applications by incorporating programmable logic, memory, debug facilities, numerous interface resources, and peripheral component interconnect (PCI) mezzanine cards (PMCs) allowing daughter-card expansion. The board is designed to operate at high speeds, providing accurate, real-time testing results that reduce design verification time and increase overall design productivity.

The System-on-a-Programmable-Chip Development Board is designed for the integration and debugging of intellectual property (IP) functions from multiple sources, including Altera MegaCore™ functions, Altera Megafunction Partners Program (AMPP℠)

functions, and custom-designed IP, without the burden of having to develop a custom hardware platform.

The System-on-a-Programmable-Chip Development Board offers unmatched flexibility and user-customization opportunities. The board includes an EP20K400E programmable logic device (PLD) with 16,640 logic elements (LEs) and over 400,000 gates.

The memory subsystem on the board includes:

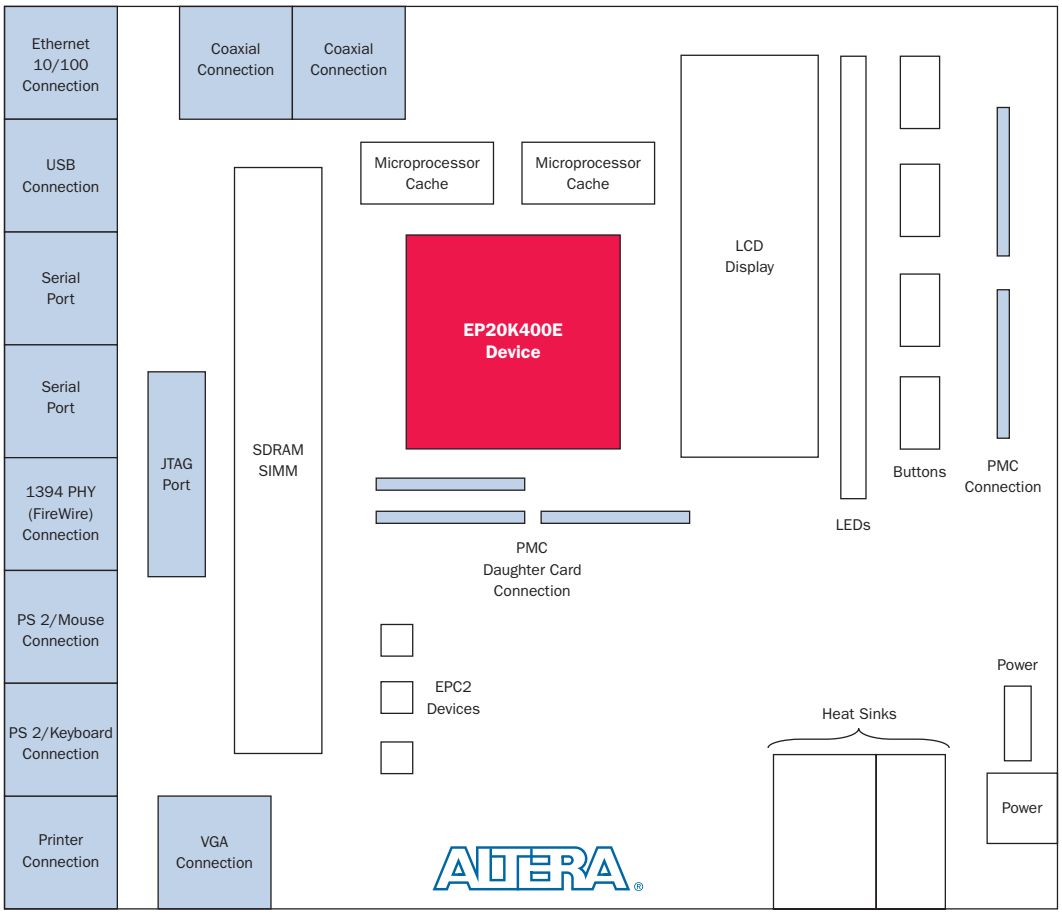
- Two banks of 1-Mbyte cache memory
- 64-Mbyte SDRAM in a DIMM socket
- 4-Mbyte FLASH memory
- 256-Kbyte EPROM

Figure 2 on page 6 shows a diagram of the System-on-a-Programmable-Chip Development Board.

To accommodate a wide variety of embedded applications, the board provides a robust set of I/O standards, such as IEEE Std. 1394a, IEEE Std. 1284, RS-232 DTE, 10/100 fast ethernet, and universal serial bus (USB) host. These standards allow design engineers to select the appropriate resources required to verify their application-specific IP. Additionally, the board features many debugging capabilities, including extended Joint Test Action Group (EJTAG), IEEE Std. 1149.1 JTAG, USB, and parallel port connections for accessing the on-board PLD. The APEX™ EP20K400E device included with the board supports in-circuit reconfigurability (ICR) through the MasterBlaster™ communications cable (included with the board) or EPC2 configuration devices, allowing you to repeatedly modify and verify your design.

With all of the resources on the System-on-a-Programmable-Chip Development Board, you

Figure 2. System-on-a-Programmable-Chip Development Board

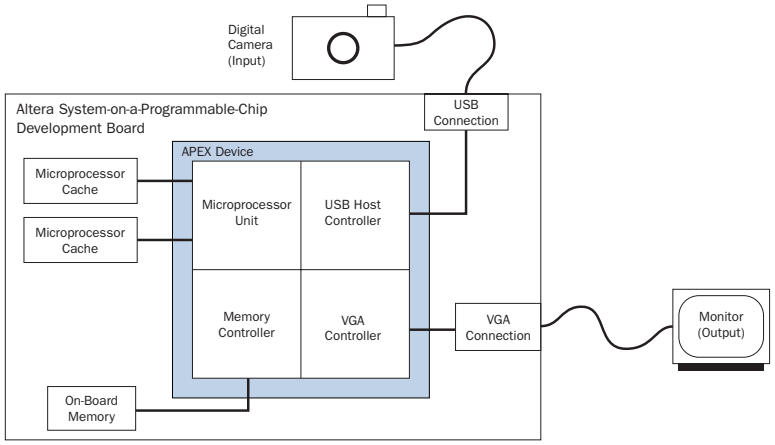


continued on page 6

System-on-a-Programmable-Chip Development Board Speeds Verification, continued from page 5

can implement a limitless number of designs. For example, by connecting a digital camera to the USB port and a VGA monitor to the VGA port, you have a digital display (see Figure 3). To utilize these I/O ports, you could implement a USB host controller, a processor, and a VGA controller within the EP20K400E device. A memory controller is also necessary to store the images in the SDRAM memory included on the board.

Figure 3. Digital Display Example



The speed of the APEX device is sufficient for the USB host controller (~48 MHz) and the processor function (~33 MHz). The approximate LE consumption for the necessary functions is shown in Table 1. The total LE consumption is approximately 9,300, which is far less than the 16,640 LEs available on the APEX device.

Table 1. Approximate APEX LE Consumption

Core	Approximate LE Consumption	% of Total LEs
Microprocessor	4,000	24
USB Host Controller	3,000	18
Memory Controller	2,000	12
VGA Controller	300	2
Total	9,300	56

With the complexity of larger designs, engineers need a way to view specific test points of their design within the device. Using the SignalTap™ embedded logic analyzer, a feature of the Quartus™ development system, an engineer can closely examine signals from internal nodes within the APEX device. The SignalTap logic analyzer is especially useful for today's ball-grid array (BGA) packages where pin access is limited by the package design. The SignalTap user decides how many internal signals to view and can filter out extraneous information to view only problematic circuitry.

The APEX device also supports many Altera MegaCore functions and AMPP megafunctions. You can use these off-the-shelf megafunctions together with the System-on-a-Programmable-Chip Development Board to bring your product to market quickly. OpenCore™ versions of MegaCore functions and AMPP megafunctions are available for testing.

The Future

As costs decrease and PLD speeds and density increase, many new applications will abandon ASICs and adopt programmable logic. The System-on-a-Programmable-Chip Development Board is designed to accommodate these trends through its capability to be upgraded to higher density APEX devices in the same 652-pin BGA package, including EP20K1500E devices with over 50,000 LEs.

Altera and AMPP partners are designing daughter cards for the board's PMC slots. These daughter cards will supplement the board by increasing its functionality and memory capacity. For example, if your application needs analog capability for a digital signal processing (DSP)-based system, you could easily add this functionality to the System-on-a-Programmable-Chip Development Board via an analog PMC daughter card. For microprocessor designs, the CPU could be included in the system, implemented in the form of an IP function ported to the PLD, or implemented as a PMC processor card.

Altera created the System-on-a-Programmable-Chip Development Board with the flexibility to accommodate a multitude of designs for many application areas. With the board's high-density programmable logic, breadth of I/O standards, and available on-board memory, the System-on-a-Programmable-Chip Development Board is a productive and cost-effective way to develop, integrate, and verify your complex system-on-a-programmable-chip designs.

APEX

More APEX 20KE Devices Now Available

New APEX™ 20KE package and speed grade offerings for EP20K100E, EP20K200E, EP20K400E, and EP20K600E devices are now available. The EP20K400E and EP20K600E devices include embedded circuitry supporting multiple low-voltage differential signaling (LVDS) channels with bandwidth of up to 622 megabits per second (Mbps) each. The remaining APEX 20KE devices are scheduled to ship soon. Software support is currently available for EP20K60E, EP20K100E, EP20K200E, EP20K300E, EP20K400E, EP20K600E, and EP20K1000E devices in the Quartus™ software version 2000.02 (see Table 1).

New APEX Family Member

Altera has added a new, low-cost, high-performance APEX 20KE device. The 30,000-gate EP20K30E device contains 1,200 logic elements (LEs) and 24,576 bits of on-chip RAM. Quartus software support will be available in the second quarter of 2000.

5.0-V Tolerant APEX 20K Devices

The APEX 20K device family has been enhanced to provide 5.0-V tolerant I/O buffers, allowing full compliance with the 5.0-V peripheral component interconnect (PCI) specification. These devices will begin shipping in March 2000.

1,020-Pin FineLine BGA Packages

EP20K600E, EP20K1000E, and EP20K1500E devices will be available in a 1,020-pin FineLine BGA™ package, providing up to 808 I/O pins. These devices will use an FC33 designation in the ordering code, which is based on the 33-mm body size rather than the 1,020 pin count. For example, the ordering code for an EP20K1000E device with phase-locked loop (PLL) circuitry in this package is EP20K1000EFC33-1X.

Table 1. APEX 20KE Device & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K30E	144-pin TQFP	Q2 2000
	144-pin FineLine BGA	Q2 2000
	208-pin PQFP	Q2 2000
	324-pin FineLine BGA	Q2 2000
EP20K60E	144-pin TQFP *(1)*	Now
	144-pin FineLine BGA	March 2000
	208-pin PQFP *(1)*	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA *(1)*	Now
EP20K100E	144-pin TQFP	Now
	144-pin FineLine BGA	March 2000
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	Now
EP20K160E	144-pin TQFP	March 2000
	208-pin PQFP	March 2000
	240-pin PQFP	March 2000
	356-pin BGA	March 2000
	484-pin FineLine BGA	March 2000
EP20K200E	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K300E	240-pin RQFP *(1)*	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K400E	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	984-pin PGA *(1)*	Q2 2000
	1,020-pin FineLine BGA	Now
EP20K1500E	652-pin BGA	Q2 2000
	984-pin PGA	Q2 2000
	1,020-pin FineLine BGA	Q2 2000

Note:

(1) TQFP: thin quad flat pack, PQFP: plastic quad flat pack, BGA: ball-grid array, RQFP: power quad flat pack, PGA: pin-grid array.

continued on page 8

Devices & Tools, continued from page 7

APEX 20K Product Transition

Altera is migrating the 2.5-V EP20K400 device from a 0.25-µm process to a 0.22-µm process. Information regarding this device migration can be found in PCN 0005, available on the Altera® web site at **http://www.altera.com**.

APEX PLL Offerings

APEX devices with PLL circuitry are now shipping. These devices are identified with an "X" suffix in the ordering code (i.e., EP20K400EBC652-1X). The PLL feature is offered in all APEX device densities in both -1 and -2 speed grades. APEX PLLs contain enhanced ClockLock™ circuitry for skew reduction, ClockBoost™ circuitry for flexible rate multiplication and division, and ClockShift™ circuitry for phase-shift and delay capability. Additionally, you can use APEX 20KE PLLs for LVDS I/O interfaces to support high-speed data transfer rates and to convert LVDS and CMOS data.

ACEX

Interest Grows for Low-Cost ACEX Family

The new low-cost ACEX family has been expanded to include both 1.8-V and 2.5-V devices. These devices are designed for high-volume, price-sensitive communications and computing market applications.

The new low-cost ACEX™ family has been expanded to include both 1.8-V and 2.5-V devices. These devices are designed for high-volume, price-sensitive communications and computing market applications, including cable and xDSL modems, switches, and routers. ACEX devices are also used in remote-access concentrators, where high-volume production creates a strong sensitivity to cost-per-function, and complex communications processes require high performance capability and support for advanced features. ACEX devices meet these needs head-on with a low-cost, mid-range-density programmable solution.

The 2.5-V ACEX 1K offerings will be supported in the MAX+PLUS® II software version 9.51. These offerings will have devices ranging from 10,000 to 100,000 typical gates and have embedded memory for dual-port RAM, PLL support for clock management capabilities, and 64-bit, 66-MHz PCI compliance. ACEX 1K devices will be available in quad flat pack (QFP) and FineLine BGA packages.

Altera will also introduce 1.8-V ACEX 2K devices later this year. These devices combine the functionality of embedded memory with support for a large number of embedded RAM blocks. Support for a wide range of specialized I/O standards is also included in ACEX 2K devices. These advanced I/O standards provide high-speed board-level communication. Additionally, an embedded PLL includes ClockShift circuitry and can use a wide range of multiplication factors to drive two separate ClockLock- and ClockBoost-generated signals. Altera will offer ACEX 2K devices in QFP and FineLine BGA packages.

Quartus software support for ACEX 2K devices is scheduled to be available in the third quarter of 2000. For the latest information on ACEX devices, visit the Altera web site at **http://www.altera.com**.

FLEX

FLEX 10KE Devices Available in All Densities

FLEX® 10KE devices are now available in all densities. All EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices are fabricated on 0.22-µm die sizes. These devices, in all packages, are shipping in the -1, -2, and -3 speed grades and have a programmable delay to provide full 64-bit, 66-MHz PCI compliance.

FLEX 10KE Device Offerings

FLEX 10KE devices provide high-speed and high-density solutions for efficient designs. FLEX 10KE devices are offered with the PLL feature in -1 and -2 speed grades to reduce clock skew and allow clock multiplication. These devices have an "X" suffix in the ordering code (e.g., EPF10K100EQC208-1X). To assist designers in implementing their projects in FLEX 10KE devices, the MAX+PLUS II software offers design support for all device package options. Table 3 shows all of the 2.5-V FLEX 10KE device packages and speed grades.

Table 3. FLEX 10KE Devices

Device	Offerings	Speed Grade
EPF10K30E	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K50S	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K100E	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K130E	240-pin PQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K200S	240-pin RQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X

FLEX 10K Product Transitions

Altera is migrating 2.5-V EPF10K50E and EPF10K200E devices from a 0.25-µm process to a 0.22-µm process, and EPF10K50V devices from a 0.30-µm, 3-layer-metal process to a 0.30-µm, 4-layer-metal process. All other members of the FLEX 10KE family are already manufactured on a 0.22-µm process. Table 4 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com.**

Table 4. FLEX 10K Device Migration

Device	Core Voltage (V)	Date	Reference	Process (µm)
EPF10K10A	3.3	Done	PCN 9810	0.30
EPF10K30A	3.3	Done	PCN 9810	0.30
EPF10K50V	3.3	Done	PCN 9810	0.30 *(1)*
		June 2000	PCN 9915	0.30 *(2)*
EPF10K100A	3.3	Done	PCN 9810	0.30
EPF10K10	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K20	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K30	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50E	2.5	Feb. 2000	PCN 9911	0.22
EPF10K200E	2.5	Mar. 2000	PCN 9911	0.22

Notes:
(1) 3-layer metal process.
(2) 4-layer metal process.

FLEX 10KE devices provide high-speed and high-density solutions for efficient designs.

FLEX 10KE Industrial-Temperature Devices

EPF10K30EQI208-2, EPF10K30EFI256-2, EPF10K50SQI208-2, and EPF10K200SFI672-2 devices are now available. Additional EPF10K50S and EPF10K200S industrial-temperature grade devices are scheduled to ship soon. Table 5 on page 10 lists the availability of industrial-temperature FLEX 10KE devices.

continued on page 10

Devices & Tools, continued from page 9

Table 5. FLEX 10KE Industrial-Temperature Device Availability

Device	Availability
EPF10K30EQI208-2	Now
EPF10K30EFI256-2	Now
EPF10K50ETI144-2	Now
EPF10K50EQI240-2	Now
EPF10K50EFI256-2	Now
EPF10K50SQI208-2	Now
EPF10K50SBI356-2	April 2000
EPF10K50SFI484-2	April 2000
EPF10K100EQI208-2	Now
EPF10K100EFI256-2	Now
EPF10K100EFI484-2	Now
EPF10K130EQI240-2	Now
EPF10K130EBI356-2	Now
EPF10K130EFI484-2	Now
EPF10K200EBI600-2	Now
EPF10K200SRI240-2	April 2000
EPF10K200SBI356-2	March 2000
EPF10K200SFI672-2	Now

MAX®

MAX 7000B devices support advanced I/O standards such as GTL+, SSTL-2, and SSTL-3.

MAX 7000B Full-Featured Devices

2.5-V MAX® 7000B devices range from 32 to 512 macrocells with propagation delays as fast as 3.5 ns. MAX 7000B devices support advanced I/O standards such as Gunning transceiver logic plus (GTL+), stub-series terminated logic for 2.5 V (SSTL-2), and 3.3-V SSTL-3. These devices also feature enhanced in-system programmability (ISP), MultiVolt™ I/O pins, hot-socketing capability, and pin compatibility with industry-standard MAX 7000 devices. Table 6 shows all MAX 7000B commercial package and speed grade options.

MAX 7000A Devices Available Now

All MAX 7000A devices are now available. 3.3-V MAX 7000A devices range from 32 to 512 macrocells with propagation delays as fast as 4.5 ns. MAX 7000A devices support enhanced ISP, MultiVolt I/O pins, hot-socketing capability, and pin compatibility with the industry-standard MAX 7000 devices. All MAX 7000A devices are available in industrial-temperature grades. Table 7 shows MAX 7000A device commercial package and speed grade options.

Table 6. MAX 7000B Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032B	44-pin PLCC *(1)*	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
EPM7064B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA *(2)*	-3, -5, -7
	100-pin TQFP	-3, -5, -7
	100-pin FineLine BGA	-3, -5, -7
EPM7128B	49-pin Ultra FineLine BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
	144-pin TQFP	-4, -7, -10
	169-pin Ultra FineLine BGA	-4, -7, -10
	256-pin FineLine BGA	-4, -7, -10
EPM7256B	100-pin TQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512B	100-pin TQFP	-6, -7, -10
	144-pin TQFP	-6, -7, -10
	169-pin Ultra FineLine BGA	-6, -7, -10
	208-pin PQFP	-6, -7, -10
	256-pin BGA	-6, -7, -10
	256-pin FineLine BGA	-6, -7, -10

Notes:
(1) PLCC: plastic J-lead chip carrier.
(2) Ultra FineLine BGA packages are Altera's newest 0.8-mm BGA packages.

MAX 7000S Devices

All MAX 7000S devices are now available. 5.0-V MAX 7000S devices offer features such as 5.0-ns speed grades, ISP, an open-drain output option, and IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in industrial-

temperature grades. Table 8 shows the packages and speed grades available in the commercial-temperature grade.

Table 7. MAX 7000AE Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM7064AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	49-pin Ultra FineLine BGA *(1)*	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
EPM7128AE	84-pin PLCC	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	100-pin PQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7256AE	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512AE	144-pin TQFP	-7, -10, -12
	208-pin PQFP	-7, -10, -12
	256-pin BGA	-7, -10, -12
	256-pin FineLine BGA	-7, -10, -12

Note:
(1) Ultra FineLine BGA packages are Altera's newest 0.8-mm BGA packages.

Table 8. Commercial-Temperature MAX 7000S Devices

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

Low-Cost MAX 3000A Devices

3.3-V MAX 3000A devices are product-term-based programmable logic devices (PLDs) targeted for high-volume, low-cost designs. These devices have an enhanced ISP feature set and range in density from 32 to 256 macrocells (see Table 9). With propagation delays as fast as 4.5 ns, MAX 3000A devices provide exceptional performance at the lowest price per macrocell among Altera MAX devices.

With propagation delays as fast as 4.5 ns, MAX 3000A devices provide exceptional performance at the lowest price per macrocell among Altera MAX devices.

Table 9. MAX 3000A Devices

Device	Package	Speed Grade
EPM3032A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM3064A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	100-pin TQFP	-4, -7, -10
EPM3128A	100-pin TQFP	-5, -7, -10
	144-pin PQFP	-5, -7, -10
EPM3256A	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10

CONFIGURATION

4-Mbit Configuration Device Coming Soon

The new 4-Mbit EPC4E configuration device is scheduled for release in May 2000. This device will be offered in a 44-pin TQFP package as well as a 0.8-mm, 84-pin Ultra FineLine BGA package. A new 9-Mbit EPC9E configuration device is also being developed and is slated for release in the third quarter of 2000. A single EPC4E device will configure a 400,000-gate EP20K400E device, and a single EPC9E device will configure a 1-million-gate EP20K1000E device.

These new devices will include features such as faster configuration times and parallel configuration, and intellectual property (IP) security. Additionally, you can use a single device to configure several FLEX or APEX devices for higher board space efficiency.

continued on page 12

Devices & Tools, continued from page 11

TOOLS

Quartus Version 2000.02 Improves Design Performance (f_{MAX})

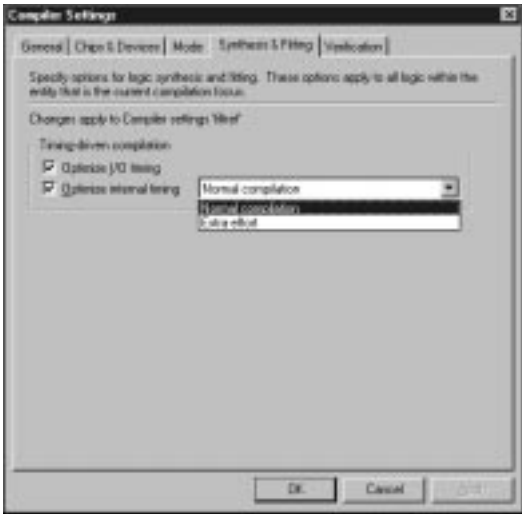
The Quartus software version 2000.02 is available to all Altera customers with a current subscription. This latest version of the Quartus software features significant timing-driven compilation (TDC) enhancements as well as new device support.

The optimized compilation algorithms in the Quartus software version 2000.02 improve design performance (f_{MAX}) by over 40% for designs targeting high-density APEX 20KE devices (i.e., EP20K400 devices and higher).

Version 2000.02 allows designers to separately specify timing constraints for both I/O pins and for internal (core) logic, as shown in Figure 1.

The optimized compilation algorithms in the Quartus software version 2000.02 improve design performance (f_{MAX}) by over 40% for designs targeting high-density APEX 20KE devices.

Figure 1. Setting Timing in Quartus



I/O Timing

Designers can now set t_{SU} and t_{CO} assignments, which forces the Quartus Compiler to implement input and output registers respectively in the I/O cells to meet the timing requirements. These settings optimize the overall system performance.

Internal Timing

Internal (core) timing optimization takes into account the user settings, including inverted clocks and relationships between different clocks. There are two settings for internal timing optimization: **Normal compilation** and **Extra effort**. The default setting is normal.

In addition to the devices supported by the Quartus software version 1999.10, the Quartus software version 2000.02 supports the APEX 20K devices listed in Table 10.

Table 10. New Devices Supported by Quartus 2000.02

Support	Device	Package
Full Compilation, Simulation, and Programming Support	EP20K200	240-pin RQFP *(1)*
	EP20K400	652-pin BGA *(2)*
	EP20K400E	672-pin FineLine BGA *(1)*
Compilation, Simulation, and Pinout Support Only	EP20K100	144-pin TQFP *(1)*, 208-pin PQFP *(1)*, 240-pin PQFP *(1)*, 324-pin FineLine BGA *(1)*, 356-pin BGA *(1)*
	EP20K200	208-pin RQFP *(1)*, 356-pin BGA *(1)*, 484-pin FineLine BGA *(1)*, 652-pin BGA *(1)*, 672-pin FineLine BGA *(1)*
	EP20K300E	652-pin BGA *(1)*, 672-pin FineLine BGA *(1)*
Compilation and Simulation Support Only	EP20K60E *(3)*	144-pin TQFP, 208-pin PQFP, 240-pin PQFP, 324-pin FineLine BGA, 356-pin BGA

Notes:
(1) These devices contain PLLs.
(2) -2 speed-grade devices in industrial-temperature grades only.
(3) The Quartus software version 2000.02 supports EP20K60E devices with and without PLLs.

MAX+PLUS II Version 9.5 Compiles 30× Faster & Increases Design Performance 30%

The MAX+PLUS II software version 9.5 features an enhanced compilation engine optimized for the FLEX 10K device family. The new compilation engine dramatically speeds up TDC times for FLEX 10K-based designs. The compile time improvement depends on both design density and device utilization. In general, high-density designs with a high degree of device utilization show the most significant improvement in timing-driven compilation times.

High-density FLEX 10K designs compile up to 30× faster in the MAX+PLUS II software version 9.5 when compared to version 9.4. To put this in perspective, a high-density design with high device utilization which would have run overnight with the MAX+PLUS II software version 9.4 should now compile in under 30 minutes with version 9.5.

MAX+PLUS II version 9.5 also enhances the design performance for FLEX 10K designs. Customers should expect f_{MAX} to increase by up to 30%. Design performance improvement is also design-dependent and, in general, a higher degree of improvement can be expected for high-density designs. The same design targeting the same speed-grade device will achieve 30% faster f_{MAX} by utilizing advanced compilation algorithms.

The EPF10K30E and EPF10K50S timing models in MAX+PLUS II version 9.5 have been updated to reflect a performance increase indicated by the latest characterization results. The new register-to-register delays (t_{DRR}) are compared to the old t_{DRR} numbers in Table 11.

Table 11. Increased EPF10K30E & EPF10K50S Performance in MAX+PLUS II Version 9.5

Speed Grade	Version 9.5 t_{DRR} (ns)	Version 9.4 t_{DRR} (ns)
-1	8.0	8.5
-2	9.5	10.0
-3	12.5	13.5

Quartus Operating System Update

The Quartus software now supports the operating systems listed in Table 12. Support for the Windows 2000 and the HP-UX 11.0 operating systems is scheduled to be added later this year.

Table 12. Quartus Operating System Support

Platform	Operating System
PC	Windows 98, Windows NT
UNIX	Solaris 2.6, HP-UX 10.20

E+MAX Provides a Complete Design System for Product-Term Architecture PLDs

The E+MAX software is a full-featured development system optimized for Altera's popular product-term architectures, including all MAX 7000 and MAX 3000 devices. The E+MAX software includes hardware description language (HDL) synthesis. Designers targeting product-term architectures now have a powerful tool that they can download for free from the Altera web site (**http://www.altera.com**). Table 13 lists the E+MAX features:

High-density FLEX 10K designs compile up to 30× faster in the MAX+PLUS II software version 9.5.

Table 13. E+MAX Software Features

Feature	Details
Design Entry	Schematic capture VHDL, Verilog HDL, and AHDL synthesis
Device Support	MAX 7000 family (including MAX 7000A, MAX 7000AE, MAX 7000B, MAX 7000E, and MAX 7000S devices) MAX 3000A devices
Design Verification	Functional and timing simulation Static timing analysis
Other Features	Graphical floorplanner OpenCore evaluation for Altera MegaCore functions Integration with third-party EDA tools Support for the library of parameterized modules (LPM)

The E+MAX software features VHDL and Verilog HDL design entry.

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Implementing CAM in an APEX Device

Content-addressable memory (CAM) devices are used in applications that require fast searches. The data contained in CAM is organized as a set of patterns that can be thoroughly searched in a single clock cycle. If the input pattern presented to CAM matches one of the patterns stored in CAM, the address of the matching stored pattern is generated. APEX™ 20KE devices support ternary CAM, a type of CAM that allows stored patterns in memory words to contain "don't care" bits.

The Quartus™ software version 1999.10 and higher supports designs using CAM. You can implement CAM through the Quartus software using the `altcam` megafunction.

The altcam Megafunction

The `altcam` megafunction (see Figure 1) allows each stored pattern bit to be specified as a binary `1` bit, binary `0` bit, or a don't care bit.

Writing Patterns into CAM

Writing a new pattern in the `altcam` megafunction or replacing its stored patterns with new patterns involves the `pattern[]`, `wrx[]`, `wrxused`, `wrdelete`, `wren`, and `wraddress[]` ports. Patterns without don't care bits can be written in two clock cycles, while those with don't care bits require three clock cycles. During all write cycles, `wren` must be asserted and `wraddress[]` and `pattern[]` must remain unchanged.

If the pattern does not contain don't care bits, then asserting `pattern[]`, `wren`, and `wraddress[]` for two clock cycles is sufficient. Don't care bits can be added by using the `wrx[]` port. Bits with `0` in the `wrx[]` mark valid pattern bits, and bits with `1` in the `wrx[]` mark don't care pattern bits. When the `wrx[]` port is used, the `wrx[]`, `wrxused`, `pattern[]`, `wren`, and `wraddress[]` must be asserted for three clock cycles.

You can also delete `altcam` entries by asserting `wrdelete` and `wren` for two clock cycles. During this time, `wraddress[]` must indicate the address containing the data to be deleted. The `pattern[]`, `wrx[]`, and `wrxused` inputs are ignored during delete cycles.

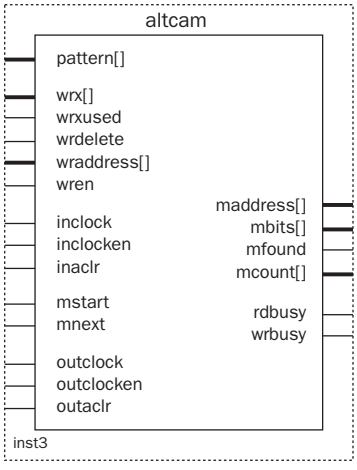
You can use Intel Hexadecimal Format Files (**.hex**) or Memory Initialization Files (**.mif**) to initialize CAM during device configuration. MIFs support don't care and never match bits. To support these extra states in HEX files, you must use a second HEX file; one file initializes the data (0 and 1) and the second file sets the don't care and never match bits. If you use the optional second initialization file, it must be named <*first file name*>**_udc.hex**.

Reading from CAM

You can use three different modes to read data from the `altcam` megafunction:

- Single-match mode
- Multiple-match mode
- Fast multiple-match mode

Figure 1. altcam Megafunction



Parameter	Value
WIDTH	
WIDTHAD	
NUMWORDS	2^WIDTHAD
LPM_FILE	"UNUSED"
LPM_FILEX	"UNUSED"
MATCH_MODE	"MULTIPLE"
OUTPUT_REG	"UNREGISTERED"
OUTPU_ACLR	"ON"
PATTERN_REG	"INCLOCK"
PATTERN_ACLR	"ON"
WRADDRESS_ACLR	"ON"
WRX_REG	"INCLOCK"
WRX_ACLR	"ON"
WRCONTROL_ACLR	"ON"
USE_EAB	

In multiple-match and fast multiple-match modes, an external priority encoder generates the encoded match address output maddress[]. As a result, using this output in the modes listed above results in higher logic utilization.

In all three modes, you can use both encoded (maddress[]) and unencoded (mbits[]) outputs. External logic generates mfound and mcount[], which give the total number of matches.

Single-Match Mode

In single-match mode (match_mode = "multiple"), only one inclock clock cycle is required to read from altcam.

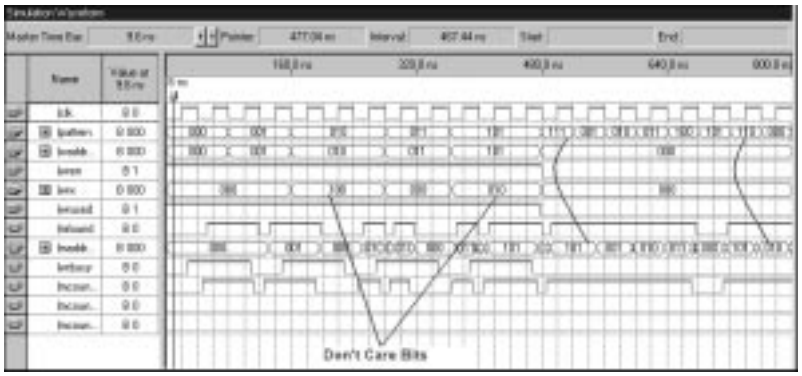
When the input pattern matches one of the stored patterns in altcam, a match flag (mfound) is asserted and the address of the match is presented on maddress[]. Output port mbits[] gives the unencoded version of the match. The output that indicates the number of matches (mcount[]) is always either value 0 or value 1 in this mode.

In single-match mode, altcam will not operate properly if there are multiple patterns stored that match the same input pattern. altcam will give a warning during simulation if there are multiple input patterns.

In this single-match mode, the altcam megafunction uses multiple embedded system blocks (ESBs) to support CAM blocks deeper than 32 words. However, the longest data width supported is 32 bits. For input pattern widths greater than 32 bits, altcam automaticaly switches to the fast multiple-match mode of operation.

To write don't care bits into altcam, assert wrused high and hold waddress[], pattern[] and wren[]valid for three clock cycles. The bits in wrx[] with 1 indicate don't care bits. For example, in Figure 2, at address 010 the wrx[] is 100, which means the most significant bit is a don't care bit. As a result, reading 110 or 010 will find a match at address 010.

Figure 2. Single-Match CAM Simulation with "Don't Care" Bits



Multiple-Match Mode

In multiple-match mode (match_mode = "multiple"), the megafunction takes two inclock cycles to read from altcam and generate valid outputs, because the ESB generates 16 outputs at each clock cycle. As a result, you need two cycles to generate all 32 outputs from an ESB.

To search the altcam megafunction for a new pattern, apply the pattern data to the pattern[] port and assert the mstart input. If the input pattern matches any of the stored patterns, mfound asserts high, and maddress[] provides the address of the first match (after a two-cycle delay). Other match addresses can be generated on subsequent clock cycles. Assert mnext and hold it high for no more than two clock cycles after mstart. Output port mbits[] gives the unecoded version of the matches. Output port mcount[] counts the total number of matches.

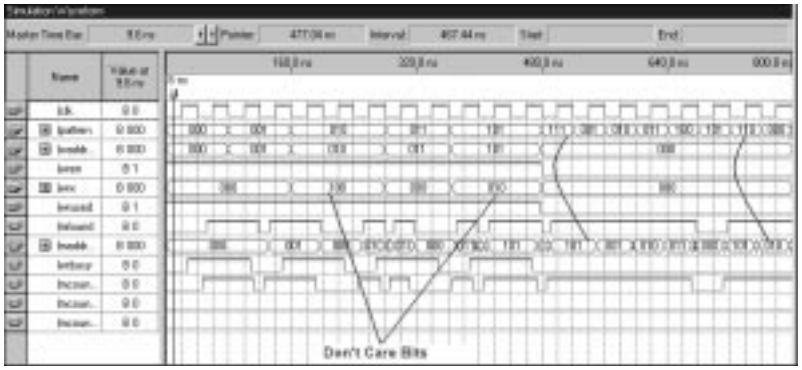
In this multiple-match mode, each ESB supports 31 bits of data because the MSB bit is used to select between the even or odd outputs of the ESB at each clock cycle. However, multiple-match mode supports both deeper and wider CAMs by cascading 32-word × 31-bit ESBs.

Figure 3 on page 16 shows the waveform for multiple-match mode. In multiple-match mode, mstart provides the lowest match address location, and mnext provides the consequent match locations on maddress[]. Do not assert the mnext signal for more than two clock cycles after mstart is asserted. In this example, data 1 is written in three locations: 1, 3, and 5.

continued on page 16

Implementing CAM in an APEX Device, continued from page 15

Figure 3. Multiple-Match Mode Simulation



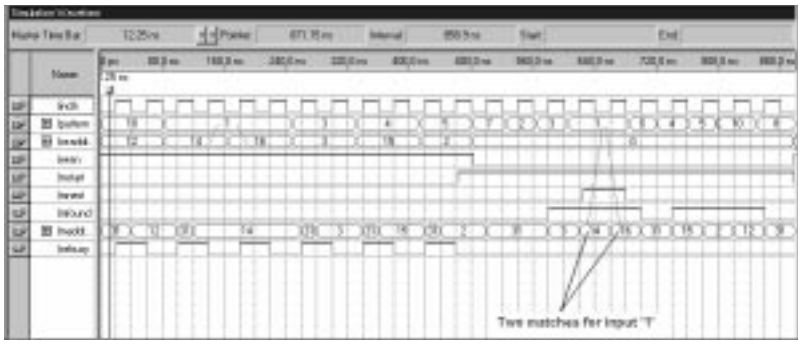
Asserting `mstart` provides address location `1` on the `maddress[]` port, and asserting `mnext` provides the consequent locations, `3` and `5`. The `mcount[]` signal shows the total number of matches, which is three in this example.

Fast Multiple-Match Mode

Fast multiple-match mode (`match_mode = "fast_multiple"`) is similar to multiple-match mode. The difference is that fast multiple-match mode takes one `inclock` clock cycle to read from `altcam` and generate valid outputs. This acceleration comes at the cost of using only half of the memory available in each ESB. As a result, ESB utilization is higher, but data is read out of `altcam` in one cycle.

Most of the input and output ports used in fast multiple-match mode are identical to multiple-match mode with a few exceptions. Ports such as `maddress[]`, `mcount[]`, `mfound`, `pattern[]`, `wrx[]`, and `wren` function the same as in multiple-match mode. The `rbusy` port is not used in fast multiple-match mode because the read does not exceed one clock cycle. The `mstart` and `mnext` ports are not required for this mode if the location of the matched address is not required (if `maddress[]` is not used), and only the `mbits[]` output gives the unencoded version of the matching address. If `maddress[]` output port is used, `mstart` and `mnext` must be used to give the first and next matching addresses.

Figure 4. Fast Multiple-Match Mode Simulation



In fast multiple-match mode, the `altcam` megafunction supports CAM blocks deeper and wider than 32 words and bits by cascading multiple ESBs. Figure 4 shows the simulation result of a fast multiple-match mode.

CAM Modes Comparison

To compare the performance and utilization of CAM modes, a 32-word × 32-bit CAM was compiled for an EP20K200E-1 device. Table 1 shows the result for this comparison.

Table 1. Performance & Utilization of CAM Modes

Parameter	Usage		
	Single-Match Mode	Mutiple-Match Mode	Fast Multiple-Match Mode
RAM Blocks (ESBs)	1	1	2
LEs	35	98	79
f_{MAX} (MHz)	198.89	94.45	190.91

Conclusion

The Quartus software version 1999.10 and higher supports CAM implementation in APEX 20KE devices. Depending on your design requirements, you can implement any CAM mode by using the `altcam` megafunction. Additionally, MIFs and HEX files support CAM initialization. By using CAM, you can speed up any design that requires searches.

APEX PLLs Offer Advanced Clock Synthesis

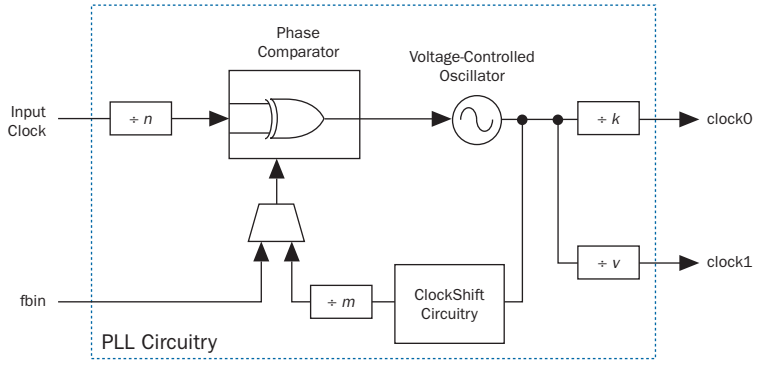
APEX™ 20KE devices support the ClockLock™, ClockBoost™, ClockShift™, and external clock output features, which are implemented with phase-locked loops (PLLs). The ClockLock feature minimizes clock delay and clock skew within the device, reducing clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry provides a clock multiplier to scale or multiply the input clock by integers or fractional ratios. The designer can use the programmable clock phase within the ClockShift circuitry for phase shift applications or for clock delay control to meet strict timing requirements. The external clock output drives a locked clock off-chip to external devices with optional zero delay or external feedback. The ClockLock, ClockBoost, and ClockShift features work in conjunction with the APEX 20KE device's high-speed clock to provide advanced clock synthesis capabilities. This article discusses the enhanced clock synthesis features within APEX 20KE devices.

APEX 20KE PLLs Provide Clock Synthesis

APEX 20KE devices incorporate up to four PLLs with advanced circuitry and feature low-voltage differential signaling (LVDS) support, ClockShift circuitry, and external clock outputs with optional external feedback inputs. Figure 1 shows the ClockLock and ClockBoost circuitry in one of the four APEX 20KE PLLs. You can instantiate APEX 20KE PLLs and adjust parameters to control advanced features in the Quartus™ software with the `altclklock` megafunction.

Each APEX 20KE PLL includes circuitry that provides clock synthesis using $m/(n \times k)$ or $m/(n \times v)$ scaling, depending on the output clock used. When a PLL is locked, the locked output clock aligns to the rising edge of the input clock. Because the PLL output contains dual dividers, you can output two different frequencies from a single PLL. The closed loop equation for Figure 1 gives output frequencies of

Figure 1. ClockLock & ClockBoost Circuitry in APEX 20KE Devices

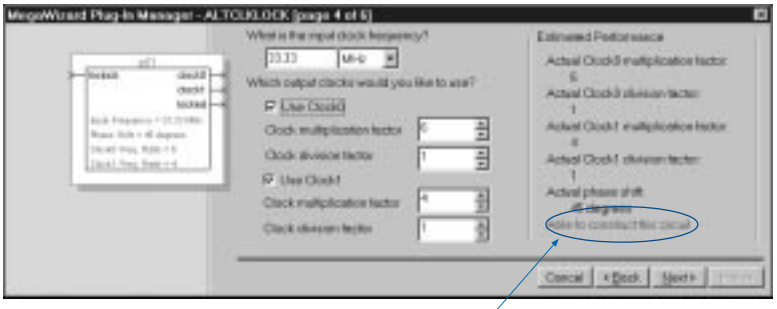


$$f_{clock0} = f_{in}(m/(n \times k))$$

$$f_{clock1} = f_{in}(m/(n \times v))$$

The Quartus software handles these equations for the user; the user only needs to enter the desired integer multiplication and division ratios. The MegaWizard™ Plug-In Manager provides a simple interface to enter parameters into the `altclklock` megafunction to achieve the desired PLL outputs. The MegaWizard Plug-In Manager notifies the designer if the multiplication and division rate is possible for the given frequency (see Figure 2).

Figure 2. Parameters Set Via the MegaWizard Plug-In Manager



continued on page 18

APEX PLLs Offer Advanced Clock Synthesis, continued from page 17

The advanced ClockBoost feature allows the designer to reduce the effects of high-speed signals by using a low-speed clock on the printed circuit board (PCB). The ClockBoost feature can internally multiply those low-speed clocks. The ability to generate multiple scaled clocks within the device allows for easier board design.

Designers can use the versatile multiplication capability to generate up to four scaled clocks within the same device from a single clock source. This process is useful in microprocessor-based systems, where a system clock may run at a lower rate than other system components. Figure 3 shows clock synthesis for an embedded application in an APEX 20KE device.

Figure 3. Embedded Applications Using APEX 20KE Devices for Clock Synthesis

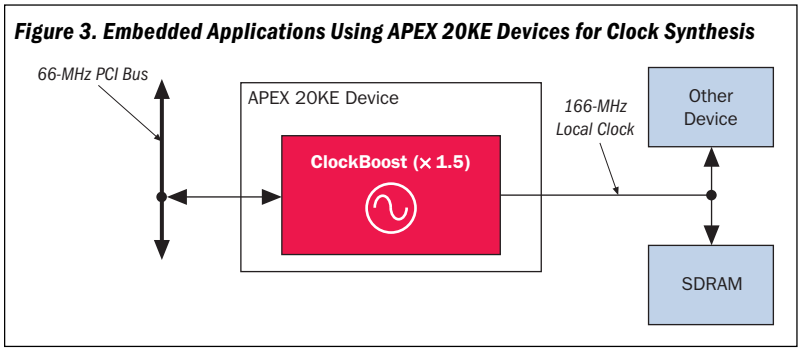


Figure 4. Phase & Delay Shifting

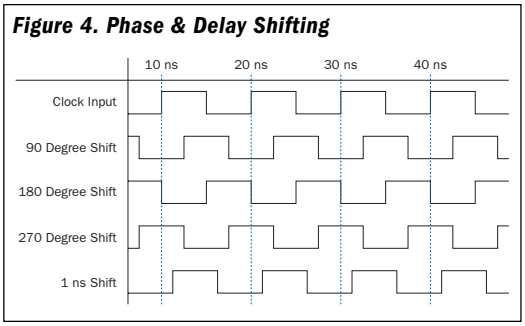
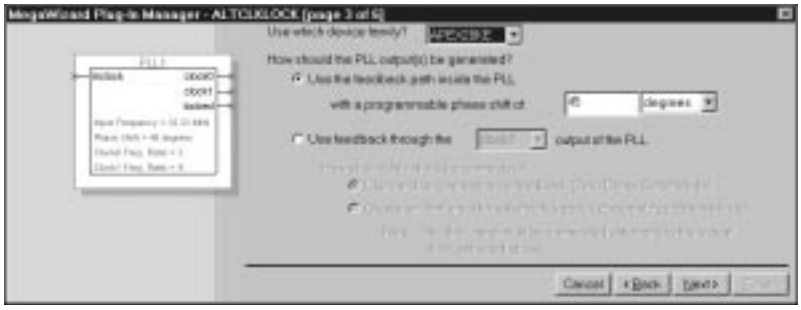


Figure 5. Setting Phase Shift & Other PLL Features



APEX 20KE PLLs have ClockShift circuitry that provides programmable clock delay and phase shift. The clock phase can be adjusted to lag the input by 90, 180, or 270 degrees, or to any desired phase or time shift with fine resolution (see Figure 4). The resolution steps range from 0.5 ns to 1.0 ns, depending on the input frequency and scaling rates. Users enter the desired phase shift in the MegaWizard Plug-In Manager (see Figure 5). The dialog box in Figure 2 displays the closest achievable shift with the frequency and scaling used.

Low-jitter external clocks are available in APEX 20KE devices for external clock sources. Other devices on the board can use these outputs as clock sources. The external clock output can also be configured as a zero delay buffer, i.e., the output-clock pin can be phase-aligned with the input clock pin.

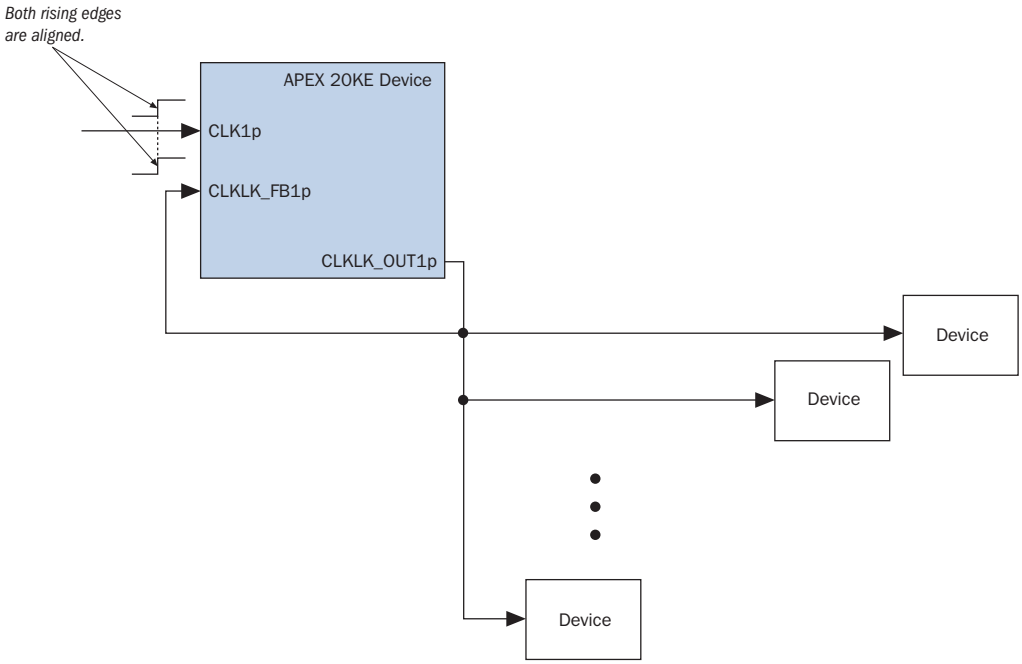
In addition to the clock output capability, you can use feedback inputs to align the external feedback clock pin with the input clock pin. By aligning these clocks, you can actively remove clock delay and skew between devices. Board delay is actively adjusted independent of process, temperature, or voltage.

Matching the return delay that contains the feedback input pin with the delay to each device ensures that delay is eliminated. See Figure 6.

Summary

The advanced feature set of APEX PLLs, including ClockLock, ClockBoost, and ClockShift features, work in conjunction with the APEX device's high-speed clock to provide significant improvements in system performance, bandwidth, and clock synthesis. For more information on APEX 20KE PLLs, see *Application Note 115 (Using the ClockLock and ClockBoost Features in APEX Devices)* and the *Using APEX 20K & APEX 20KE PLLs in Quartus White Paper.*

Figure 6. Reducing Board Delay Using an APEX 20KE Device *Note (1)*



Note:
(1) For board design, the route delay from `CLKLK_OUT1` to each device and the return-route delay to `CLKLK_FB1` should be equal.

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Using I/O Standards in the Quartus Software

APEX™ 20KE I/O banks support 14 I/O standards (see Table 1) and are the first programmable logic devices (PLDs) in the industry with dedicated circuitry supporting low-voltage differential signaling (LVDS). Altera's APEX 20KE devices offer the highest density, highest performance programmable logic solution with the necessary I/O standards for use in the communication and computer industries.

APEX 20KE I/O buffers are designed to meet the voltage, drive strength, and AC characteristics necessary to be compliant with the I/O standards listed in Table 1.

This article discusses the support for the selectable I/O standards for APEX 20KE devices in the Quartus™ software.

- Users can specify which pins support which I/O standard on a pin-by-pin basis, similar to pin assignments.
- The pin-assignment windows in the Quartus software have been updated so that users can make I/O standard assignments, pin assignments, and reserved pin assignments in one dialog box.
- The enhanced Floorplan Editor displays the separate I/O banks and the LVDS transmitter and receiver blocks.
- The Quartus software verifies user placement and I/O standard assignments, and automatically places I/O pins based on V_{REF} and I/O standard assignments.

Table 1. APEX 20KE Supported I/O Standards

I/O Standard *(1)*	Type	Input Reference Voltage (V_{REF}) (V)	Output Supply Voltage (V_{CCIO}) (V)	Board Termination Voltage (V_{TT}) (V)
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
3.3-V PCI	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
GTL+	Voltage referenced	1.0	N/A	1.5
SSTL-2 Class I and II	Voltage referenced	1.125	2.5	1.125
SSTL-3 Class I and II	Voltage referenced	1.5	3.3	1.5
HSTL Class I	Voltage referenced	0.75	1.5	0.75
AGP	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

Notes:

(1) AGP: advanced graphics port, CTT: center-tap-terminated, GTL+: Gunning transceiver logic plus, HSTL: high-speed transceiver logic, LVCMOS: low-voltage complementary metal-oxide semiconductor, LVTTL: low-voltage transistor-to-transistor logic, PCI: peripheral component interconnect, SSTL: stub-series terminated logic.

Device & Pin Options Dialog Box (Compiler Settings Dialog Box)

The **Voltage** tab in the **Device & Pin Options** dialog box contains a **Default I/O standard** drop-down menu used to set the default I/O standard for a device. The user can set any I/O standard to be the default.

All I/O pins without a specific I/O standard assignment default to the I/O standard specified in this drop-down menu. Figure 1 shows the **Device & Pin Options** dialog box for a design targeting an APEX 20KE device.

Figure 1. Device & Pin Options Dialog Box

Pin Assignments Dialog Box

In the **Pin Assignments** dialog box, designers make pin assignments, specify I/O standards, make V_{REF} assignments, and view each pin setting. Figure 2 shows the **Pin Assignments** dialog box.

Figure 2. Pin Assignments Dialog Box

Follow the steps below to make pin assignments, designate I/O standard types, and reserve pins. Designers should reserve I/O pins that may be needed in the future.

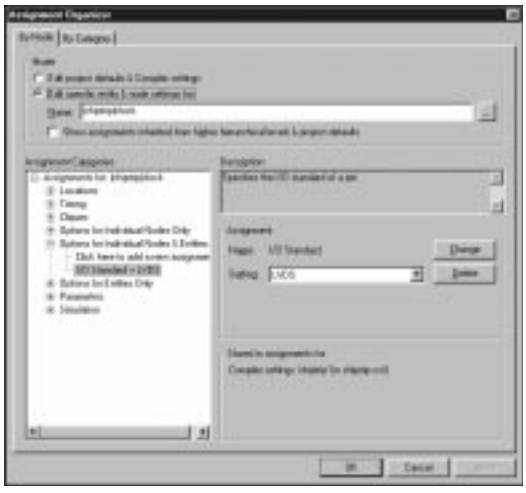
1. Choose **Compiler Settings** (Processing menu).
2. Click **Assign Pins**.
3. Turn on **Show 'no connect' pins** in the **Pin Assignments** dialog box to show the pins that you cannot assign a node name in the **Available pins & existing assignments** list.
4. In the **Available pins & existing assignments** list, select the pin number for the pin to which you want to assign, change, or delete a node name assignment.
5. To delete the node name assignments from the pin, click **Delete** (Assignment menu).
6. To assign a new node name to the pin or change the existing node name assignment for the pin, under **Assignment**, type a node name in the **Pin name** box.
   or
   Use the **Node Finder** to copy the node name to the **Pin Assignments** dialog box.
7. If you added or changed the node name assignment for the pin and you want to assign an I/O standard to the pin, select a standard from the **I/O Standard** list (Assignment menu).
8. If you added or changed the node name assignment or I/O standard and you want to reserve the pin for future use, turn on **Reserve pin** (Assignment menu), even if it does not exist in the design file, and select **As input tri-stated**, **As output driving ground**, **As output driving an unspecified signal**, or **As V_{REF} from the list**.
9. To save a new assignment and add the assignment to the **Available pins & existing assignments** list (Assignment menu), click **Add.**
10. To save the changed assignment and add the assignment to the **Available pins & existing assignments** list (Assignment menu), click **Change**.
11. Repeat steps 4 to 11 for each additional assignment you want to make, change, or delete.
12. Click **OK**.

Assignment Organizer

The easiest way to make I/O standard assignments is to use the **Assignment Organizer** to assign the pins in the design file.

1. Select a pin in your Graphic Design File (**.gdf**) or highlight the pin name in Text Design Files (**.tdf**).
2. Right click on the pin and choose **Assignment Organizer** to open the **Assignment Organizer** dialog box, as shown in Figure 3.
3. The **Assignment Organizer** dialog box automatically opens to the **By Node** tab. In

Figure 3. Assignment Organizer Dialog Box



continued on page 22

Using I/O Standards in the Quartus Software, continued from page 21

this tab, users can make I/O standard, pin, or other logic option or location assignments. The pin name that you selected in the design file is listed in the **Name** box.

The Floorplan Editor contains several enhancements to support new features in APEX 20KE devices: multiple I/O standards, the PLL, and the LVDS transmitter and receiver block.

4. To make an I/O standard assignment to that pin, expand the view under **Options for Individual Nodes & Entities** by double-clicking on it or by clicking on the + next to it. Click on the **Click here to add an assignment** to activate the **Assignment** section.
5. In the Assignment section, make sure **I/O Standard** is selected under **Name**. If not, click **Change** and select **I/O Standard**. Under the **Setting** pull-down menu, choose the I/O standard that you want to assign to the pin.
6. Click **Add**, and then click **OK**.

Representation of I/O Banks & I/O Standards in the Floorplan Editor

The Floorplan Editor contains several enhancements to support new features in APEX 20KE devices: multiple I/O standards, the phase-locked loop (PLL), and the LVDS transmitter and receiver block.

I/O Bank Coloring & Numbering

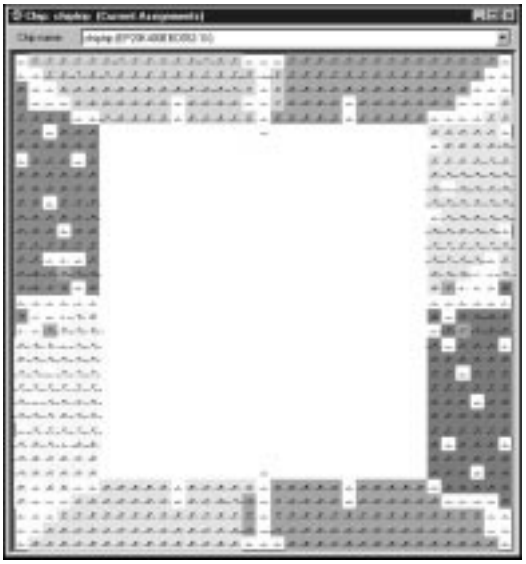
The Floorplan Editor shows membership in I/O banks by using a unique background fill color around each pin for each I/O bank. In addition, the bank number is shown. Only I/O and VCCIO pins have the colored background, GNDINT, GNDIO, and VCCINT pins do not. Figure 4 shows the Floorplan Editor for a EP20K400EBC652-1X device in package view.

The display of I/O bank colors is controlled by the **Show I/O Banks** command under the **View** pull-down menu when the Floorplan Editor is open. This command also displays the I/O bank colors and bank numbers in the three interior views.

LVDS-Paired Pin Labeling

LVDS pins have a specific naming convention; they begin with LVDS. The next two characters

Figure 4. Package View with Show I/O Banks On



for data pins indicate whether they belong to the receiver (RX) or transmitter (TX), followed by the two-digit channel <*number*>, ranging from 01 to 16. The last character at the end of the pin name indicates polarity—p for positive polarity and n for negative polarity. Table 2 summarizes names for all LVDS pins.

The dedicated clock pins (CLK1p, CLK2p, CLK3p, CLK4p) support LVDS and have optional dual-purpose negative polarity pins associated with them. The PLL feedback pins (CLKLK_FB1p, CLKLK_FB2p) and the PLL output pins (CLKLK_OUT1p, CLKLK_OUT2p) also support LVDS following the same convention as the dedicated clock pins.

Figure 5 shows the LVDS receiver in the Floorplan Editor. The LVDS input receiver clock (LVDSRXINCLK1p, LVDSINCLK1n) clocks the serial-to-parallel converter. The serial-to-parallel converter is shown by the filled rectangle.

Automatic Placement & Verification of Selectable I/O Standards

The Quartus software verifies correct placement of all I/O and V_{REF} pins and intelligently places I/O pins by following the same rules outlined in the "Guidelines for Selectable I/O Standards" section of the *Using I/O Standards in the Quartus Software White Paper*. Designers must assign VREF pins for all voltage-referenced I/O

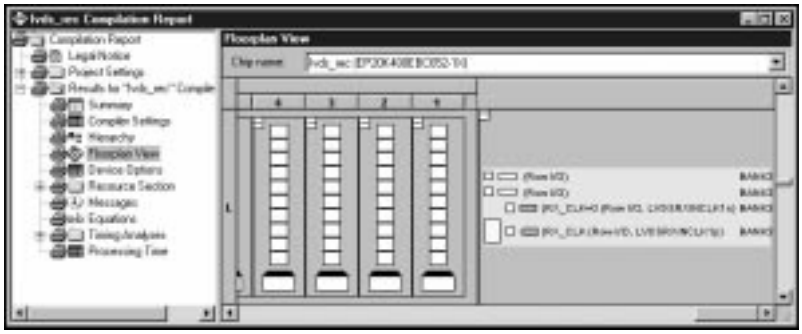
Table 2. LVDS Pin Naming Convention

Pin Names	Function
LVDSRX<*number*>p	Receiver positive data pin
LVDSRX<*number*>n	Receiver negative data pin
LVDSTX<*number*>p	Transmitter positive data pin
LVDSTX<*number*>n	Transmitter negative data pin
LVDSRXINCLK1p	Receiver input clock positive pin
LVDSRXINCLK1n	Receiver input clock negative pin
LVDSTXINCLK1p	Transmitter input clock positive pin
LVDSTXINCLK1n	Transmitter input clock negative pin
LVDSTXOUTCLK1p	Transmitter output clock positive pin
LVDSTXOUTCLK1n	Transmitter output clock negative pin
CLK1p	Dedicated clock 1 positive pin (PLL 1)
CLK1n	Dedicated clock 1 negative pin (PLL 1)
CLK2p	Dedicated clock 2 positive pin (PLL 2)
CLK2n	Dedicated clock 2 negative pin (PLL 2)
CLK3p	Dedicated clock 3 positive pin (PLL 3)
CLK3n	Dedicated clock 3 negative pin (PLL 3)
CLK4p	Dedicated clock 4 positive pin (PLL 4)
CLK4n	Dedicated clock 4 negative pin (PLL 4)
CLKLK_FB1p	Dual-purpose ClockLock feedback positive pin (PLL 1)
CLKLK_FB1n	Dual-purpose ClockLock feedback negative pin (PLL 1)
CLKLK_FB2p	Dual-purpose ClockLock feedback positive pin (PLL 2)
CLKLK_FB2n	Dual-purpose ClockLock feedback negative pin (PLL 2)
CLKLK_OUT1p	Dual-purpose ClockLock output positive pin (PLL 1)
CLKLK_OUT1n	Dual-purpose ClockLock output negative pin (PLL 1)
CLKLK_OUT2p	Dual-purpose ClockLock output positive pin (PLL 2)
CLKLK_OUT2n	Dual-purpose ClockLock output negative pin (PLL 2)

pins. The Quartus software automatically places I/O pins of different V_{REF} standards without pin assignments in separate I/O banks. The Quartus software:

- Verifies that no two voltage-referenced I/O pins requiring different V_{REF} levels are placed in one bank.
- Ensures that an I/O pin requiring a VREF pin is no more than 16 pins from a VREF pin. All 16 voltage-referenced I/O pins may be placed on only one side of the VREF pin or staggered on both sides of the VREF pin.
- Reports an error message if the current limitation is exceeded between GNDIO pins. It uses the equations documented in the *Using I/O Standards in the Quartus Software White Paper*.
- Ensures that no more than 16 voltage-referenced I/O standard pins are using a single V_{REF}.
- Does not allow you to place an output pin within two pins of a VREF pin if a power pin does not separate them. Use the **Show Pads** view in the Floorplan Editor to view the pad orientation.
- Reserves the unused LVDS channels in the LVDS transmitter and receiver blocks when any of the LVDS channels are being used. The software also reserves the two I/O pins adjacent to the LVDS blocks that share V_{CCIO} with the LVDS blocks.
- Does not allow placement of non-LVDS output pins in or within two I/O pins (with a common V_{CCIO}) of the LVDS blocks.

Figure 5. LVDS Receiver Block In the Floorplan Editor



The Quartus software verifies correct placement of all I/O and VREF pins and intelligently places I/O pins.

Summary

The Quartus software supports APEX 20KE designs with 14 programmable I/O standards, allowing customization for use in a wide variety of applications. Pin assignments, I/O standard assignments, and reserved pin assignments are easily made from either the **Pin Assignments** dialog box or through the **Assignment Organizer**. The Quartus software verifies the user assignments and automatically places pins based on guidelines outlined in the *Using I/O Standards in the Quartus Software White Paper*. For more information on selectable I/O standards, see *Application Note 117 (Using the Selectable I/O Standards in APEX 20KE Devices)*.

Quartus Timing Analysis Verifies Design Performance

The Quartus software provides the features necessary to perform advanced timing analysis for today's system-on-a-programmable-chip designs.

As designs become more complex, the need for advanced timing analysis capability grows. Timing analysis measures the delay of every design path and reports the maximum system clock speed for the design. Static timing analysis does not check design functionality. Therefore, designers should perform timing analysis together with simulation to verify overall design operation.

The Quartus™ software provides the features necessary to perform advanced timing analysis for today's system-on-a-programmable-chip designs. For example, during design compilation, the Quartus software can automatically activate the Static Timing Analyzer, removing the need to launch a separate timing analysis tool after each successful compilation. The Quartus Static Timing Analyzer also reports results in several distinct tables and provides immediate and direct access to all timing analysis results.

Timing Analysis Basics

To perform comprehensive timing analysis, designers need to observe setup times, hold times, clock-to-output delays, clock skews, maximum clock frequencies, and slack times for their designs. This information lets designers validate circuit performance and identify possible timing violations. Undetected violations could present timing hazards and race conditions, both of which could lead to circuit failure.

Setup Time (t_{SU})

Data that feeds a register via its data or enable input(s) must arrive at the input pin before the register's clock signal is asserted at the clock pin. Setup time is the minimum length of time this data must arrive before the active clock edge.

Hold Time (t_H)

Data that feeds a register via its data or enable input(s) must be held at an input pin after the register's clock signal is asserted at the clock pin. Hold time is the minimum length of time this data must be stable after the active clock edge.

Clock–to-Output Delay (t_{CO})

Clock-to-output delay is the time required to obtain a valid output at an output pin after a clock transition on the pin that clocks the register.

Clock Skew

Clock skew is the difference in arrival time of a clock signal at two different registers. This timing difference occurs when two clock signal paths have different lengths. Clock skew is common in designs that contain clock signals that are not routed globally. The Quartus software reports clock skews for all clocks, whether they are on pins or are internally derived clocks.

Maximum Clock Frequency (f_{MAX})

Maximum clock frequency is the fastest speed the design clock can run without violating internal setup and hold time requirements. The Quartus software performs timing analysis on both single and multiple clock designs, reporting a design's internal and system $\mathbf{f_{MAX}}$. An internal f_{MAX} analysis calculates the register-to-register timing within the device. System $\mathbf{f_{MAX}}$ includes external delays to the device.

To determine internal f_{MAX}, the circuit's clock period must be calculated. The clock period depends on the data path delay, the clock skew between registers, the source register's clock-to-

output time, and the destination register's setup time.

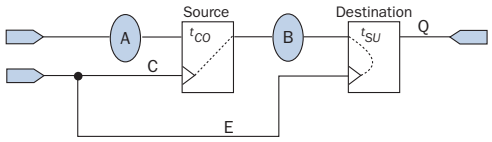
The Quartus software uses the following equations to calculate clock period and internal f_{MAX}. Register-to-register delay (t_{RD}) in the clock period equation represents the data path delay between two registers.

Clock period = t_{RD} – *Clock Skew* + *Micro* t_{CO} + *Micro* t_{SU}

Internal f_{MAX} = 1 / Clock period

Figure 1 shows a sample internal f_{MAX} diagram.

Figure 1. Quartus Internal f_{MAX} Diagram (Not Including External Delays)



The following equation calculates the internal f_{MAX} for the circuit shown in Figure 1.

Internal f_{MAX} = 1 / [*B* – (*E* – *C*) + *Source Micro* t_{CO} + *Destination Micro* t_{SU}]

Slack

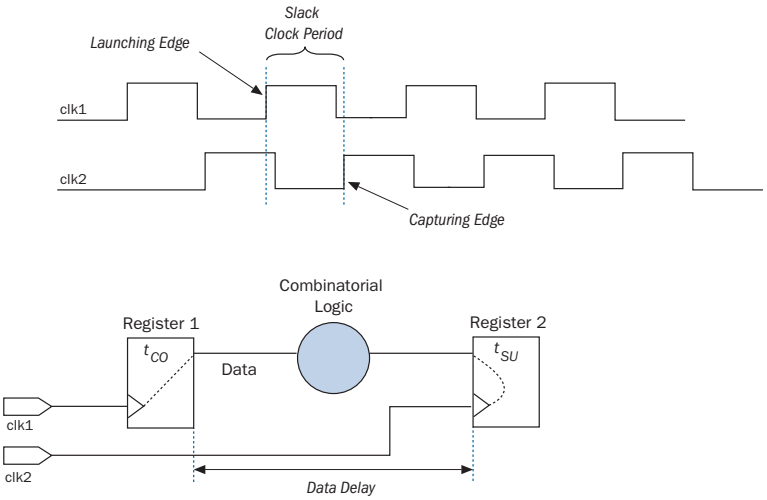
Slack is the margin by which a timing requirement (e.g., f_{MAX}) was met or not met. A positive slack indicates that the circuit met the timing requirements; negative slack indicates that the design contains timing violations. The Quartus software determines slack with the following equations.

Slack = *Required clock period* – *Actual clock period*

Slack = *Slack clock period* – (*Micro* t_{CO} + *Data Delay* + *Micro* t_{SU})

Figure 2 shows a slack calculation diagram.

Figure 2. Slack Time Calculation Diagram



Advanced Features

The Quartus software can perform timing analysis of designs containing paths that cross multiple clock domains and designs that contain multicycle paths, offering designers greater control over design functionality. This section describes these advanced features.

For detailed instruction on how to use these or any of the Quartus Static Timing Analyzer features, see Quartus Help.

Multiple Clock Domains

Multiple clock circuits are designs that have more than one clock driving a circuit. After the clocks are specified, the Quartus software analyzes timing for register-to-register paths controlled by different clocks, and the results are reported as slack. If the clocks are not specified, the Quartus software reports f_{MAX} for each clock pin.

Multicycle Paths

Multicycle paths are paths between registers that intentionally require more than one clock cycle to become stable. For example, a register may

continued on page 26

Quartus Timing Analysis Verifies Design Performance, continued from page 25

need to trigger a signal on every second rising clock edge.

To obtain accurate results, designers can configure the Quartus Static Timing Analyzer to ignore (i.e., cut) these paths during static timing analysis.

Figure 3 shows a timing diagram of a multicycle path between registers that exists in a design with multiple clocks that have a small offset between them.

Designers can set multicycle paths in their designs to avoid incorrect setup time violation reports. These assignments can be made in the Quartus **Assignment Organizer**.

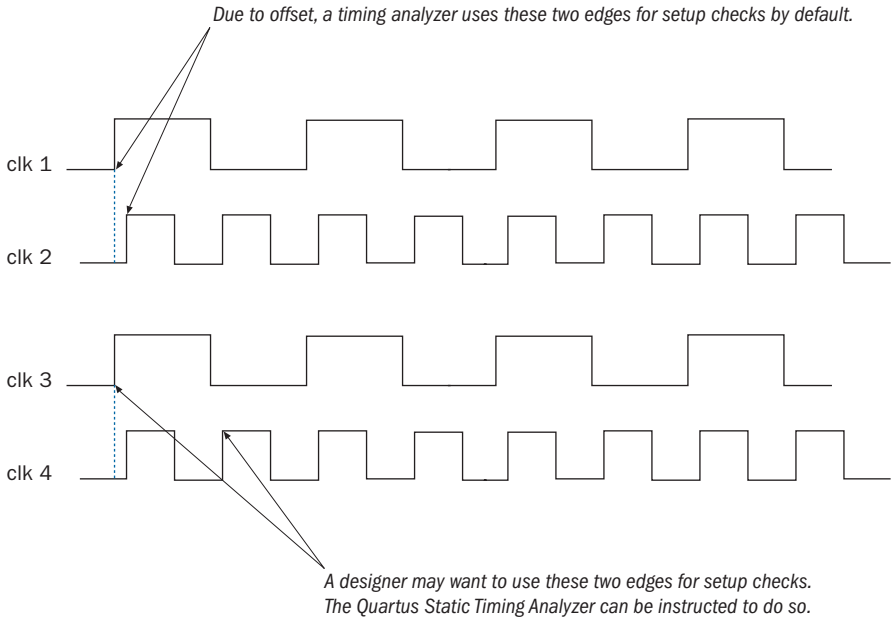
False Paths

Designs may contain paths between registers that are not relevant to the circuit's operation. These paths are referred to as false paths. To obtain accurate results, designers can configure the Quartus Static Timing Analyzer to ignore (i.e., cut) these paths during static timing analysis. Examples of false path signals are signals that are not used under normal operation (e.g., reset or test-mode). Designers can cut paths in the Quartus software using the **Timing Settings** (Project menu) or **Assignment Organizer** (Tools menu) dialog boxes.

Conclusion

Evolving design methodologies and aggressive process technologies call for larger and higher-performance designs to be implemented in programmable logic devices (PLDs). This increasing design complexity initiates a need for enhanced timing analysis tools that aid designers in verifying design timing requirements. Without advanced timing analysis tools, designers risk circuit failure of their intricate multiclock and multipath designs. The Quartus Static Timing Analyzer incorporates a set of powerful, new timing analysis features that are critical in enabling system-on-a-programmable-chip designs.

Figure 3. Multicycle Paths with Offset Between Clocks



Customer *Application*

Altera Devices on the Cutting Edge of Medical Technology

Cutting-edge applications are using more and more programmable logic devices because of their flexibility and efficiency. Altera is proud to be at the forefront of medical research, as FLEX® 10K devices form an integral part of the latest positron emission tomography (PET) scanner from CTI PET Systems, Inc. CTI PET Systems is a joint venture by Siemens Medical Systems and CTI, Inc., the company that produced the first commercial PET scanner.

The ECAT High Resolution Research Tomograph (HRRT) offers very high resolution PET scanning for use in clinical diagnosis of brain disorders. With PET, doctors can effectively pinpoint the location of many common cancers, heart diseases, and neurological diseases, without resorting to exploratory surgery or ineffective medical treatments. PET reduces medical costs and makes treatment less traumatic and less costly for the patient.

What is PET?

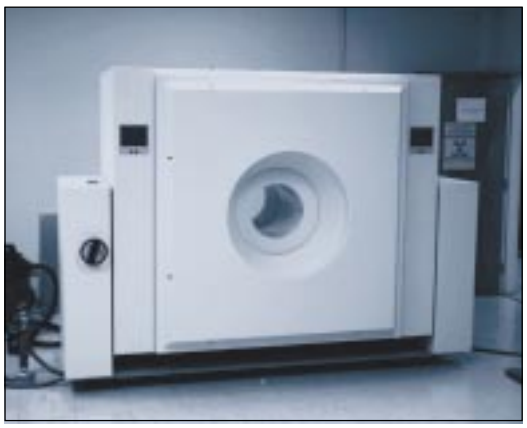
In PET scanning, compounds tagged with radioactive isotopes are injected into patients to obtain images of metabolic or physiologic processes. The isotopes undergo radioactive decay, resulting in the emission of positively charged electrons or positrons. The positrons travel only a few millimeters in the body tissue before they collide with negatively charged electrons, and the total mass of the two is converted into two photons of pure energy. The two photons are emitted simultaneously at 180 degrees from each other toward the opposite sides of the body. Detectors in the PET scanner record the relative position of the pairs of photons, identifying and locating millions of positron-electron collisions per second. The scanner's computer then reconstructs this data as a visual image showing the distribution of the isotope inside the tissues being examined. The image shows both normal organ function and failure of organ systems due to disease.

Depending on the type of isotope used, different metabolic functions can be observed. PET scanning is particularly effective, for example, in diagnosing cancers, as it can follow the course of the cancer through the body and accurately show the extent of the disease. Another area of PET application that continues to develop is in the diagnosis of common neurological disorders, such as Alzheimer's disease, Hodgkins disease, and stroke.

The ECAT HRRT PET Scanner

The ECAT HRRT is composed of the main assembly, patient bed, computer, and operator's workstation. The main assembly, shown in Figure 1, has a gantry with a ring-shaped opening where the detectors and their electronics are located. The patient bed transports the patient through the detector ring, and the computer is used for data acquisition and the control system.

Figure 1. The ECAT HRRT



The ECAT HRRT is by far the most high-resolution PET scanner produced by CTI PET Systems. It contains 936 detectors, nearly four times the number of detectors found in the ECAT EXACT HR+, which was till now the highest performance PET scanner in the world. The HRRT detectors are arranged in a ring of

continued on page 28

CTI, Inc.
810 Innovation Drive
Knoxville, TN
37932-2571
(423) 966-7539
http://www.cti-pet.com

Altera Devices on the Cutting Edge of Medical Technology, continued from page 27

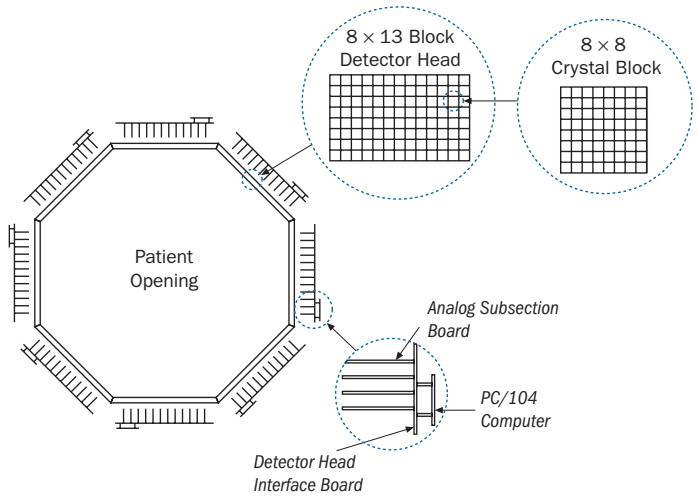
eight panels formed of 9 × 13 detector blocks. Each detector block is composed of an 8 × 8 block of lutetium oxyorthosilicate (LSO) scintillating crystals, as shown in Figure 2. The crystals are in pairs, the one having a fast decay time and the other a slow decay time. Therefore, the HRRT has just under 120,000 crystals to detect the photon's gamma rays (compared to just 18,432 crystals in the ECAT EXACT HR+).

As shown in Figure 2, each of the eight detector panels has its own set of electronics. The detector head interface board distributes the system clocks, loads the configuration information, and performs event rate reporting and system diagnostics. It holds an embedded PC/104 computer to perform administrative and low-speed communications tasks, a bleeder board with four photomultiplier tubes (PMTs) to capture and convert the light signals detected by the crystals, and 39 analog subsection boards, each of which processes the events for three crystal blocks.

EPF10K10 Devices Provide a Flexible Solution

Because of the large number of detectors and the advanced features found in the HRRT, CTI PET Systems needed a fast, powerful, flexible, low-cost solution for the front-end processing.

Figure 2. Detector Configuration



Rather than using the ASIC implementation found in the company's other products, the company chose to use 1,016 Altera® EPF10K10QC208-3 devices and 20 EPF10K30RC208-4 devices for the HRRT. "The Altera PLD architecture reduced our development time and risk compared to a mask-based ASIC architecture, while maintaining costs and density," said John Young, Senior Development Engineer.

The advantages of using PLDs in the HRRT rather than an ASIC were obvious to the CTI PET Systems engineers. The in-circuit reconfigurability (ICR) of FLEX 10K devices means that they can be configured for set-up, reconfigured for the actual detection process, and reconfigured as necessary for self-diagnostics. For example, during setup, the PC/104 computer programs the Altera devices with calibration algorithms that allow all of the block processing channels to perform calibration at once, reducing the setup time for the detectors.

"The EPF10K10 device's reconfigurability means it can easily handle all these functions. We just reconfigure it in-system at each step of the process. Also, signal processing time is kept to a minimum because the Altera device can simultaneously access all the other devices in the sub-system," said John Young.

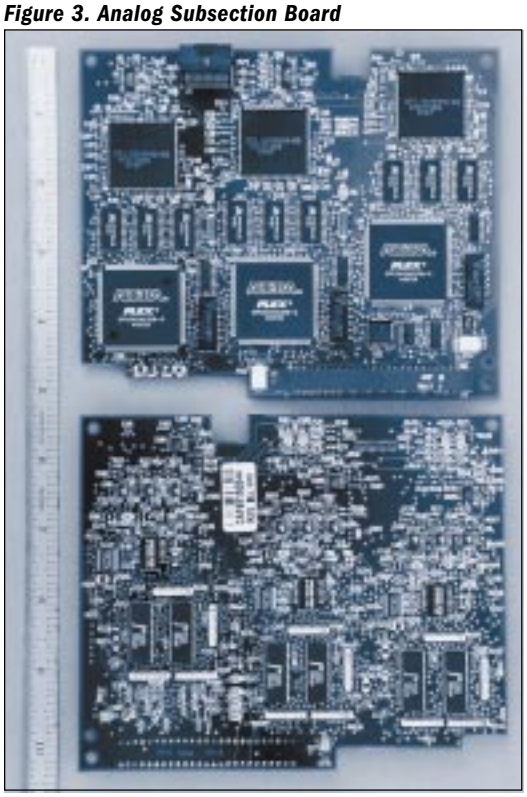
FLEX 10K Devices in the Detection Process

The HRRT scanner is a highly complex system in which Altera FLEX 10K devices play a vital role. This section concentrates on how these devices operate in the detection process.

Figure 3 shows the analog subsection block diagram. Three EPF10K10QC208 devices are located on each analog sub-section board, as shown in Figure 3, for a total of 936 devices per system, one for each crystal block on the HRRT. The EPF10K10 device interfaces with three 8-bit FLASH analog-to-digital-converters (ADCs), a time-to-digital converter (TDC) circuit, and two 128-Kbyte × 8 look-up RAM devices. It also performs energy qualification, shape discrimination, and time correction.

During scanning, a crystal absorbs incoming photon energy (an event) and generates a light signal. The detector block's four photomultiplier tubes (PMTs) then convert the light signal into four digital signals, which are passed to an analog application-specific integrated circuit (ASIC) with a built-in constant fraction discriminator (CFD). The ASIC generates a time-mark signal indicating when a gamma ray is detected. This time-mark signal is sent to the TDC where it is digitized with respect to the master system clock. Meanwhile, the energy signal, consisting of the sum of the four PMT signals, is sampled twice by an 8-bit FLASH ADC to determine the decay shape of the energy. Two other 8-bit FLASH ADCs digitize the position of the event in the *x* and *y* directions. The output from the FLASH ADCs then passes to the EPF10K10 device.

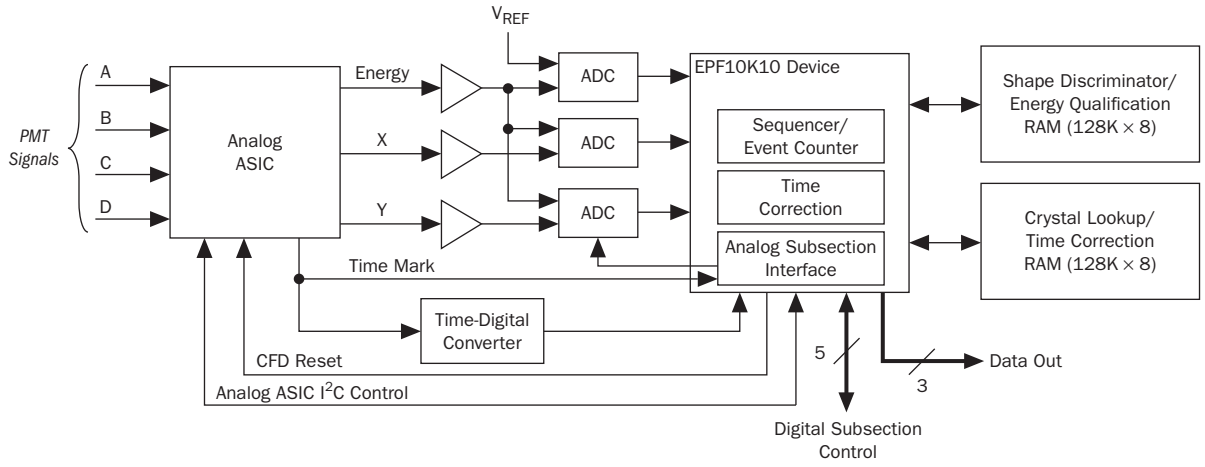
Figure 3. Analog Subsection Board



The PCI/104 computer programs the EPF10K10 device with a control sequencer, which controls the integration time for the energy and the *x* and *y* signals. The sequencer starts when it detects the time mark from the analog ASIC. It clocks the FLASH ADCs and sequences the energy and *x* and *y* signals through the lookup RAM devices.

For this event processing to take place, the EPF10K10 device must be configured during block setup to allow writing to the analog ASIC setup registers and loading the look-up RAM blocks. The PC/104 computer then loads the RAM contents serially. To reduce the time to load the RAMs, the data is compressed using run-length encoding, and the EPF10K10 device is configured to uncompress the RAM data. To load the analog ASIC registers, the I^2C bus operation is loaded into the control register and the analog ASIC data is shifted into the EPF10K10 device, which then controls the I^2C bus signals.

Figure 4. Analog Subsection Block Diagram



continued on page 30

Altera Devices on the Cutting Edge of Medical Technology, continued from page 29

The look-up RAM blocks are used to decrease event processing time and to reduce the amount of logic needed in the Altera devices. The RAM blocks perform the shape discrimination, energy qualification, crystal position determination, and time correction look-up. Two passes are made through the two RAM blocks, which have sufficient memory to hold the look-up data.

On the first pass, the energy signal is used as input to the shape discriminator. The shape discriminator determines the decay constant of the crystal that detected the event. Because the scanner uses crystals with fast and slow decay times, the shape of the energy integration can be used to report the depth of interaction; that is, to determine the location of the event more precisely, an important new feature in the HRRT. The *x* and *y* signal values are used to determine which of the crystals in the block detected the event, using the crystal position look-up table stored in the RAM.

CTI PET Systems chose EPF10K10 devices for their most advanced PET scanner because Altera PLDs can easily be reconfigured in-system.

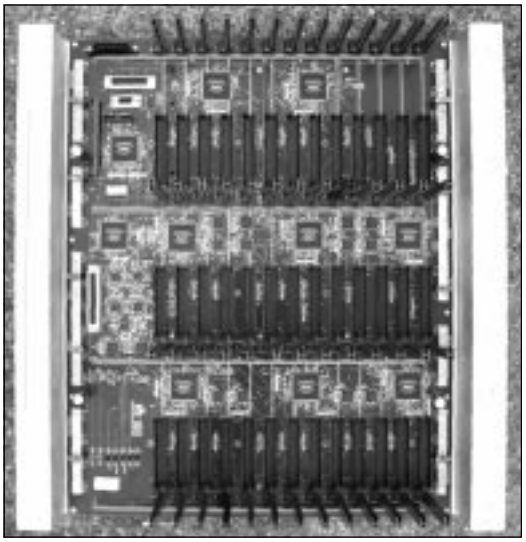
On the second pass, energy qualification determines whether the energy signal level falls within the upper and lower settings given in the energy look-up table for that particular crystal. At the same time, because the signal transmit time may vary based on its location on the PMT, the event time for each crystal is corrected using a time correction look-up table and an adder circuit.

Next, the sequencer sends the event data serially to the detector head interface for priority selection and transmission to the coincidence processor.

The detector head interface prioritizes the multiple events sent by the analog subsection and passes them to the coincidence processor, which has twenty EPF10K30RC208-4 devices. Figure 5 shows a coincidence processor board.

The coincidence processor takes the time difference from the time-to-digital converter values of all the events detected and determines the events that are actually in coincidence

Figure 5. Coincidence Processor Board with Ten EPF10K30RC208-4 Devices



(simultaneous emissions of photons) and those that are random. Next, the real-time sorter converts the raw coincidence data into sinograms, specifying the line along which the event apparently occurred, and accounting for the image plane, time gating, and time sequence selections. The array processor adds the necessary corrections to the sinograms and reconstructs them to form the emission images. The final step in the whole scanning process takes place on the workstation, where the images are displayed for evaluation.

Conclusion

CTI PET Systems chose EPF10K10 devices for their most advanced PET scanner because Altera PLDs can easily be reconfigured in-system. They are able to implement the setup, the detection process, and the self-diagnosis in the same FLEX 10K devices, reducing development time, saving board space, and lowering power consumption and costs. As an added benefit, they are also assured of support for any future changes that may occur in the system requirements or configuration. The ECAT HRRT scanner shows how Altera products are not only being used in manufacturing and communications, but are also creating rapid and accurate solutions in the medical field.

Altera: The DSP Leader for Programmable Logic

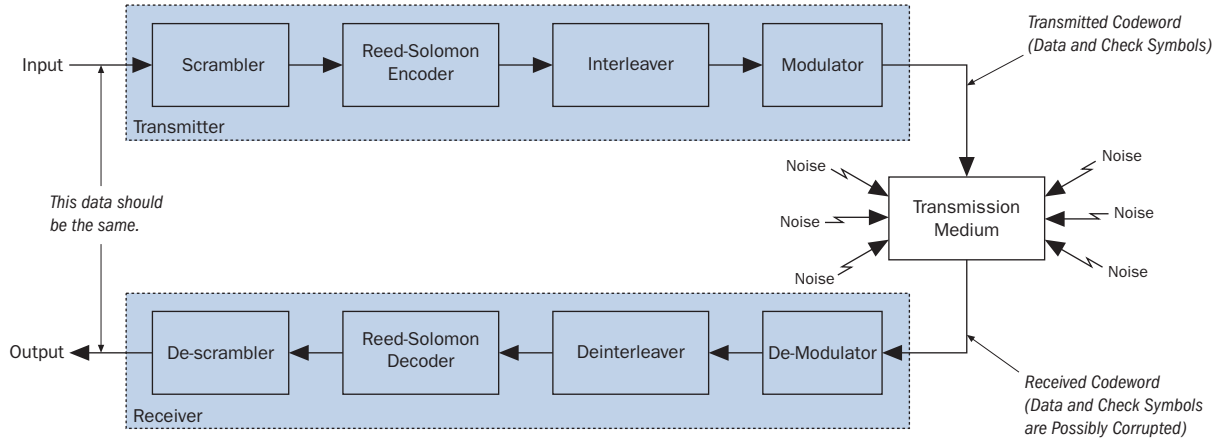
Altera® programmable logic devices (PLDs) provide designers with the flexibility and density necessary to bring their products to market quickly, which is critical for digital signal processing (DSP) applications. In addition to PLDs, Altera offers silicon-proven megafunctions designed specifically for APEX™ and FLEX® devices to accelerate the design process. With over 60 DSP megafunctions, Altera has the largest portfolio of high-performance DSP MegaCore™ functions available, and this selection is constantly expanding. Altera's DSP portfolio consists of functions such as the FIR Compiler, FFT Processor, Symbol Interleaver/Deinterleaver, and Color Space Converter (CSC).

Altera recently added two new DSP error-correction MegaCore functions to the portfolio: the Reed-Solomon Compiler and high-speed Viterbi decoder. These new megafunctions are ideal for wireless and other high-performance communication systems.

The Reed-Solomon Compiler was originally developed by HammerCores, Inc., a company recently acquired by Altera. The acquisition of HammerCores strengthens Altera's position as the industry leader in DSP functions. HammerCores, founded in 1997, created DSP and communications megafunctions optimized for Altera devices. Together, HammerCores and Altera have sold over 120 Reed-Solomon functions during the past two years—more than any other IP provider.

The Reed-Solomon Compiler consists of a continuous, variable, discrete, and streaming decoder megafunction that works seamlessly with the symbol interleaver/deinterleaver MegaCore function. A system-level overview of the Reed-Solomon Compiler is shown in Figure 1. Designers can select any Reed-Solomon polynomial and symbol-bit width by using this megafunction with Altera PLDs. The Reed-Solomon compiler also offers encoding speeds of over 1 Gbyte per second and decoding speeds of 800 Mbytes per second. These fast speeds make the Reed-Solomon function ideal for wireless communication systems, as shown in Figure 2 on page 32. Through the MegaWizard™ Plug-In Manager, designers can

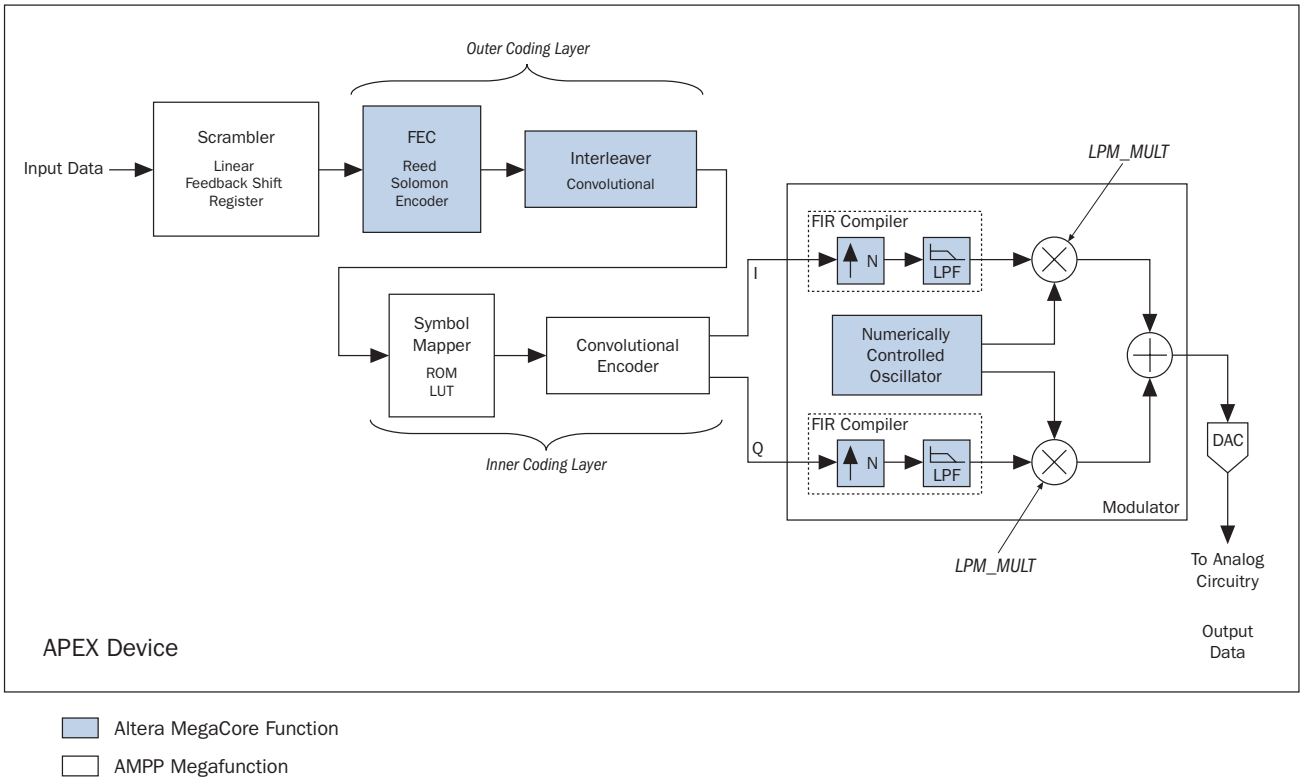
Figure 1. Reed-Solomon System-Level Description



continued on page 32

Altera: The DSP Leader for Programmable Logic,
continued from page 31

Figure 2. Typical Modulator in a Communication System



select either a discrete or a streaming architecture. A discrete architecture uses fewer device resources and only transfers one packet at a time, while a streaming architecture has a higher flow. Additionally, the designer can use the parameters in the MegaWizard Plug-In Manager to optimize the Reed-Solomon compiler for speed or area efficiency.

For applications requiring greater error-correction capabilities, Altera also offers a new high-speed Viterbi decoder MegaCore function. With a 100-megabits per second (Mbps) decoding rate, it is the fastest Viterbi decoder available. This parameterizable megafunction supports both soft and hard decision-making. The new high-speed Viterbi decoder features an integrated test-case generator for Additive White Gaussian Noise (AWGN) and allows designers to optimize the megafunction for either speed or error detection.

OpenCore™ versions of both the Reed-Solomon Compiler and the high-speed Viterbi decoder are available for free from the Altera web site (**http://www.altera.com/IPmegastore**). You can also download other DSP megafunctions for a free evaluation within the Quartus™ or MAX+PLUS® II development systems. These two new MegaCore functions increase the number of options available to designers using Altera devices. North American customers can purchase these new MegaCore functions and other megafunctions from the Altera IP MegaStore™ on the Altera web site.

Enhanced APEX PLLs Aid in Clock Management

Altera has enhanced the phase-locked loop (PLL) circuitry on APEX™ devices to increase device and board-level performance. PLLs minimize clock skew and clock delay, and support clock synthesis applications. To support multiple-clock system-on-a-programmable-chip designs, Altera offers up to four PLLs in APEX 20KE devices.

Clock delay and clock skew affect system timing and printed circuit board (PCB) reliability. To address these issues, designers can use either PLLs found in APEX devices or the alternative digital delay-locked loops (DLLs) found in other programmable and ASIC devices. Although both can be used to reduce the amount of skew and delay for system clocks, PLLs are more flexible than DLLs for frequency synthesis applications.

PLLs in APEX devices help meet the clock management requirements for integrating multiple system-level functions onto a single device. The APEX architecture features up to four PLLs per device and contains ClockLock™, ClockBoost™, and ClockShift™ circuitry for increased performance and flexible clock frequency multiplication and division. Table 1 describes the functions of each circuitry type.

Table 1. APEX PLL Circuitry Features

Circuitry	Description
ClockLock	Reduces internal delay and clock skew between other devices on the PCB.
ClockBoost	Provides programmable clock frequency multiplication and division, and allows time domain multiplexing.
ClockShift	Provides programmable phase shift and precise clock delay management.

PLL Fundamentals

PLL circuits monitor a reference signal, such as a system clock, to manage or synthesize other clocks. In a PLL, a phase comparator measures the difference between the phase and frequency of an external reference signal and an internal feedback signal. Based on this difference, the phase comparator adjusts the voltage-controlled oscillator (VCO), which produces a timing signal clock that is fed back to the phase detector. This signal is compared with the incoming reference signal. When the reference signal and the VCO feedback signal are identical, the PLL is "locked" onto the reference signal. The PLL continues to monitor the reference signal and adjust the VCO output to compensate for any temperature or voltage fluctuations.

Benefits of APEX 20KE PLLs

APEX 20KE PLLs provide the following benefits:

- Provide full multiplication and division capabilities.
- ClockShift circuitry provides fine control of clock phase and clock delay.
- Support for the low-voltage differential signaling (LVDS) standard with data transfer rates up to 622 megabits per second (Mbps).
- Support for very low input clock frequencies (as low as 1.5 MHz).
- Support T1/E1 rate conversions.
- Filtering for high-frequency jitter.
- Able to output 50/50 duty-cycle correction.

PLLs in APEX devices help meet the clock management requirements for integrating multiple system-level functions onto a single device.

ClockBoost Circuitry for Programmable Clock Synthesis

A system clock may run at a different frequency than some of the PCB components. A CPU, for example, may require an internal clock that is several times faster than the system I/O bus clock. The APEX 20KE PLLs provide *m*/*n* scaling that supports frequency multiplication of up to 133× and division by any number up to

continued on page 34

Enhanced APEX PLLs Aid in Clock Management, continued from page 33

106. This advanced feature provides designers with true programmable clock synthesis, greatly enhancing design flexibility and performance. The limited multiplication and division capabilities in DLLs do not address the needs for high-performance designs. For more information on clock synthesis, see "APEX PLLs Offer Advanced Clock Synthesis" on page 17.

APEX 20KE devices have special de-skew circuitry, dedicated parallel-to-serial circuitry, and PLLs that provide 8× clock multiplication to support LVDS at 622 Mbps.

ClockShift Circuitry for Precise Phase & Time Delay Management

APEX 20KE ClockShift circuitry provides programmable phase shift and precise time delay management. The fine clock adjustment uses incremental step delays of 0.5 to 1.0 ns, allowing the output clock to lead or lag the input clock by up to 360°. For example, you can shift an input clock running at 100 MHz (10 ns) by 0 to 10 ns in increments of 0.5 ns. The coarse clock adjustment allows clock phase to be adjusted by 90°, 180°, or 270°. The programmable delay also lets designers implement strict timing margins that cannot be met without clock adjustment. This feature enables designers to improve t_{CO} and t_{SU} times to meet high-speed interface requirements. DLLs are typically limited to 90°, 180°, or 270°, and do not support the fine clock adjustments required by designs with strict timing requirements.

LVDS Support

Low-voltage differential signalling (LVDS) is a high-speed I/O interface standard that supports data rates at speeds up to 622 Mbps. The standard LVDS implementation currently used in discrete chips requires a 7× or 8× clock multiplication. APEX 20KE devices have special de-skew circuitry, dedicated parallel-to-serial circuitry, and PLLs that provide 8× clock multiplication to support LVDS at 622 Mbps. Because DLLs do not support 7× or 8× clock multiplication, it is unlikely that devices relying on them can support the LVDS I/O standard at 622 Mbps.

T1/E1 Conversion Rates

The general-purpose PLLs in APEX 20KE devices can convert T1 input frequencies to E1 frequencies. The T1 telecommunications standard (used in the United States) uses a 1.544-MHz clock rate while the E1 telecommunications standard (used in Europe) uses a 2.048-MHz clock rate. There is a special scaling ratio of 193/256 that is allowed for E1 to T1 clock-rate conversion (and 256/193 for T1 to E1 conversion). Since DLLs do not support such high multiplication and division rates, they cannot perform T1 to E1 and E1 to T1 clock-rate conversions.

Conclusion

APEX PLLs, supported by advanced ClockLock, ClockBoost, and ClockShift circuitry, provide significant improvements in system performance and design versatility by minimizing clock skew and clock delay. The flexible clock synthesis and robust clock shift capabilities of APEX PLLs provide precise phase and delay adjustment. Designers can further increase system performance by minimizing t_{SU} and t_{CO}. PLLs allow support for high-performance I/O standards, such as LVDS, and provide the flexibility and the capability unattainable by DLLs. With these advantages, APEX PLLs dramatically increase system performance.

Questions & Answers

Q *Can the MAX+PLUS® II software read out the USERCODE and UESCODE from a MAX® device?*

A Yes. The MAX+PLUS II software can read out the USERCODE and UESCODE from a MAX device. To read out the USERCODE and UESCODE, perform the following steps:

1. Extract the Programmer Object File (**.pof**) from the device by using the **Examine** feature in the Programmer.
2. Save the extracted POF by choosing **Save Programming Data As** (File menu).
3. With the POF saved and loaded into the Programmer, choose **Info** (File menu) to display the USERCODE or UESCODE.

The USERCODE and UESCODE can be read from a MAX device even if the security bit is turned on.

For more information on USERCODE and UESCODE, refer to *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Q *Can I simulate my design in the Quartus™ software with external pull-up or pull-down resistors?*

A Yes. Designers often wish to see simulation outputs with pull-up or pull-down resistors on pins. The Quartus Simulator can include the effect of weak pull-up and pull-down resistors on output and bidirectional pins. This option is often used in conjunction with OPNDRN or TRI primitives. When the **Passive Resistor** option is turned on, the results show up as a weak high (H) or a weak low (L).

You can turn on this option in the Quartus software by following the steps below:

1. Select the output or bidirectional pin and open the **Assignment Organizer**.
2. Select **Simulation** under the **Assignments** category.
3. Select **Passive Resistor** from the **Assignment** drop down box.
4. Choose **Pull-up** or **Pull-down** from the **Setting** drop down box and click **Add**. Click **OK**.

This setting will model the effect of pull-ups and pull-downs. Since this is a simulation option, you do not need to recompile the project.

Q *Why does my multiple-match content-addressable memory (CAM) not match an input pattern even though I stored the pattern in the CAM?*

A Your input pattern may not match with a multiple-match CAM because the input pattern was not held at the input to the CAM long enough.

Another reason could be that you did not correctly write in the input pattern. Multiple-match CAMs require input patterns to be asserted for at least two clock cycles. If you only apply a pattern for one clock cycle, the multiple-match CAM will not find a match for the pattern. Single-match and fast multiple-match CAMs allow input patterns to be asserted for just one clock cycle.

Q *How does the Turbo Bit™ logic option affect signal edges in MAX devices?*

A When the Turbo Bit logic option is enabled for a macrocell, both the propagation delays for rising and falling edges of the signal are decreased. These decreased propagation delays are shown in MAX+PLUS II simulation under worst-case conditions, where the propagation delays for rising and falling edges have the same delay.

Q *Why do I get the Internal Error: "Sub-system: DBC, File: dbc_root.cpp, Line: 304"*

A You may get this internal error when you compile a design that has been previously compiled using an earlier version of the Quartus software. To avoid this error, choose **Purge Compiler Results from Database** (Processing menu). Alternatively, you can delete the **db** folder in the **Project** directory.

continued on page 36

Questions & Answers, continued from page 35

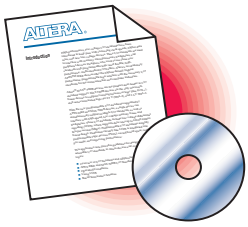
Q *Can I program my MAX 7000B device with my MAX 7000AE programming file?*

A You can program a MAX 7000B device with the POF, Jam™ File (**.jam**), or Jam Byte-Code File (**.jbc**) of an equivalent-density MAX 7000AE device. Jam and JBC Files must be generated with a version of the MAX+PLUS II software that can program MAX 7000B devices.

If you use a MAX 7000AE POF, Jam, or JBC File, the MAX 7000B I/O pins are programmed as low-voltage transistor-transistor logic (LVTTL) pins and the dual-purpose voltage reference V_{REFIO} pins are programmed as I/O pins.

You cannot program a MAX 7000B device with a MAX 7000AE Serial Vector File (**.svf**).

New Altera Publications



New publications are available from Altera Literature Services. Individual documents are available on the Altera web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- ***Altera Digital Library CD-ROM***, version 2000.01 (P-CD-ADL2000-01)
- *AN 114: Designing with FineLine BGA Packages* (A-AN-114-01)
- *AN 123: Using Timing Analysis in the Quartus Software* (A-AN-123-01)
- *SB 46: FLEX PCI Development Kit* (A-SB-046-01)
- *TB 58: In-Circuit Test Support with MAX 7000 Devices* (M-TB-058-01)
- *TB 60: Advantages of APEX PLLs over Virtex DLLs* (M-TB-060-01)
- *TB 61: CAM Comparison: APEX 20KE vs. Virtex-E Devices* (M-TB-061-01)
- *TB 62: MAX 7000AE Performance Comparison* (M-TB-062-01)
- *ARCTAN Function White Paper* (M-WP-HC-ARCTAN-01)
- *CORDIC Functions CDPP & CDPS White Paper* (M-WP-HC-CORDIC-01)
- *DES Cores White Paper* (M-WP-HC-DES-01)
- *NCO Core White Paper* (M-WP-HC-NCO-01)
- *u-Law Companders & A-Law Compander White Paper* (M-WP-HC-COMPAND-01)
- *Using APEX 20K & APEX 20KE PLLs in the Quartus Software White Paper* (M-WP-APQUARTUS-01)
- *Using I/O Standards in the Quartus Software White Paper* (M-WP-QUARTUSIO-01)
- *Using LVDS in APEX 20KE Devices White Paper* (M-WP-LVDSAPEX-01)
- *Viterbi Decoders White Paper* (M-WP-HC-VITERBI-01)

Current Software Versions

The Quartus™ version 2000.02 software is the latest release, and is available for the following operating systems:

- Microsoft Windows 98
- Microsoft Windows NT
- Sun Solaris version 2.6
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported

The MAX+PLUS® II version 9.5 software is available for the following operating systems:

- Microsoft Windows 95 and Windows 98
- Microsoft Windows NT version 3.51 and higher
- Sun Solaris version 2.5 and higher
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported
- AIX version 4.1 and higher

Altera Programming Support

Programming Hardware Support

Table 1 contains the latest programming hardware information for Altera® MAX® 9000, MAX 7000, MAX 3000, and configuration devices. For correct programming, use the software version shown in "Current Software Versions" on page 6.

Table 1. Altera Programming Adapters (Part 1 of 3) Note (1)

Device	Package	Adapter
EPC1064 (2) EPC1064V (2) EPC1441 (3)	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 (3) EPC1213 (2)	DIP, J-lead	PLMJ1213
EPC2 (4)	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC (5)
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC (5) PLMR9000-240NC (5)
EPM7032	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032B	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

Table 1. Altera Programming Adapters (Part 2 of 3) Note (1)

Device	Package	Adapter
EPM7064S	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC (5)
EPM7064AE EPM7064B	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin) FineLine BGA (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC (5) PLMF7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A EPM7128AE EPM7128B EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) TQFP (144-pin) PQFP (160-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMJ7000-84 PLMQ7000-100NC (5) PLMT7000-100NC (5) PLMT7000-144NC (5) PLMQ7128/7160-160NC (5) PLMF7000-100 PLMF7000-256
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC (5) PLMQ7128/7160-160NC (5)
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC (5)

continued on page 38

Altera Programming Support, continued from page 37

Table 1. Altera Programming Adapters (Part 3 of 3) *Note (1)*

Device	Package	Adapter
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A EPM7256S EPM7256AE EPM7256B	TQFP (100-pin) TQFP (144-pin) PQFP (208-pin) RQFP (208-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMT7256-208NC *(5)* PLMF7000-100 PLMF7000-256
EPM7512AE EPM7512B	TQFP (144-pin) PQFP (208-pin) BGA (256-pin) FineLine BGA (256-pin)	PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMB7000-256 PLMF7000-256
EPM3032A	J-lead (44-pin) TQFP (44-pin)	PLMJ3000-44 PLMT3000-44
EPM3064A	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ3000-44 PLMT3000-44 PLMT3000-100NC *(5)*
EPM3128A	TQFP (100-pin) TQFP (144-pin)	PLMT3000-100NC *(5)* PLMT3000-144NC *(5)*
EPM3256A	TQFP (144-pin) PQFP (208-pin)	PLMT3000-144NC *(5)* PLMR3256-208NC *(5)*

Notes:

(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on Classic™ devices.
(2) FLEX® 8000 configuration device.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(4) APEX™ 20K, FLEX 10K, or FLEX 6000 configuration device.
(5) These devices are not shipped in carriers.

Third-Party Programming Support

Data I/O, BP Microsystems, and System General provide programming hardware support for selected Altera devices. Algorithms are available on these companies' respective web sites (**http://www.data-io.com**, **http://www.bpmicro.com**, **http://www.sg.com.tw**). Programming support information for configuration, MAX 9000, and MAX 7000 devices is shown in Table 2. All information is subject to change.

Table 2. Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*	System General *(3)*
EPC1064	✓	✓	✓ *(4)*
EPC1213	✓	✓	✓ *(4)*
EPC1	✓	✓	✓ *(4)*
EPC1441	✓	✓	✓ *(4)*
EPC2	*(5)*	✓	✓ *(4)*
EPM3032A	✓	✓	✓ *(4)*
EPM3064A	✓	✓	✓ *(4)*
EPM3128A	*(5)*	✓	✓ *(4)*
EPM3256A	*(5)*	*(5)*	✓ *(4)*
EPM7032	✓	✓	✓ *(4)*
EPM7032AE	*(5)*	✓	✓ *(4)*
EPM7032S	✓	✓	✓ *(4)*
EPM7064	✓	✓	✓ *(4)*
EPM7064AE	✓	✓	✓ *(4)*
EPM7064S	✓	✓	✓ *(4)*
EPM7096	✓	✓	✓ *(4)*
EPM7128A	✓	✓	✓ *(4)*
EPM7128S	✓	✓	✓ *(4)*
EPM7128AE	*(5)*	✓	✓ *(4)*
EPM7128E	✓	✓	✓ *(4)*
EPM7160E	✓	✓	✓ *(4)*
EPM7192S	✓	✓	✓ *(4)*
EPM7192E	✓	✓	✓ *(4)*
EPM7256A	*(5)*	✓	✓ *(4)*
EPM7256AE	*(5)*	*(5)*	✓ *(4)*
EPM7256S	✓	✓	✓ *(4)*
EPM7256E	✓	✓	✓ *(4)*
EPM7512AE	*(5)*	✓ *(6)*	✓ *(4), (5)*
EPM9320	✓	✓	✓ *(4)*
EPM9320A	✓	✓	✓ *(4)*
EPM9400	✓	✓	✓ *(4)*
EPM9480	✓	✓	✓ *(4)*
EPM9560	✓	✓	✓ *(4)*
EPM9560A	✓	✓	✓ *(4), (5)*

Notes to Table 2:
(1) These devices are supported by the Data I/O UniSite programmer version 6.2.
(2) These devices are supported by BP Microsystems programmers version 3.46a.
(3) These devices are supported by System General programmers version 1.03.
(4) Although these devices are currently supported, Altera is in the process of verifiying the programming hardware support.
(5) Contact Data I/O, BP Microsystems, or System General about programming support for these devices.
(6) Contact Data I/O, BP Microsystems, or System General about programming support for 256-pin ball-grid array (BGA) and FineLine BGA™ packages.

Download Cables

Table 3 provides programming and configuration compatibility information for the MasterBlaster™ serial or universal serial bus (USB) communications cable and the BitBlaster™ serial and ByteBlasterMV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable.)

Table 3. Download Cable Compatibility

Device	MasterBlaster *(1)*	ByteBlasterMV	BitBlaster *(2)*
APEX 20K	✓	✓ *(3)*	
APEX 20KE	✓	✓ *(3)*	
FLEX 10K	✓	✓	✓
FLEX 10KA	✓	✓	✓
FLEX 10KE	✓	✓	✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A	✓	✓	✓
MAX 7000B	✓	✓ *(3)*	
MAX 3000A	✓	✓	✓

Notes:
(1) The MasterBlaster communications cable can be used with the Quartus software for device download and SignalTap logic analysis. It can also be used with the MAX+PLUS II software version 9.3 for device downloads.
(2) The BitBlaster download cable must operate at 5.0 V.
(3) The ByteBlasterMV download cable must operate at 3.3 V for these devices. `VCCIO` pins can be set to either 2.5 V or 3.3 V.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera.

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	General Literature Request *(2)*	**lit_req@altera.com**	**lit_req@altera.com**
	News & Views Subscriptions and Address Changes	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline	(800) 800-EPLD (6 a.m. to 6 p.m. Pacific Time) (408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time) *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**support@altera.com**	**support@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**

Notes:
(1) The ***MAX+PLUS II Getting Started*** and ***Quartus Tutorial*** manuals are available from the Altera® web site. To obtain other Quartus™ and MAX+PLUS® II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

Discontinued Devices Update

Altera's EPM7032V device is discontinued. Details about this product's obsolescence are available in product discontinuance notice (PDN) 9907.

Altera distributes advisories (ADVs) and PDNs that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

Altera Device Selection Guide

Current information for the Altera® APEX™ 20K, FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, MAX 7000, MAX 3000, and configuration devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide*.

For the most up-to-date information, go to the Altera web site at **http://www.altera.com**. Some of the devices listed may not yet be available. Contact Altera or your local sales office for the latest device availability.

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[1]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	MACROCELLS
EP20K30E	30,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 324-Pin BGA[2]	92, 108, 128, 128	1.8 V	1,200	24,576	192
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 108, 151, 183, 204, 204	1.8 V	2,560	32,768	256
EP20K100	100,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	101, 106, 159, 189, 252, 252	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 108, 151, 183, 246, 246	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	87, 143, 175, 273, 324	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2]	144, 174, 279, 382	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 652-Pin BGA, 672-Pin BGA[2]	136, 168, 273, 376, 376, 376	1.8 V	8,320	106,496	832
EP20K300E	300,000	208-Pin RQFP, 240-Pin RQFP, 652-Pin BGA, 672-Pin BGA[2]	120, 152, 408, 408	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin BGA[2]	502, 502, 502	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	652-Pin BGA, 672-Pin BGA[2]	488, 488	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 508, 588	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin BGA[2], 984-Pin PGA, 1,020-Pin BGA[2]	488, 508, 716, 708	1.8 V	38,400	327,680	2,560
EP20K1500E	1,500,000	652-Pin BGA, 984-Pin BGA[2], 1,020-Pin BGA[2]	488, 858, 808	1.8 V	51,840	442,368	3,456

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 189, 191, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA 672-Pin BGA[2]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[2]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA, 672-Pin BGA[2]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	71, 102	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	81, 81, 117, 171, 171	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[2]	117, 171, 199, 218, 218	3.3 V	-1, -2, -3	1,960	1,960

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[3]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[3]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[3]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX, FLEX 10K, FLEX 10KE, and FLEX 6000 devices
EPC4E[4]	44-Pin TQFP, 84-Pin BGA[5]	2.5/3.3 V	4-Mbit serial/parallel configuration device designed to configure all APEX and FLEX 10K devices.

continued on page 42

Altera Device Selection Guide, continued from page 41

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032B	32	44-Pin PLCC/TQFP, 48-Pin TQFP	36, 36	2.5 V	-3, -5, -7
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064AE	64	44-Pin PLCC/TQFP, 49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68	3.3 V	-4, -7, -10
EPM7064B	64	44-Pin PLCC/TQFP, 48-pin TQFP, 49-Pin BGA[1], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68, 68	2.5 V	-3, -5, -7
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 256-Pin BGA[2]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[5], 256-Pin BGA[2]	68, 84, 84, 100, 100, 100	3.3 V	-5,-7,-10
EPM7128B	128	49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[5], 256-Pin BGA[2]	40, 84, 84, 100, 100, 100	2.5 V	-4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S	256	208-Pin PQFP	164	5.0 V	-7, -10, -15
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 84, 120, 164, 164	3.3 V	-5, -7, -10
EPM7256B	256	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 164, 164, 164	2.5 V	-5, -7, -10
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	120, 176, 212, 212	3.3 V	-7, -10, -12
EPM7512B	512	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 212, 212, 212	2.5 V	-6, -7, -10

MAX 3000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM3032A	32	44-Pin PLCC, 44-Pin TQFP	34, 34	3.3 V	-4, -7, -10
EPM3064A	64	44-Pin PLCC, 44-Pin TQFP, 100-Pin TQFP	34, 34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-Pin TQFP, 144-Pin PQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-Pin TQFP, 208-Pin PQFP	116, 158	3.3 V	-5, -7, -10

MAX 9000 Devices

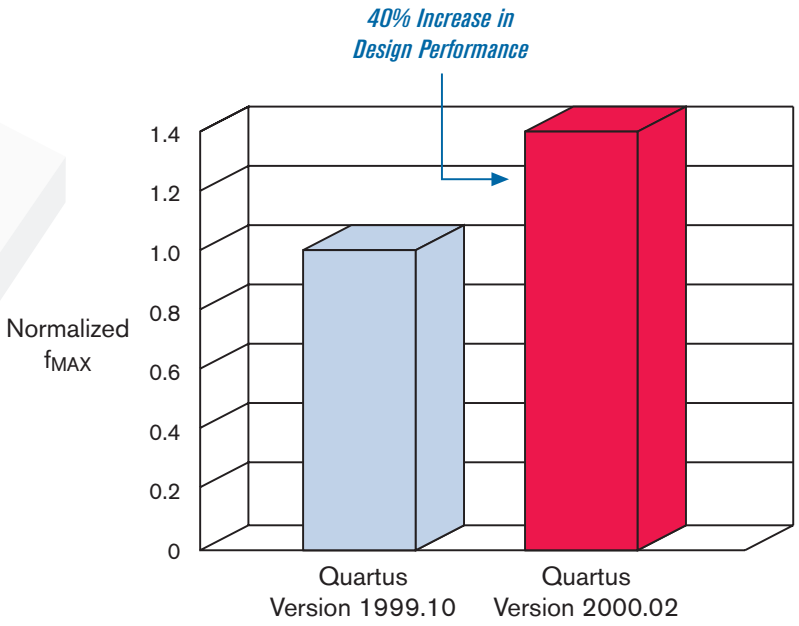
DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

Notes to Tables:

(1) Preliminary. Contact Altera for latest information.
(2) This package is a space-saving FineLine BGA package.
(3) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.
(4) This device can be programmed by the user to operate at either 2.5 V or 3.3 V.
(5) This package is a space-saving Ultra FineLine BGA package, Altera's newest 0.8-mm BGA package.

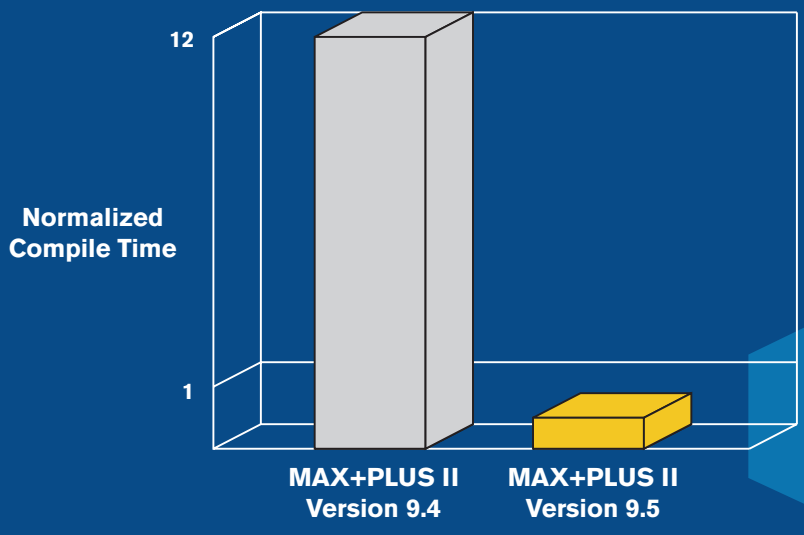
Improved Performance with Quartus Version 2000.02

- New timing-driven comilation algorithms improve performance by over 40%
- Now shipping



MAX+PLUS II Version 9.5 Offers Significant Performance Boost

FLEX 10K Designs Compile 30× Faster



- Optimized timing-driven compilation algorithms for FLEX 10K devices
- Compile times up to 30× faster
- Up to 30% higher design performance
- Now Shipping

Dynamite solutions.

When you're counting on a high-performance breakthrough, Altera's APEX™ device family is the perfect solution.

APEX™

The APEX MultiCore™ architecture combines look-up table and product-term logic with dual-port RAM and content-addressable memory to ensure maximum internal performance. Embedded LVDS circuitry and up to four phase-locked loops (PLLs) provide support for data rates of up to 622 Mbps. With device I/O bandwidth over 200 Gbits/second and up to 1.5 million gates (2.5 million maximum system gates), APEX offers a true system-on-a-programmable-chip (SOPC) solution.

Eliminate design barriers.

The Altera Quartus™ development software enhances productivity and shortens design cycles. A variety of MegaCore™ and AMPP℠ intellectual property megafunctions, optimized for the APEX architecture, are available to further streamline development.

No time to lose.

Find the speed you need. Visit the Altera web site at http://www.altera.com/dynamite to find out how Altera's system-on-a-programmable-chip solution—the APEX solution—can save the day.

APEX Performance Features

- 64-bit, 66-MHz PCI compliant
- LVDS bandwidth of up to 20 Gbits/second
- Multiple 622-Mbps LVDS channels
- Up to four PLLs for ClockLock™, ClockBoost™, and ClockShift™ capabilities
- Support for multiple low-voltage, high-bandwidth I/O standards
- Embedded CAM support for high-performance networking applications

ALTERA®

The Programmable Solutions Company™

http://www.altera.com/dynamite

The System-on-a-Programmable-Chip Solution.