News & Views

Third Quarter, 2000

Newsletter for Altera Customers

MAX 7000B

2.5-V ISP
Now Shipping

ALTERA MAX
EPM7128BFC100-4

MAX 7000B Devices Maintain Leadership Through Innovation & Technology

Altera has successfully rolled out the industry's fastest product-term-based device family: MAX® 7000B devices. Fabricated using advanced 0.22-μm CMOS technology, MAX 7000B devices offer propagation delays as fast as 3.5 ns and counter frequencies of over 200 MHz. MAX 7000B devices are also the most feature-rich product-term-based devices in the programmable logic device (PLD) industry.

MAX 7000B devices provide a tremendous performance advantage, especially in the higher macrocell count (256 and 512 macrocell) designs. As Table 1 shows, the fast propagation delays offered by MAX 7000B devices extend Altera's performance leadership in the marketplace.

Low-Power Leader in the High-Performance Spectrum

MAX 7000B devices also have the lowest power consumption for high-performance applications. Power consumed by a device is a function of the operating current as well as the operating core voltage (Power = Voltage × Current). Because the MAX 7000B core operates at 2.5 V, these devices consume 30% less power than 3.3-V Altera CPLDs.

MAX 7000B devices also feature a programmable power-saving mode, allowing you to configure one or more macrocells to operate at less than 50% of the normal power while adding only a nominal timing delay. This feature allows intelligent speed/power tradeoffs for different portions of the design. At high operating frequencies, MAX 7000B devices are a clear industry leader in low-power consumption.

Advanced I/O Standards Support

Altera MAX 7000B devices are the leader in advanced I/O standard support. These devices are the only product-term architecture capable
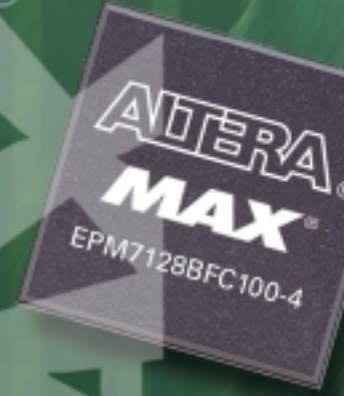
Table 1. Typical Propagation Delay Times

Macrocell Range	Propagation Delay Times (ns)			
	MAX 7000B *(1)*	**XC9500XL** *(1)*	**CoolRunner** *(1)*	**ispLSI2000VE** *(2)*
32 to 36	**3.5**	5.0	5.0	4.5
64 to 72	**3.5**	5.0	6.0	5.0
128 to 144	**4.0**	5.0	6.0	6.0
192 to 288	**5.0**	7.5	7.5	7.0
512 and higher	**5.5**	–	–	–

Notes:
(1) t_{PD} values taken from device literature.
(2) t_{PD} value through a typical logic path consisting of five product-term elements and the output routing pool.

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MAX 7000B Devices Maintain Leadership through Innovation & Technology, continued from page 1

of supporting GTL+, SSTL-3, and, SSTL-2. Table 2 compares the I/O standards supported by MAX 7000B devices to other devices.

Table 2. Competitive Comparison of I/O Standards				
I/O Standard	MAX 7000B	XC9500XV (2.5 V)	ispLSI2000VL (2.5 V)	CoolRunner (XPLA3-XL)
GTL+	✓			
SSTL-2 class I and II	✓			
SSTL-3 class I and II	✓			
LVTTL	✓	✓	✓	✓
LVCMOS	✓	✓	✓	✓
2.5 V	✓	✓	✓	
1.8 V	✓	✓	✓	
64-bit, 66-MHz PCI	✓			

Support for advanced I/O standards (GTL+, SSTL-2, and SSTL-3) allows designers to use MAX 7000B devices in high-speed design applications such as processor interfaces, backplane drivers, and SDRAM memory interfaces.

Programming Times Leader

Preliminary results show that MAX 7000B devices have programming times equivalent to MAX 7000AE devices. In a production environment, quick programming times represent substantial savings in overall cost.

In a manufacturing flow, each extra second spent on programming adds about $0.10 to $0.25 to the system cost. MAX 7000B devices can be programmed in a fraction of the time required to program the Xilinx XC9500XL devices, as shown in Table 3.

Table 2. Programming Times with In-Circuit Testers	
Device	Programming Time with 2-MHz TCK Rate
EPM7128B (erase, program, and verify)	2.2 seconds
XC95144XL (erase, program, and verify)	1.6 minutes
XC95144XL (program and verify only)	1.5 minutes

Using a Xilinx CPLD instead of a MAX 7000B device can add between $9.40 to $23.50 in programming cost alone.

MAX 7000B Versatility

MAX 7000B devices range in density from 32 to 512 macrocells and are offered in a wide range of packages, including 1.0-mm FineLine BGA™ and 0.8-mm Ultra FineLine BGA packages.

MAX 7000B devices offer vertical migration across devices (as shown in Table 4), and also support the SameFrame™ pin-out feature for FineLine BGA and Ultra FineLine BGA packages, providing designers additional flexibility for package migration.

By offering a wide range of density, package, and speed grade options, MAX 7000B devices present an ideal solution for today's high-performance designs.

Table 4. MAX 7000B Package Migration Paths										
Device	Package									
	44-Pin PLCC	44-Pin TQFP	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	169-Pin Ultra FineLine BGA	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA
EPM7032B	✓	✓	✓							
EPM7064B	✓	✓	✓	✓	✓					
EPM7128B			✓	✓	✓	✓	✓			✓
EPM7256B				✓		✓	✓	✓		✓
EPM7512B						✓	✓	✓	✓	✓

APEX 20KE True-LVDS Solution Enables 840-Mbps Data Rate

With the latest advancements in next generation communication systems, the requirement for higher bandwidth and I/O performance has increased dramatically. This increase has been assisted by the creation of newer I/O standards such as the LVDS standard. LVDS has been identified as the best solution for communication applications because of its high performance, high noise immunity, and low power consumption.

To combine these benefits with the inherent advantages of the programmable logic devices (PLDs) such as flexibility and time-to-market, Altera has incorporated True-LVDS™ dedicated circuitry within the APEX™ 20KE family of devices. The True-LVDS solution in the APEX 20KE devices makes them industry's first system-on-a-programmable-chip (SOPC) solution to support data transfer rate up to 840 Megabits per second per channel.

This article outlines the robust performance of the True-LVDS circuitry in APEX 20KE devices through the following features:

■ High speed data transfer rates of up to 840 Mbps per channel
■ Dedicated LVDS circuitry such as LVDS Transmitter and LVDS Receiver
■ High quality true differential I/O drivers
■ Easy design flow in Quartus™ software
■ Integrated deskew circuitry
■ Low power consumption
■ Simple board-level design requirements

True-LVDS Solution

The APEX 20KE True-LVDS solution not only provides a high data transfer rate of up to 840 Mbps per channel, but also offers high noise immunity, low power consumption, and low electromagnetic interference (EMI), benefits that are utilized by high-speed communication applications. The True-LVDS solution is made possible by the following innovative technology:

■ Dedicated receiver and transmitter circuitry performing serial-to-parallel and parallel-to-serial conversions makes the high toggle rates (840 Mbps) possible.

Figure 1. APEX EP20K400E LVDS I/O Performance at 840 Mbps

The APEX 20KE True-LVDS solution is very easy to implement via push button compilation support in the Quartus software tool.
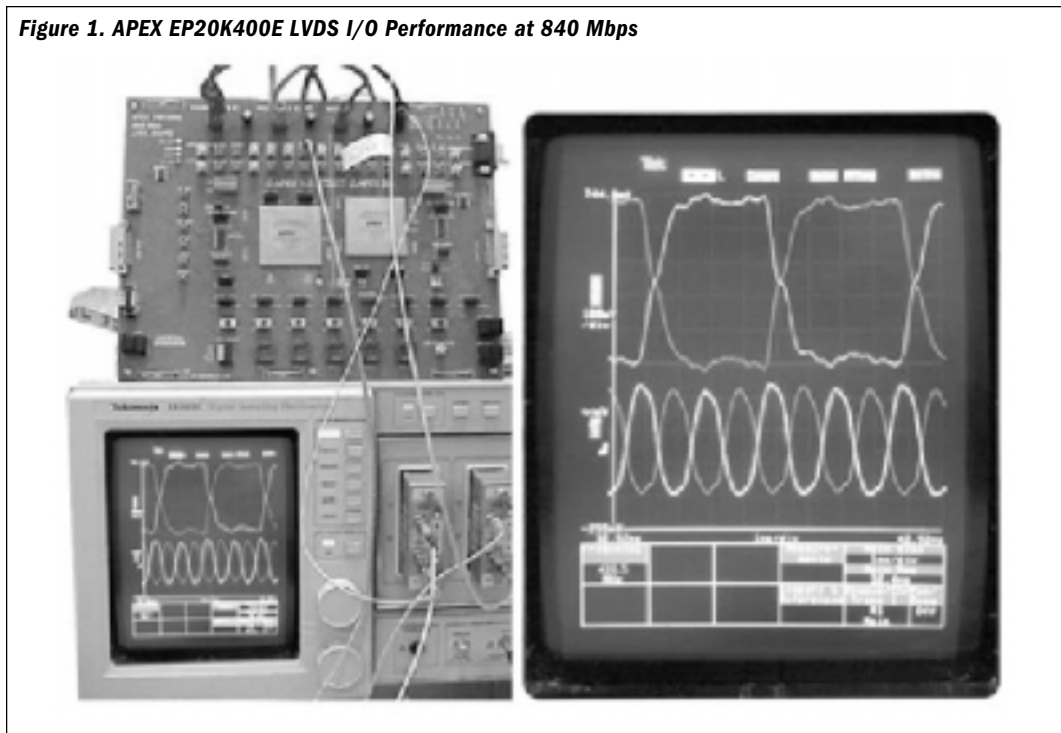
- On-chip phase-locked loop (PLL) circuitry with 8× multiplication internally boosts the input clock to 840 MHz.
- Dedicated deskew circuitry ensures clock and data signals are internally aligned.
- True differential I/O drivers enable high noise immunity, low power consumption, and low EMI.

True-LVDS Performance

The APEX 20KE True-LVDS feature has been verified to run at 840 Mbps per channel under worst-case conditions. This confirms the robustness of the APEX 20KE True-LVDS feature. Figure 1 on page 5 shows the performance of True-LVDS circuitry at 840 Mbps.

When analyzing LVDS I/O performance, it is important to consider various specifications including channel skew on the output pins and maximum receiver input skew margin. These specifications are required to determine LVDS system performance. They also indicate whether the data captured by a particular channel will be correct or not. Table 1 defines the specifications and provides the APEX 20KE LVDS values at 840 Mbps.

Table 1. APEX 20KE True-LVDS Specifications

Specification	Definition	APEX 20KE True-LVDS Values
f_{LVDSDR}	Maximum LVDS data transfer rate	840 Mbps
TCCS	Transmitter channel-to-channel skew	400 ps
SW	Sampling window: required time that data must be stable for LVDS receiver to capture it.	440 ps
RSKM	Receiver input skew margin: allowable board skew, specified with de-skew feature engaged	473 ps

True-LVDS Quality

The overall quality of the LVDS I/O is typically measured using an "eye diagram" generated by a data sampling oscilloscope. An "eye diagram" is a visual representation of the jitter and output driver quality of an LVDS output signal. It is obtained by sending pseudo-random data over the LVDS channel and using a sampling oscilloscope to perform a persistence measurement. The transitions are captured and plotted over time. Horizontal eye closure is due to jitter, while vertical eye closure is due to signal attenuation or noise. Therefore, a larger "eye" indicates a better quality driver. Figure 3 shows the "eye diagram" for an APEX EP20K400E device operating at 840 Mbps data rate.

True-LVDS Software Support

The APEX 20KE True-LVDS solution is very easy to implement via push button compilation support in the Quartus™ software tool. The `altlvds_tx` and `altlvds_rx` megafunctions shown in Figure 2 are available in the Quartus software and allow for drop-in implementation of the LVDS Transmitter and LVDS Receiver, respectively. Designers can customize the number of channels, operating frequency, and data transfer modes for these megafunctions, thereby gaining greater design flexibility.

Figure 2. altlvds & altlvds_rx Megafunctions

```
                                    NUMBER_OF_CHANNELS=16
                                    DESERIALIZATION_FACTOR=4
                                    REGISTERED_OUTPUT="ON"
                                    INCLOCK_PERIOD
        altlvds_rx
    rx_in[]        rx_out[]
    rx_inclock     rx_outclock
    rx_deskew      rx_locked
  inst

                                    NUMBER_OF_CHANNELS=16
                                    DESERIALIZATION_FACTOR=4
                                    REGISTERED_OUTPUT="ON"
                                    MULTI_CLOCK="OFF"
                                    INCLOCK_PERIOD
                                    CLOCK_SETTING="UNUSED"
        altlvds_tx
    tx_in[]        tx_out[]
    tx_inclock     tx_outclock
    sync_inclock   tx_locked
  inst1
```

Figure 3. LVDS Eye Diagram at 840 Mbps
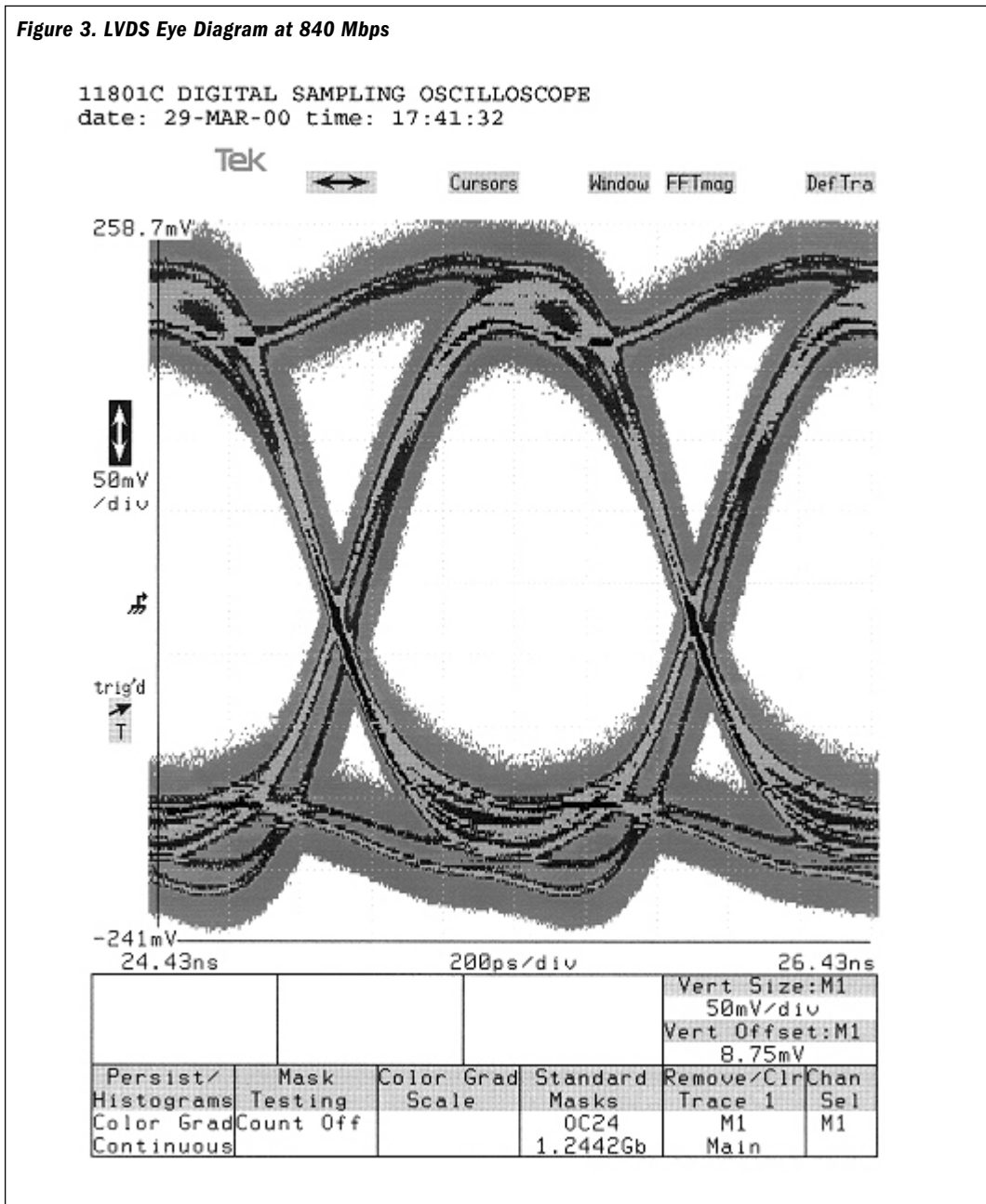
The APEX 20KE True-LVDS solution is ideal for telecommunication, data communication, and computing applications.

The APEX 20KE True-LVDS feature supports the 1×, 4×, 7×, and 8× data transfer modes that allow the designer to interface with other industry-standard LVDS devices such as the National Semiconductor LVDS chip that uses the 7× mode.

True-LVDS Applications

APEX 20KE True-LVDS solution is ideal for telecommunication, data communication, and computing applications. The 840 Mbps data transfer rate provides full support for Dense Wave Division Multiplexing (DWDM) systems transmitting and receiving OC-12 data with Reed-Solomon forward error correction encoding running at 666 Mbps per channel.

With LVDS, APEX 20KE devices offer the highest performance, highest bandwidth, and lowest power system-on-a-programmable-chip solution for high speed data transmission designs.

Devices&Tools

APEX

APEX EP20K1500E Devices Now Shipping

The largest APEX™ 20KE device, the APEX EP20K1500E device, is now shipping. With a maximum of 2.4 million system gates, 51,840 logic elements (LEs), 416 KBytes of RAM, and 808 user I/O pins, this device addresses the needs of system-on-a-programmable-chip (SOPC) applications.

Nine out of the ten APEX 20KE family members are now shipping, including the EP20K60E, EP20K100E, EP20K160E, EP20K200E, EP20K300E, EP20K400E, EP20K600E, EP20K1000E, and EP20K1500E devices. The smallest APEX 20KE device, the EP20K30E device, is scheduled to be available in the fourth quarter of 2000. These devices are available in multiple packages, including the FineLine BGA™ package.

APEX 20KE Devices Support Advanced I/O Standards

APEX 20KE devices offer support for many advanced I/O standards, including LVDS. The APEX True-LVDS™ dedicated circuitry has data transfer rates as high as 840 megabits per second (Mbps) per channel and is ideal for high-speed telecommunication, data communication, and computing applications. APEX 20KE devices also support the low-voltage positive emitter coupled logic (LVPECL) standard that can be used in high-performance clocking schemes, backplanes, optical transceivers, high-speed networking, and high-end video applications.

5.0-V Tolerant APEX 20K & APEX 20KE Devices

The APEX 20K device family has been enhanced to provide a 5.0-V tolerant I/O buffer, providing full compliance with the 5.0-V PCI specification. 5.0-V tolerant devices are now shipping and have a "V" suffix in the ordering code (e.g., EP20K400BC652-1V).

Table 1. APEX 20KE Device & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K30E	144-pin TQFP (1)	Q3 2000
	144-pin FineLine BGA	Q3 2000
	208-pin PQFP (1)	Q3 2000
	324-pin FineLine BGA	Q3 2000
EP20K60E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA (1)	Now
EP20K100E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	Now
EP20K160E	144-pin TQFP	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K200E	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K300E	240-pin PQFP	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K400E	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1500E	652-pin BGA	Now
	1,020-pin FineLine BGA	Now

Note:
(1) TQFP: thin quad flat pack, PQFP: plastic quad flat pack, BGA: ball-grid array.

You can use APEX 20KE devices with an additional external resistor to make these devices 5.0-V tolerant and provide flexibility for system design. The technical details for this improvement are described in the Altera *5.0-V Tolerance in APEX 20KE Devices White Paper*.

APEX 20K Product Transition

Altera is migrating the 2.5-V EP20K400 device from a 0.25-µm process to a 0.22-µm process. Information regarding this device migration can be found in process change notification (PCN) 0005, available on the Altera web site at **http://www.altera.com**.

ACEX

ACEX 1K Devices Shipping Now

ACEX™ 1K devices are now shipping in all packages for 30,000-, 50,000-, and 100,000-gate densities (see Table 2). These cost-optimized devices are especially well suited for low-cost, high-performance communications applications, and can be used to attain the lowest cost per programmable logic device (PLD) for high-volume designs.

Table 2. ACEX 1K Device Offerings		
Device	**Package**	**Availability**
EP1K10	100-pin TQFP	September 2000
	144-pin TQFP	September 2000
	208-pin PQFP	September 2000
	256-pin FineLine BGA	September 2000
EP1K30	144-pin TQFP	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
EP1K50	144-pin TQFP	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now
EP1K100	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now

ACEX 1K devices provide full phase-locked loop (PLL) capability for ClockLock™ and ClockBoost™ features in every -1 and -2 speed grade device, embedded dual-port RAM, and

full 64-bit, 66-MHz PCI compliance. Developed on an innovative 0.22-µm/0.18-µm hybrid process, and featuring a 2.5-V core operating voltage, ACEX 1K devices offer an ideal combination of cost, performance, and features.

Full software support for ACEX 1K devices is available from the MAX+PLUS® II software version 10.0. In addition, a wide range of ACEX-optimized intellectual property (IP) functions can now be found at the Altera IP MegaStore™ on-line store.

FLEX

All FLEX 10KE Devices Available

All EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices are now shipping in -1, -2, and -3 speed grades. These devices are fabricated on a 0.22-µm process and have a programmable input buffer delay for full 64-bit, 66-MHz PCI compliance.

FLEX® 10KE devices are offered with the PLL feature in -1 and -2 speed grades to reduce clock skew and allow clock multiplication. These devices have an "X" suffix in the ordering code (e.g., EPF10K100EQC208-1X). The MAX+PLUS II software now offers design support for all device package options. Table 3 on page 10 shows all of the 2.5-V FLEX 10KE device packages and speed grades.

FLEX 10K Product Transitions

2.5-V EPF10K50E and EPF10K200E devices have migrated from a 0.25-µm process to a 0.22-µm process. All other FLEX 10KE devices are already manufactured on a 0.22-µm process. EPF10K50V devices are migrating from a 0.30-µm 3-layer-metal process to a 0.30-µm 4-layer-metal process in September 2000. 5.0-V EPF10K40 and EPF10K70 devices are migrating from 0.5 µm to 0.42 µm in October and December, respectively. Table 4 on page 10 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com**.

ACEX 1K devices are now shipping in all packages in the 30,000, 50,000, and 100,000 gate densities.

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FLEX®

All FLEX 10KE devices are now available in industrial-temperature grades.

Table 3. FLEX 10KE Devices

Device	Offerings	Speed Grade
EPF10K30E	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K50S	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K100E	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K130E	240-pin PQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X
EPF10K200S	240-pin RQFP *(1)*	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL (all packages)	-1X, -2X

Note:
(1)   RQFP: power quad flat pack,

FLEX 10KE Industrial-Temperature Devices

All FLEX 10KE devices are now available in industrial-temperature grades. Table 5 lists the industrial-temperature FLEX 10KE devices.

Table 4. FLEX 10K Device Migration

Device	Core Voltage (V)	Date	Reference	Process (μm)
EPF10K10A	3.3	Done	PCN 9810	0.30
EPF10K30A	3.3	Done	PCN 9810	0.30
EPF10K50V	3.3	Done	PCN 9810	0.30 *(1)*
		Sept. 2000	PCN 9915	0.30 *(2)*
EPF10K100A	3.3	Done	PCN 9810	0.30
EPF10K10	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K20	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K30	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K40	5.0	October 2000	PCN 9901 ADV 9909	0.42
EPF10K50	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K70	5.0	Dec. 2000	PCN 9901 ADV 9909	0.42
EPF10K50E	2.5	Done	PCN 9911	0.22
EPF10K200E	2.5	Done	PCN 9911	0.22

Notes:
(1)   3-layer metal process.
(2)   4-layer metal process.

Table 5. FLEX 10KE Industrial-Temperature Device Availability

Device	Availability
EPF10K30EQI208-2	Now
EPF10K30EFI256-2	Now
EPF10K50ETI144-2	Now
EPF10K50EQI240-2	Now
EPF10K50EFI256-2	Now
EPF10K50SQI208-2	Now
EPF10K50SFI484-2	Now
EPF10K100EQI208-2	Now
EPF10K100EFI256-2	Now
EPF10K100EFI484-2	Now
EPF10K130EQI240-2	Now
EPF10K130EBI356-2	Now
EPF10K130EFI484-2	Now
EPF10K200EBI600-2	Now
EPF10K200SBI356-2	Now
EPF10K200SFI672-2	Now

MAX

MAX 7000A Devices

The feature-rich MAX® 7000A devices support enhanced in-system programmability (ISP), MultiVolt™ I/O pins, hot-socketing, and pin compatibility with the industry-standard MAX 7000 devices. 3.3-V MAX 7000AE devices range from 32 to 512 macrocells with propagation delays as fast as 4.5 ns. All MAX 7000AE devices are available in industrial-temperature grades. Table 6 shows the commercial package and speed-grade options for MAX 7000AE devices.

MAX 7000B Devices

2.5-V MAX 7000B devices range from 32 to 512 macrocells with propagation delays as fast as

3.5 ns. Additionally, MAX 7000B devices feature enhanced ISP, MultiVolt™ I/O pins, and pin compatibility with the industry-standard MAX 7000 devices. Table 7 shows all commercial package and speed grade options. All devices are available now. Most MAX 7000B devices are expected to be available in industrial-grade temperature by October 2000. Contact your Altera sales representative for device availability. For more information, see "MAX 7000B Devices Maintain Product-Term Leadership through Innovation & Technology" on page 1.

MAX 7000S Devices

5.0-V MAX 7000S devices offer features such as 5.0-ns speed grades, in-system programmability

Table 6. MAX 7000AE Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032AE	44-pin PLCC *(1)*	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM7064AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	49-pin Ultra FineLine BGA *(2)*	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
EPM7128AE	84-pin PLCC	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	100-pin PQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7256AE	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512AE	144-pin TQFP	-7, -10, -12
	208-pin PQFP	-7, -10, -12
	256-pin BGA	-7, -10, -12
	256-pin FineLine BGA	-7, -10, -12

Notes:
(1) PLCC: plastic J-lead chip carrier.
(2) Ultra FineLine BGA™ packages are Altera's 0.8-mm pitch BGA packages.

Table 7. MAX 7000B Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA	-3, -5, -7
EPM7064B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA	-3, -5, -7
	100-pin TQFP	-3, -5, -7
	100-pin FineLine BGA	-3, -5, -7
EPM7128B	49-pin Ultra FineLine BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
	144-pin TQFP	-4, -7, -10
	169-pin Ultra FineLine BGA	-4, -7, -10
	256-pin FineLine BGA	-4, -7, -10
EPM7256B	100-pin TQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512B	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10

MAX 7000B devices feature enhanced ISP, MultiVolt I/O pins, and pin compatibility with the industry standard MAX 7000 devices.

(ISP), an open-drain output option, and IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in industrial-temperature grades. Table 8 shows the packages and speed grades available in the commercial-temperature grade.

Table 8. Commercial-Temperature MAX 7000S Devices		
Device	**Package**	**Speed Grade**
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

MAX 3000A Devices

MAX 3000A devices are the ideal low-cost ISP solution for designers looking for high performance at a low price-per-macrocell. 3.3-V product-term-based MAX 3000A devices are targeted for high-volume, low-cost designs. These devices have an enhanced ISP feature set and range in density from 32 to 256 macrocells (see Table 9) with propagation delays as fast as 4.5 ns.

Table 9. MAX 3000A Devices		
Device	**Package**	**Speed Grade**
EPM3032A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM3064A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	100-pin TQFP	-4, -7, -10
EPM3128A	100-pin TQFP	-5, -7, -10
	144-pin PQFP	-5, -7, -10
EPM3256A	144-pin TQFP	-6, -7, -10
	208-pin PQFP	-6, -7, -10

CONFIGURATION

High Density Configuration Devices Coming Soon

The new 4-Mbit EPC4E and 16-Mbit EPC16F configuration devices are scheduled for release in December 2000. These new devices will include features such as faster configuration times, parallel configuration, reprogrammability, and much more. Additionally, you can use a single device to configure several APEX or FLEX devices in parallel to further speed configuration time and board space.

A single EPC16F device will configure two 1.5-million-gate EP20K1500E devices with new data compression options.

TOOLS

Quartus Version 2000.09 Coming Soon

The Quartus software version 2000.09, which includes the PowerFit fitter, is scheduled to ship to all customers on active subscription in October.

PowerFit Fitter Provides Dramatic f_{MAX} & Compile Time Improvements

The Quartus™ software version 2000.09 includes the second generation PowerFit™ fitter, to provide optimal placement and fitting for high-density PLD designs. Benchmarks show significant f_{MAX} improvements coupled with reduced compile times for designs targeting APEX EP20K600E and larger devices. The PowerFit fitter is scheduled to ship to all customers on active subscription in October.

New Device Database

A new Altera-developed database technology will replace the ObjectStore database. This new technology improves installation flows in UNIX environments and reduces UNIX-specific compile time bottlenecks.

More Powerful Timing Analysis

Several new timing analysis assignment options are available in the Quartus software version 2000.09 including those listed in Table 10.

The Quartus software version 2000.09 timing analyzer provides designers the ability to more accurately analyze circuits that include complex clock structures where a clock is derived from another clock using combinatorial logic. Other timing analysis enhancements provide designers the ability to better specify multicycle path relationships. More information on these features will be published at the time of release.

Support for Windows 2000

The Quartus software version 2000.09 and the MAX+PLUS II software version 10.0 are certified to operate on the Windows 2000 operating system. The Quartus and MAX+PLUS II development systems now support the operating systems listed in Table 11.

Table 10. Quartus Software Version 2000.09 Timing Analysis Assignments

Assignments	Description
NOT_CLOCK	Specifies signal should not be interpreted as a clock
INVERTED_CLOCK	Specifies inversion of a derived clock generated with complex logic
MIN_TPD_REQUIREMENT	Specifies the minimum delay required for combinatorial logic between two registers
HOLD_MULTICYCLE SRC_MULTICYCLE SRC_HOLD_MULTICYCLE	Used to enhance support for multicycle timing analysis

Table 11. Quartus & MAX+PLUS II Operating System Support

Software	Operating System Support
Quartus version 2000.09	Windows 2000, Windows 98, Windows NT version 4.0 and higher, Sun Solaris 2.6 and 2.7, HP-UX 10.2*x*
MAX+PLUS II version 10.0	Windows 2000, Windows 98, Windows NT version 4.0 and higher, Sun Solaris 2.5 and 2.6, HP-UX 10.2*x*, AIX version 4.1 and higher

Improved Support for Third-Party Simulation & Timing Analysis Tools

To account for the differences in how various EDA tools process verification netlists, the Quartus software now generates verification output netlists that vary depending on the targeted EDA tool. For example, if you select the Model*Sim*-Altera software for the simulation tool and the PrimeTime software for the timing analysis tool, distinct VHDL or Verilog HDL netlists and Standard Delay Format Output Files (**.sdo**) are placed in unique Model*Sim* and PrimeTime folders. This methodology guarantees accurate results using all third-party simulation and timing analysis tools.

Block-Level Design Enhanced to Support Third-Party EDA Tools

You can use the **Create HDL Design File for Current File** option (Tools menu) to convert a top-level Block Design File (**.bdf**) from the Quartus software into a VHDL or Verilog HDL output file. Use any third-party HDL synthesis tool to synthesize the output file.

Expanded APEX Device-Package Support

The Quartus software version 2000.09 supports new devices and packages, which are listed in Table 12.

Table 12. New Devices Supported by Quartus Version 2000.09

Support	Device	Package
Full Compilation, Simulation, and Programming Support	EP20K60E	144-pin FineLine BGA, 324-pin FIneLine BGA, 356-pin BGA
	EP20K100E	144-pin FineLine BGA
	EP20K160E	144-pin TQFP, 208-pin RQFP, 240-pin PQFP, 356-pin BGA, 484-pin FineLine BGA
	EP20K600E	1,020-pin FineLine BGA
	EP20K1500E	652-pin BGA, 1,020-pin FineLine BGA
Compilation and Simulation Support	EP20K30E	144-pin TQFP, 144-pin FineLine BGA, 208-pin RQFP, 324-pin FineLine BGA, 356-pin BGA

The MAX+PLUS II software version 10.0 is shipping to all customers with current subscriptions, and features support for the new ACEX 1K device family.

Devices & Tools, continued from page 13

Quartus Software 2000.05 Service Pack 1 Released

The Quartus software version 2000.05 Service Pack 1 was released in July 2000. This service pack is to be used with version 2000.05 of the Quartus software. Service Pack 1 is the first Quartus version to have Windows 2000 certification and includes full support for 23 new APEX 20K and APEX 20KE devices, including the EP20K1500E in a 652-pin BGA package and EP20K1000E-X in 652-pin BGA and 1,020-pin FineLine BGA packages (see Table 13). Customers with an active subscription can download this update from **https://websupport.altera.com**.

MAX+PLUS II Software Supports New ACEX Devices

The MAX+PLUS II software version 10.0 is scheduled to ship with the Quartus software version 2000.09 as a single upgrade package in

Table 13. New Devices with Full Support from the Quartus Software Version 2000.05 Service Pack 1

Device	Package
EP20K60E	144-pin TQFP *(1)*
	208-pin RQFP *(1)*
	240-pin RQFP *(1)*
EP20K100	144-pin TQFP *(2)*
	208-pin PQFP *(2)*
	240-pin PQFP *(2)*
	324-pin FineLine BGA *(2)*
	356-pin BGA *(2)*
EP20K200E	356-pin BGA *(1)*
EP20K300E	672-pin FineLine BGA *(1)*
EP20K400	652-pin BGA *(2)*
	672-pin FineLine BGA *(2)*
EP20K1000E	652-pin BGA *(2)*
	672-pin FineLine BGA *(1)*
	1,020-pin FineLine BGA *(1)*
EP20K1500E	652-pin BGA *(3)*

Notes:
(1) These packages refer to devices either with or without PLLs.
(2) These packages only refer to devices with PLLs.
(3) These packages only refer to devices without PLLs.

Table 14. New Devices with Full Support from the MAX+PLUS II Software Version 10.0

Device	Package
EPM7032B	44-pin TQFP
	49-pin Ultra FineLine BGA
EPM7064B	49-pin Ultra FineLine BGA
	100-pin FineLine BGA
EPM7064AE	49-pin Ultra FineLine BGA
EPM7128B	49-pin Ultra FineLine BGA
EPM7256B	169-pin Ultra FineLine BGA
EPM7512B	144-pin TQFP
	256-pin BGA
	256-pin FineLine BGA
	169-pin Ultra FineLine BGA
EP1K10	100-pin TQFP
	144-pin TQFP
	208-pin PQFP
	256-pin BGA

October 2000. This release features new device support for many MAX 7000B devices and packages as well as ACEX EP1K10 devices (see Table 14).

World Class Synthesis & Simulation Tools Now Shipping

Synopsys FPGA *Express*-Altera version 3.4, Exemplar Logic LeonardoSpectrum-Altera version 1999j, and Model Technology Model*Sim*-Altera version 5.3 are shipping to all customers on active subscription. These products provide access to world class HDL synthesis and simulation tools to all of Altera's customers on active subscription. For more information on these tools, or to obtain a license file, visit the Altera web site at **http://www.altera.com**.

Design *Tips*

Using Ternary Content Addressable Memory

Altera's APEX™ 20KE devices contain embedded content addressable memory (CAM) that supports a number of different design configurations. APEX 20KE CAM supports ternary operation, where user-programmable memory bits can store 0, 1, or "don't care" values. "Don't care" values force the CAM blocks to produce a match when either a 0 or a 1 is presented as an input signal and can be used for many applications, such as masking fields in Internet protocol addresses. The "don't care" feature is a very flexible feature that is not supported by any other programmable logic vendor. "Don't care" values can be written to APEX 20KE devices with the following three methods:

- Memory Initialization File (.**mif**) initialization method
- `wrx` port method
- `pattern` port method

MIF Initialization Method

The easiest way to store "don't care" values in CAM is to initialize the CAM with a MIF. The MIF allows you to enter both "don't care" values and normal pattern values into CAM. Figure 1 shows a MIF and illustrates how "don't care" values are initialized in a CAM block.

In Figure 1, the MIF contains "don't care" values, denoted by an X. A "don't care" value of

Figure 1. Example MIF

Addr	+0	+1	+2	+3	+4	+5	+6	+7
0	00000001	00000002	00000003	00000004	00000005	00000006	00000007	00000008
8	00000009	0000000A	0000000B	0000000C	0000000D	0000000E	0000000F	00000010
16	00000011	00000012	00000013	00000014	00000015	00000016	00000017	00000018
24	00000019	0000001A	0000001B	0000001C	0000001D	0000001F	00000100	XXXXFFFF

Figure 2. 32-Word CAM Using the wrx Port Method

XXXXFFFF is written to address 24. Therefore, any patterns between `0000FFFF` and `FFFFFFFF` will produce matches at address 24.

wrx Port Method

In most designs, the system must update the CAM's contents after the device has been configured. The CAM MegaWizard® Plug-In can create a `wrx` port and a `wrxused` port to write "don't care" values to a CAM block after configuring the device. Figure 2 shows a 32-word CAM block generated by the MegaWizard Plug-In that uses the `wrx` port and the `wrxused` port to write "don't care" values.

A CAM block configured with the `wrx` port method requires three clock cycles to write a "don't care" value. Bits configured as normal bits are written with the pattern bus, and bits configured as "don't care" bits are set high on the `wrx` bus. For example, you can write a value of `BX` to CAM by placing a value of `B0` on the pattern bus and `0F` on the `wrx` bus. Figure 3 shows how to write a "don't care" value of `000000BX` to CAM at address location 7.

The `wrx` port method provides a simple method for writing "don't care" values to a CAM. Bits

that will be "don't care" bits are set to 1 on the `wrx` bus. The 32-word CAM block shown in Figure 2 is capable of running at speeds in the range of 100 MHz. This speed is sufficient for many designs. If your design requires CAM to operate at frequencies faster than 100 MHz, use the `pattern` port method.

pattern Port Method

"Don't care" values can also be written with the `pattern` port. The `pattern` port method requires less logic than the `wrx` port method and can run at faster clock frequencies. However, writing the "don't care" bits is slightly more complicated. Figure 4 shows a MegaWizard instantiation of a 32-word CAM block that does not use the `wrx` port or the `wrxused` port.

In Figure 4, "don't care" values can be written in three clock cycles. A normal bit is written to the CAM by writing a `0` or a `1` to the normal bit on the first clock cycle and by writing a `0` or a `1` to the normal bit on the third clock cycle. You can write a "don't care" bit to the CAM by writing a `0` to the "don't care" bit on the first clock cycle and a `1` to the "don't care" bit on the third clock cycle. Table 1 shows how to write a value of `000000BX` to the CAM at address location 7.

In Table 1 on page 17, since bits `[3..0]` need to be "don't care" values, a `0` is written to each

Figure 3. Writing a "Don't Care" Value to CAM with the wrx Port Method
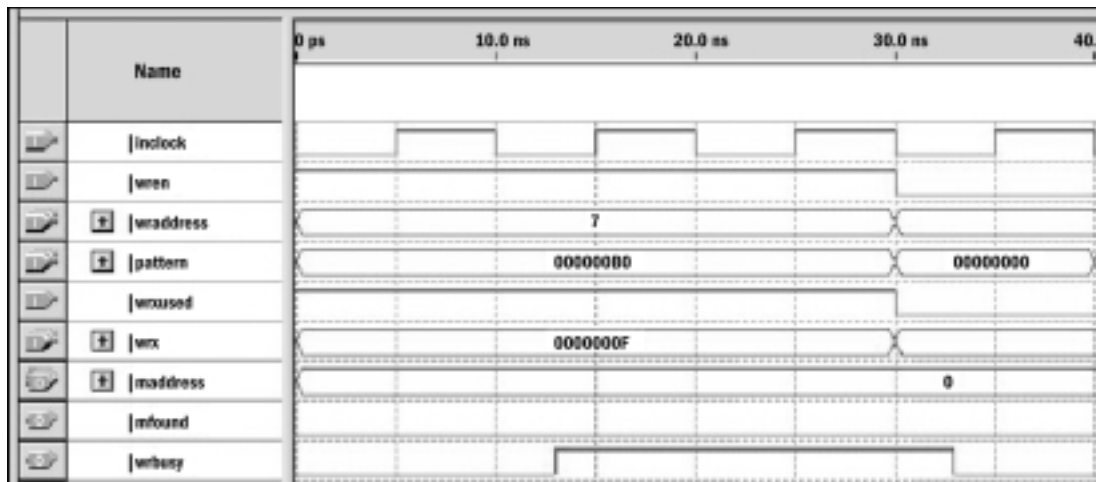
Table 1. Writing into CAM			
Port	**Clock Cycle 1**	**Clock Cycle 2**	**Clock Cycle 3**
wren	1	0	1
pattern	0000000B0	UUUUUUUU *(1)*	000000BF
wraddress	7	7	7

Note:
(1) The pattern value on the second clock cycle is not written to CAM; therefore, you can apply any data value to the pattern bus during this clock cycle.

of these bits' locations on the first clock cycle and a 1 is written to each of these bits' locations on the third clock cycle. Also, since bits [7..4] need to be set to B, a B is written to each of these bits on the first clock cycle and on the third clock cycle. Finally, since bits [31..8] need to be all 0s, a 0 is written to the CAM on both the first and third clock cycles.

Writing "don't care" values to CAM using the pattern port method is slightly more complicated than the wrx port method. However, the pattern port method significantly increases the CAM's overall performance. The pattern port method eliminates the critical path caused by the wrx port, thereby increasing performance. The 32 × 32 CAM block shown in

Figure 4 will run at 160 MHz compared to the CAM block shown in Figure 2 that runs at 100 MHz.

You should choose which method will adapt best to your design. Designs that require a simple method of writing "don't care" values should use the wrx port method. Since very little decoding is required to write an X value to the CAM, the wrx port method is simple. You should consider using the pattern port method for designs that are speed-critical. The pattern port method requires somewhat more complex user logic, but the pattern port method significantly increases the CAM's overall speed.

Conclusion

APEX 20KE devices contain high-speed CAM that can be used for a wide variety of applications. Altera's CAM can store "don't care" values with three separate methods, each of which has different benefits. The MIF initialization method is the easiest method to use. However, if your design requires you to write "don't care" values to the CAM after device configuration, you can write these values with the wrx port method or, for high-frequency designs, the pattern port method.

Figure 4. 32-Word CAM Using the pattern Port Method
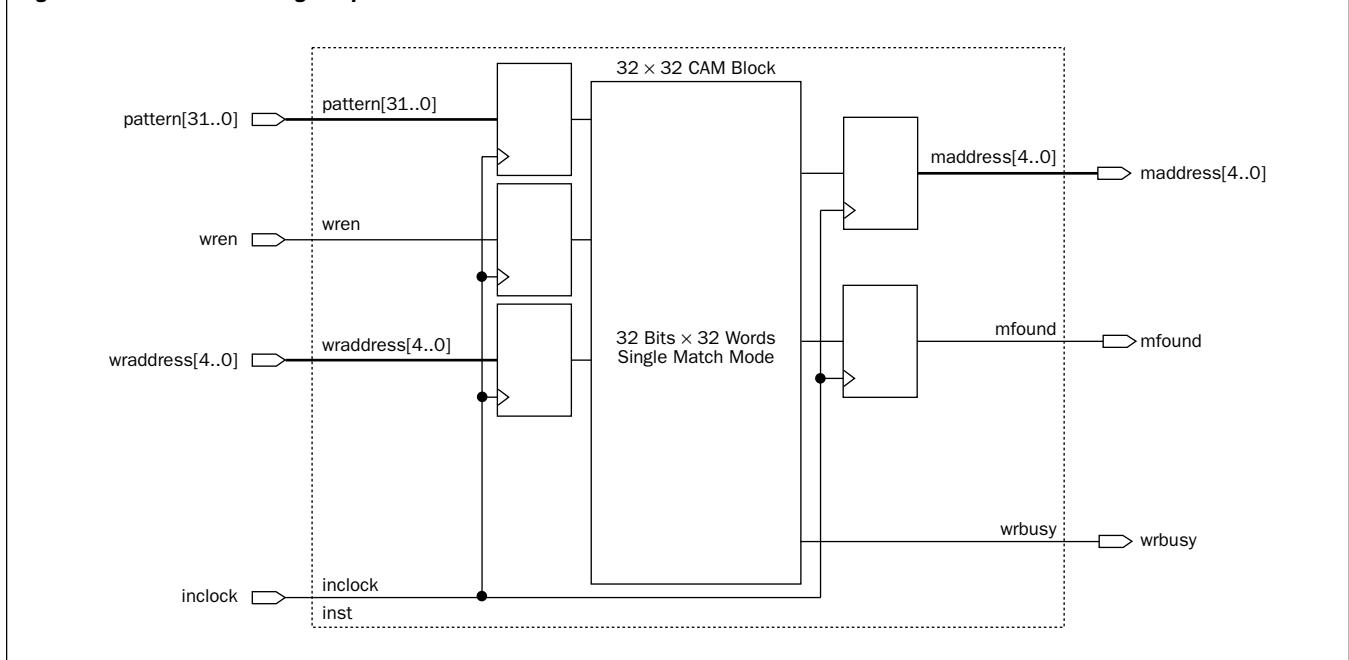
OEM Licensing Details for Mentor Graphics Software

Altera has entered into OEM agreements with Mentor Graphics to provide Altera customers with world-class synthesis and simulation products.

All Altera customers on active subscription have received the LeonardoSpectrum for Altera and Model*Sim*-Altera software with their Altera software products. You can request license files to enable these tools on the Altera web site (**http://www.altera.com**).

Each active Altera subscription enables one HDL (VHDL or Verilog) support license for each Mentor Graphics software product. For example, if you have a single active subscription, you can be licensed for LeonardoSpectrum VHDL synthesis support and Model*Sim*-Altera Verilog HDL simulation support, but then are not entitled to LeonardoSpectrum Verilog HDL synthesis support or Model*Sim*-Altera VHDL simulation support for the same subscription. If you have a FLOATNET or FLOATPC subscription, you can request any sum of VHDL and Verilog HDL support licenses that does not exceed your total number of active floating seats.

The license file FEATURE lines for the Mentor Graphics software products differ from the Altera and Synopsys OEM FEATURE lines. The Mentor Graphics software licenses expire 15 months from the date you request a license or from the date your Altera subscription expires, whichever is earlier. Therefore, if you remain on active subscription by purchasing a renewal subscription, you will continue to receive active Mentor Graphics software license files.

See Figure 1 for an example of a license file for an Altera software guard, enabling VHDL synthesis support for LeonardoSpectrum for Altera and Verilog simulation support for Model*Sim*-Altera. Please note that the Mentor Graphics software products run off of the `mgcld` license daemon, rather than the `alterad` license daemon.

Figure 1. Example License File

```
FEATURE maxplus2 alterad 2000.06 permanent uncounted 66C915DD65AE \
    HOSTID=GUARD_ID=T0000ABCDE
FEATURE quartus alterad 2000.06 permanent uncounted 03390A577AFE \
    HOSTID=GUARD_ID=T0000ABCDE
FEATURE altera_fpgaexpress alterad 2000.06 permanent uncounted \
    2519310F6E7A HOSTID=GUARD_ID=T0000ABCDE

FEATURE leospecls1 mgcld 2000.06 14-sep-2001 uncounted \
    8C08EA3E061C00DA0A6F VENDOR_STRING=9F4E552B \
    HOSTID=GUARD_ID=T0000ABCDE SUPERSEDE ISSUER=Alterav1.0
FEATURE leospecls1alt mgcld 2000.06 14-sep-2001 uncounted \
    ACB81A2EBF530DC69313 VENDOR_STRING=51B30168 \
    HOSTID=GUARD_ID=T0000ABCDE SUPERSEDE ISSUER=Alterav1.0
FEATURE leospecls1vhdl mgcld 2000.06 14-sep-2001 uncounted \
    9CA82A3E9A5E01B4AC86 VENDOR_STRING=A639B072 \
    HOSTID=GUARD_ID=T0000ABCDE SUPERSEDE ISSUER=Alterav1.0
FEATURE alteramtivlog mgcld 2000.06 14-sep-2001 uncounted \
    4C589ADEF140EB9D8F2C VENDOR_STRING=A066BEE0 \
    HOSTID=GUARD_ID=T0000ABCDE SUPERSEDE ISSUER=Alterav1.0
```

Customer *Application*

LGIC Uses FLEX Devices to Pioneer Broadband CDMA WLL System

In the wireless world, the demand for advanced information services is growing. Voice and low-rate data services are insufficient in a world where high-speed Internet access is taken for granted. The trend is toward global information networks that offer flexible multimedia information services to users on demand, anywhere, anytime. The need to support bandwidth-intensive multimedia services places new and challenging demands on cellular systems and networks.

Evolving Standards Need Flexible Solutions

LG Information & Communications, Ltd. (LGIC) is the biggest supplier of code division multiple access (CDMA) infrastructure equipment to the largest cellular operator in Korea, and is one of the biggest handset suppliers to major operators such as Bell Atlantic Mobile, Airtouch, Sprint, and Telesp. In 1997, five companies—including LGIC—began developing a wideband CDMA (W-CDMA) modem for wireless local loop (WLL) service for Hanaro Telecom. Because the

service standard was still under development, LGIC decided to use Altera FLEX® 10K devices to build their prototype system. The other four companies decided to use ASICs.

LGIC's initial prototype used four EPF10K100GC503-3 devices in each modem. Because of the modem complexity and because the standard was evolving, the engineers had to carefully fine-tune the design. Unfortunately, fine-tuning could not be tested with computer simulation; it had to be checked in-system. Because the Altera devices were reconfigurable, the LGIC designers could make changes quickly and see the results. In contrast, when the ASICs used by the competing companies began to have various problems, the ASICs had to be refabricated several times, wasting considerable time and money.

LGIC's second prototype had additional features and used EP10K100A and EPF10K250A devices for both the base station and the terminals. The operating clock frequency was more than 60 MHz, and the devices implemented key

Figure 1. Base Station Modem Prototype Board
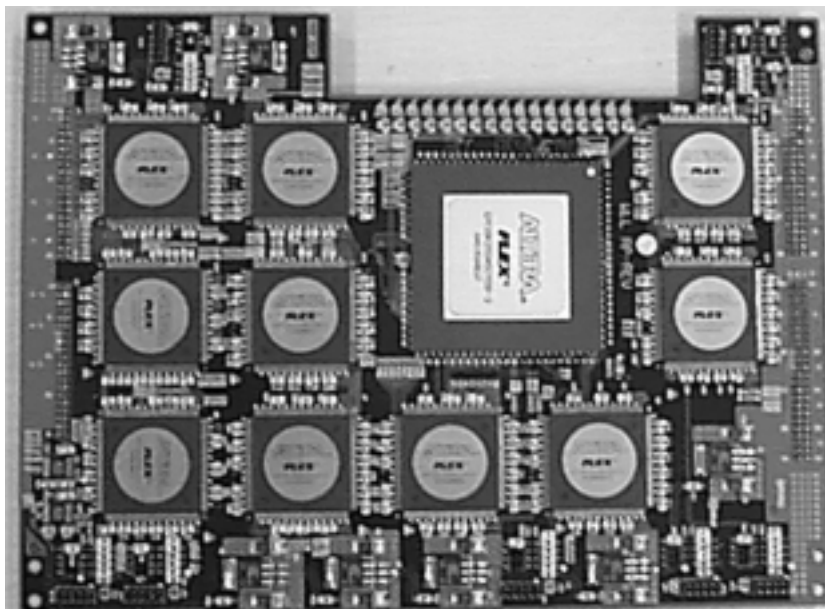
LGIC is upgrading their system design and will use Altera APEX™ devices in upcoming revisions.

functions of the modem such as the searcher, finger, Viterbi decoder, combiner, and FIR filters.

"The device usage was mostly more than 90%, but we still managed to do a very good job," stated Kim Youn Hwan, a senior research design for LGIC. "It was really exciting that we did such a hard thing. Furthermore, because the MAX+PLUS II software had such good performance and was so easy to use, we didn't use any other third-party tools for VHDL synthesis."

In the Hanaro Telecom field tests, LGIC engineers used thousands of FLEX 10K devices. After successful field testing, LGIC built an ASIC to be used in the production system. Because of the performance and stability of the system, Hanaro Telecom chose LGIC as the provider of Korea's WLL systems and subscriber units.

Looking Forward: IMT-2000

The International Telecommunications Union (ITU), under an initiative named IMT-2000, devised a number of standards that support emerging third-generation wireless requirements. However, these standards will continue to evolve as new services and technologies are identified. Systems that implement these standards must be flexible enough to accomodate changes easily. Because of LGIC's success in Korea with W-CDMA WLL, the company is well-positioned to expand their products to support third-generation wireless communications such as IMT-2000.

LGIC is upgrading their system design and will use Altera APEX™ devices in the next revision. "We expect the high-performance APEX devices will help us improve the system, and we are also impressed by the powerful Quartus™ software," Kim Youn Hwan said. "I definitely think that the APEX/Quartus combination will be a good choice."

Discontinued Devices Update

Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

JTAG Technologies Adds Jam STAPL Support
to On-Board Programming Software

JTAG Technologies has added Jam™ Standard Test and Programming Language (STAPL) support to PLDPROG, its on-board programming solution for Altera® programmable logic devices (PLDs). With this product line extension, JTAG Technologies allows users to choose any of the popular PLD programming formats within boundary-scan designs of virtually any level of complexity.

PLD Programming Development

PLD programming support from JTAG Technologies now includes the Jam STAPL standardized format as well as the prior JEDEC and Serial Vector File (**.svf**) formats. As a result, JTAG Technologies provides in-system programmability (ISP) for all Altera MAX® 7000A, MAX 7000B, MAX 7000S, MAX 9000, MAX 3000A, and EPC2 devices. Regardless of the device type or format used, the system presents a common interface to the user, avoiding a proliferation of tools throughout the organization. The system allows the rapid creation of files that perform all on-board device operations, such as erase, blank-check, programming, verification, security fuse programming, and user-code readback. JTAG Technologies tools also provide JTAG-based in-circuit reconfigurability (ICR) support for ACEX™ 1K, APEX™ 20K, APEX 20KE, FLEX® 10K, and FLEX 10KE devices.

The PLDPROG system handles a wide variety of scan chain configurations, ranging from a simple single chain structure up to multi-chain, multi-level hierarchical scan architectures. Scan chains of any length are possible, with automatic, safe board configuration during PLD programming. The software's graphical user interface (GUI) guides the developer in verifying boundary-scan description language (BSDL) files, testing the board's boundary-scan chain, and performing the programming functions.

Production Support

PLD programming applications run on a wide variety of fully-compatible hardware controllers in a broad range of operating environments. Interfaces are available for peripheral component interconnect (PCI), ISA, universal serial bus (USB), VXI, and PC parallel port. The production environments include:

- Stand-alone PC or work stations with a convenient GUI for sequencing desired operations
- Full integration within an existing production step, such as functional test, through delay-locked loop (DLL)-based applications
- Support for incorporating PLD programming within a National Instruments LabWindows/CVI or LabView platform
- Client/server operation, in which the boundary-scan software and hardware are controlled within a single computer or across a network

The JTAG Technologies tools allow designers to properly sequence PLD programming with other powerful boundary-scan applications, board testing, and in-system flash programming. Multiple authorization levels are provided for operators, technicians, and engineers. Production personnel benefit from having quick and easy controls, typically via single-button operation, along with execution reports that summarize the results.

About JTAG Technologies

JTAG Technologies was founded in 1993 and focuses its R&D effort at providing powerful, cost-effective boundary-scan solutions for electronics producers. Corporate headquarters are in Eindhoven, the Netherlands, with a US
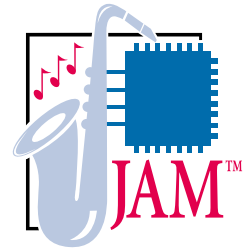
JTAG Technologies Adds Jam STAPL Support to On-Board Programming Software, continued from page 21

JTAG
Technologies B.V.

Customer Support Center in Stevensville, MD, and a regional office in the United Kingdom. The company maintains an experienced staff of Development Engineers and Application Engineers to support customer needs, and is represented by authorized distributors around

the world. There are now over 1,200 JTAG Technologies systems in operation around the world.

JTAG Technologies
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    (877) FORJTAG (367-5824)
United Kingdom: 01234 27 22 26
Email: **info@jtag.nl**
Web site: **http://www.jtag.com**

Figure 1. PLDPROG System

Technical *Articles*
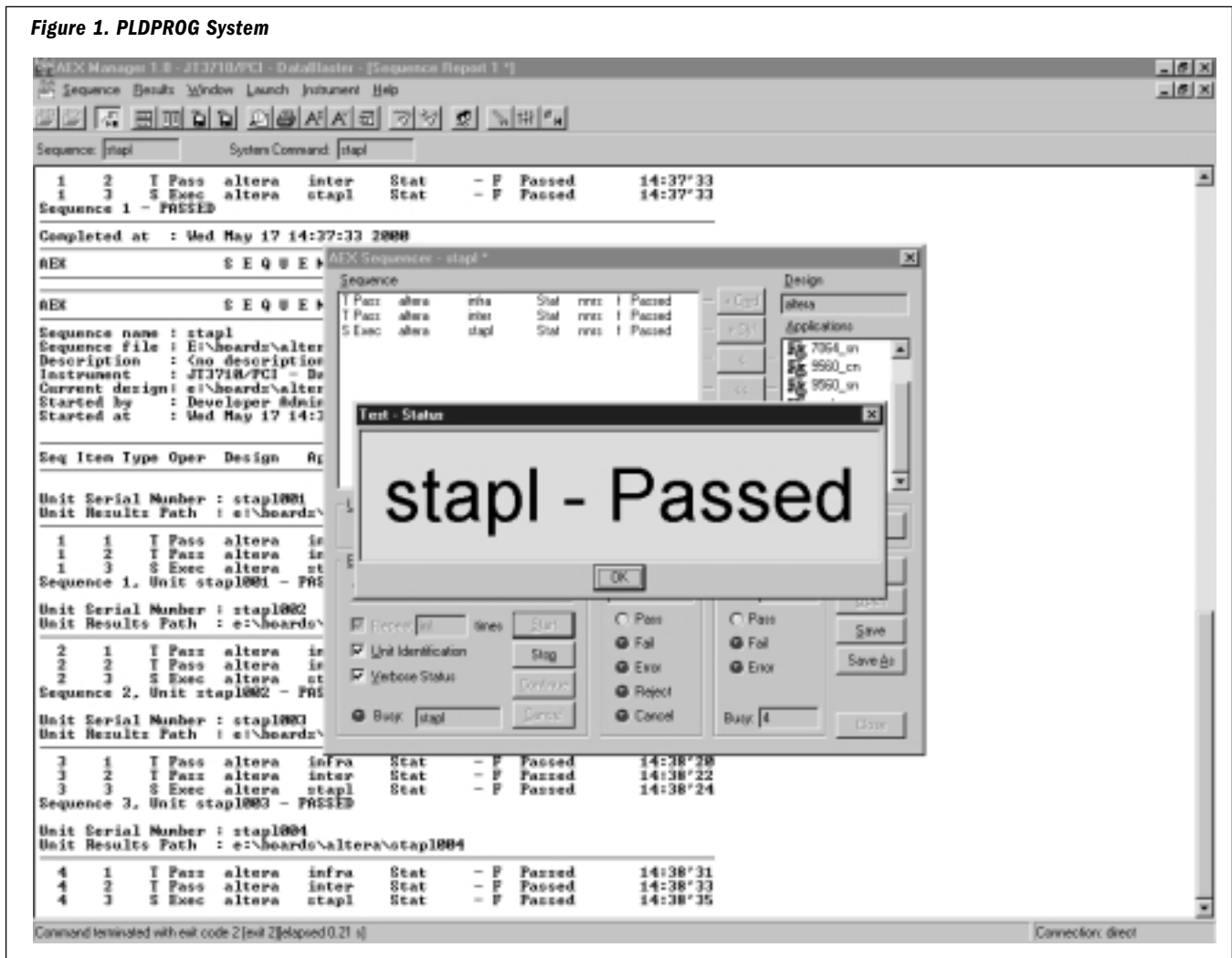
Implementing LVDS Interfaces with General-Purpose I/O Pins

Increases in programmable logic device (PLD) density have led designers to include more functions in their designs. This improvement in device functionality has allowed PLDs to play a major role in data transmission between devices, boards, or nearby systems, making accessibility to a variety of I/O buffers with different capabilities an important PLD feature.

Altera's APEX™ devices offer a wide variety of I/O buffers, allowing designers to interface with LVTTL, LVCMOS, SSTL-3, SSTL-2, CTT, and GTL+ buffers. The most innovative of these I/O buffers is LVDS.

LVDS is a data interface standard defined in the TIA/EIA-644 and the IEEE 1596.3 specifications. The LVDS standard has industry-wide popularity with system designers who use it in a variety of applications. Ranging from flat panel display to high-end, low-power switch applications, LVDS has proven to be the technology of choice. This signaling standard is differential, which has high noise immunity, and its low voltage swing allows for high-speed data transmission and low power consumption.

The Altera APEX device family has 16 input and 16 output dedicated True-LVDS™ channels equipped with embedded serializer/deserializer phase-locked loops (PLLs) capable of transferring data at speeds up to 840 megabits per second (Mbps) per channel with low power dissipation and low cost per channel. The multiplexing of parallel TTL/CMOS signals allows system designers to reduce bus widths between two points while transmitting the same bandwidth.

While 16 LVDS channels meet the needs of most applications, some applications may require more channels. APEX devices address this need by allowing the other I/O pins to communicate with other LVDS devices at speeds up to 155 Mbps.

This article describes a technique to use other APEX I/O pins to communicate via LVDS.

APEX I/O Banks

Altera's APEX product line has eight I/O banks that support many I/O technologies. Six I/O banks support LVTTL, LVCMOS, 1.8 V, 2.5 V, 3.3-V PCI, 3.3-V AGP, CTT, SSTL-3 class I or II, SSTL-3 class I or II, and GTL+. Two other banks support all these I/O standards as well as the LVDS I/O standard. A unique feature of I/O banks is the use of a separate V_{REF} reference level for each bank. The ability to use a separate V_{REF} level allows these I/O pins to be used as LVDS I/O pins at lower speeds.

Driving LVDS Signals into Any I/O Bank

The availability of V_{REF} for each I/O bank works as an advantage for APEX devices. Designers can use the V_{REF} to control the offset voltage, which allows these eight I/O banks to receive data from any LVDS driver.

To receive low-speed LVDS signals (155 Mbps) on general-purpose I/O pins, set the I/O buffers to SSTL-2 Class II buffer type, terminate the LVDS channels using two 50-Ω resistors, and connect the VREF pin to the LVDS common mode voltage at the center of the two termination resistors (see Figure 1). Specify a VREF pin within your design.

For a guide to setting I/O standards and VREF pins, refer to *AN 117 (Using Selectable I/O Standards in Altera Devices)* and the *Using I/O Standards in the Quartus Software White Paper.*

When more than one LVDS channel is connected to the same I/O bank, you do not need to terminate the other channels with two 50-Ω resistors. A standard 100-Ω termination is adequate (the LVDS common mode voltage is set by the first channel).

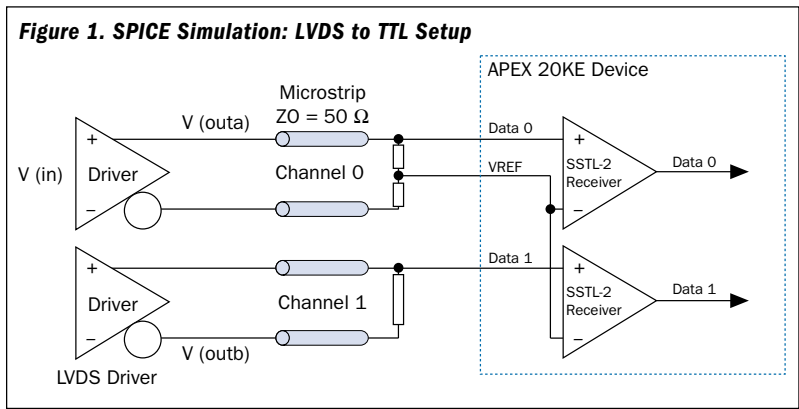*Designers can use the V_{REF} to control the offset voltage, which allows the I/O banks to receive data from any LVDS driver.*

Implementing LVDS Interfaces with General-Purpose I/O Pins, continued from page 23

simulated using APEX SSTL-2 class II drivers and LVDS receiver SPICE models.

SPICE Simulation: LVDS to TTL

SPICE simulations may be used to validate circuit designs. The simulation was arranged using Altera LVDS and SSTL class II SPICE models. The media was a pair of 6-inch differential microstrip printed circuit board (PCB) traces. Figure 1 is a schematic representation of the setup. A typical TTL signal at 155 MHz was applied to the LVDS driver, and the signals were monitored at the driver output and the receiver input and output. V_{REF} was connected to LVDS common mode voltage to establish the output offset voltage or V_{OS}. The simulation showed that data transferred successfully up to and beyond 155 Mbps.

SPICE Simulation: 2.5-V TTL to LVDS

Simulation was arranged using models used in the previous experiment. The media was also kept constant: a pair of 6-inch differential microstrip PCB traces. Figure 2 is a schematic representation of the setup. Two signals at 155 MHz were applied to the drivers with opposite polarity. Signals were monitored at various locations of the circuit. The simulation showed that data transferred successfully up to and beyond 155 Mbps.

Choosing LVDS Output Pins

The LVDS output pin pairs should be chosen to minimize skew between the positive and negative signals of the differential pair. Choose pairs of pins that are adjacent on the die. I/O cell registers should also be used to minimize skew between the LVDS signals.

Figure 1. SPICE Simulation: LVDS to TTL Setup

APEX SSTL-2 Class II Buffers to LVDS

The interface from a non-LVDS I/O buffer to a LVDS receiver buffer is realized by using a resistor network. The resistors attenuate the driver outputs to levels similar to LVDS signaling; therefore, an LVDS receiver can recognize the outputs. This method was also

Conclusion

Altera's 16 input and 16 output True-LVDS channels receive and transmit data at 840 Mbps and are available for many applications. If your application requires more LVDS I/O pins, or True-LVDS I/O pins are not available on the chosen device, use an external resistor network to interface LVDS signals to APEX devices using general-purpose I/Os.

For more information on I/O standards supported by APEX 20KE devices, see *AN 117 (Using Selectable I/O Standard in Altera Devices)* and the *Using I/O Standards in the Quartus Software White Paper*.

Figure 2. SPICE Simulation: TTL to LVDS Setup
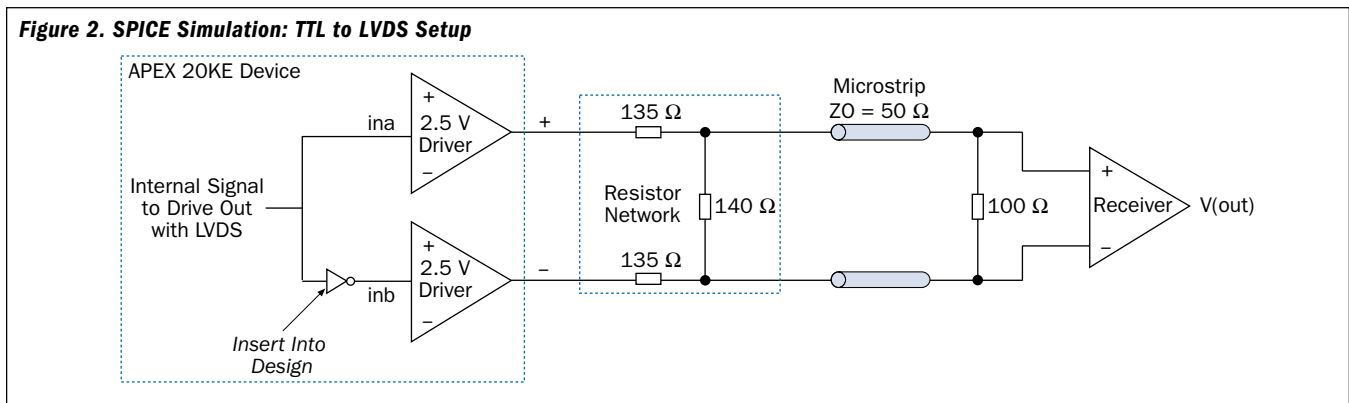
Using Model*Sim*-Altera: Frequently Asked Questions

Model Technology Model*Sim*-Altera simulation software is now available to all customers on active subscription. The following are some of the frequently asked questions regarding Model*Sim*-Altera.

Q: Which operating systems are supported for Model*Sim*-Altera?

Model*Sim*-Altera is supported on Windows 98, Windows NT 4.0, Solaris, and HP-UX operating systems.

Q: Why are precompiled libraries provided with ModelSim-Altera?

When Model*Sim*-Altera performs a post place-and-route timing simulation, you must use the precompiled libraries to avoid degradation in simulation performance. These libraries are specifically provided to enhance simulation times with the ModelSim-Altera version. Failure to use these precompiled libraries can result in excessive simulation times and/or errors and warning messages.

Q: Where are the precompiled libraries for VHDL and Verilog HDL located?

The precompiled libraries are available in the Model*Sim*-Altera installation directory at:

<ModelSim directory>**Altera\Verilog***
*<ModelSim directory>***Altera\VHDL**

On the UNIX system, the libraries are located at:

<Installation directory>/**modeltech/altera/ verilog/***<Installation directory>*/**modeltech/ altera/vhdl/**

See Tables 1 and 2 for Verilog HDL and VHDL library descriptions.

Table 1. Verilog HDL Libraries

Library	Description
APEX20K	Precompiled atoms library for APEX 20K designs
APEX20KE	Precompiled atoms library for APEX 20KE designs
ALT_VER	Precompiled primitives library for MAX and FLEX designs
SRC	Verilog HDL source code directory

Table 2. VHDL Libraries

Library	Description
APEX20K	Precompiled VITAL atoms library for APEX 20K designs
APEX20KE	Precompiled VITAL atoms library for APEX 20KE designs
ALT_VTL	Precompiled VITAL library for MAX and FLEX designs
ALT	Precompiled components library
SRC	VHDL source code directory

Model Technology ModelSim-Altera simulation software is now available to all customers on active subscription.

Q: How does Model*Sim*-Altera access the precompiled libraries when simulating Verilog HDL and VHDL code?

When performing a timing simulation, you must point to the precompiled libraries.

Verilog HDL: When loading the design for simulation through the graphical user interface (GUI) from the **Load Design** dialog box, go to the Verilog tab and specify the appropriate precompiled library's complete path. (See Figure 1.)

The vsim command can be used to point to the precompiled libraries while loading the design in command line mode. A general example is shown below.

vsim -L *<Complete Path to Precompiled Library>* -sdftyp /=*<Standard Delay Format Output File (.sdo)>* work.*<Design Module>*

Figure 1. Load Design
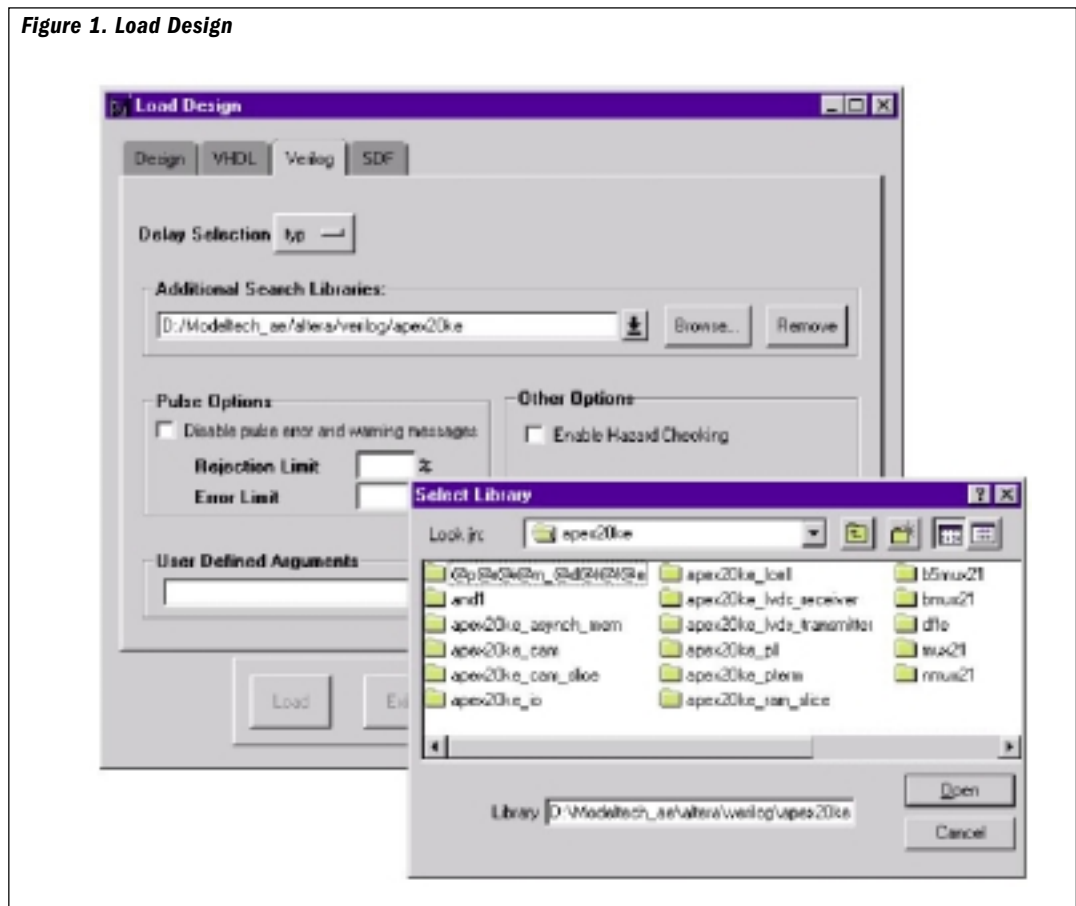
*Use the vmap alt_vtl
c:/Modeltech_ae/
altera/vhdl/apex20ke
command to map in
command line mode.*

VHDL: For VHDL designs, the appropriate precompiled library must be mapped to the ALT_VTL library. This mapping can be done through the GUI, from the **Create a New Library** command (Design menu). Turn on the "map to an existing library" option, specify the name of the library as ALT_VTL, and choose the correct path to the precompiled library. (See Figure 2.)

Use the following command to map in command line mode:

```
vmap alt_vtl c :/Modeltech_ae/
altera/vhdl/apex20ke
```

Q: Where are the functional simulation models for library of parameterized modules (LPM) functions and APEX™ megafunctions located?

The functional simulation models for LPM functions and APEX megafunctions are located in the Quartus™ installation directory. Both VHDL and Verilog HDL models are available.

C:\Quartus\eda\sim_lib\PC Environment

<Installation Directory>/quartus/eda/sim_lib <space>hyphen<space>Unix Environment

These simulation models are used when functionally simulating register transfer level

Figure 2. Create New Library
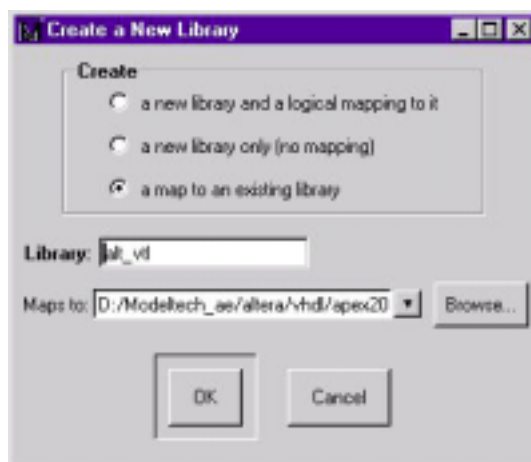
Precompiled libraries will be updated with newer library versions when newer versions of ModelSim-Altera are shipped.

(RTL) code that contains LPM components and APEX megafunctions.

Q: Can the latest versions of the APEX 20K and APEX 20KE device atoms files from the Quartus software \quartus\eda\sim_lib directory be compiled into the existing precompiled libraries of Model*Sim*-Altera?

No. The precompiled libraries should not be overwritten with newer versions of atom files. This will prevent Model*Sim*-Altera from simulating APEX 20K and APEX 20KE device designs. The precompiled libraries will be updated with newer library versions when newer versions of Model*Sim*-Altera are shipped.

Q: Can multiple installations of Model*Sim* (different versions) exist on a single PC?

Yes. Multiple installations can co-exist on a single machine because each installation uses different registry settings.

Q: Which environment variables have to be set in Solaris and HP-UX for Model*Sim*-Altera?

You must set the LM_LICENSE_FILE and MGLS_HOME environment variables for Model*Sim*-Altera to work on Solaris or HP-UX operating systems. Set the LM_LICENSE_FILE variable to the appropriate **port@hostname** for Solaris and HP-UX. MGLS_HOME must be set to:

Solaris: *<Installation Directory>*/**modeltech/ sunos5aloem/mgls.ss5**

HP-UX: *<Installation Directory>*/**modeltech/ hp700aloem/mgls.hpu**

For more information on licensing and installation, refer to the readme file on the Model*Sim*-Altera CD. More information on Model*Sim*-Altera is also available from the Altera web site at **http://www.altera.com/html/ tools/oem/ms.html.**

Using Intellectual Property in Third-Party Synthesis

Programmable logic devices (PLDs) have traditionally offered the benefits of faster time-to-market and flexibility. Recent advancements in performance and capacity, coupled with decreasing costs, have made PLDs a viable alternative to ASIC devices. Altera® devices have densities over one million usable gates and can easily integrate existing logic from a complex system to provide higher system performance, greater reliability, and lower system cost. Altera offers a total design solution by combining intellectual property (IP) with state-of-the-art development tools that optimally map designs. By using IP, designers can focus more time and energy on improving and differentiating their system-level product, rather than redesigning common functions.

Altera has worked closely with third-party synthesis partners to enhance existing IP design flows. Unlike traditional design flows, many of

Altera's partner's synthesis tools can now synthesize Altera IP blocks, offering designers access to the best-in-class synthesis features that improve existing IP flow. This article discusses third-party synthesis IP, highlighting the benefits of IP flow and addressing its limitations.

Traditional IP Design Flow

In traditional IP design flows (see Figure 1), the designer licenses an encrypted function from an IP provider and then "black-boxes" the IP function in the synthesis tool. Since the IP function cannot be decrypted by third-party synthesis tools, the designer has no choice but to exclude the IP while synthesizing the design. In this traditional IP design flow, the designer cannot gain the full benefits of a third-party synthesis tool. The designer can work around the problem using pre-optimized third-party IP

Figure 1. Traditional IP Design Flow
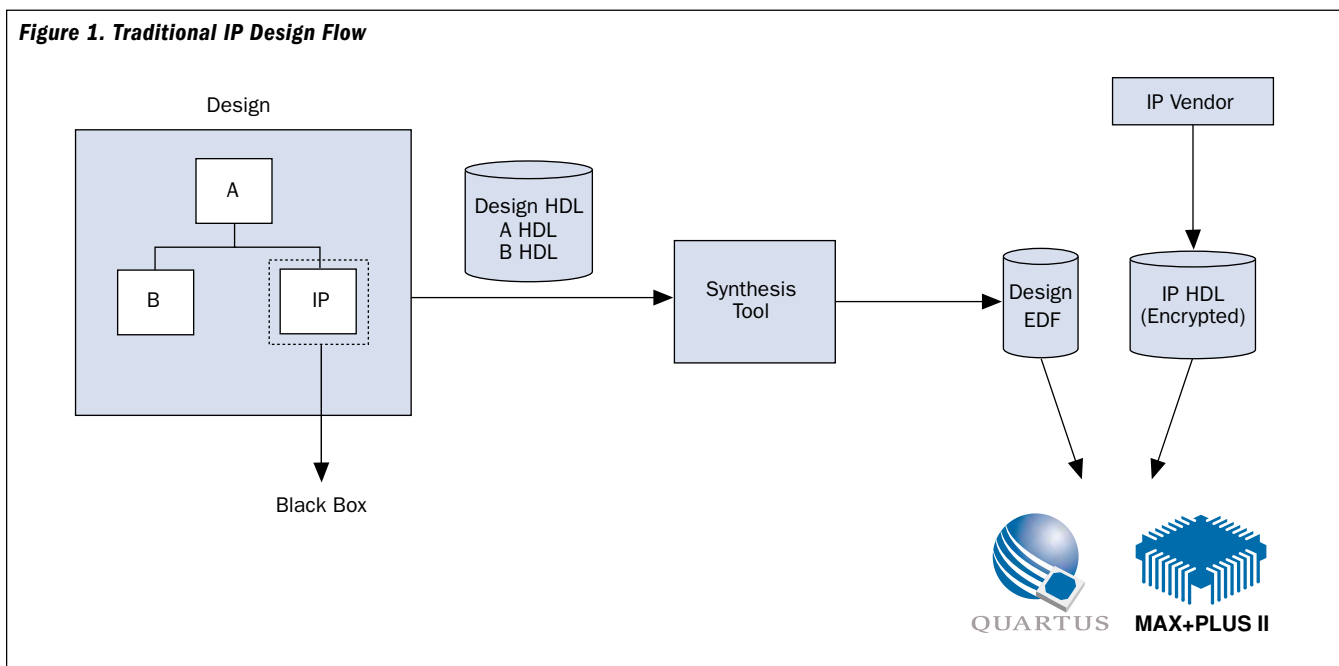
Figure 2. Fully Encrypted IP Design Flow
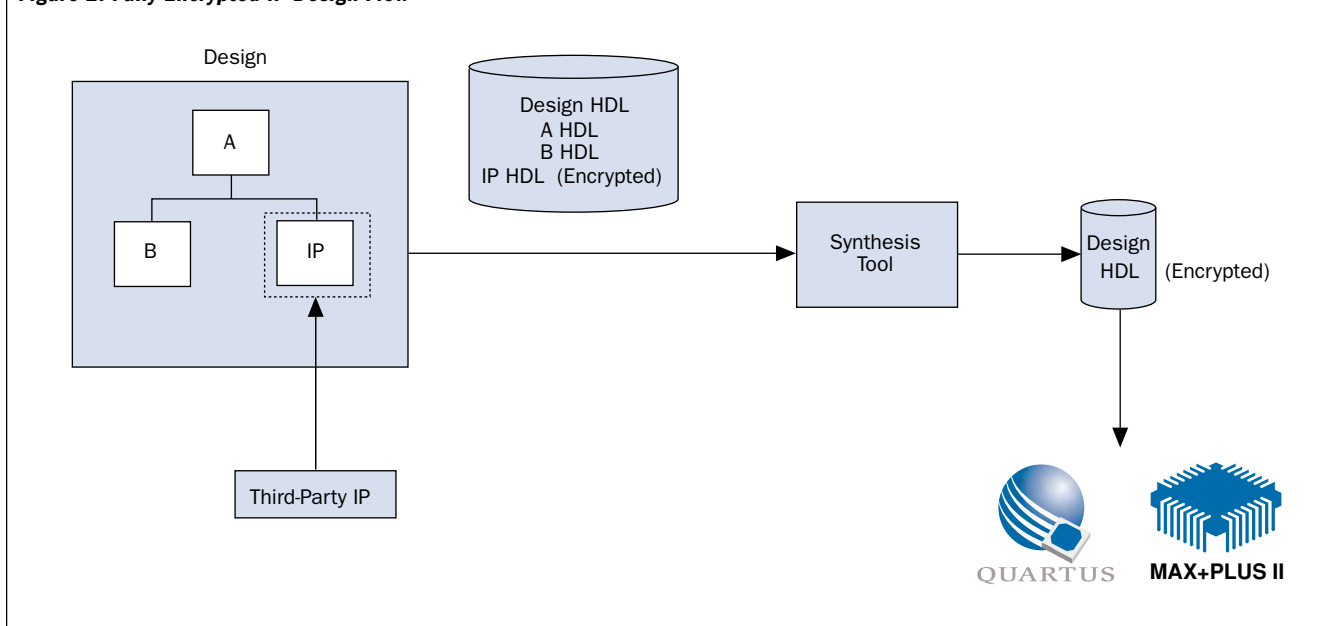
for a specific device architecture. However, this method does have limitations; the designer has a limited view into the encrypted design.

Enhanced Solution

Because designers using IP cannot take advantage of third-party synthesis tool capabilities, Altera has formed partnerships with third-party synthesis companies to solve this problem. Altera's IP licensing includes a license key to allow third-party synthesis tools to decrypt, synthesize, and then re-encrypt the IP output to preserve the integrity of the IP function (see Figure 2).

This presents two possible design flows: fully-encrypted design flow and partial black-box design flow.

Fully-Encrypted Design Flow

In a fully-encrypted design flow, the encrypted IP functions are included in the synthesis tool along with other design files (similar to those in Figure 2). This inclusion allows the third-party synthesis tool to synthesize the IP along with the rest of the design. However, because the synthesis tool must write out an encrypted

netlist for the entire design, this IP inclusion poses a challenge for the synthesis tool in preserving the IP encryption in the output netlist. This design flow seriously limits the designer's view into the output design file.

Partial Black-Box Design Flow

A partial black-box design flow (see Figure 3) is similar to a partial bottom-up design flow in that the IP blocks are synthesized individually while other components are synthesized across hierarchical boundaries, plugged into the place-and-route tool's top level, and recompiled all the way to the top. In this flow, the black box procedure is used the same way as the traditional IP design flow; however, you can now synthesize the encrypted IP in the third-party synthesis tool instead of the place-and-route tools.

The IP blocks are individually read in and compiled with their constraints in the third-party synthesis tools. Encrypted EDIF netlists for each IP design component are generated. This can be an iterative process if necessary, until the design constraints are met for the individual IP components. Then, the encrypted EDIF netlists are black-boxed in the original design for

Figure 3. Partial Black-Box Design Flow
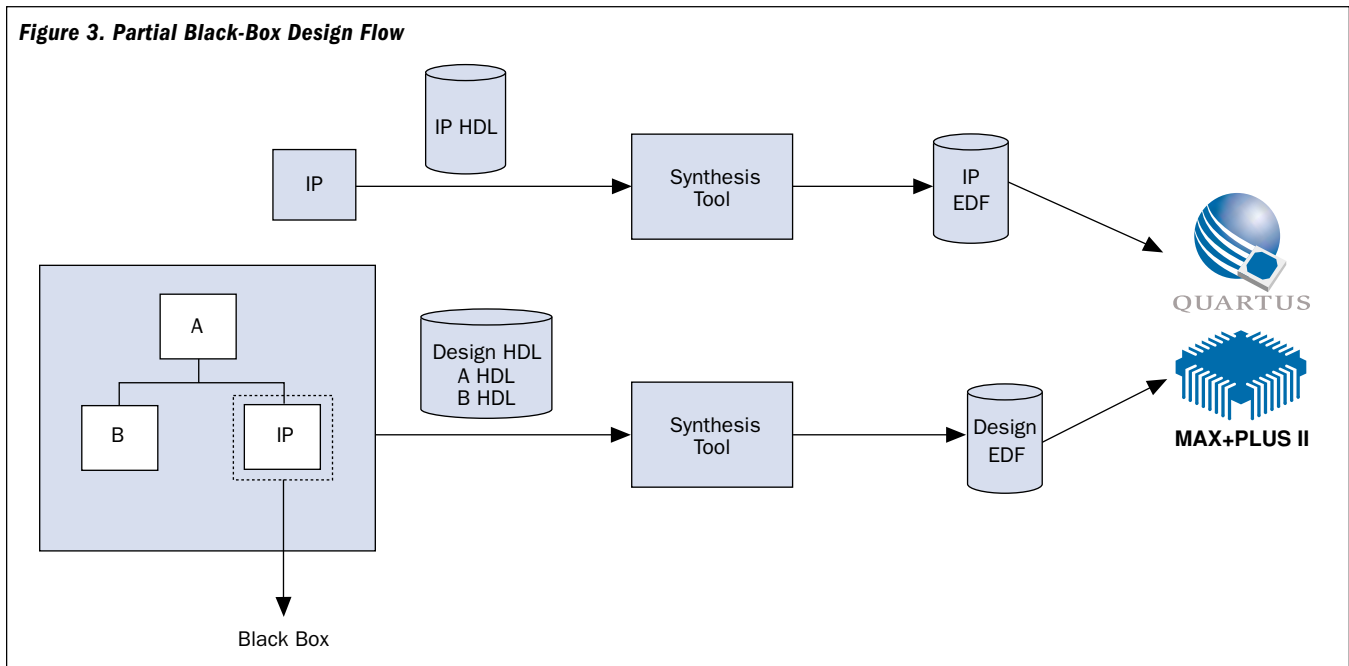
synthesis. The design is now free of any encrypted IP components, and the resulting EDIF netlist is unencrypted, providing better visibility into the design than with the fully-encrypted design flow. The resulting EDIF and the EDIF representations of the IP blocks can now be read into either the Quartus™ or MAX+PLUS® II software for compilation. Designers take advantage of the best-in-class features that the third-party synthesis tools offer for synthesizing IP.

Integration with Altera's Design Environment

Designers targeting the ACEX™, FLEX®, or MAX® architectures can use third-party synthesis tools to generate an EDIF netlist to place-and-route the design in the Altera MAX+PLUS II design software. The software generates a constraint file to forward-annotate the timing constraints for the place-and-route tool.

Third-party synthesis tools generate a technology-mapped EDIF netlist and launch the

Altera Quartus development software to place-and-route designs targeting the APEX architecture. Altera's NativeLink™ EDA integration technology enables many third-party synthesis tools to seamlessly integrate with the Quartus software and launch the place-and-route process in the background.

Conclusion

In the past, designers using IP functions have been unable to take advantage of synthesis tools in design flows due to IP encryption issues. Altera has solved this piece of the IP puzzle by allowing system designers to take full advantage of best-in-class synthesis results and compile IP to meet their constraints. This flow enables seamless design re-use for system designers who want to take advantage of the time-to-market benefits offered by Altera's design solutions, while fully realizing the benefits of IP and third-party design tools. Altera is working closely with third-party synthesis vendors to provide the capabilities to support this flow by the end of the year.

Altera & HelloBrain.com:
Using the Internet to Facilitate Customer/Partner Interaction

Programmable logic device (PLD) designers are always looking for ways to shorten the time-to-market of their products. The Altera Megafunction Partners Program (AMPP[SM]) and Altera Consultants Alliance Program (ACAP®) have been instrumental in helping designers complete complex designs in a timely fashion by providing high-quality intellectual property (IP) functions and excellent design services. With an ever-growing list of apt partners, automation of the partner selection process provides a beneficial resource to Altera® users. To automate this process, Altera has joined forces with HelloBrain.com, which provides a web-based intellectual capital exchange for the exclusive use of Altera's designers and partners.

HelloBrain.com has created an efficient method of easily bringing together designers and partners by implementing the world's first web-based intellectual capital exchange (see Figure 1). The new, private Altera exchange, accessible by clicking on the puzzle piece icon (shown at right) found at **http://www.altera.com/ipmegastore**, immediately brings PLD designers together with an existing global network of Altera AMPP and ACAP partners.

At the private exchange, designers can post technical descriptions of critical projects. Altera partners around the world see the posted projects and submit bids to provide a solution. HelloBrain.com's public and private discussion tools allow the designer to anonymously evaluate multiple solutions without commitment and then select the best solution provider for the project. With this quick partner selection, designers save valuable time in bringing their products to market.

HelloBrain.com's transaction infrastructure also eliminates many of the administrative hassles of outsourcing projects. On-line evaluation, transaction, and payment mechanisms allow designers and Altera partners to focus on technological solutions instead of paperwork.

To see some of the projects already transacting on the private Altera exchange, please visit the Altera exclusive intellectual capital exchange by clicking on the HelloBrain.com puzzle piece icon found at **http://www.altera.com/ipmegastore**.

Figure 1. Altera Exclusive Intellectual Capital Exchange Website
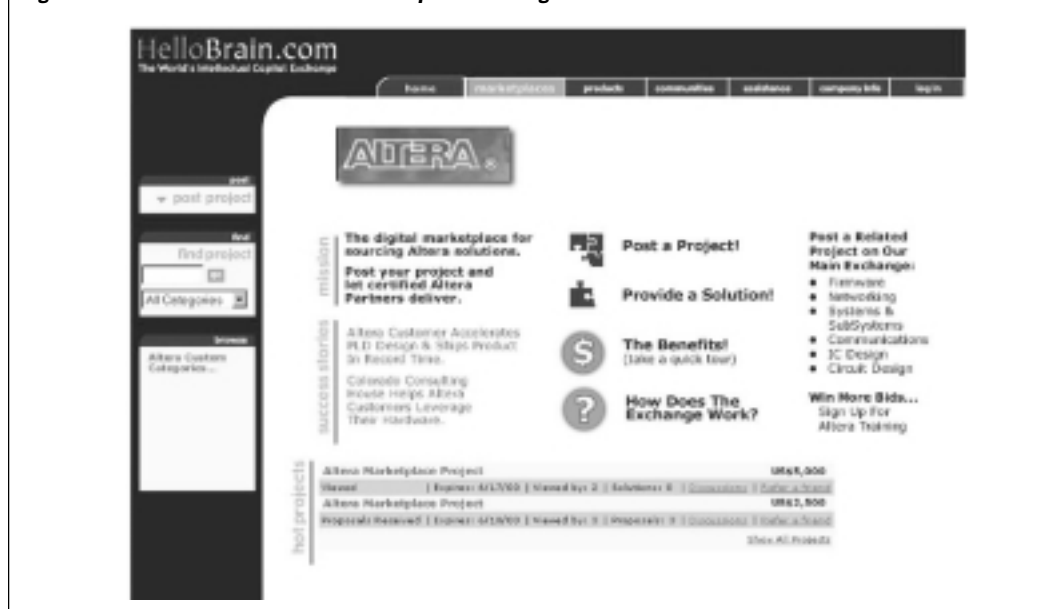
Synplicity's Physical Synthesis Boosts Performance by up to 40%

Programmable logic devices (PLDs) now have the capacity and performance to address a range of applications that was unthinkable a few years ago. With multi-million-gate capacity and performance pushing 200 MHz, programmable logic is now used in many applications that previously could only be accomplished with an ASIC. However, along with this aggressive increase in device performance and capacity comes several challenging issues that must be addressed in order to maintain the productivity and fast time-to-market that is expected of programmable logic. Synplicity is addressing one of the key challenges with a new class of tool—physical synthesis for programmable logic.

The Amplify Physical Optimizer is a true timing-driven physical synthesis product that arrives at timing closure within hours as opposed to weeks.

Amplify Physical Optimizer Delivers the Best Device Performance

A significant problem with designing multi-million gate devices is accounting for the physical routing characteristics of the device during synthesis. As process technology gets smaller, more of the overall circuit delay is due to routing, not logic. For this reason, Synplicity has introduced physical synthesis in a new product for programmable logic designers called the Amplify Physical Optimizer.

The Amplify Physical Optimizer is a timing-driven physical synthesis product that allows you to push circuit performance to the limit and arrive at timing closure within hours as opposed to weeks. Circuits demonstrate up to a 45% performance increase when using the Amplify Physical Optimizer as opposed to traditional synthesis alone. Larger designs typically show a more significant improvement than smaller designs. Accordingly, the larger the device capacity, the more benefits you will see from the Amplify Physical Optimizer. Table 1 shows results from real customer designs that have gone through the the Amplify Physical Optimizer flow. For these examples, timing performance with the Amplify Physical Optimizer was about 27% faster than with traditional synthesis alone.

Table 1. Design Improvements Using Amplify		
Design Number	**Device**	**% Improvement**
1	EPF10K100	15.8
2	EPF10K100	10.1
3	EPF10K100	16.0
4	EPF10K130	27.3
5	EPF10K130	31.1
6	EP20K100E	11.0
7	EP20K100E	18.0
8	EP20K100E	24.6
9	EP20K200E	45.8
10	EP20K200E	36.0
11	EP20K400E	37.6
12	EP20K400E	33.0
13	EP20K400E	34.0

What is Physical Synthesis?

Performing simultaneous placement and synthesis, physical synthesis uses both normal timing constraints as well as physical constraints during the synthesis process (think of physical constraints as an abstract, register transfer level floorplan), producing a highly-optimized design as shown in Figure 1. Designs, or the netlists themselves, synthesized with physical synthesis will be different than those synthesized without; you will most likely see a significant performance improvement if the physical constraints are good. In addition, physical synthesis performs logic placement on the device based upon this combination of timing and physical constraints. The Amplify physical synthesis does not simply annotate delay and re-synthesize logic placement with better delay estimations, but it constrains critical paths to physical regions and then performs a variety of special physical optimizations. The tool can perform these operations only when it is known that certain logic resides in a specific region of the device. The Amplify Physical Optimizer helps prevent timing problems on the front end instead of trying to solve them through time-consuming iterations of back-annotation and re-synthesis.

Figure 1. Physical Synthesis Produces Optimized Designs

Delay is shorter in a column, half-column, or MegaLAB Structure
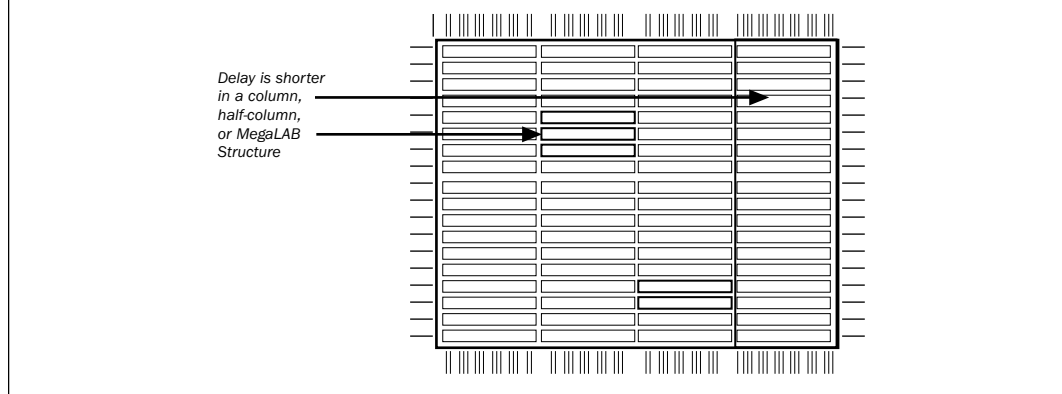
By allowing designers to easily constrain critical paths (at the register transfer level) to physical regions (MegaLAB™ structure), delay estimation is much more accurate and can be used to perform more aggressive circuit optimizations as described below.

■ *Logic Tunneling* — The ability to place registers, moving them across physical boundaries to meet timing constraints, including the ability to move registers into the I/O pins for critical paths going to device output pins.
■ *Logic Replication* — In addition to logic replication performed during normal logic synthesis, the Amplify Physical Optimizer can perform additional replication based upon physical region constraints provided by the user. The Amplify Physical Optimizer also provides the user with the ability to force logic replication without making changes to the HDL source code.
■ *Structure Decomposition* — In some cases, you can achieve the desired performance if you decompose large (wide) structures, such as multipliers, into several smaller structures. The Amplify Physical Optimizerwill automatically perform structure decomposition without HDL code changes if performance is improved by placing several smaller multipliers in different regions of the device.

Additional proprietary physical optimizations are also performed by the Amplify Physical Optimizer. Since the Amplify Physical

Optimizer is truly timing-driven, it will only perform these additional physical optimizations when necessary to meet your timing constraints.

Because the Amplify Physical Optimizer operates at the register transfer level (as opposed to the gate level), it is easier to use than netlist floor planning tools and much more effective. For example, with a netlist floor planning tool, you must re-create the floorplan every time you make HDL code changes, which can be very difficult. Because the Amplify Physical Optimizer acts at the register transfer level, modifications such as changing an 8-bit adder to a 10-bit adder or adding a state to a state machine do not require new physical constraints. If the adder or state machine was constrained to a particular MegaLAB structure before your code change, your existing physical constraints remain valid.

In addition to optimizing your design based upon physical constraints, Amplify also creates placement and sends the information to the Quartus software so that logic is guaranteed to be where you expect it. The unique combination of Amplify physical synthesis algorithms, placement, and intuitive user interface enables a design to reach its performance potential quickly .

For more information on the Amplify Physical Optimizer, visit the Synplicity web site (**http://www.synplicity.com**).

The Amplify Physical Optimizer also creates placement and sends the information to the Quartus software so that logic is guaranteed to be where you expect it.

Improved Performance Specifications
for APEX 20KE PLLs

APEX™ 20KE devices support the ClockLock™, ClockBoost™, and external clock output features, which are all implemented with general purpose phase-locked loops (PLLs). Characterization data from the general-purpose PLL in APEX 20KE devices has led to an increase in its high-speed specifications. The extended range of input and output frequencies to and from the PLL allows for even broader application support.

Input Frequency

The maximum input frequency for the APEX 20KE general-purpose PLLs has been raised, as shown in Table 1. The maximum frequency is only limited by the maximum clock input frequency of the dedicated clock input buffers according to its selectable I/O standard. The dedicated clock inputs have selectable I/O, allowing for selection of different I/O standards. This increase in input frequency expands the operating input range of the PLL, allowing for even more robust performance and versatility with the APEX 20KE PLLs.

VCO Frequency

The frequency range of the voltage-controlled oscillator (VCO) for the PLL has also been extended. The extended range for the VCO is 200 to 500 MHz for all APEX 20KE general-purpose PLLs. The expanded VCO range allows for more possibilities on multiple frequency outputs from a single PLL. The dual frequency outputs from the PLL are generated from the division of a least-common multiple of the two output frequencies. For example, if PLL outputs of 70 and 60 MHz are desired, then the VCO must be running at the least-common multiple of those frequencies, in this case, at 420 MHz. Without the increase in the VCO's operating range up to 500 MHz, this combination of frequencies would require two PLLs.

Output Frequency

Table 2 shows the maximum output frequency for the APEX 20KE general-purpose PLLs. The maximum frequency from the PLL output to the internal global clock is 335 MHz for the -1× speed grade and 200 MHz for the -2× speed grade.

The maximum output clock frequency from the dedicated clock output pin of the PLL (`CLKLK_OUT`) is shown in Figure 1 according to the I/O standard chosen.

This extended range allows for high-speed clock synthesis to the global clocks of APEX 20KE devices. These high-speed clock rates can be used for double date rate (DDR) applications. In APEX 20KE devices, DDR is implemented by

Table 1. PLL Clock Input Frequency Specifications				
I/O Standard	**External Clock Input f_{MAX} (MHz)**			
	-1×		**-2×**	
	Minimum	**Maximum**	**Minimum**	**Maximum**
3.3-V LVTTL	1.5	290	1.5	257
2.5-V LVTTL	1.5	281	1.5	250
1.8-V LVTTL	1.5	272	1.5	243
GTL+	1.5	303	1.5	261
SSTL-2 class I	1.5	291	1.5	253
SSTL-2 class II	1.5	291	1.5	253
SSTL-3 class I	1.5	300	1.5	260
SSTL-3 class II	1.5	300	1.5	260
LVDS	1.5	420	1.5	350

Table 2. PLL Maximum Output Frequency Inside Device	
-1×	**-2×**
335 MHz	200 MHz

using a doubled clock to drive data on- and off-chip. For example, if a 166-MHz clock is used for DDR, then a 333-MHz clock can be generated from the PLL to achieve the 333-Mbps DDR.

Summary

Characterization of APEX 20KE general-purpose PLLs has shown a robust and wide operating range. This has allowed for extended frequency specifications for input, output and VCO. The improved performance specifications of the APEX 20KE further enhance its versatility and application usage. Figure 1 shows a summary of the extended maximum values of the APEX 20KE general-purpose PLL.

Table 3. PLL Off-Chip Clock Output Frequency Specifications				*Note (1)*
I/O Standard	**Off-Chip Output f_{MAX} (MHz)**			
	-1×		**-2×**	
	Minimum	**Maximum**	**Minimum**	**Maximum**
3.3-V LVTTL	1.5	245	1.5	226
2.5-V LVTTL	1.5	234	1.5	221
1.8-V LVTTL	1.5	223	1.5	216
GTL+	1.5	205	1.5	193
SSTL-2 class I	1.5	158	1.5	157
SSTL-2 class II	1.5	142	1.5	142
SSTL-3 class I	1.5	166	1.5	162
SSTL-3 class II	1.5	149	1.5	146
LVDS	1.5	420	1.5	350

Note:
(1) Minimums shown are for the `clock0` output of `altclklock` (PLL). The `clock1` output port has a minimum of 20 MHz.

Figure 1. Extended Maximum Values of the APEX General-Purpose PLL

I/O Standard	CLKIN Input f_{MAX} (MHz)	
	-1×	-2×
3.3-V LVTTL	290	257
2.5-V LVTTL	281	250
1.8-V LVTTL	272	243
GTL+	303	261
SSTL-2 class I	291	253
SSTL-2 class II	291	253
SSTL-3 class I	300	260
SSTL-3 class II	300	260
LVDS	420	350

Global Clock f_{MAX} (MHz)	
-1×	-2×
335	200

I/O Standard	EXTCLKOUT f_{MAX} (MHz)	
	-1×	-2×
3.3-V LVTTL	245	226
2.5-V LVTTL	234	221
1.8-V LVTTL	223	216
GTL+	205	193
SSTL-2 class I	158	157
SSTL-2 class II	142	142
SSTL-3 class I	166	162
SSTL-3 class II	149	146
LVDS	420	350

Implementing an ATM Switch with APEX Embedded CAM

Content addressable memory (CAM) can accelerate the performance of any application that requires faster search results of its databases, lists, or patterns. An example of a CAM application is the asynchronous transfer mode (ATM) switch, in which CAM can be used as virtual channel identifier/virtual path identifier translation tables in ATM switching networks.

ATM Switch

The ATM switch is a high-speed device that uses packet switching techniques in public networks and is capable of supporting many classes of traffic, such as data, video, and voice. ATM traffic consists of a series of fixed-length packets called "cells," with each cell having a 5-byte fixed length header and a 48-byte payload.

ATM networks, which are connection-oriented, need a virtual circuit to be set up across the network prior to any data transfer. Two types of circuits include the virtual path, which is identified by a virtual path identifier, and a virtual channel identifier, which is identified by the channel path identifier.

The time required to compute virtual channel indentifier/ virtual path identifier translations is a critical issue to determine the performance of ATM networks.

Virtual path connection is used to route multiple virtual channels through an ATM network, and virtual channel connection is a bidirectional facility used to transfer ATM traffic between layers.

Because virtual channel identifier/virtual path identifier values are localized, each segment of the connection has a unique virtual channel identifier/virtual path identifier combination. When a cell travels through the network from the user network interface through the switch to the network node interface, the virtual channel identifier/virtual path identifier value is changed to the value the next segment of connection uses through the virtual channel identifier/virtual path identifier translation process, shown in Figure 1.

Figure 2 shows the function of an ATM switch where virtual channel identifier/virtual path identifier values are translated. virtual channel identifier/virtual path identifier values are unique per interface; however, the values can be reused along the network. For example, in Figure 2, the virtual channel identifier/virtual path identifier value of 29 is used in two different interfaces.

Figure 1. Virtual Channel Identifier/Virtual Path Identifier Translation
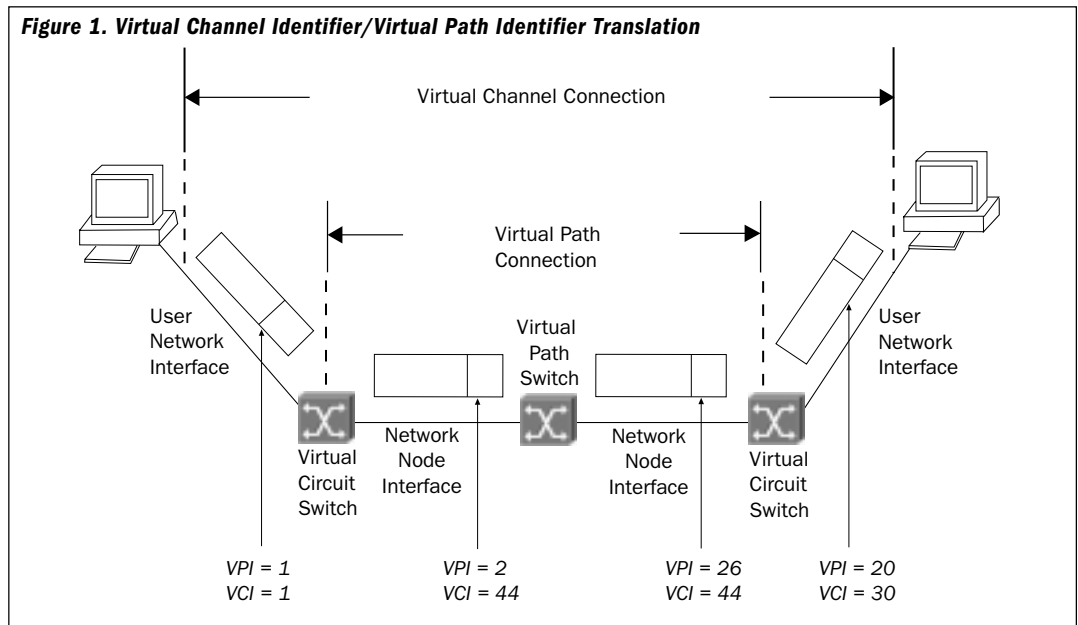
CAM in ATM Switch

The time required to compute virtual channel identifier/virtual path identifier translations is a critical issue to determine the performance of ATM networks. CAM can act as an address translator for look-up tables in ATM switches and perform virtual channel identifier/virtual path identifier translation quickly. virtual channel identifier/virtual path identifier fields from the ATM controller (cell header) are compared against a list of current connections stored in the CAM array. The CAM block generates an address that is used to access an embedded RAM, where virtual channel identifier/virtual path identifier mapping data and other connection information is stored. virtual channel identifier/virtual path identifier data from RAM is added on to the cell and sent to the switch, as shown in Figure 3.

In some ATM applications, there may be a need for a larger CAM than can be supported within the APEX™ device. In such cases, use CAM on an APEX device as cache for an external CAM. The external CAM will store all the connections, while the faster CAM on the device will hold the more frequently accessed connections. Caching the more recently or frequently accessed connections increases system performance.

The performance of an ATM switch is determined in part by the speed of the virtual channel identifier/virtual path identifier translation. The APEX device's embedded CAM can optimize this translation, improving system performance.

Figure 2. Virtual Channel Identifier/Virtual Path Identifier Values Re-Used in the Network

	Input		Output	
Port	**Virtual Path Identifier/ Virtual Channel Identifier**	**Port**	**Virtual Path Identifier/ Virtual Channel Identifier**	
1	29	2	45	
2	45	1	29	
1	64	3	29	
3	29	1	64	
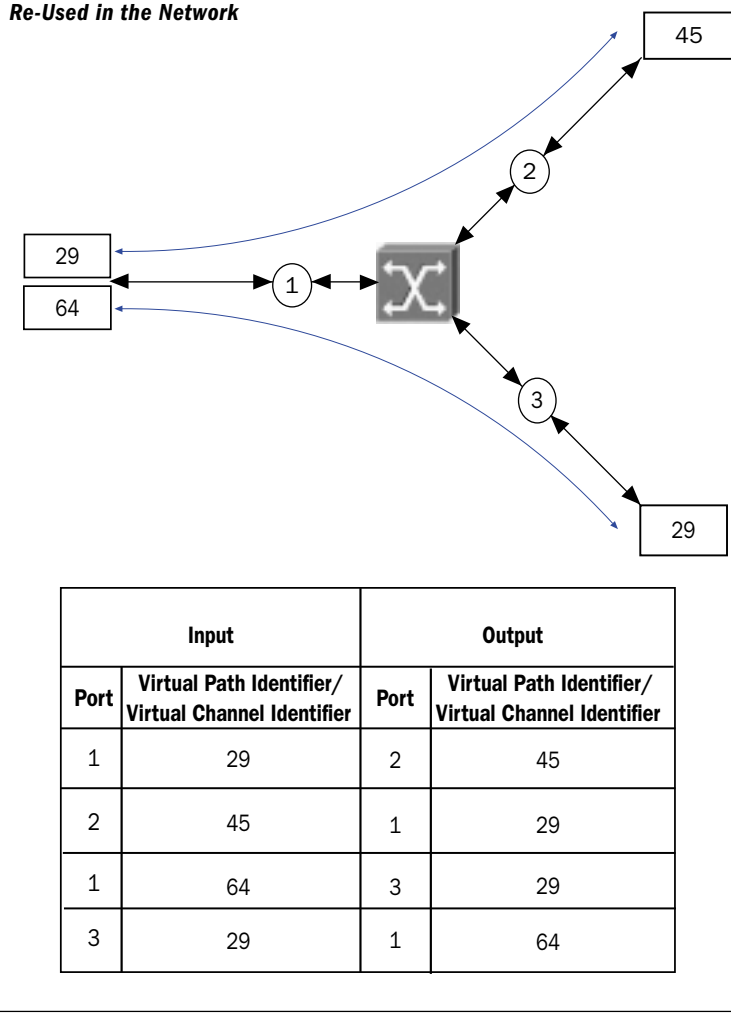
For more information on CAM cache, refer to the *APEX CAM as Cache for External CAM White Paper*.

Figure 3. CAM in ATM Switches
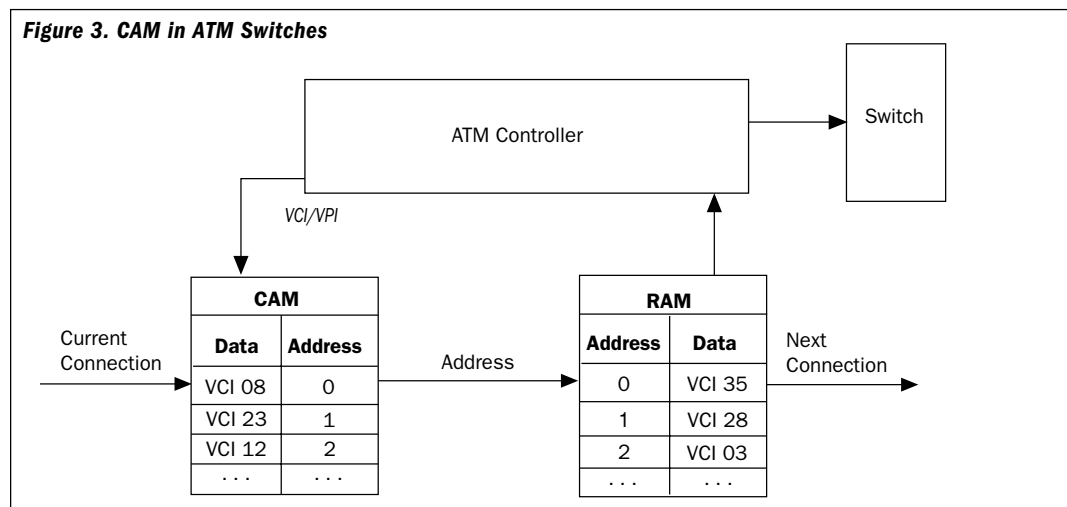
Questions & Answers

Q *What ball-grid array (BGA) packages are available for APEX™ 20K and APEX 20KE devices?*

A APEX 20K and APEX 20KE devices are available in five types of BGA packages, listed in Table 1.

Table 1. APEX 20K & APEX 20KE BGA Packages

Package Name	Ball-Pitch Size (mm)	Pin Count	Device Offered	Maximum Package Height (mm)	Package Description
BGA	1.27	652	EP20K200E EP20K300E	2.3	Plastic BGA package without lid
Super BGA	1.27	356	EP20K60E EP20K100 EP20K100E EP20K160E EP20K200E	1.65	Plastic BGA with metal lid
		652	EP20K400 EP20K400E EP20K600E		
Thermally-enhanced BGA	1.27	652	EP20K1000E EP20K1500E	3.5	Plastic Flip-Chip BGA with ceramic lid
FineLine BGA™	1.0	144	EP20K30E EP20K60E EP20K100E	2.1	FineLine BGA package without lid
		324	EP20K30E EP20K60E EP20K100 EP20K100E		
		484	EP20K160E EP20K200 EP20K200E		
		672	EP20K200E EP20K300E		
Thermally-enhanced FineLine BGA	1.0	672	EP20K400 EP20K400E EP20K600E EP20K1000E	3.5	FineLine BGA Flip-Chip package with ceramic lid
		1,020	EP20K1000E EP20K1500E		

Q *Are the Altera® OEM synthesis tools available to designers using the MAX+PLUS® II BASELINE or E+MAX software with licenses locked to the hard disk volume serial number?*

A The FPGA *Express*-Altera software is available to MAX+PLUS II users who have a BASELINE or E+MAX license tied to the hard disk volume serial number.

The LeonardoSpectrum-Altera software is available to BASELINE or E+MAX users, but they must request a license tied to their network interface card (NIC) number. Exemplar/Mentor Graphics does not permit their tools to be licensed using the hard disk volume serial number. The new NIC-locked license will also be valid for MAX+PLUS II and FPGA *Express*-Altera software, so you do not need more than one active license file.

Both the LeonardoSpectrum-Altera and FPGA *Express*-Altera software can be downloaded from Altera's web site. You can request a free license file from the Altera web site. Select **Free Software** from the Development Tools pull-down menu on the left. Click the **Download** button in the appropriate software box.

The Mentor Graphics' Model*Sim*-Altera software tool is not available for download with the MAX+PLUS II BASELINE or E+MAX software, and is available only to licensed Altera customers.

Q *What is the power consumption of a device while it is performing boundary-scan test (BST)?*

A A device performing BST consumes, at most, the same amount of power that the device will consume while in user mode. You can use *Application Note 74 (Evaluating Power for Altera Devices)* to calculate the power consumption of the device during user mode, and use that same figure to represent the power consumption during BST.

BST operates by using the Joint Test Action Group (JTAG) controller and certain specialized registers to shift data in and out of the chip. The maximum number of toggling registers is equal to the boundary-scan length defined in the boundary-scan description language (BSDL) file for each individual device. The power consumed when shifting test data into these registers is negligible compared to the power consumed by the rest of the device.

When performing BST, power consumption is more a function of the load on the I/O pins than the internal shift register.

Q *Why do I get a "stack overflow" error when running my ported version of the Jam™ Standard Test and Programming Language (STAPL) Player or Jam STAPL Byte-Code Player?*

A If you get a "stack overflow" run-time error, you must tell the compiler used to compile the Jam Player source code how large the stack needs to be. Both the Jam STAPL Player, and the Jam STAPL Byte-Code Player must store at least 50,000 bytes on the stack. Some compilers make their default stack sizes smaller than this, which results in the ensuing run-time error.

When any program runs, the system must provide a certain amount of physical memory, with some of this physical memory allocated for the stack. This stack memory is typically used to store the values of different program variables. Operating systems handle stack memory allocation in either of two ways: fixed stack size or dynamically allocated stack size.

In systems with a large amount of memory (e.g., systems running on Windows NT/95/98/2000 or UNIX environments), the system will usually dynamically allocate memory for the stack. Therefore, you do not need to specify the amount of the available physical memory allocated for the stack.

However, in systems with less memory (such as DOS or embedded processors with less than 64 Kbytes of addressable memory), the operating system has limited memory space with which to work. Therefore, you must specify the size of the physical memory allocated for the stack. This direct specification allows you to specify only what is needed for the stack, thereby getting the best utilization of the limited memory space.

The provided PC-based and UNIX-based 32-bit implementations of the Jam Players can dynamically allocate stack memory. The PC-based 16-bit implementation of the Jam Players must have the stack size specified because the 16-bit DOS and Windows 3.*x* operating systems cannot expand the application's stack space on demand. When porting the Jam STAPL Player or Jam STAPL Byte Code Player to a specific microprocessor, compile the code with the appropriate stack memory settings.

Q *What revision of the Serial Vector Format (.**svf**) specification does Altera support?*

A The MAX+PLUS II software generates SVF Files that use syntax compliant to revision D and E of the SVF specification. These revisions are the latest of the SVF standard.

For more information on the SVF specification, refer to the Asset Intertech web site (**http://www.asset-intertech.com**).

Q *Can I specify an external input delay for clock pins in the Quartus™ software?*

A External input delay is only supported for data pins and the external feedback pin of an APEX 20KE phase-locked loop (PLL) in feedback mode.

To place an external input delay on a feedback clock, you must first instantiate the altclklock megafunction into your design with the feedback mode enabled. Then, you can use the assignment organizer to specify the delay on your clock pin, similar to specifying input delay on a data pin. The setting should be applied to the `CLKLK_FB` signal.

For more information on APEX 20KE PLLs and their applications, see *Application Note 115 (Using the ClockLock & ClockBoost PLL Features in APEX Devices)*.
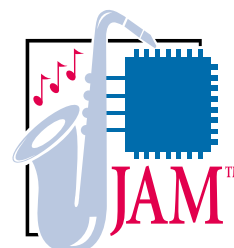
Current Software Versions

The Quartus™ software version 2000.05 is the latest release, and is available for the following operating systems:

- Microsoft Windows 98
- Microsoft Windows NT
- Sun Solaris version 2.6
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported

The MAX+PLUS® II software version 9.6 is available for the following operating systems:

- Microsoft Windows 95 and Windows 98
- Microsoft Windows NT version 3.51 and higher
- Sun Solaris version 2.5 and higher
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported
- AIX version 4.1 and higher

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on the Altera web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- Altera Digital Library CD-Rom, Version 4 (P-CD-ADL2000-04)
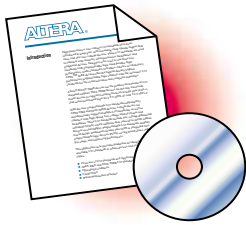- *APEX Devices Brochure* (M-GB-APEX-20K-03)
- *Excalibur Brochure* (M-GB-EXCALIBUR-01)
- *Quartus Brochure* (M-GB-QUARTUS-01)
- *Installing the Visual IP Software User Guide* (A-UG-VISINSTALL-01)
- *PCI-X MegaCore Function User Guide* (A-UG-IPPCIX-01)
- *Simulating the a6402 Model with the Visual IP Software User Guide* (A-UG-A6402VIS-01)
- *Simulating the a8237 Model with the Visual IP Software User Guide* (A-UG-A8237VIS-01)

- *Simulating the a8251 Model with the Visual IP Software User Guide* (A-UG-A8251VIS-01)
- *Simulating the a8259 Model with the Visual IP Software User Guide* (A-UG-A8259VIS-01)
- *Altera Device Package Information Data Sheet, ver. 8.03* (A-DS-PKG-08.03)
- *FLEX 10KE PCI Development Board Data Sheet, ver. 1.01* (A-DS-PCI-C-01.01)
- *AN 116: Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices, ver. 1.03* (A-AN-116-1.03)
- *AN 128: Implementing Voice Over Internet Protocol* (A-AN-128-01)
- *Board Design Guidelines for LVDS Systems White Paper* (M-WP-DESLVDS-01)
- *Implementing ATM Switch with APEX Embedded CAM White Paper* (M-WP-APEXATM-01)
- *Area Optimized Soft Decision Viterbi Decoder Functions White Paper*
- *PIB 29: LVDS Comparison: APEX 20KE vs. Virtex-E Devices* (A-PIB-029-01)

Altera Programming Support

Programming Hardware Support

Table 1 contains the latest programming hardware information for Altera® MAX® 9000, MAX 7000, MAX 3000, and configuration devices. For correct programming, use the software version shown in "Current Software Versions" on page 40.

Table 1. Altera Programming Adapters (Part 1 of 3) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)* EPC1064V *(2)* EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)* EPC1213 *(2)*	DIP, J-lead	PLMJ1213
EPC2 *(4)*	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(5)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(5)* PLMR9000-240NC *(5)*
EPM7032	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032B	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

Table 1. Altera Programming Adapters (Part 2 of 3) *Note (1)*

Device	Package	Adapter
EPM7064S	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(5)*
EPM7064AE EPM7064B	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin) FineLine BGA (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC *(5)* PLMF7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A EPM7128AE EPM7128B EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) TQFP (144-pin) PQFP (160-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMQ7128/7160-160NC *(5)* PLMF7000-100 PLMF7000-256
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMQ7128/7160-160NC *(5)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC *(5)*

Altera Programming Support, continued from page 41

Table 1. Altera Programming Adapters (Part 3 of 3)   Note (1)

Device	Package	Adapter
EPM7256E	PQFP (160-pin)	PLMQ7192/7256-160
	PGA (192-pin)	PLMG7256-192
	PQFP (208-pin)	PLMR7256-208
	RQFP (208-pin)	PLMR7256-208
EPM7256A	TQFP (100-pin)	PLMT7000-100NC (5)
EPM7256S	TQFP (144-pin)	PLMT7000-144NC (5)
EPM7256AE	PQFP (208-pin)	PLMR7256-208NC (5)
EPM7256B	RQFP (208-pin)	PLMT7256-208NC (5)
	FineLine BGA (100-pin)	PLMF7000-100
	FineLine BGA (256-pin)	PLMF7000-256
EPM7512AE	TQFP (144-pin)	PLMT7000-144NC (5)
EPM7512B	PQFP (208-pin)	PLMR7256-208NC (5)
	BGA (256-pin)	PLMB7000-256
	FineLine BGA (256-pin)	PLMF7000-256
EPM3032A	J-lead (44-pin)	PLMJ3000-44
	TQFP (44-pin)	PLMT3000-44
EPM3064A	J-lead (44-pin)	PLMJ3000-44
	TQFP (44-pin)	PLMT3000-44
	TQFP (100-pin)	PLMT3000-100NC (5)
EPM3128A	TQFP (100-pin)	PLMT3000-100NC (5)
	TQFP (144-pin)	PLMT3000-144NC (5)
EPM3256A	TQFP (144-pin)	PLMT3000-144NC (5)
	PQFP (208-pin)	PLMR3256-208NC (5)

Notes:
(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on Classic™ devices.
(2) FLEX® 8000 configuration device.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(4) APEX™ 20K, FLEX 10K, or FLEX 6000 configuration device.
(5) These devices are not shipped in carriers.

Third-Party Programming Support

Data I/O, BP Microsystems, and System General provide programming hardware support for selected Altera devices. Algorithms are available on these companies' respective web sites (**http://www.data-io.com**, **http://www.bpmicro.com**, and **http://www.sg.com.tw**). Programming support information for configuration, MAX 9000, and MAX 7000 devices is shown in Table 2. All information is subject to change.

Table 2. Third-Party Programming Hardware Support

Device	Data I/O (1)	BP Microsystems (2)	System General (3)
EPC1064	✓	✓	✓
EPC1213	✓	✓	✓
EPC1	✓	✓	✓
EPC1441	✓	✓	✓
EPC2	✓	✓	✓
EPM3032A	✓	✓	✓
EPM3064A	✓	✓	✓
EPM3128A	✓	✓	✓
EPM3256A	(4)	✓	✓
EPM7032	✓	✓	✓
EPM7032AE	✓	✓	✓
EPM7032S	✓	✓	✓
EPM7064	✓	✓	✓
EPM7064AE	✓	✓	✓
EPM7064S	✓	✓	✓
EPM7096	✓	✓	✓
EPM7128A	✓	✓	✓
EPM7128S	✓	✓	✓
EPM7128AE	✓	✓	✓
EPM7128E	✓	✓	✓
EPM7160E	✓	✓	✓
EPM7192S	✓	✓	✓
EPM7192E	✓	✓	✓
EPM7256A	(4)	✓	✓
EPM7256AE	(4)	(4)	✓
EPM7256S	✓	✓	✓
EPM7256E	✓	✓	✓
EPM7512AE	✓	✓	✓
EPM9320	✓	✓	✓
EPM9320A	✓	✓	✓
EPM9400	✓	✓	✓
EPM9480	✓	✓	✓
EPM9560	✓	✓	✓
EPM9560A	✓	✓	✓

Notes:
(1) These devices are supported by the Data I/O UniSite programmer version 6.3.
(2) These devices are supported by BP Microsystems programmers version 3.51A.
(3) These devices are supported by System General programmers version 1.0.
(4) Contact Data I/O, BP Microsystems, or System General about programming support for these devices.

Download Cables

Table 3 provides programming and configuration compatibility information for the MasterBlaster™ serial or universal serial bus (USB) communications cable and the BitBlaster™ serial and ByteBlasterMV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable.)

Table 3. Download Cable Compatibility			
Device	**MasterBlaster** *(1)*	**ByteBlasterMV**	**BitBlaster** *(2)*
APEX 20K	✓	✓ *(3)*	
APEX 20KE	✓	✓ *(3)*	
ACEX 1K	✓	✓	✓
FLEX 10K	✓	✓	✓
FLEX 10KA	✓	✓	✓
FLEX 10KE	✓	✓	✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A	✓	✓	✓
MAX 7000B	✓	✓ *(3)*	
MAX 3000A	✓	✓	✓

Notes:
(1) The MasterBlaster communications cable can be used with the Quartus software for device download and SignalTap logic analysis. It can also be used with the MAX+PLUS II software version 9.3 for device downloads.
(2) The BitBlaster download cable must operate at 5.0 V.
(3) The ByteBlasterMV download cable must operate at 3.3 V for these devices. VCCIO pins can be set to either 2.5 V or 3.3 V.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera.

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	General Literature Request *(2)*	**lit_req@altera.com**	**lit_req@altera.com**
	News & Views Subscriptions	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**
	News & Views Address Changes	**n_v@altera.com**	**n_v@altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline	(800) 800-EPLD (6 a.m. to 6 p.m. Pacific Time) (408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time) *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**support@altera.com**	**support@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**

Notes:
(1) The *MAX+PLUS II Getting Started* and *Quartus Tutorial* manuals are available from the Altera® web site. To obtain other Quartus™ and MAX+PLUS® II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

Altera Device Selection Guide

Current information for the Altera® APEX™ 20K, ACEX™ 1K, FLEX® 10K, FLEX 6000, MAX® 9000, MAX 7000, MAX 3000, and configuration devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide.*

For the most up-to-date information, go to the Altera web site at **http://www.altera.com**. Some of the devices listed may not yet be available. Contact Altera or your local sales office for the latest device availability.

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[1]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	MACROCELLS
EP20K30E	30,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 324-Pin BGA[2]	92, 93, 128, 128	1.8 V	1,200	24,576	192
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 93, 148, 151, 196, 196	1.8 V	2,560	32,768	256
EP20K100	100,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	101, 159, 189, 252, 252	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 93, 151, 183, 246, 246	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	88, 143, 175, 271, 316	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2]	144, 174, 277, 382	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 652-Pin BGA, 672-Pin BGA[2]	136, 168, 271, 376, 376, 376	1.8 V	8,320	106,496	832
EP20K300E	300,000	240-Pin RQFP, 652-Pin BGA, 672-Pin BGA[2]	152, 408, 408	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin BGA[2]	502, 502, 502	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	652-Pin BGA, 672-Pin BGA[2]	488, 488	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 508, 588	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 508, 708	1.8 V	38,400	327,680	2,560
EP20K1500E	1,500,000	652-Pin BGA, 1,020-Pin BGA[2]	488, 808	1.8 V	51,840	442,368	3,456

ACEX 1K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[2]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS
EP1K10	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	66, 102, 130, 130	2.5 V	576	12,288
EP1K30	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	102, 147, 171	2.5 V	1,728	24,576
EP1K50	50,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 186, 249	2.5 V	2,880	40,960
EP1K100	100,000	208-Pin PQFP, 256-Pin BGA[2], 484 Pin BGA[2]	147, 186, 333	2.5 V	4,992	49,152

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 189, 191, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA 672-Pin BGA[2]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[2]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA, 672-Pin BGA[2]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	71, 102	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	81, 81, 117, 171, 171	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[2]	117, 171, 199, 218, 218	3.3 V	-1, -2, -3	1,960	1,960

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[3]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[3]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[3]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX, FLEX 10K, FLEX 10KE, and FLEX 6000 devices
EPC4E[4]	44-Pin TQFP, 84-Pin BGA[5]	1.8/2.5 V	4-Mbit serial/parallel configuration device designed to configure all APEX and FLEX 10K devices.

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MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032B	32	44-Pin PLCC/TQFP, 48-Pin TQFP	36, 36	2.5 V	-3, -5, -7
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064AE	64	44-Pin PLCC/TQFP, 49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68	3.3 V	-4, -7, -10
EPM7064B	64	44-Pin PLCC/TQFP, 48-pin TQFP, 49-Pin BGA[1], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68, 68	2.5 V	-3, -5, -7
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 256-Pin BGA[2]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[5], 256-Pin BGA[2]	68, 84, 84, 100, 100, 100	3.3 V	-5,-7,-10
EPM7128B	128	49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[5], 256-Pin BGA[2]	40, 84, 84, 100, 100, 100	2.5 V	-4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S	256	208-Pin PQFP	164	5.0 V	-7, -10, -15
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 84, 120, 164, 164	3.3 V	-5, -7, -10
EPM7256B	256	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 164, 164, 164	2.5 V	-5, -7, -10
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	120, 176, 212, 212	3.3 V	-5, -7, -10, -12
EPM7512B	512	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 212, 212, 212	2.5 V	-5, -6, -7, -10

MAX 3000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM3032A	32	44-Pin PLCC, 44-Pin TQFP	34, 34	3.3 V	-4, -7, -10
EPM3064A	64	44-Pin PLCC, 44-Pin TQFP, 100-Pin TQFP	34, 34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-Pin TQFP, 144-Pin PQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-Pin TQFP, 208-Pin PQFP	116, 158	3.3 V	-6, -7, -10

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

Notes to Tables:
(1) Preliminary. Contact Altera for latest information.
(2) This package is a space-saving FineLine BGA package.
(3) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.
(4) This device can be programmed by the user to operate at either 1.8 V or 2.5 V.
(5) This package is a space-saving Ultra FineLine BGA package, Altera's 0.8-mm pitch BGA package.