News & Views
Fourth Quarter 2000
Newsletter for Altera Customers

ALTERA®
The Programmable Solutions Company®

QUARTUS™ 2000.09

Quartus Version 2000.09 Dramatically Improves f_{MAX} & Compile Times

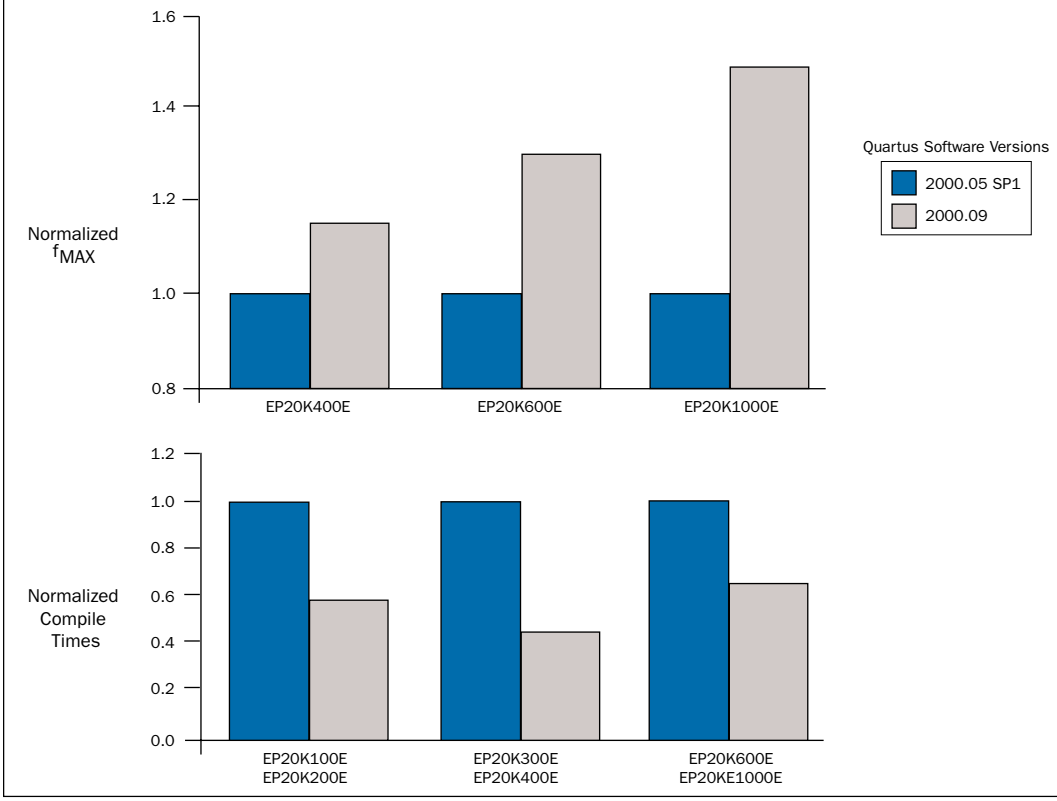
The Quartus™ software version 2000.09 includes the new PowerFit™ fitter that delivers an average of 15% to 45% faster f_{MAX} and 1.5× to 3.0× faster compile times for designs targeting APEX™ EP20K400E and larger devices. This new PowerFit fitter technology optimizes designs based on the user's timing specifications and meets design requirements with only minimal user effort.

Figure 1 shows the design performance enhancements and compile time reductions achieved with the PowerFit technology. The charts in Figure 1 demonstrate these improvements over a design set compiled using random pin assignments in the Quartus software versions 2000.05 Service Pack 1 and 2000.09.

With each new release, the Quartus software has consistently improved compile times. Figure 2 on page 4 highlights compile time improvements for designs targeting high-density devices.

continued on page 4

Figure 1. Median Design Performance & Relative Compile Time Improvement by Device



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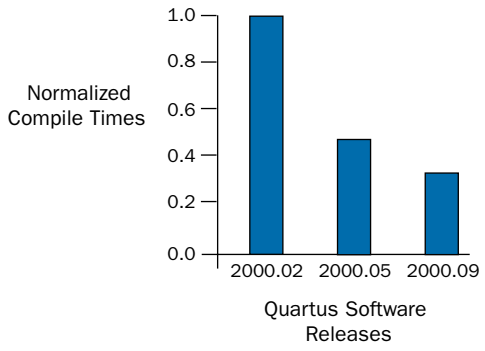
Quartus Version 2000.09 Dramatically Improves f_{MAX} & Compile Times, continued from page 1

Figure 2. EP20K600E & EP20K1000E Device Compile Times



PowerFit Technology Improves Device Fitting

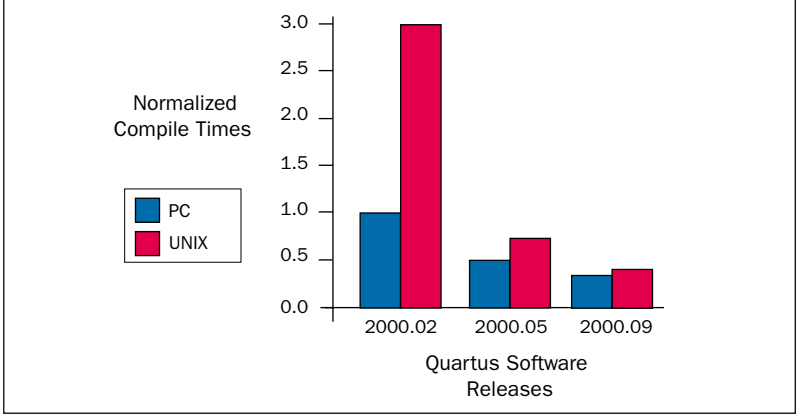
The PowerFit technology dramatically enhances the stability of the fitter as well as device fitting, particularly for the highest density APEX 20KE devices. This enhancement allows designers to fit larger designs into a given APEX device.

UNIX Installation & Compile Time Improvements

In addition to the PowerFit technology improvements, the Quartus software version 2000.09 includes new database technology developed by Altera. This database technology simplifies installation in UNIX environments and reduces UNIX-specific compile time bottlenecks.

Figure 3 shows the PC and UNIX compile time improvements.

Figure 3. PC & UNIX Compile Time Improvement



With previous versions of the Quartus software, high-density designs took longer to compile on Solaris platforms. The Quartus software version 2000.09 eliminates this problem through Solaris compiler optimization. The Quartus software version 2000.09 for Solaris offers compile times over 8× faster than version 2000.02.

Compile times for the Quartus software version 2000.09 for Solaris are now only 1.15× longer than PC compile times (SPECint normalized to account for performance differences in PC- and UNIX-based processor architectures).

Reduced Memory Requirements

The minimum physical RAM required to compile high-density APEX devices drops significantly with the Quartus software version 2000.09.

The Quartus software version 2000.05 required 1,331 Mbytes of RAM to compile large EP20K1000E and EP20K1500E devices. The Quartus software version 2000.09 enables mainstream PCs using Windows NT to compile designs for the largest APEX 20KE devices without this high memory requirement. Table 1 lists the memory requirements for the Quartus software version 2000.09.

Table 1. Quartus 2000.09 Memory Requirements

Device	Minimum Physical RAM
EP20K30E EP20K60E EP20K100E EP20K160E EP20K200E	256 Mbytes
EP20K300E EP20K400E EP20K600E	512 Mbytes
EP20K1000E EP20K1500E	1,024 Mbytes

HP-UX 11.0 Support Now Available

The Quartus development tool is now available for both the HP-UX 11.0 and 10.2 operating systems. HP-UX versions of the software are not included in Altera's standard software shipments. If you have an active FLOATNET subscription and would like to receive the

Quartus development tool for HP-UX, fill out the on-line request form on the Altera web site at **http://www.altera.com/hpux**, and the software will be sent to you.

Timing Analysis Enhancements

The Quartus software version 2000.09 includes timing analysis enhancements that make it easier to analyze circuits with complex clocking structures as well as specify multicycle path relationships. The Quartus software version 2000.09 optimizes support for third-party simulation and timing analysis tools by creating distinct VHDL or Verilog HDL verification netlists and Standard Delay Format Files (**.sdo**) targeted to specific third-party tools.

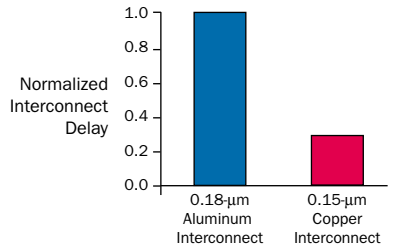
Third-Party Integration Enhancements

Top-level block design schematic files can now be converted to VHDL or Verilog HDL design files using the Quartus software version 2000.09. The VHDL or Verilog output files can be processed by third-party synthesis and simulation tools. The Quartus software version 2000.09 also facilitates the use of encrypted Altera intellectual property (IP) MegaCore® functions through third-party synthesis tools to produce optimal results. For more information on these features, visit the Altera web site at **http://www.altera.com**.

APEX 20KC Devices with All-Layer Copper Interconnect Enhance Internal Performance by 25% to 35%

The new APEX™ 20KC devices are the first programmable logic devices (PLDs) with an all-layer copper metal interconnect, providing a 25% to 35% performance advantage over 0.18-µm-based devices using aluminum interconnect (see Figure 1).

Figure 1. Relative Interconnect Delay



Because of the relatively small routing delays with copper, APEX 20KC devices can support the high-bandwidth needs of advanced networking standards that exist in the communication marketplace.

APEX 20KC devices provide a feature set comparable to APEX 20KE devices, including content-addressable memory (CAM), True-LVDS™ circuitry, and advanced clock management. These features make APEX 20KC devices the industry-leading, high-density device for high-end system-on-a-programmable-chip (SOPC) solutions.

0.15-µm all-layer copper interconnect-based APEX 20KC devices offer a 25% to 35% performance improvement over 0.18-µm-based devices.

All-Layer Copper Interconnect

Breakthroughs in semiconductor performance have been primarily in transistor fabrication. However, in advanced processes, a large portion of chip delays are due to routing structure delays, not transistors. Therefore, significant performance enhancements can be achieved by replacing aluminum—which is traditionally used in routing structures—with a superior conductor of electricity that significantly decreases routing delays and increases overall system performance.

continued on page 6

APEX 20KC Devices with All-Layer Copper Interconnect Enhance Internal Performance by 25% to 35%, continued from page 5

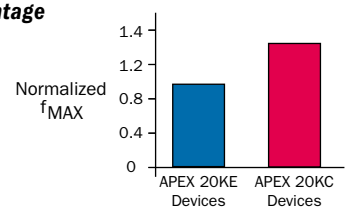
The primary benefit of using copper for the interconnect layers is improved internal performance. For example, APEX 20KC devices with all-layer copper interconnect technology provide a 25% to 35% performance advantage over the aluminum interconnects found in APEX 20KE devices (see Figure 2). A faster interconnect increases the operating frequencies of designs.

The largest APEX 20KC device will have 1.5 million system gates and more than 800 user I/O pins.

All-Layer Copper Interconnect vs. Partial Copper Interconnect

All-layer copper interconnect technology uses copper for all metal layers. Partial copper interconnect has copper on the top layers only.

Figure 2. APEX 20KC Device Performance Advantage



The top layers are power planes, while the bottom layers are performance-critical interconnect layers. Figure 3 shows a cross-section of these interconnect layers.

Copper on the top layer only does not offer a significant performance increase because these power layers do not have a major impact on performance. In fact, using copper on the top two layers will create silicon/copper design challenges without providing significant performance benefits. Only the all-layer copper interconnect, including the performance-critical bottom layers, will lead to a significant performance advantage.

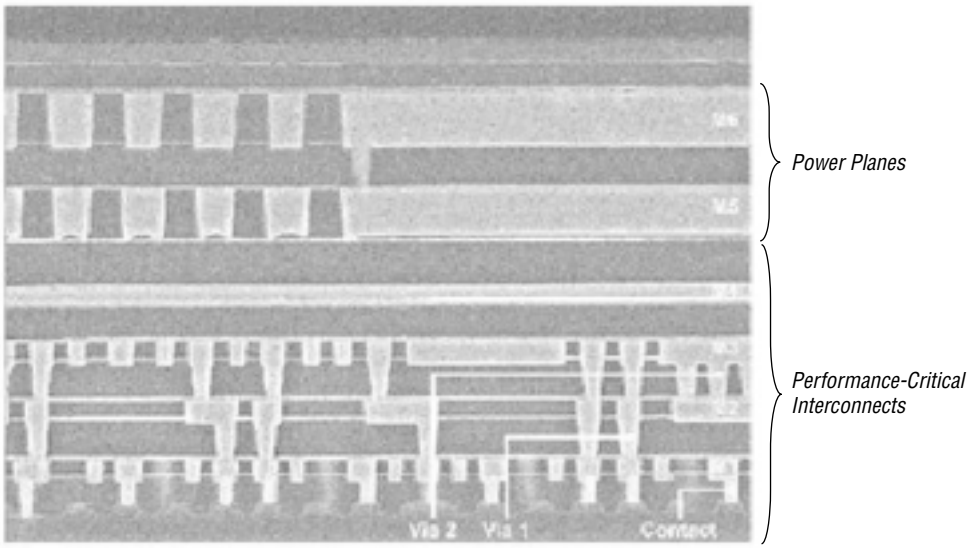
APEX 20KC Process Technology

APEX 20KC devices will be fabricated on a state-of-the-art 0.15-µm, 8-layer metal process with a copper interconnect. This more advanced process technology and all-layer copper interconnect will provide significant performance advantages over APEX 20KE devices.

APEX 20KC Device Offering & Features

APEX 20KC devices will continue Altera's leadership in density and user I/O pins. The

Figure 3. Cross-Section of Interconnect Layers



largest APEX 20KC device will have 1.5 million system gates and more than 800 user I/O pins. Table 1 outlines the APEX 20KC device features.

APEX 20KC devices will have many of the same features as APEX 20KE devices, including True-LVDS circuitry, CAM, phase-locked loops (PLLs), and advanced I/O standards.

True-LVDS Support

APEX 20KC devices will support True-LVDS circuitry up to 840 megabits per second (Mbps), which make them ideal for advanced network protocols that require high data transfer rates.

Content Addressable Memory

APEX 20KC devices will support CAM applications in embedded system blocks (ESBs). The copper interconnect of APEX 20KC devices will further reduce access times and make high-speed CAM applications possible in Altera devices without the use of external CAM chips.

Phase-Locked Loops

APEX 20KC PLLs will offer higher operating frequency ranges than the APEX 20KE PLLs.

Advanced I/O Standards

APEX 20KC devices will support all APEX 20KE advanced I/O standards, including HSTL, GTL+, and SSTL.

Advanced feature support, high density, and fast performance make APEX 20KC devices ideal for SOPC applications.

APEX 20KC devices will support True-LVDS circuitry, CAM, PLLs, and advanced I/O standards.

Software Support & Device Availability

APEX 20KC devices will be supported in Altera's industry-leading Quartus™ software by the end of 2000. Devices will be available in the first half of 2001.

Table 1. APEX 20KC Device Overview

Device	Maximum System Gates	Logic Elements (LEs)	Maximum RAM Bits	PLLs	Speed Grades *(1)*
EP20K100C	263,000	4,160	53,248	2	-7, -8, -9
EP20K200C	526,000	8,320	106,496	2	-7, -8, -9
EP20K400C	1,052,000	16,640	212,992	4	-7, -8, -9
EP20K600C	1,537,000	24,320	311,296	4	-7, -8, -9
EP20K1000C	1,772,000	38,400	327,680	4	-7, -8, -9
EP20K1500C	2,392,000	51,840	442,368	4	-7, -8, -9

Note:
(1) The -7 speed grade is the fastest speed grade.

Discontinued Devices Update

Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

ARM- & MIPS-Based Excalibur Products Provide Industry-Leading Performance & Flexibility

Altera's Excalibur™ embedded microprocessor-based products are the first in the industry to combine the design flexibility of programmable logic with high-performance embedded processors, large on-chip SRAM memory arrays, and peripherals that are essential for system-level design. Altera has licensed both a MIPS32™ 4Kc™ processor core from MIPS® Technologies and an ARM922 core from ARM® Ltd., two of the most widely used instruction set architectures in the embedded systems market. These cores eliminate customer processor licensing and per-unit royalties; Altera takes care of these business issues and offers standard products that customers can immediately design for faster time-to-market.

Altera's ARM-based Excalibur products will be available in Q1 of 2001, followed by the MIPS-based products in Q2 of 2001. Both Excalibur products have hardmacro processor implementations for maximum performance and will operate at 200-MHz processor clock frequencies. Both ARM- and MIPS-based Excalibur products include on-chip single port memory (up to 256 Kbytes), dual-port memory (up to 128 Kbytes), external flash memory support (up to 32 Mbytes), and an SDRAM controller capable of supporting up to 512 Mbytes of 133-MHz (PC133) external memory or up to 256 Mbytes of 266-MHz (PC266) double data rate (DDR) external memory.

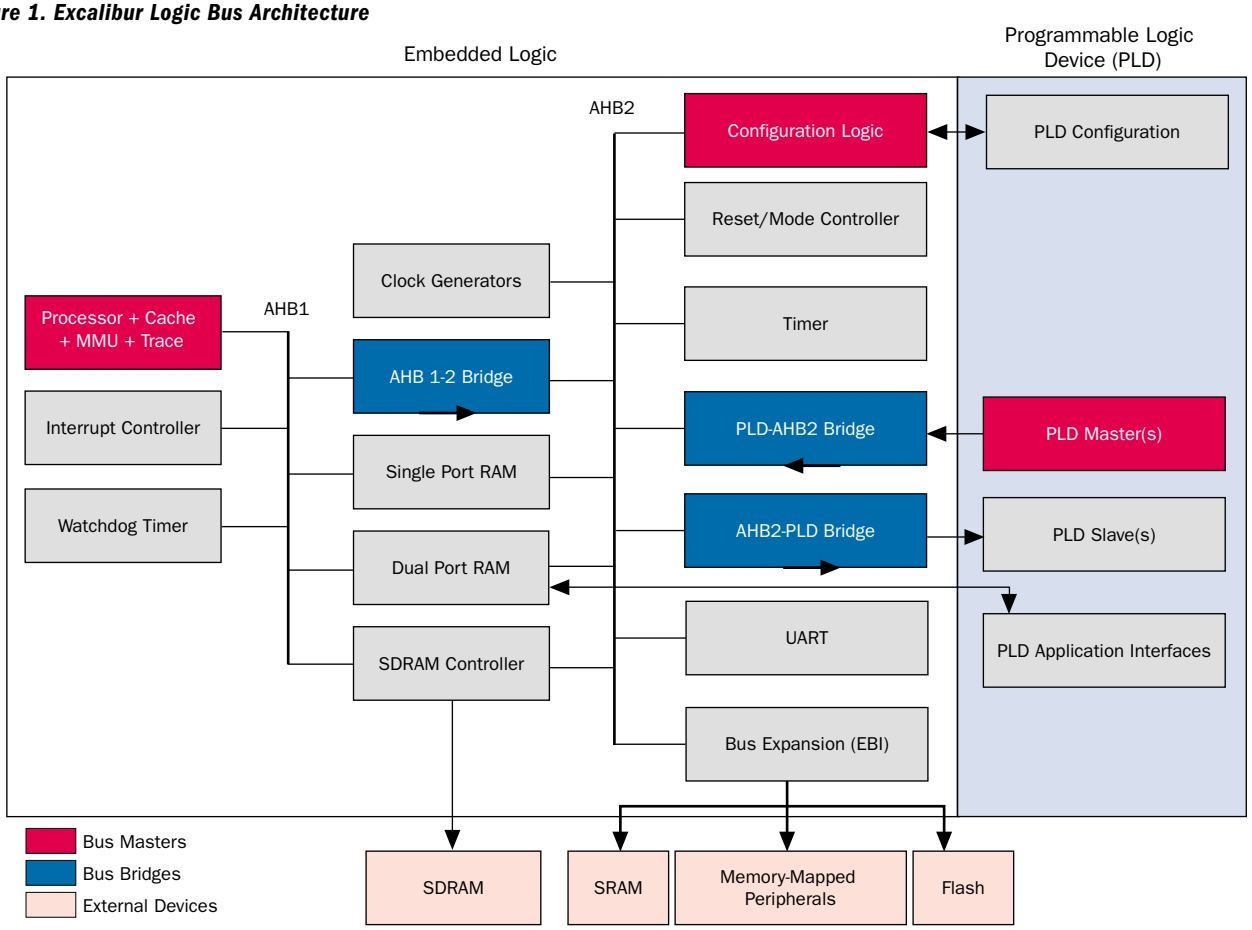
On-chip peripherals include interrupt controllers, universal asynchronous receiver / transmitters (UARTs), general purpose timers, watchdog timers, an ETM9 embedded trace module, and JTAG support for the ARM922-based products as well as EJTAG support for the MIPS 4Kc-based products. Altera's high-performance APEX™ 20KE architecture is implemented in the Excalibur products. Table 1 shows the three different Excalibur ARM- and MIPS-based product features.

One of the key advantages of both Excalibur hard core products is that the on-chip processor system buses operate at full processor clock frequencies (up to 200 MHz) for maximum system bandwidth and performance. This enables superior system-level performance. Other conventional, discrete processor-based solutions may be limited by processor system buses that operate at half the CPU clock frequency or by system controller chip sets that only offer 133 MHz SDRAM controller support. The advanced Excalibur hard core embedded processor products that feature key on-chip peripherals support, large on-chip memory arrays, APEX embedded system blocks (ESBs) memory bits, and the design flexibility and time-to-market advantages of integrated programmable logic structures makes the Excalibur products ideal for system-level design.

Table 1. ARM- & MIPS-Based Excalibur Device Features

Feature	EPXA1/EPXM1	EPXA4/EPXM4	EPXA10/EPXM10
Maximum system gates	263,000	1,052,000	1,772,000
Typical gates	100,000	400,000	1,000,000
Logic elements (LEs)	4,160	16,640	38,400
ESBs	26	104	160
Maximum RAM bits	53,248	212,992	327,680
Maximum macrocells	416	1,664	2,560
Maximum user I/O pins	178	360	521
Single-port SRAM	32 Kbytes	128 Kbytes	256 Kbytes
Dual-port SRAM	16 Kbytes	64 Kbytes	128 Kbytes

Figure 1. Excalibur Logic Bus Architecture



Both Excalibur ARM- and MIPS-based products implement the advanced microcontroller bus architecture (AMBA™) high-performance bus (AHB). This is an industry-standard bus architecture capable of multiple bus masters, slave modules, locked transfers, split transactions, and bus frequencies of up to 200 MHz. The AMBA AHB is used as an interface between the processor stripe, bus masters, and slave modules implemented in the programmable logic architecture (see Figure 1).

The processor and the PLD bus master can simultaneously access different blocks of the on-chip single-port memory and on-chip dual-port memory. In addition, different system functions (e.g., processor and on-chip memory, SDRAM controller and peripherals, and PLD structure) are decoupled from each other through localized bus structures and are driven by phase-locked loops (PLLs) in different clock domains. The AMBA bus interface can be used to interface with the Altera® MegaCore® intellectual property (IP) functions or third-party Altera Megafunction Partners Program (AMPP℠) partner IP blocks.

Both Excalibur ARM- and MIPS-based products are fully supported by industry-standard real-time operating systems (RTOSs) and embedded software tool chains (e.g., compilers, debuggers, assemblers, linkers, and loaders). The Quartus™ development tool is used for design entry, simulation, and synthesis through third-party tools, and optimized place and route of designs implemented in the programmable logic structure.

EXCALIBUR™

APEX

Introducing New APEX 20KC Devices

The new high-performance APEX™ 20KC devices address the high-bandwidth needs of system-on-a-programmable-chip (SOPC) applications. These devices combine the state-of-the-art features found in APEX 20KE devices with industry-leading, 0.15-µm all-layer copper interconnect technology to provide performance improvements of 25% to 35% over 0.18-µm-based devices. For more information on these new APEX devices, see "APEX 20KC Devices with All-Layer Copper Interconnect Enhance Performance by 25% to 35%" on page 5.

All 10 APEX 20KE Devices Now Shipping

The APEX EP20K30E device, the smallest APEX 20KE device, is now shipping. With 30,000 typical gates (113,000 maximum system gates), 1,200 logic elements (LEs), 24 Kbits of RAM and 128 maximum user I/O pins, this device addresses low-density application needs. All 10 APEX 20KE devices are now shipping: EP20K30E, EP20K60E, EP20K100E, EP20K160E, EP20K200E, EP20K300E, EP20K400E, EP20K600E, EP20K1000E, and EP20K1500E. These devices are available in multiple packages, including the advanced Fineline BGA™ package.

LVDS & PLL Support Now Available in Industrial-Speed-Grade Devices

In addition to offering data transfer rates up to 840 megabits per second (Mbps) on commercial temperature grade devices, APEX 20KE devices now support LVDS in industrial-speed-grade devices. APEX 20KE industrial-grade devices also feature phase-locked loops (PLLs). Table 1 summarizes the LVDS support in APEX 20KE devices. Table 2 summarizes PLL support in APEX 20KE devices.

The True-LVDS™ solution, with data transfer rates as high as 840 Mbps per channel, is ideal for high-speed telecommunication, data communication, and computing applications.

Table 1. LVDS Support in APEX 20KE Devices

Device	Maximum Data Transfer Rate Per True-LVDS Channel (Mbps)		
	Commercial -1X	Commercial -2X	Industrial -2X
EP20K300E	156	156	156
EP20K400E	840	700	625
EP20K600E	840	700	625
EP20K1000E	750	625	625
EP20K1500E	750	625	625

Table 2. PLL Support in APEX 20KE Devices

Speed Grade	Maximum Internal Output Frequency from PLL (MHz)
Commercial -1X	335
Commercial -2X	250
Industrial -2X	250

The PLLs offer flexible frequency synthesis and zero clock skew capability for high-performance design needs. APEX 20KE devices also support the LVPECL standard that can be used in high-performance clocking schemes, backplanes, optical transceivers, high-speed networking, and high-end video applications.

APEX 20KE Production Devices

All APEX 20KE -ES and -XES engineering sample devices have changed to production -1 and -1X speed grade devices. These production-ready devices are available today in all packages and replace the engineering sample devices.

5.0-V Tolerant APEX 20K & APEX 20KE Devices

The APEX 20K device family has been enhanced to provide a 5.0-V tolerant I/O buffer, providing full compliance with the 5.0-V PCI specification. 5.0-V tolerant devices are now shipping and have a "V" suffix in the ordering code (e.g., EP20K400BC652-1V).

APEX 20KE devices can be used with an additional external resistor to make them 5.0-V

tolerant and provide flexibility for system design. For details on this improvement, see the *5.0-V Tolerance in APEX 20KE Devices White Paper* on the Altera® web site (**http://www.altera.com**).

Table 3. APEX 20KE Device & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K30E	144-pin TQFP *(1)*	Now
	144-pin FineLine BGA	Now
	208-pin PQFP *(1)*	Now
	324-pin FineLine BGA	Now
EP20K60E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA *(1)*	Now
EP20K100E	144-pin TQFP	Now
	144-pin FineLine BGA	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	Now
EP20K160E	144-pin TQFP	Now
	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K200E	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K300E	240-pin PQFP	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K400E	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1500E	652-pin BGA	Now
	1,020-pin FineLine BGA	Now

Note:
(1) TQFP: thin quad flat pack, PQFP: plastic quad flat pack, BGA: ball-grid array.

APEX 20K Product Transition

Altera is migrating the 2.5-V EP20K400 device from a 0.25-µm process to a 0.22-µm process. Information regarding this device migration can be found in process change notification (PCN) 0005, available on the Altera web site at **http://www.altera.com**.

ACEX

ACEX 1K Devices Shipping Now

ACEX™ 1K devices are now shipping in all packages for 10,000-, 30,000-, 50,000-, and 100,000-gate densities (see Table 4). These cost-optimized devices are especially suited for low-cost, high-volume applications and can be used to attain the lowest cost per PLD for high-volume designs.

ACEX 1K devices are now shipping in all packages in the 10,000, 30,000, 50,000, and 100.000 gate densities.

Table 4. ACEX 1K Device Offerings

Device	Package	Availability
EP1K10	100-pin TQFP	Now
	144-pin TQFP	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
EP1K30	144-pin TQFP	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
EP1K50	144-pin TQFP	Now
	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now
EP1K100	208-pin PQFP	Now
	256-pin FineLine BGA	Now
	484-pin FineLine BGA	Now

ACEX 1K devices provide full PLL capability for ClockLock™ and ClockBoost™ features, such as embedded dual-port RAM and full 64-bit, 66-MHz PCI compliance in every -1X and -2X speed grade device. Developed on a cost-optimized 0.22-µm/0.18-µm hybrid process, and featuring a 2.5-V core operating voltage, ACEX 1K devices offer an ideal combination of cost, performance, and features.

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Devices & Tools, continued from page 11

Full software support for ACEX 1K devices is available from the MAX+PLUS® II software version 10.0. In addition, a wide range of ACEX-optimized intellectual property (IP) functions can now be found at the Altera IP MegaStore™ on-line store.

MAX

Broad Range of FineLine BGA Packages Available for MAX Devices

MAX® devices are available in a wide range of FineLine BGA™ packaging, including both the 1.0-mm pitch (FineLine BGA) and the 0.8-mm pitch (Ultra FineLine BGA) packages. Table 5 shows the FineLine BGA and Ultra FineLine BGA packaging options for MAX 7000B devices.

FineLine BGA packages occupy a smaller footprint than traditional TQFP packages and can offer more I/O pins to the designer.

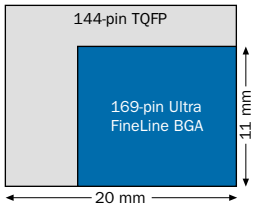
Table 5. FineLine BGA Packages Available for MAX Devices

Device	100-Pin FineLine BGA	256-Pin FineLine BGA	49-Pin Ultra FineLine BGA	169-Pin Ultra FineLine BGA
EPM7032B			✓	
EPM7064B	✓		✓	
EPM7128B	✓	✓	✓	✓
EPM7256B		✓		✓
EPM7512B		✓		✓
EPM7064AE	✓		✓	
EPM7128AE	✓	✓		✓
EPM7256AE	✓	✓		
EPM7512AE		✓		

FineLine BGA packages occupy a smaller footprint than traditional TQFP packages and can offer more I/O pins to the designer. For example, Figure 1 shows a 169-pin Ultra FineLine BGA package that occupies less than half the board space occupied by the 144-pin TQFP package.

An EPM7512B device in a 169-pin FineLine BGA package offers 141 I/O pins compared to the 120 I/O pins offered in a 144-pin TQFP package.

Figure 1. Ultra FineLine BGA Package



This variety of BGA packages and pin counts offers flexibility in choosing the device that is right for your specific application.

MAX 7000B Industrial-Grade Availability

Altera now offers the popular 2.5-V MAX 7000B devices in industrial-grades. Table 6 shows which packages are now available in the industrial grade. Contact your local Altera sales representative for availability and lead times on specific packages.

Table 6. MAX 7000B Industrial-Temperature Devices

Device	Package	Speed Grade
EPM7032B	44-pin TQFP	-5
EPM7064B	44-pin PLCC	-5
	44-pin TQFP	-5
	100-pin TQFP	-5
EPM7128B	100-pin TQFP	-7
	100-pin FineLine BGA	-7
	144-pin TQFP	-7
	256-pin FineLine BGA	-7
EPM7256B	100-pin TQFP	-7
	144-pin TQFP	-7
	208-pin PQFP	-7
	256-pin FineLine BGA	-7
EPM7512B	256-pin BGA	-7
	256-pin FineLine BGA	-7

MAX 7000AE Devices Migrate to Advanced Process

MAX 7000AE devices will migrate to a 0.30-µm quad-layer-metal process. This process is a linear shrink of the existing 0.35-µm quad-layer-metal process that uses the same equipment and process flow. These devices will be pin-, function-, timing-, and programming file-compatible with existing 0.35-µm versions of the MAX 7000AE devices.

This transition will begin on March 20, 2001. After this date, you may receive devices from either the 0.35-µm or 0.30-µm quad-layer-metal processes.

For additional information regarding this transition, contact your local Altera sales representative. Initial qualification and characterization data will be available on December 20, 2000. Contact Altera's Customer Quality Engineering Manager at (408) 544-7563 for more details.

CONFIGURATION

High-Density Configuration Devices Coming Soon

The new 4-Mbit EPC4 and 16-Mbit EPC16 configuration devices are scheduled for release in January 2001. These new devices will include features such as faster configuration times and reprogrammability. Additionally, you can use a single device to configure several APEX™ or FLEX® devices in parallel to further speed configuration and save board space.

A single EPC16 device will configure two 1.5-million-gate EP20K1500E devices using the new data compression features.

TOOLS

Quartus Version 2000.09 & MAX+PLUS II Version 10.0 Now Available

Version 2000.09 of the Quartus™ development tool brings dramatic performance improvements to Altera customers. The new PowerFit™ fitting technology improves customer design performance by up to 45% and decreases compile times by 1.5× to 3.0×, depending on the device density for the design. For more details on the Quartus software version 2000.09 see the "Quartus Version 2000.09 Dramatically Improves f_{MAX} & Compile Times" feature article on page 1, or visit the Altera web site at **http://www.altera.com**.

Table 7 lists the new devices supported by the Quartus software version 2000.09.

Table 7. New Devices Supported by the Quartus Software Version 2000.09

Support	Device	Package
Full Compilation, Simulation, and Programming Support	EP20K60E	144-pin FineLine BGA, 324-pin FlneLine BGA, 356-pin BGA
	EP20K100E	144-pin FineLine BGA
	EP20K160E	144-pin TQFP, 208-pin RQFP, 240-pin PQFP, 356-pin BGA, 484-pin FineLine BGA
	EP20K600E	1,020-pin FineLine BGA
	EP20K1500E	652-pin BGA, 1,020-pin FineLine BGA
Compilation and Simulation Support	EP20K30E	144-pin TQFP, 144-pin FineLine BGA, 208-pin RQFP, 324-pin FineLine BGA, 356-pin BGA

The MAX+PLUS II software version 10.0 adds support for the latest MAX 7000B device package combinations and adds programming support for the new ACEX EP1K10 devices. Table 8 lists the new devices supported by the MAX+PLUS II software version 10.0.

Table 8. New Devices with Full Support from the MAX+PLUS II Software Version 10.0

Device	Package
EPM7032B	44-pin TQFP 49-pin Ultra FineLine BGA
EPM7064B	49-pin Ultra FineLine BGA 100-pin FineLine BGA
EPM7064AE	49-pin Ultra FineLine BGA
EPM7128B	49-pin Ultra FineLine BGA
EPM7256B	169-pin Ultra FineLine BGA
EPM7512B	144-pin TQFP 256-pin BGA 256-pin FineLine BGA 169-pin Ultra FineLine BGA
EP1K10	100-pin TQFP 144-pin TQFP 208-pin PQFP 256-pin BGA

continued on page 14

Devices & Tools, continued from page 13

Operating System Update

The Quartus software version 2000.09 and the MAX+PLUS II software version 10.0 both support the Windows 2000 operating system. The Quartus software version 2000.09 also adds support for the HP-UX 11.0 operating system. Table 9 shows the Quartus and MAX+PLUS II operating system support.

The next release of the Quartus software will include a software mode to allow designers to co-design software and hardware within the Quartus environment.

Table 9. Quartus & MAX+PLUS II Operating System Support

Software	Operating System Support
Quartus version 2000.09	Windows 2000, Windows 98, Windows NT version 4.0 and higher, Sun Solaris 2.6 and 2.7, and HP-UX 10.2*x* and 11.0 *(1)*
MAX+PLUS II version 10.0	Windows 2000, Windows 98, Windows 95, Windows NT version 4.0 and higher, Sun Solaris 2.5 and 2.6, HP-UX 10.2*x*, and AIX version 4.1 and higher *(1)*

Note:
(1) Support for Solaris 2.8 will be added in the initial releases in 2001.

Quartus Roadmap

The next major release of the Quartus software is scheduled for Q1 2001. This release will support the Altera Excalibur™ hard core embedded processor solutions and include major enhancements that help designers with PLD and system-level design issues.

In addition to the compilation and simulation modes, the next release of the Quartus software will include a software mode to allow designers to co-design software and hardware within the Quartus environment. This new mode will provide the capability to configure the ARM, MIPS, and Nios embedded processors and their integration with C/C++ compiler tools.

MAX+PLUS II BASELINE, E+MAX & ASAP2 Version 10.0 Now Available

MAX+PLUS II BASELINE development software, E+MAX™ development software, and ASAP2 programmer software version 10.0 are now available for download from the Altera web site at **http://www.altera.com**. These software programs provide support for the latest MAX 7000B devices. The MAX+PLUS II BASELINE software version 10.0 also adds support for the latest ACEX EP1K10 devices.

MAX+PLUS II BASELINE and E+MAX software customers can download and license the world-class Synopsys FPGA *Express* software and/or Exemplar Logic LeonardoSpectrum-Altera software from the Altera web site (**http://www.altera.com**) to support HDL synthesis.

MAX+PLUS II BASELINE

The MAX+PLUS II BASELINE software features a seamless development flow that allows designers to enter, compile, and perform timing analysis on designs and program a wide range of Altera PLDs—including the new ACEX 1K family and FLEX 6000, MAX 7000, and MAX 3000 devices. The MAX+PLUS II BASELINE software download file is 45,822,459 bytes.

E+MAX

The E+MAX software is a subset of the MAX+PLUS II BASELINE software targeted at the industry's most popular product-term architectures—the MAX 7000 and MAX 3000 devices. The E+MAX software no longer includes Altera's native VHDL and Verilog HDL synthesis, as it provides access to world-class synthesis tools from Exemplar Logic and Synopsys on the Altera web site (**http://www.altera.com**). The E+MAX software download file is 20,025,630 bytes.

ASAP2

The ASAP2 software is a subset of the MAX+PLUS II software that only supports device programming. The ASAP2 software download file is 13,907,408 bytes.

Download files are now available from the Altera web site at **http://www.altera.com**.

Download the Latest OEM Synthesis & Simulation Tools

All customers with an active subscription can download the latest versions of the OEM synthesis and simulation tools Altera includes with software subscriptions. These tools can be downloaded from the Altera web site at **http://www.altera.com**. The new versions include support for the latest APEX 20KE, ACEX 1K, and MAX 7000B devices and include enhancements to improve design flows. The new LeonardoSpectrum-Altera and ModelSim-Altera also include support for the Microsoft Windows 2000 operating system. Table 10 shows the versions available.

Table 10. OEM Synthesis & Simulation Tools

Tool	Version	Availability
Synopsys FPGA *Express*	3.5	Now
Exemplar Logic LeonardoSpectrum-Altera	2000.1b	Now
Model Technology ModelSim-Altera	3.4c	Now

Design *Tips*

Designing Memory-Mapped Peripherals for the Nios Embedded Processor

The Nios™ embedded processor provides high levels of integration by allowing a microprocessor, memory, peripherals, and programmable logic to reside on the same device. The Excalibur™ Development Kit, featuring the Nios embedded processor, contains a number of peripherals, including a timer, a universal asynchronous receiver/transmitter (UART), and a parallel input/output (PIO). Other peripherals can be designed to interface with the Nios embedded processor using memory-mapped techniques. Memory-mapped peripherals provide a straightforward interface to the Nios embedded processor.

Memory-Mapped Peripherals

All peripherals that connect to the Nios embedded processor should be designed as memory-mapped I/O peripherals. Memory-mapped peripherals occupy a specific range in the address space of the Nios embedded processor. A memory-mapped peripheral is accessed by either reading or writing to addresses within the peripherals' address range.

The Nios embedded processor interfaces to memory-mapped peripherals by using the following signals:

```
clk
irq_from_the_peripheral
data_to_cpu_from_the_peripheral
address_to_the_peripheral
cpu_be_n_to_the_peripheral
cpu_read_n_to_the_peripheral
cpu_write_n_to_the_peripheral
data_from_cpu_to_the_peripheral
select_to_the_peripheral
```

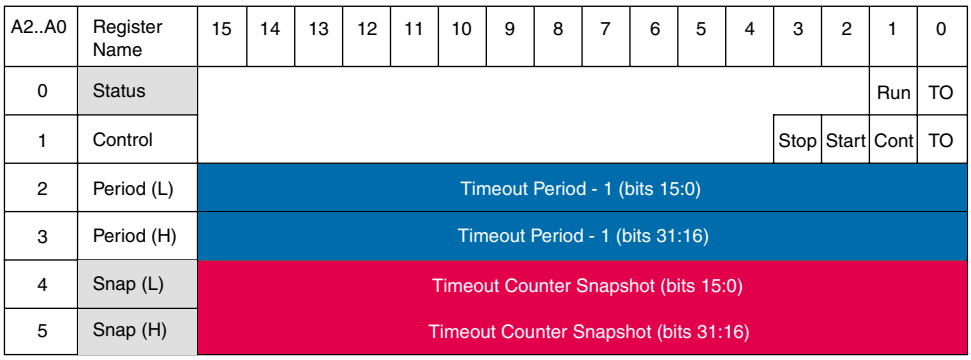
The Nios embedded processor supplies `write enable`, `read enable`, `byte enable`, `chip select`, `data`, and `address` lines to the peripheral. These signals are used to read or write from a register bank within the peripheral. The register map shown in Figure 1 on page 16 describes an example of the operation of each register within the register bank.

Figure 1 on page 16 illustrates the register map for the timer peripheral included in the Excalibur Development Kit.

continued on page 16

Designing Memory-Mapped Peripherals for the Nios Embedded Processor, continued from page 15

Figure 1. Timer Peripheral Register Map



The timer contains six registers in its register map. Registers in a memory-mapped peripheral can be read-only or read- and write-capable. The timer is controlled by writing to register `1`. Writing a `1` to bit `2` of register `1` starts the timer, and writing a `1` to bit `3` of register `1` stops the timer. Values can be pre-loaded into the timer by writing the upper half of the 32-bit word to register `3` and the lower half of the 32-bit word to register `2`.

Additional information on timer operation is available with the Excalibur Development Kit.

Creating a Custom Memory-Mapped Peripheral

Custom memory-mapped peripherals can be designed for the Nios embedded processor by following these three steps:

1. Determine the design requirements of the peripheral.
2. Create a peripheral register.
3. Code the peripheral using a hardware description language (HDL).

The following example demonstrates these three steps by creating a custom memory-mapped first-in first-out (FIFO) peripheral.

Determine the FIFO Peripheral Design Requirements

The FIFO in this example is designed to allow the Nios embedded processor to interface with a fast I/O source. The FIFO requires that the fast I/O source writes to the FIFO, and the Nios processor reads from the FIFO. The FIFO needs to assert an interrupt request signal whenever the FIFO is full. Therefore, the FIFO buffer would have the characteristics shown in Table 1.

Table 1. Example FIFO Buffer Characteristics

Description	Criteria
Width	32 bits
Depth	128 words
FIFO input signals	`clock`, `reset`, `write`, `read`, `data`
FIFO output signals	`data`, `empty_flag`, `full_flag`, `word_count`, `interrupt_request`

The I/O source will directly drive the data input port of the FIFO. The Nios embedded processor outputs `cpu_write_n_to_the_peripheral` and `cpu_be_n_to_the_peripheral` signals for each peripheral to which it interfaces. However, for the example in Table 1, the FIFO cannot be written by the Nios embedded processor (it can only be written by the I/O source), so the `cpu_be_n_to_the_peripheral` and

Figure 2. FIFO Peripheral Register Map

AO	Register Name	31	30	29..7	6	5	4	3	2	1	0
0	Read Data	Data to be read from the FIFO (bits 31:0)									
1	Status	Full	Empty		Usedw (bits 6:0)						

Read-only value
Host-written control value. Can be read back at any time

`cpu_write_n_to_the_peripheral` signals will not be used.

FIFO Peripheral Register Map

The layout of the FIFO's register map is determined by how many input and output signals are connected to it (see Figure 2). The FIFO has two control signal inputs (`write` and `read`) and one data input (`data`). The I/O source directly writes to the FIFO, so write registers are not required in the FIFO memory map. The register map consists of two readable registers: Read Data and Status. The Read Data register contains the 32-bit output of the FIFO, and the Status register indicates the current state of the FIFO. The full, empty, and word count (`usedw`) signals are placed in the same 32-bit register to conserve address space. However, if address space is not a consideration, each output signal can be placed in a separate register in the register map.

This FIFO peripheral can be implemented using the block diagram shown in Figure 3. The I/O source writes to the FIFO directly using the FIFO's `data`, `wrreq`, and `wrclock` signals. The FIFO will update the Read Data register by writing to Register 0 whenever the Nios embedded processor sets the `address_to_the_peripheral` signal to 0 and when it asserts the `select_to_the_peripheral` and the `cpu_read_n_to_the_peripheral`

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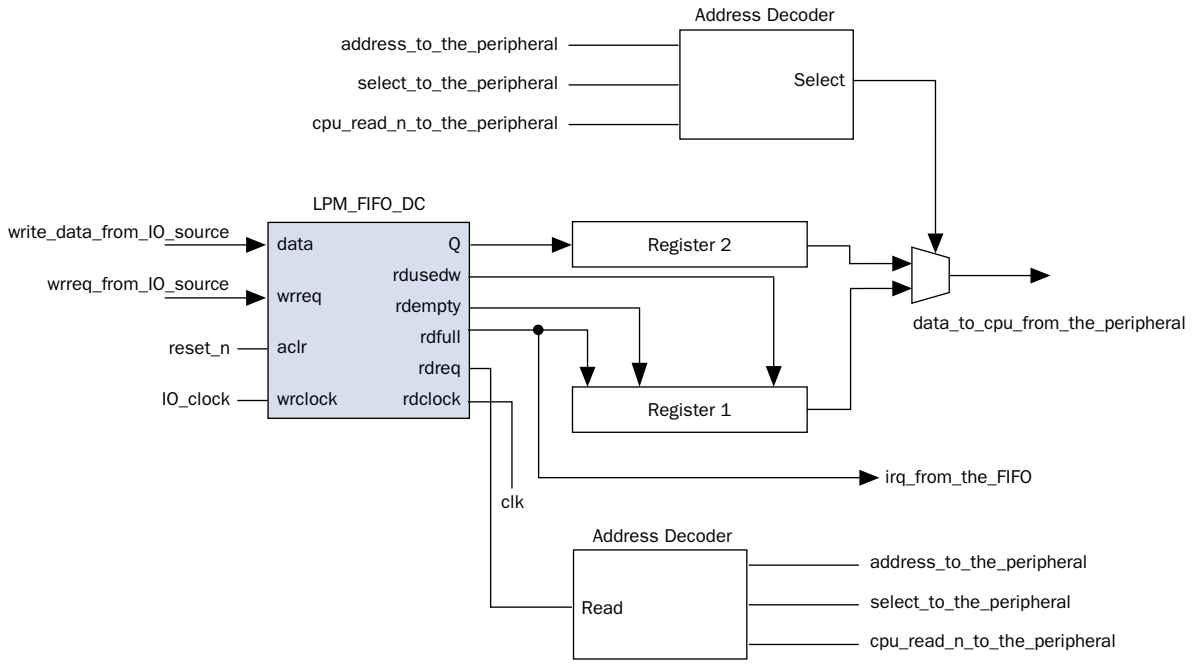
Figure 3. FIFO Peripheral Block Diagram



Designing Memory-Mapped Peripherals for the Nios Embedded Processor, continued from page 17

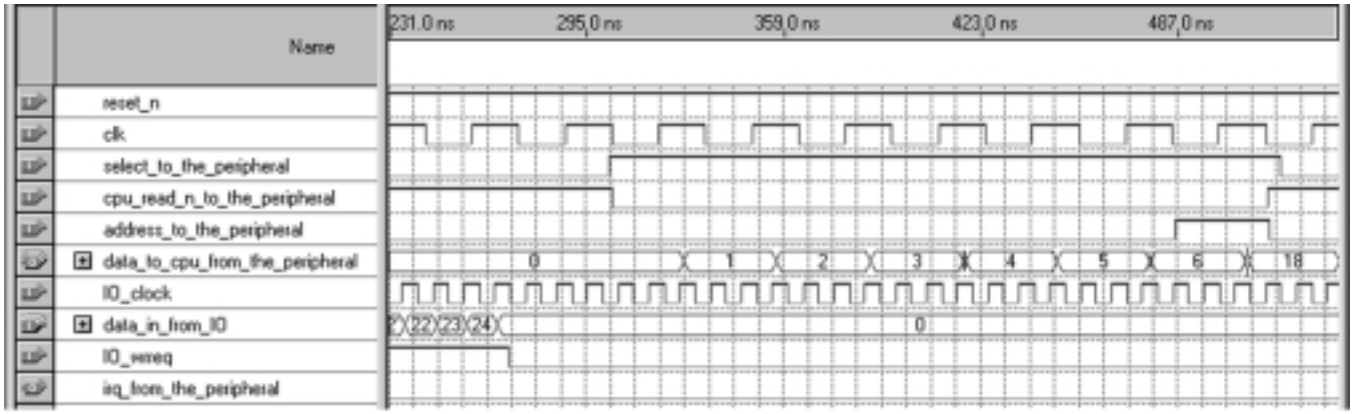
signals. The Status register (Register 1) is updated by the FIFO whenever reads or writes are performed. The contents of the Status register can be read by setting the `address_to_the_peripheral` signal to 1 and by asserting the `select_to_the_peripheral` and the `cpu_read_n_to_the_peripheral` signals.

Simulation Example

Figure 4 depicts a simulation example for the custom FIFO. The values 1 through 24 are written to the FIFO by asserting the `IO_wrreq` signal and applying the values 1 through 24 to the FIFO's `data_in_from_IO` bus. After 24 `IO_clock` cycles, the `IO_wrreq` line is deasserted. The Nios embedded processor begins reading from the FIFO by asserting the `select_to_the_peripheral` and `cpu_read_n_to_the_peripheral` lines at 300 ns. The address bus holds a value of 0 from 300 ns to 480 ns, which causes the FIFO to update the `data_to_cpu_from_peripheral` bus with the current output of the FIFO. These results are verified in the waveform because the `data_to_cpu_from_peripheral` bus outputs the values 1 through 6. The Status register is read at time 502 ns by setting the `address_to_the_peripheral` signal to 1 and by asserting the `select_to_the_peripheral` and `cpu_read_n_to_the_peripheral` signals. The Status register value is output to the `data_to_cpu_from_peripheral` bus at time 510 ns. The `data_to_cpu_from_peripheral` bus reads a value of 18 at time 510 ns, indicating that 18 words remain in the FIFO.

Memory-mapped peripherals create a simple interface between a peripheral and the Nios embedded processor. When using memory-mapping, the Nios embedded processor communicates to its peripherals by reading and writing to the system memory space. You can optimize the register map of a memory-mapped peripheral by designing it with a knowledge of which input and output signals of the Nios embedded processor are important for your application. The register map is central to creating an efficient interface between the Nios embedded processor and your peripheral. A design aim should be to create a small register map, as this will conserve address space and in some instances increase the maximum speed of the peripheral.

Figure 4. FIFO Peripheral Simulation Example



Customer Application

OMEGA-TECHNOLOGIES S.A.: APEX Device Doubles Processing Power in Signal Processing Application

Hybrid radio frequency (RF) simulation is now widely used for radar, electronic warfare (EW), or laboratory communication equipment tests. This laboratory-based simulation reproduces "real life" electromagnetic environments seen by receivers such as handsets or complex radar systems.

Because RF simulation involves the generation of millions of RF pulses and signals, it consumes much real-time computing power to control the synthesizers in charge of microwave generation. This real-time data processing was traditionally dedicated to digital signal processing (DSP) equipment, while high-level software ran on workstations or multiprocessor-networked PCs.

OMEGA-TECHNOLOGIES S.A., a subsidiary of Thomson-CSF in Massy Cedex, France, is now introducing its new CARIBOU real-time simulation engine, which replaces the 200-MHz TMS320C6201 device with a single Altera® APEX™ device. This APEX device offers a 100% increase in computing power.

A Typical DSP Job

In DSP-based simulations, the system architecture is based on a real-time unit (RTU) with a PCI interface plugged into a multiprocessor PC (Windows NT).

The first DSP-based RTU had a multiprocessor 320C40 board (see Figure 1), which evolved into a single 320C6 board.

Nevertheless, drawbacks of DSP sets the following system-wide limitations:

- High price of DSPs and associated circuits
- Need for a very detailed code optimization (assembly level) to get full performance of parallel computing (Software was written in C for portability, but optimization was difficult.)
- Speed limitation due to memory architecture

These drawbacks led to the natural conclusion that the next generation of systems would need a different approach.

Using an APEX Device: The CARIBOU Project

The first phase of replacing a DSP-based system is to transfer the C core algorithms for pulse processing into VHDL. Simulation in the Quartus™ software helps to define the new system architecture.

Implementing an APEX device increased the CARIBOU simulation engine's computing power by 100%.

During each 100-ms time slice, the CARIBOU architecture performs the following tasks:

- Downloads up to 800 Kbytes of raw data from the PCI interface to memory bank A or B
- Extracts from the other bank (A or B) up to 32 emitter parameters from the same amount of data
- Computes up to 50,000 pulse descriptors
- Generates up to 8 RF channel control words (amplitude or phase) for each descriptor
- Emits output data to a proprietary bus (32 bits wide)

The CARIBOU system is simple: one PCI main board with one APEX device, one PCI interface chip, and two SRAM banks on two daughter boards.

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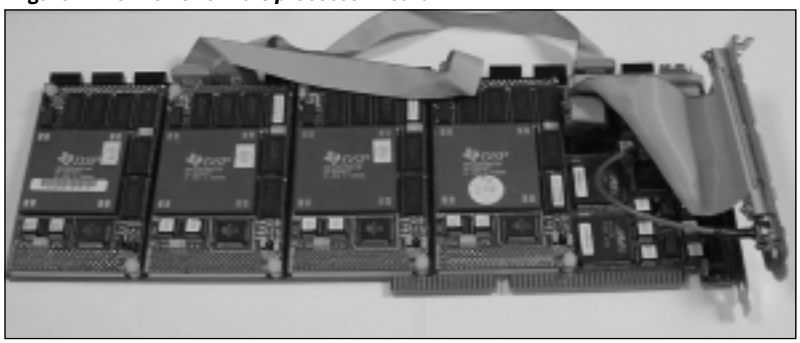
Figure 1. Former C40 Multiprocessor Board



OMEGA-TECHNOLOGIES S.A.: APEX Device Doubles Processing Power in Signal Processing Application, continued from page 19

Table 1 shows the CARIBOU system features. Figure 2 shows the CARIBOU printed circuit board (PCB).

Using VHDL core simulation in the Quartus software provides programming flexibility and simplifies system implementation.

Conclusion

Implementing the Altera APEX device not only allows OMEGA-TECHNOLOGIES S.A. to double the processing power of their new CARIBOU system, but it also reduces production costs by 40%.

Table 1. CARIBOU System

Feature	Description
APEX devices *(1)*	EP20K400E EP20K600E EP20K1000E
APEX device usage	< 25%
Clocks	32 & 64 MHz (PLL) *(2)*
SRAMs	8 Mbytes per bank
Memory	256 Mbytes
Power supplies	5 V @ 0.9 A 3.3 V @1.2 A

Notes:
(1) The basic CARIBOU system includes the EP20K400EFC672-1X device in the 672-pin ball-grid array (BGA) package.
(2) PLL: phase-locked loop.

Using VHDL core simulation provides programming flexibility, and system implementation is greatly simplified: no boot ROMs, no loader codes, and no power-greedy digital signal processors. The new CARIBOU system shows that using an APEX device for high-end signal processing is faster and much more flexible than classical DSP-based simulation.

About OMEGA-TECHNOLOGIES S.A.

OMEGA-TECHNOLOGIES S.A. is a wholly-owned subsidiary of THOMSON-CSF and is located in the high-tech area of Massy (20 km from Paris).

The Company is developing innovative products in the frequency synthesis field and is a major player in the EW simulator business.

Products range from microwave modules and digital synthesizers to radar and communications simulators, mainly in the DC to 26 GHz range.

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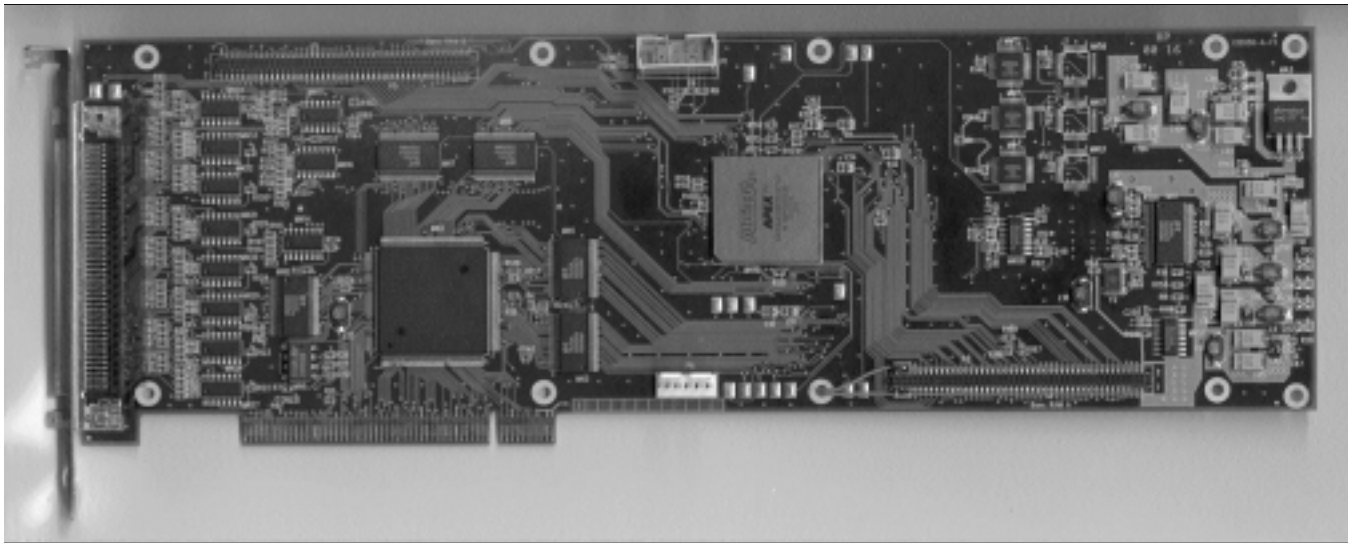
Figure 2. The CARIBOU System PCB



Contributed *Article*

Multi-Channel, Full-Duplex ADPCM Solutions from ISS for APEX, ACEX & FLEX Devices

Integrated Silicon Systems (ISS) recently extended its adaptive differential pulse code modulator (ADPCM) megafunction offering to include 32-, 64-, 128- and 256-channel full-duplex ADPCM codecs optimized for Altera's APEX™, ACEX™, and FLEX® programmable logic devices (PLDs). Typical implementation figures for these megafunctions are shown in Table 1. The megafunctions are fully supported by ISS and are also available for OpenCore™ evaluation. A bit-accurate C model, test bench, and documentation are included.

The extension of ISS's range of ADPCM megafunctions is a direct result of the exponential growth of voice traffic over voice and data networks and the need for the simultaneous compression/decompression of voice data at the network interface. The consequence of this growth from the system manufacturer's side is an explosion in the development of systems that can economically handle the increased capacity. PLDs are a cost-effective solution for these implementations in systems that used to be dominated by digital signal processing (DSP) processors.

ISS has used a number of selectable variables to implement the ADPCM megafunctions and provide customers with a range of solutions that can be matched to their specific needs. The megafunctions are used in applications such as voice-over-DSL, voice-over-ATM systems, and cordless telephony.

The megafunctions fully support the ADPCM standards G.726, G.726a, G.727, and G.727a and facilitate individual channel reset and control – a major requirement in most voice systems. In addition, the functions support burst mode operation. The megafunctions require 16 clock cycles per sample per direction (CSC4110AA, CSC4120AA, and CSC4125AA) or six clock cycles per sample per direction (CSC4130AA and CSC4190AA).

For more information on these megafunctions, contact ISS by visiting their web site at **http://www.issdsp.com.**

Altera PLDs are a cost-effective solution for implementations in systems that used to be dominated by DSP processors.

Table 1. Typical Implementation Figures for ADPCM Megafunctions

Product Code	Duplex Channels	Device	Minimum Required Clock Rate	Maximum Achieved Clock Rate	Pins	Logic Elements (LEs)	Memory Bits/ Embedded System Blocks (ESBs)
CSC4110AA	8	EP20K300EBC652-1	2.048	21.90	63	4,294	9,088/11
CSC4120AA	32	EP20K300EBC652-1	8.192	22.50	65	4,302	18,176/16
CSC4125AA	64	EP20K300EBC652-1	16.384	20.10	66	4,307	36,352/24
	64	EP1K100FC256-1	16.384	21.83	66	3,888	36,352/12
CSC4130AA	128	EP20K300EBC652-1	12.288	26.70	67	7,174	72,192/47
	128	EP20K200QC240-1	12.288	30.94	67	7,174	72,192/47
CSC4130AA	256	EP20K400EBC652-1	24.576	27.90	68	7,178	144,384/72
	256	EP20K300EBC652-1	24.576	30.20	68	7,178	144,384/72

Designing Switches & Routers with APEX CAM

Content-addressable memory (CAM) allows a design to search a table for a particular item. The data is supplied by the user or the system, and CAM uses the information provided to determine the location of the requested data.

CAM is especially useful in speeding up search operations in switches and routers. This article describes how APEX™ CAM can be used in specific applications such as:

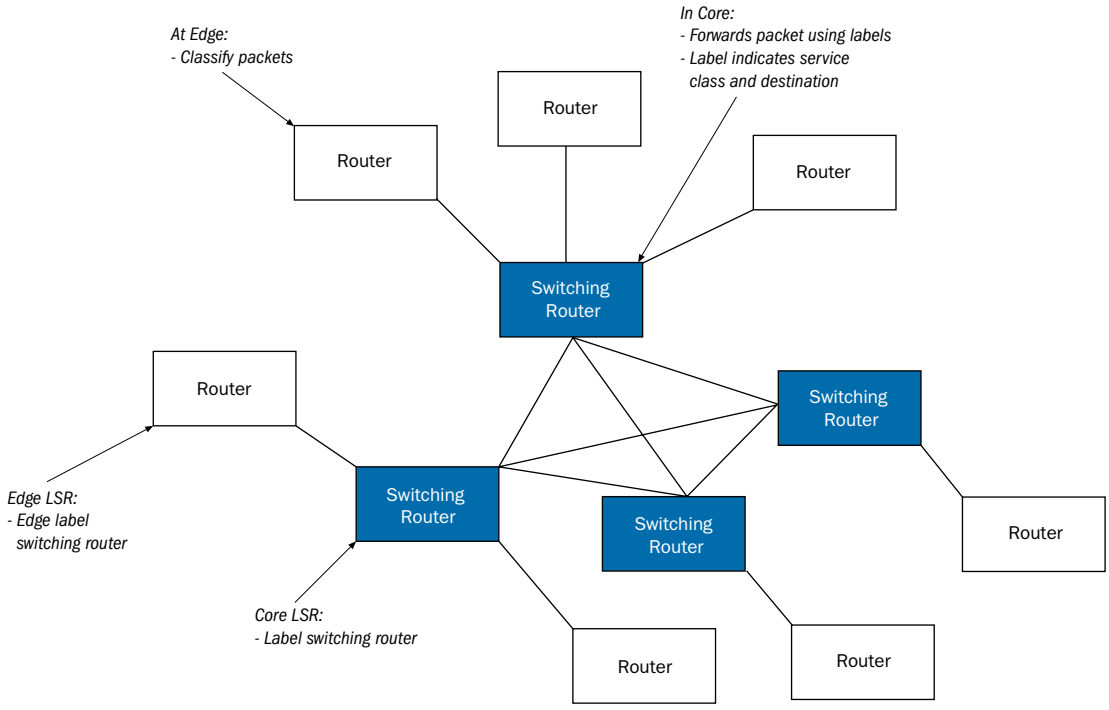
- Multi-protocol label switching (MPLS)
- Internet protocol address resolution

Multi-Protocol Label Switching

MPLS provides solutions that combine the control of Internet protocol routing with the simplicity of layer 1 switching. MPLS is a new technique in the evolution of routing/forwarding technology for the core of the Internet and supports the use of advanced routing services. This technique solves problematic issues such as quality of services and delivery of new routing capabilities. Figure 1 shows MPLS by indicating that routers on the edge or in the core of the network have separate functions.

A multi-protocol label switching system is composed of two functional components: control and forwarding. The control component uses standard routing protocol to exchange information and maintain a forwarding table with other routers along the network. When a router receives a packet, the forwarding component searches the forwarding table, which is maintained by the control component, to make a routing decision for each packet. The forwarding component is based on a label-swapping forwarding algorithm. Each control component is responsible for assigning and maintaining other relevant control information.

Figure 1. Multi-Protocol Label Switching Network *Note (1)*



Note:
(1) Routers using MPLS are highlighted in blue.

Because MPLS allows different modules to assign labels to packets, it decouples the forwarding of a packet from the contents of the packet's Internet protocol header.

At the ingress edges (entry) of the network, each incoming packet is classified and an initial label is assigned. The label switch performs a "longest-match routing" table look-up, assigns a label to the packet, then forwards it to the next hop on the label-switched path. In the core of the network, when a labeled packet arrives at a switch, the forwarding component uses the input port number and label to perform an exact match search of its forwarding table. If a match is found, the forwarding component retrieves the outgoing label, the outgoing interface and the next hop address from forwarding table. The forwarding component then replaces the incoming label with the outgoing label and directs the packet to the outbound interface for transmission to the next hop in the label-switched path. When the packet reaches the egress edge, the forwarding component searches its forwarding table. If the next hop is not a label switch, the egress switch discards the label and forwards the packet using conventional longest-match Internet protocol forwarding. Figure 2 shows the MPLS basic operation.

A CAM block can implement the required table and perform the fast search operation in the multi-protocol label switching operation. A CAM block finds the appropriate label for the incoming packet by searching the look-up table (LUT) in the ingress label switch. The label is used as an index into a table that specifies the next hop and the new label. The packet is forwarded to its next hop with the label attached. At the last edge of the network or egress label switch section, a CAM block can efficiently implement the table to remove the label from the incoming packet and forward the packet using Internet protocol forwarding.

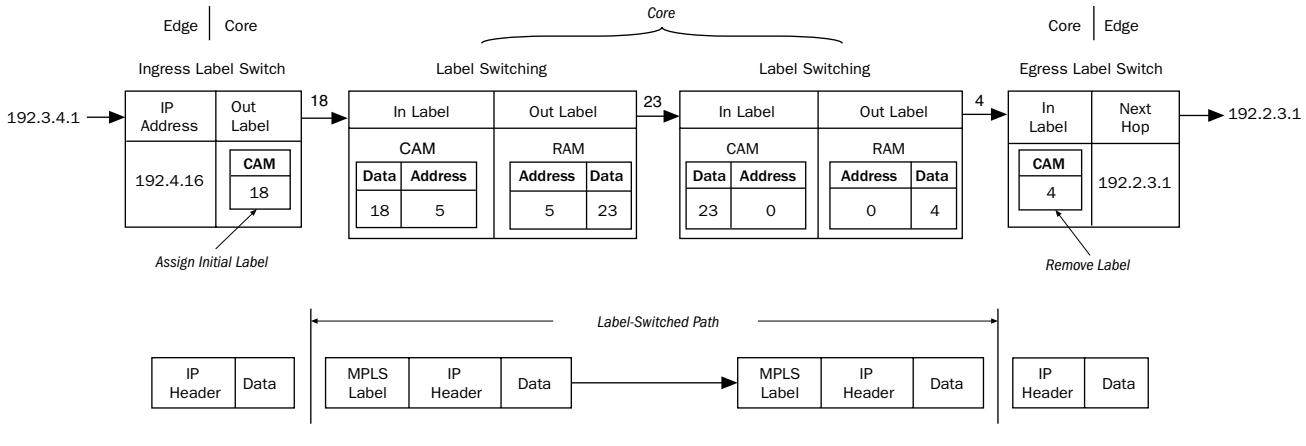
A combination of CAM and RAM can be used to implement the table, which routes the incoming labeled packet to its next hop and finds the new label. Typical MPLS switches store up to 1,024 labels at a time, therefore requiring a 1,024 × 32 CAM block. This CAM only takes 32 ESBs, so it can be implemented within APEX devices. Because the out-label is another label, a 1,024 × 32 bit RAM block that consumes 16 ESBs can assign the appropriate label to the incoming label. A total of 48 ESBs can perform the multi-protocol label switching operation (see Figure 2).

Internet Protocol Address Resolution

Internet protocol address resolution is used in layer 3 switches to convert Internet protocol addresses to Ethernet or media access control (MAC) addresses and vice versa. An Internet protocol address is a 32-bit value that identifies each sender or receiver of information that is sent in packets across the Internet. When a source attempts to send data over the Internet, the Internet protocol portion of the transmission control protocol/Internet protocol (TCP/IP) includes the source Internet protocol

continued on page 24

Figure 2. MPLS Basic Operation



Designing Switches & Routers with APEX CAM, continued from page 23

A combination of CAM and RAM can be used to maintain a correlation between each MAC address and its corresponding Internet protocol address.

address and the destination Internet protocol address in the packet. Once all the required information for delivery is included in the packet, the TCP/IP stack sends the entire packet across the Internet to the destination. The destination receives the data, and a response can be sent to the source by using the existing Internet protocol address.

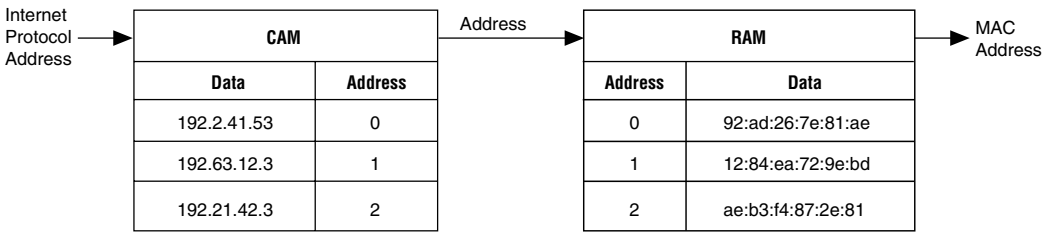
A MAC address, or Ethernet address, is the unique physical address designated to a hardware device (such as PC) when it is manufactured. When a computer is connected to a local area network (LAN), a correspondence table relates the Internet protocol address to the device's MAC address. A combination of CAM and RAM can be used to implement a table to maintain a correlation between each MAC address and its corresponding Internet protocol address and perform address conversion in both directions. CAM contains the Internet protocol addresses that point to corresponding locations in RAM, which contain the MAC or Ethernet address.

Address resolution protocol (ARP) is used to map an Internet protocol address to a recognized MAC address in the local network. When a host machine receives a packet, ARP runs a search to verify that the packet's destination address is on its particular network. The CAM and RAM combination, implemented in the ARP, compares the Internet protocol address against the content of the CAM table to find the appropriate MAC address in RAM. If CAM contains the Internet protocol address, the packet can be converted to the appropriate length and format, then sent to the destination device. If no match is found, ARP broadcasts a request packet to all the devices on the LAN in search of the corresponding address. If a device recognizes the Internet protocol addresses, it sends a message to the ARP claiming the Internet protocol address. ARP updates the contents of CAM and RAM for future reference and sends the packet to the destination machine. Figure 3 shows this Internet protocol address resolution process. This process can be implemented in software; however, implementing the search in hardware improves system performance.

Conclusion

Many networking applications require a fast search operation. APEX CAM can provide a solution for search operations in critical applications such as multi-protocol label switching, or Internet protocol address resolution. Using CAM simplifies and accelerates these functions and applications by increasing the performance of table look-up and translation implementation.

Figure 3. IP Address Resolution



LVDS Timing Analysis

The LVDS I/O standard allows data to be transmitted at very high speeds. This high data transmission rate results in better overall system performance. To take advantage of this high system performance, designers need to understand how to analyze timing for LVDS. LVDS timing analysis is different from traditional synchronous timing analysis techniques; rather than focusing on clock-to-output and setup times, LVDS timing analysis is based on the skew between the data and the clock signals.

To verify the overall timing budget, high-speed LVDS data transmission requires the use of LVDS timing parameters provided by Altera and other LVDS vendors. Designers must also consider board skew, cable skew, and clock jitter. By using LVDS designs, data can be transmitted at rates of up to 840 megabits per second (Mbps). This article defines LVDS timing parameters for APEX™ 20KE devices and explains how to use LVDS timing parameters to determine a design's maximum performance.

LVDS Timing Parameters

Typically, LVDS is used in a source synchronous implementation where the clock is forwarded along with the data from the transmitting device to the receiving device. Timing analysis of source synchronous LVDS involves verifying that there is sufficient receiver input skew margin (RSKM) after taking into account transmitter channel-to-channel skew (TCCS) and receiver sampling window (SW) requirements. Figure 1 shows the APEX 20KE LVDS timing diagram that defines the relationship of these LVDS timing parameters with respect to the internal clock period and the LVDS data bit positions. Table 1 defines the LVDS parameters.

Figure 1. LVDS Timing Diagram

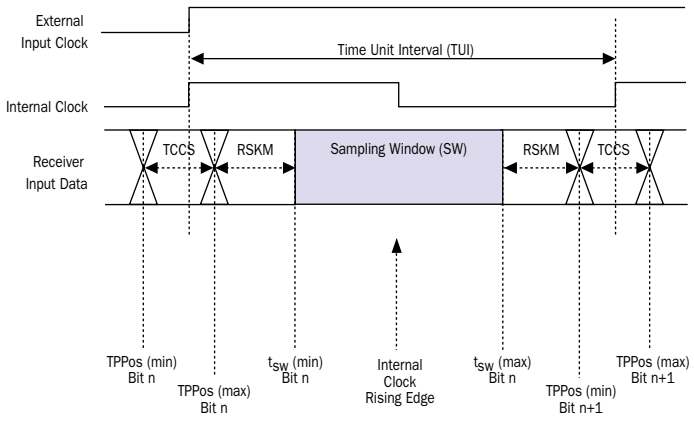


Table 1. LVDS Timing Parameters

Parameter	Description
t_C	LVDS receiver/transmitter input and output clock period
f_{INLVDS}	LVDS receiver/transmitter input and output clock frequency
t_{LHT}	Low-to-high transmission time
t_{HLT}	High-to-low transmission time
Time unit interval (TUI)	Timing budget allowed for transition times, skew, propagation delays, and data sampling window (TUI = 1/receiver input clock frequency_multiplication factor) = t_C/w
f_{LVDSDR}	Maximum LVDS data transfer rate (f_{LVDSDR} = 1/TUI)
Channel-to-channel skew (TCCS)	Timing difference between the fastest and slowest output edges of the LVDS transmitter clock and data, including t_{CO} variation and clock skew
Receiver input skew margin (RSKM)	Timing margin between clock input and data input for user board design, which allows for LVDS interconnect (cable and connector) skew and jitter on the LVDS PLL (RSKM = (TUI – TCCS – SW)/2)
Sampling window (SW)	Defines the period of time during which the data must be valid in order to be correctly captured (SW = t_{SW} (max) – t_{SW} (min))
Input jitter (peak-to-peak)	Tolerable input jitter on LVDS PLLs
Output jitter (RMS)	RMS output jitter on LVDS PLLs
t_{DUTY}	Duty cycle on LVDS transmitter output clock
t_{LOCK}	Lock time for LVDS transmitter and receiver PLLs

continued on page 26

LVDS Timing Analysis, continued from page 25

The RSKM parameter must be large enough to allow for clock jitter and cable and board skew. To meet a system's requirements, designers must consider the jitter and the system skew that both affect the RSKM by evaluating the application's margin. This equation is shown below:

Margin = RSKM – (input clock jitter + system skew)

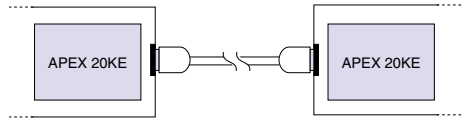
System skew is the difference in propagation delays of signals between devices and includes skew introduced from cables, connectors, and differences in signal lengths on printed circuit circuit board (PCB) traces. The input clock jitter is the allowed jitter on the input clock that will be received by the APEX 20KE LVDS receiver PLL.

APEX 20KE LVDS circuitry provides low TCCS and SW parameters that allow high-speed LVDS data transfers.

Design Example

This section describes an LVDS design example using an APEX 20KE-to-APEX 20KE connection and a data transfer rate of 624 Mbps over a 5-m cable. This design uses a cable (14526-EZ5B) and connector (10226-1A10VE) from 3M Company. Figure 2 shows a design example of APEX 20KE-to-APEX 20KE connection with a 3M Company cable assembly.

Figure 2. LVDS Design Example



The design in Figure 2 has the following characteristics:

- SW = 0.44 ns, TCCS = 0.4 ns
- RSKM = (TUI – SW – TCCS) / 2 = (1.6 – 0.44 – 0.4) / 2 = 380 ps
- Cable skew per meter (max) = 50 ps, Connector skew (max) = 17 ps (Values obtained from 3M Company)
- Because the LVDS balls are located on the outer edge of the FineLine BGA™ packages, the traces can be easily routed with little skew.
- PCB skew = 30 ps (based on the electrical length of the PCB traces)
- System skew = cable skew + connector skew + PCB skew = 297 ps
- Margin = RSKM – (input clock jitter + system skew) = 380 ps – (10 ps + 297 ps) = 63 ps

Because the margin is positive, the circuit will operate at the required speed. If a longer cable is desired, the margin may not be sufficient. In this case, the APEX 20KE deskew circuit can be used to increase RSKM and assure circuit functionality.

Preliminary test data shows that EP20K400E and EP20K600E devices can transmit data at 840 Mbps over 10 m of twisted pair (CAT5) cable under nominal conditions.

When designing for high-speed data transfer rates, designers must consider various factors that affect the margin for correct data sampling. By completing the calculations described in this section, designers can calculate the margin in LVDS designs that use APEX 20KE devices and calculate LVDS transfer speed over cables and connectors. Low skew cables and connectors can also improve margin and overall system performance. The APEX 20KE LVDS circuitry provides low TCCS and SW parameters that allow high-speed LVDS data transfers.

The APEX 20KE devices are timing and electrically compatible with source synchronous LVDS buffers offered by National Semiconductor, Texas Instruments, and other devices that comply to the EIA/TIA-644 LVDS standard.

Conclusion

When designing for high-speed data transfer rates, designers must consider various factors that affect the margin or correct data sampling. By completing the calculations described in this article, designers can calculate the margin in LVDS designs that use APEX 20KE devices and calculate LVDS transfer speed over cables and connectors. Low skew cables and connectors can improve margin and overall system performance. The APEX 20KE LVDS circuit provides low TCCS and SW parameters that allows high-speed LVDS data transfers.

MAX 7000B: I/O Standards for High-Speed Applications

System demands for increasing clock speeds and low voltage levels are driving the adoption of high-performance, low-voltage I/O standards to support faster microprocessors and high-speed memory. Product-term-based MAX® 7000B devices are increasingly found in many of these applications, where they are utilized in a variety of glue logic and control logic circuitry.

Today's product-term-based devices must support not only a variety of advanced I/O standards but also must support multiple standards within a single device. Such flexibility allows I/O pins to be configured for both LVCMOS and SSTL-2. MAX 7000B devices meet these advanced I/O support needs.

The flexible I/O buffers within MAX 7000B devices are designed to meet the voltage, drive strength, and AC characteristics necessary to comply with advanced I/O standards such as GTL+and SSTL. By implementing these I/O standards, MAX 7000B devices also help save board space and increase chip-to-chip performance by eliminating external buffers, drivers, and transceivers.

GTL+ I/O Standard

The GTL+ I/O standard characteristics (i.e., reduced I/O swing level, low output capacitance, low output generated noise, and high noise immunity) make it a dominant I/O standard for high-performance system backplanes and motherboards. The GTL+ bus is also used in high-end computer servers and laptops. For example, the Intel Pentium II and Pentium III processors interface with their core logic using the GTL+ I/O standard.

A GTL+ bus can also be found in the backplanes of many communication applications such as ATM switches, Layer 3 switches, and other high-speed routers. In these data communication applications, the system board typically communicates with other modules via a GTL+-based backplane bus.

In most cases today, I/O buffers or transceiver chips are used to convert GTL+ signals to LVCMOS/LVTTL before performing control/decode logic. MAX 7000B devices eliminate the need for such I/O standard translation, saving board space, reducing costs, and contributing to the overall system throughput. It's unique support of this popular I/O standard makes the MAX 7000B device the only product-term-based solution for these applications.

SSTL-2 & SSTL-3 I/O Standard

MAX 7000B devices also support both the SSTL-2 and SSTL-3, Class I and Class II, I/O standard. The primary application of SSTL is interfacing with SDRAMs. SSTL is used for high-speed memory interface applications, specifying switching characteristics that reach operating frequencies up to 200 MHz. 2.5-V systems use SSTL-2, and 3.3-V systems use SSTL-3. Computer servers and even high-end laptop computers use SDRAMs and DDR SDRAMs. SSTL is the interface standard of choice for these high-speed memory modules.

High-speed SDRAMs are also used in a variety of networking applications such as ATM LAN switches, Internet protocol routers and switches, and frame buffer interfaces. SSTL interfacing is widely used in these applications.

Support for advanced I/O standards, coupled with the split I/O bank architecture, gives you added flexibility and allows MAX 7000B devices to meet virtually all your I/O interfacing requirements.

The MAX 7000B device family is the product-term leader for I/O standard support, enabling high-speed design applications such as processor interfaces, backplane drivers, peripheral devices, and SDRAM memory interfaces.

Support for advanced I/O standards, coupled with the split I/O bank architecture, allows MAX 7000B devices to meet virtually all your I/O interfacing requirements.

MAX 7000B Devices Outperform the Competition

Altera® MAX® 7000B devices are the industry's fastest product-term-based device. Ranging from 32 to 512 macrocells, MAX 7000B devices offer propagation delays as fast as 3.5 ns and counter frequencies over 200 MHz. In addition, MAX 7000B devices support today's advanced I/O standards, providing simple integration into high-speed design applications.

Advanced Process Technology

Behind the MAX 7000B device's impressive performance is its advanced process technology. Fabricated on a 2.5-V, 0.22-µm CMOS technology, MAX 7000B devices are the industry's most advanced product-term-based device to date.

Table 1. Typical Propagation Delays of Available 2.5-V Devices

Macrocell Range	Pin-to-Pin Propagation Delays (ns)		
	MAX 7000B	XC9500XV *(1)*	ispLSI2000VL
32 to 36	3.5	10.0	5.0
64 to 72	3.5	10.0	5.5
128 to 144	4.0	10.0	6.0
192 to 288	5.0	15.0	6.0
512 and higher	6.0	–	–

Note:
(1) This is the fastest available device through distribution as of December 2000.

Table 2. Advanced I/O Standards Support

I/O Standard	MAX 7000B	XC9500XV	ispLSI2000VL
GTL+	✓		
SSTL-2 class I and II	✓		
SSTL-3 class I and II	✓		
LVTTL	✓	✓	✓
LVCMOS	✓	✓	✓
2.5 V	✓	✓	✓
1.8 V	✓	✓	
64-bit, 66-MHz PCI	✓		

The Industry's Fastest Product-Term Device

The fast pin-to-pin propagation delays of MAX 7000B devices maintain Altera's performance leadership in the marketplace. As Table 1 shows, MAX 7000B devices outperform the competition's fastest available devices.

Advanced I/O Standards Support

Altera MAX 7000B devices also lead the competition in advanced I/O standards support. As shown in Table 2, MAX 7000B devices are the only product-term-based device capable of supporting GTL+, SSTL-3, and SSTL-2 I/O standards.

Support for advanced I/O standards allow designers to use MAX 7000B devices in high-speed design applications such as processor interfaces, backplane drivers, and SDRAM memory interfaces.

MAX 7000B devices are available today and ready to meet your performance needs. Fabricated on a 0.22-µm CMOS process and with support for today's advanced I/O standards, the high-performance MAX 7000B solution is unmatched in the industry.

MAX EPM7128 Celebrates 50 Million Units

Driven by the Internet revolution, Altera has sold 50 million units of its industry-leading MAX® EPM7128 device. Marking this historic programmable logic device (PLD) milestone, Altera delivered a symbolic 50 millionth device to Cisco Systems, one of its leading network customers. From the earliest Ethernet switches to the most popular Internet routers and next-generation optical networking systems, almost 70% of EPM7128 devices shipped have been designed into communications systems.

The MAX EPM7128 architecture, which includes EPM7128, EPM7128A, EPM7128AE, EPM7128S, and EPM7128B devices, has held wide popularity since its release in 1991. Popular in DSL, VOIP, 3G Wireless, high-speed routers, and mass storage applications, MAX 7000A devices represent the fastest-growing product term architecture within the various MAX 7000 product generations.

Altera plans to maintain and extend this product-term market leadership by investing heavily in the development of new MAX products as well as by expanding current customer support efforts for MAX devices. Recently released MAX 7000B devices illustrate this commitment in that MAX 7000B devices are the only 2.5-V, ISP-based devices currently available.

For more information on MAX devices, visit the Altera web site (**http://www.altera.com**) or contact your local sales representative.

Questions & Answers

Q *What are the effects of slew rate control for MAX® 7000B devices?*

A MAX 7000B devices offer a slow slew rate feature that allows you to select either normal slew rate for fastest performance or slow slew rate to reduce board-level signal integrity issues.

A signal's output slew rate varies significantly based on load conditions. Altera's input/output buffer information specification (IBIS) models model the effect of turning the slow slew rate option on and off to determine how the board's transmission line effects require slowing the slew rate.

Table 1 shows slew rates measured for both rising and falling edges under the following conditions:

- From 10% to 90% of the output voltage swing
- Under a 35-pF unterminated load
- V_{CCIO} at 2.5 V
- Room temperature
- Nominal V_{CC}

Table 1. MAX 7000B Slew Rates

VCCIO (V)	Normal Slew Rate (V/ns)	Slow Slew Rate (V/ns)
3.3	1.3	0.7
2.5	1.0	0.5
1.8	0.7	0.4

continued on page 30

Questions & Answers, continued from page 29

The Slow Slew Rate logic synthesis option can be turned on and off globally in the MAX+PLUS® II software using the following steps:

1. Choose Global Project Logic Synthesis (**Assign menu**).
2. **Select** Define Synthesis Style (Global Project Logic Synthesis box).
3. Turn Slow Slew Rate on or off.
4. **Choose** OK twice.

Q *Error: "Unknown problem in <design>.vhd (DLS-E-IllNodeRef, Consumers of Channel node (number 130) in unit DLS_MAXPLUS_PROJECT:EXAMPLE3-RTL. SynthesisView refers to unattached BitWrite node; in CheckAttachNode.)"*

A This VHDL code error occurs in the MAX+PLUS II software when If Statements are nested within a For Loop. The following example demonstrates the syntax that causes the error:

```
FOR i IN 0 to 11 LOOP
      IF (a(i) = '1') THEN
      IF (b(i) = '0') THEN
      IF  c(i) <=  d(i);
      ELSE
          c(i) <= NOT d(i);
    END IF;
    ELSE
        c(i) <= 'Z';
    END IF;
END LOOP;
```

The following example demonstrates how to compensate for this error by modifying the If Statement so that it is not nested:

```
FOR i IN 0 TO 11 LOOP
      IF (a(i) = '1' AND b(i) = '0') THEN
      c(i) <=  d(i);
      ELSIF (a(i) = '1' AND b(i) = '1') THEN
    ELSE
      c(i) <= 'Z';
      END IF;
END LOOP;
```

Q *Why do I get a "Failed to find INSTANCE '/instance_name'" error when performing a timing simulation in the ModelSim simulator?*

A This error will only occur if you have modified the VHDL Output File (**.vho**) or Verilog Output File (**.vo**) by removing the reference to the Standard Delay Format Output File (**.sdo**).

Model*Sim* will flag this error when the SDO is applied to the wrong instance. By default, the SDO File is referenced in the Quartus™- or MAX+PLUS II-generated VO or VHO Files.

When you use a test bench to simulate a VHO or VO File generated by the Quartus or MAX+PLUS II software, the SDO File must be applied to the entity in the VHO or the VO File and not the top-level test bench entity.

To apply the SDO File to the correct instance, follow the steps below:

1. Open the **Load Design** dialog box in ModelSim.
2. Click on the **SDF** tab and then click on the **Add** button.
3. Browse and choose the **SDO** file.
4. In the **Apply to Region** box, type the path of the instance to which the SDO file should be applied.
5. Click **OK**.

Q *Library error: "primary unit <text> denoted by prefix <text> must exist in the library."*

A MAX+PLUS II Help lists the most common cause for this error. However, this error can also be generated if your VHDL design files are appended with **.vhdl** rather than **.vhd**. As a workaround, rename your VHDL files with a **.vhd** extension.

Q *Can I connect a tri-state signal connected to the input pins of an Altera® device?*

A A tri-state signal connected to the inputs will not cause any damage to the device.

However, when the tri-state signal drives a high impedance, the input to the pin is unpredictable and your logic may not produce the desired outputs. Tri-stated inputs cause the device to draw more current than it would if the signal were pulled to a logic level high or low. To prevent this from happening, use pull-up or pull-down resistors on these signals. Another option is to use the bus-hold feature of the MAX 7000B device

Q *How do I assign a register to an I/O cell location in the Quartus software version 2000.09?*

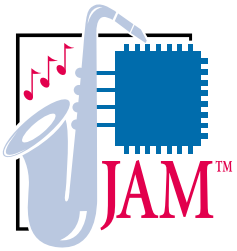
A There are three ways to assign a register to an I/O cell in the Quartus software version 2000.09:

- Apply the **Fast Input Register** or **Fast Output Register** assignment to the pins or registers directly.
- Use the **Optimize for I/O Timing** assignment with a 50 ns or less t_{SU} or t_{CO} assignment on a pin or register.
- Map to I/O ATOMs in your EDA synthesis tool

Q *Can I use Jam Standard Test and Programming Language (STAPL) or the Jam™ Byte-Code Player to configure ACEX™ or FLEX® devices?*

A Yes. You can use the Jam STAPL or Jam Byte-Code player to configure ACEX and FLEX 10K devices. Use the following steps to configure an ACEX or FLEX 10K device with Jam STAPL or the Jam Byte-Code Player:

1. Download the Jam Byte-Code Player from the Jam web site at **http://www.jamisp.com**. The download contains the **jbi.exe** Jam Byte-Code player executable.
2. Use the **Create Jam** or **SVF** option in the MAX+PLUS II software to create a Jam STAPL Byte-Code File (**.jbc**) for the JTAG chain.
3. Connect an Altera download cable to your PC's parallel port and the other end to the Joint Test Action Group (JTAG) chain on the printed circuit board (PCB). Power up the board.
4. Open a MSDOS or Command Prompt window. At the prompt, go to the directory that holds the **jbi.exe** and the JBC File created by the MAX+PLUS II software.
5. At the prompt, type the following command if the JBC File is in Jam STAPL format:
   `jbi -aconfigure <filename>.jbc`



JBC Files are the binary counter part of Jam STAPL Files (**.jam**). Jam Files are in ASCII format. Since JBC Files are in binary, the file size is usually smaller. Altera recommends using JBC Files and the JBC Player. You can use Jam Files; however, they require the Jam Player (**jam.exe**), available for download on the Jam web site **http://www.jamisp.com.**

Q *How do I set up a fixed-node MegaCore® license with my Quartus or MAX+PLUS II floating license?*

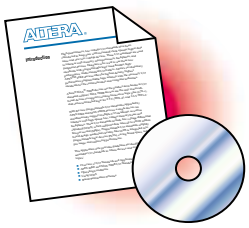
A Fixed-node and floating licenses can be used simultaneously in the **License Setup** window of the Quartus or MAX+PLUS II software. For example, if you have a fixed-node license stored at **c:\license.dat** and a floating license at **port@host** (e.g., 1800@arnold), you could enable the licenses as follows:

1. Select **Licensing** (Tools menu -> Options) in the Quartus software.
   or
   Select **License Setup** (Options menu) in the MAX+PLUS II software.
2. In the **License File** dialog box, type: c:\license.dat; 1800@arnold
3. Select **OK**.

Q *Can I use different I/O standards on the CLK and CLKLK_FBIN pins in APEX™ 20KE devices?*

A No, the `CLK` and `CLKLK_FBIN` pins must have the same I/O standard. The phase-locked loop (PLL) cannot accurately phase-match these pins in external feedback mode if they have different standards. The phase-locked loops (PLL) cannot accurately phase-match these pins in external feedback mode if they have different standards. The Quartus software will give an error if these pins are assigned different I/O standards.

New Altera Publications



New publications are available from Altera Literature Services at **lit_req@altera.com** or (888)-3-Altera. When ordering, please specify the part number shown in parentheses. On-line documents are available on the Altera web site at **http://www.altera.com**.

- Altera Digital Library CD-Rom, Version 6 (P-CD-ADL2000-06)
- *APEX Devices Brochure* (M-GB-APEX-20K-04)
- *Simulating the a8259 Model with the Visual IP Software User Guide* (A-UG-A8259VIS-01)
- *APEX 20KC Programmable Logic Devices Advance Information Brief (A-AIB-APEX20KC-01)*
- *SB 42: Interleaver/Deinterleaver MegaCore Function* (A-SB-042-01)
- *SB 48: Reed-Solomon Compiler MegaCore Function* (A-SB-048-01)
- *SB 49: NCO Compiler MegaCore Function* (A-SB-049-01)
- *SB 50: Turbo Encoder/Decoder MegaCore Function* (A-SB-050-01)
- *Board Design Guidelines for LVDS Systems White Paper (M-WP-DESLVDS-01)*
- *Designing Switches and Routers with APEX CAM White Paper (M-WP-APEXCAM-01)*
- *Configuring PLDs with Flash Memory White Paper* (M-WP-M3KPLD-01)

Current Software Versions

The Quartus™ software version 2000.09 is the latest release, and is available for the following operating systems:

- Microsoft Windows 2000
- Microsoft Windows 98
- Microsoft Windows NT version 4.0 and higher
- Sun Solaris version 2.6 and 2.7
- HP-UX version 10.2*x* and 11.0

The MAX+PLUS® II software version 10.0 is available for the following operating systems:

- Microsoft Windows 2000
- Microsoft Windows 95 and Windows 98
- Microsoft Windows NT version 4.0 and higher
- Sun Solaris version 2.5 and 2.6
- HP-UX version 10.2*x*
- AIX version 4.1 and higher

Altera Programming Support

Programming Hardware Support

Table 1 contains the latest programming hardware information for Altera® MAX® 9000, MAX 7000, MAX 3000, and configuration devices. For correct programming, use the software version shown in "Current Software Versions" on page 32.

Table 1. Altera Programming Adapters (Part 1 of 3) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)* EPC1064V *(2)* EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)* EPC1213 *(2)*	DIP, J-lead	PLMJ1213
EPC2 *(4)*	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(5)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(5)* PLMR9000-240NC *(5)*
EPM7032	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032B	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

Table 1. Altera Programming Adapters (Part 2 of 3) *Note (1)*

Device	Package	Adapter
EPM7064S	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(5)*
EPM7064AE EPM7064B	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin) FineLine BGA (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC *(5)* PLMF7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A EPM7128AE EPM7128B EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) TQFP (144-pin) PQFP (160-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMQ7128/7160-160NC *(5)* PLMF7000-100 PLMF7000-256
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMQ7128/7160-160NC *(5)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC *(5)*

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Altera Programming Support, continued from page 33

Table 1. Altera Programming Adapters (Part 3 of 3) *Note (1)*

Device	Package	Adapter
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A EPM7256S EPM7256AE EPM7256B	TQFP (100-pin) TQFP (144-pin) PQFP (208-pin) RQFP (208-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMT7256-208NC *(5)* PLMF7000-100 PLMF7000-256
EPM7512AE EPM7512B	TQFP (144-pin) PQFP (208-pin) BGA (256-pin) FineLine BGA (256-pin)	PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMB7000-256 PLMF7000-256
EPM3032A	J-lead (44-pin) TQFP (44-pin)	PLMJ3000-44 PLMT3000-44
EPM3064A	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ3000-44 PLMT3000-44 PLMT3000-100NC *(5)*
EPM3128A	TQFP (100-pin) TQFP (144-pin)	PLMT3000-100NC *(5)* PLMT3000-144NC *(5)*
EPM3256A	TQFP (144-pin) PQFP (208-pin)	PLMT3000-144NC *(5)* PLMR3256-208NC *(5)*

Notes:
(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on Classic™ devices.
(2) FLEX® 8000 configuration device.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(4) APEX™ 20K, FLEX 10K, or FLEX 6000 configuration device.
(5) These devices are not shipped in carriers.

Third-Party Programming Support

Data I/O, BP Microsystems, and System General provide programming hardware support for selected Altera devices. Algorithms are available on these companies' respective web sites (**http://www.data-io.com**, **http://www.bpmicro.com**, and **http://www.sg.com.tw**). Programming support information for configuration, MAX 9000, and MAX 7000 devices is shown in Table 2. All information is subject to change.

Table 2. Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*	System General *(3)*
EPC1064	✓	✓	✓
EPC1213	✓	✓	✓
EPC1	✓	✓	✓
EPC1441	✓	✓	✓
EPC2	✓	✓	✓
EPM3032A	✓	✓	✓
EPM3064A	✓	✓	✓
EPM3128A	✓	✓	✓
EPM3256A	*(4)*	✓	✓
EPM7032	✓	✓	✓
EPM7032AE	✓	✓	✓
EPM7032B	*(4)*	*(4)*	*(4)*
EPM7032S	✓	✓	✓
EPM7064	✓	✓	✓
EPM7064AE	✓	✓	✓
EPM7064B	*(4)*	*(4)*	*(4)*
EPM7064S	✓	✓	✓
EPM7096	✓	✓	✓
EPM7128A	✓	✓	✓
EPM7128S	✓	✓	✓
EPM7128AE	✓	✓	✓
EPM7128B	*(4)*	*(4)*	*(4)*
EPM7128E	✓	✓	✓
EPM7160E	✓	✓	✓
EPM7192S	✓	✓	✓
EPM7192E	✓	✓	✓
EPM7256A	*(4)*	✓	✓
EPM7256AE	*(4)*	*(4)*	✓
EPM7256B	*(4)*	*(4)*	*(4)*
EPM7256S	✓	✓	✓
EPM7256E	✓	✓	✓
EPM7512AE	✓	✓	✓
EPM7512B	*(4)*	*(4)*	*(4)*
EPM9320	✓	✓	✓
EPM9320A	✓	✓	✓
EPM9400	✓	✓	✓
EPM9480	✓	✓	✓
EPM9560	✓	✓	✓
EPM9560A	✓	✓	✓

Notes to Table 2:
(1) These devices are supported by the Data I/O UniSite programmer version 6.4.
(2) These devices are supported by BP Microsystems programmers version 3.51A.
(3) These devices are supported by System General programmers version 1.0.
(4) Contact Data I/O, BP Microsystems, or System General about programming support for these devices.

Download Cables

Table 3 provides programming and configuration compatibility information for the MasterBlaster™ serial or universal serial bus (USB) communications cable and the BitBlaster™ serial and ByteBlasterMV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable.)

Table 3. Download Cable Compatibility

Device	MasterBlaster *(1)*	ByteBlasterMV	BitBlaster *(2)*
APEX 20K	✓	✓ *(3)*	
APEX 20KE	✓	✓ *(3)*	
ACEX 1K	✓	✓	✓
FLEX 10K	✓	✓	✓
FLEX 10KA	✓	✓	✓
FLEX 10KE	✓	✓	✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A	✓	✓	✓
MAX 7000B	✓	✓ *(3)*	
MAX 3000A	✓	✓	✓

Notes:
(1) The MasterBlaster communications cable can be used with the Quartus software for device download and SignalTap logic analysis. It can also be used with the MAX+PLUS II software version 9.3 and later for device downloads.
(2) The BitBlaster download cable must operate at 5.0 V.
(3) The ByteBlasterMV download cable must operate at 3.3 V for these devices, except for 5.0-V tolerant APEX 20K devices with a "V" ordering code suffix. VCCIO pins can be set to either 2.5 V or 3.3 V.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera.

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	General Literature Request *(2)*	**lit_req@altera.com**	**lit_req@altera.com**
	News & Views Subscriptions	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**	**http://www.altera.com/html/forms/nview.html** **n_v@altera.com**
	News & Views Address Changes	**n_v@altera.com**	**n_v@altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline	(800) 800-EPLD (6 a.m. to 6 p.m. Pacific Time) (408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time)	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time) *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**support@altera.com**	**support@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**

Notes:
(1) The ***Quartus Installation and Licensing*** and ***MAX+PLUS II Getting Started*** manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

Altera Device Selection Guide

Current information for the Altera® Excalibur™, APEX™ 20K, ACEX™ 1K, FLEX® 10K, FLEX 6000, MAX® 9000, MAX 7000, MAX 3000, and configuration devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide*. For the most up-to-date information, go to the Altera web site at **http://www.altera.com**. Some of the devices listed may not yet be available. Contact Altera or your local sales office for the latest device availability.

Excalibur Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	EMBEDDED PROCESSOR
EPXA1	100,000	484-Pin BGA[2], 672-Pin BGA[2], 612-Pin BGA	173, 178, 178	1-8 V	4,160	53,248	ARM922T 32-bit
EPXM1	100,000	484-Pin BGA[2], 672-Pin BGA[2], 612-Pin BGA	173, 178, 178	1-8 V	4,160	53,248	MIPS32 4Kc
EPXA4	400,000	672-Pin BGA[2], 1020-Pin BGA[2], 612-Pin BGA, 864-Pin BGA	275, 360, 215, 360	1.8 V	16,640	212,992	ARM922T 32-bit
EPXM4	400,000	672-Pin BGA[2], 1020-Pin BGA[2], 612-Pin BGA, 864-Pin BGA	275, 360, 215, 360	1.8 V	16,640	212,992	MIPS32 4Kc
EPXA10	1,000,000	1020-Pin BGA[2], 864-Pin BGA	521, 365	1.8 V	38,400	327,680	ARM922T 32-bit
EPXM10	1,000,000	1020-Pin BGA[2], 864-Pin BGA	521, 365	1.8 V	38,400	327,680	MIPS32 4Kc

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[1]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS
EP20K30E	30,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 324-Pin BGA[2]	92, 93, 128, 128	1.8 V	1,200	24,576
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 93, 148, 151, 196, 196	1.8 V	2,560	32,768
EP20K100	100,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	101, 159, 189, 252, 252	2.5 V	4,160	53,248
EP20K100E	100,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 93, 151, 183, 246, 246	1.8 V	4,160	53,248
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	88, 143, 175, 271, 316	1.8 V	6,400	81,920
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2]	144, 174, 277, 382	2.5 V	8,320	106,496
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 652-Pin BGA, 672-Pin BGA[2]	136, 168, 271, 376, 376, 376	1.8 V	8,320	106,496
EP20K300E	300,000	240-Pin RQFP, 652-Pin BGA, 672-Pin BGA[2]	152, 408, 408	1.8 V	11,520	147,456
EP20K400	400,000	652-Pin BGA, 672-Pin BGA[2]	502, 502	2.5 V	16,640	212,992
EP20K400E	400,000	652-Pin BGA, 672-Pin BGA[2]	488, 488	1.8 V	16,640	212,992
EP20K600E	600,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 508, 588	1.8 V	24,320	311,296
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 508, 708	1.8 V	38,400	327,680
EP20K1500E	1,500,000	652-Pin BGA, 1,020-Pin BGA[2]	488, 808	1.8 V	51,840	442,368

ACEX 1K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[2]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS
EP1K10	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	66, 102, 130, 130	2.5 V	576	12,288
EP1K30	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	102, 147, 171	2.5 V	1,728	24,576
EP1K50	50,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 186, 249	2.5 V	2,880	40,960
EP1K100	100,000	208-Pin PQFP, 256-Pin BGA[2], 484 Pin BGA[2]	147, 186, 333	2.5 V	4,992	49,152

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 484-Pin BGA[2]	102, 147, 189, 191, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[2], 356-Pin BGA, 484-Pin BGA[2]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA 672-Pin BGA[2]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[2]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2], 600-Pin BGA, 672-Pin BGA[2]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	71, 102	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	81, 81, 117, 171, 171	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[2]	117, 171, 199, 218, 218	3.3 V	-1, -2, -3	1,960	1,960

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[3]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[3]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[3]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX, FLEX 10K, FLEX 10KE, and FLEX 6000 devices
EPC4[4]	44-Pin PLCC, 100-Pin TQFP, 144-Pin BGA[2]	1.8/2.5 V	4-Mbit serial/parallel configuration device designed to configure all APEX and FLEX 10K devices.

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Altera Device Selection Guide, continued from page 37

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032B	32	44-Pin PLCC/TQFP, 48-Pin BGA[5]	36, 36	2.5 V	-3, -5, -7
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064AE	64	44-Pin PLCC/TQFP, 49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68	3.3 V	-4, -7, -10
EPM7064B	64	44-Pin PLCC/TQFP, 48-pin TQFP, 49-Pin BGA[1], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68, 68	2.5 V	-3, -5, -7
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 256-Pin BGA[2]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[5], 256-Pin BGA[2]	68, 84, 84, 100, 100, 100	3.3 V	-5,-7,-10
EPM7128B	128	49-Pin BGA[5], 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 49-Pin BGA[5] 169-Pin BGA[5], 256-Pin BGA[2]	40, 84, 84, 100, 100, 100	2.5 V	-4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S	256	208-Pin PQFP	164	5.0 V	-7, -10, -15
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 84, 120, 164, 164	3.3 V	-5, -7, -10
EPM7256B	256	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 164, 164, 164	2.5 V	-5, -7, -10
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	120, 176, 212, 212	3.3 V	-5, -7, -10, -12
EPM7512B	512	144-Pin TQFP, 169-Pin BGA[5], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 212, 212, 212	2.5 V	-5, -6, -7, -10

MAX 3000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM3032A	32	44-Pin PLCC, 44-Pin TQFP	34, 34	3.3 V	-4, -7, -10
EPM3064A	64	44-Pin PLCC, 44-Pin TQFP, 100-Pin TQFP	34, 34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-Pin TQFP, 144-Pin PQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-Pin TQFP, 208-Pin PQFP	116, 158	3.3 V	-6, -7, -10

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

Notes to Tables:

(1) Preliminary. Contact Altera for latest information.
(2) This package is a space-saving FineLine BGA package.
(3) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.
(4) This device can be programmed by the user to operate at either 1.8 V or 2.5 V.
(5) This package is a space-saving Ultra FineLine BGA package, Altera's 0.8-mm pitch BGA package.