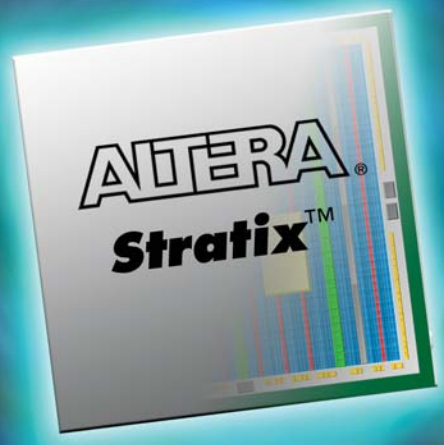
News & Views
First Quarter 2002
Newsletter for Altera Customers

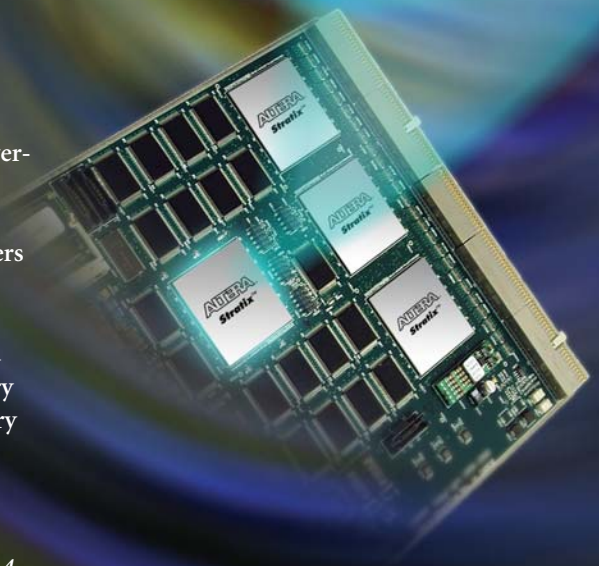
Altera Provides New Levels of System Integration with the Introduction of the Stratix Device Family

Next-generation systems demand a dramatic level of programmable logic device (PLD) bandwidth, including core processing, embedded memory, routing, and I/O bandwidth. Altera's new Stratix™ device family breaks the performance and density barriers for high-density programmable logic. Stratix devices are the first PLD family designed with a high-performance architecture, built from the ground up to enable true block-based design methodology. For the first time, designers can optimize and lock the performance of individual design blocks even when blocks are moved or integrated with other optimized functions. The Stratix family's unique combination of unmatched core performance, high memory bandwidth, digital signal processing (DSP) functionality, high-speed I/O performance, and block-based design methodology results in new levels of system integration for high-bandwidth system-on-a-programmable-chip (SOPC) designs.



New Levels of System Integration

Stratix devices are manufactured on a state-of-the-art 1.5-V, 0.13-µm, all-layer-copper SRAM process, with densities ranging from 10,570 to 114,140 logic elements (LEs). The Stratix family offers up to 10 Mbits of RAM with its TriMatrix™ memory structure. Comprised of three sizes of embedded memory blocks, the TriMatrix memory structure is optimized for high memory bandwidth and large memory storage requirements.



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ALTERA®
The Programmable Solutions Company®

Message from the *CEO*

Stratix Devices Provide New Levels of Integration

Last year was a banner year for Altera. With first-to-market products like the Mercury™ devices, the Excalibur™ embedded processor solutions, the HardCopy™ devices—and process technology milestones such as industry-first all-copper 0.13-µm programmable logic devices (PLDs)—we are in a position to further gain on our leadership position in the PLD industry. Today, Altera ushers in a new era for programmable logic with the introduction of the Stratix™ device family, the industry's fastest, most powerful PLD. Stratix devices have three times more memory and 22% more logic elements (LEs) than our competitor's devices and Stratix devices yield an astounding 40% increase in performance from our previous architecture. With the inclusion of dedicated digital signal processing (DSP) functionality, Stratix devices address DSP and computationally complex applications up to twice as fast as any other PLD in the industry. All that power is loaded onto a die that is 35% smaller than previous architectures. Building on our long history of innovation, Altera is once again breaking PLD boundaries and delivering the fastest devices in the industry while achieving the highest levels of integration with the most memory, logic elements, and DSP functionality in a PLD.

The Stratix architecture was built from the ground up and is a result of extensive customer feedback. Architectural innovations allow us to address our customers' needs for more processing power, speed, functionality, and cost efficiencies. Most significant, however, is how PLD design is changing as these devices grow in density and complexity to include more system functionality. In the past, an individual designer used multiple PLDs to create a single system. Today, we see team-based system-on-a-programmable-chip (SOPC) designs intended for a single device. Sections of a single large system design are divided among multiple engineers, resulting in a "block-based" design methodology. To address these increasing complexities, Altera simplified the design process by enabling a true timing-locked block-based design methodology. For the first time, a designer or teams of designers can work on specific areas of a design, lock in the timing integrity during the integration process, and break the endless loop of re-optimization. The powerful combination of our Stratix devices and the LogicLock™ capabilities of our Quartus® II design software allows team-based SOPC designs to not only shorten design cycles from months to weeks, but to dramatically increase overall system performance by as much as 100%.

Initial feedback on the Stratix devices has been overwhelmingly positive. Many beta customers were given access to the Quartus II software for Stratix design last November and found its increased performance to be unparalleled. PLD customers now have the performance boost they were waiting for and the option to migrate these high-density designs to a lower-cost HardCopy device—a very compelling solution.

Altera's new, powerful, Stratix device family is further proof of our steadfast commitment to deliver to our customers the best, most innovative solutions so that they can focus on their core competencies and get their products to market in a timely, risk-free, and cost efficient manner.

John Daane

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Altera Provides New Levels of System Integration with the Introduction of the Stratix Device Family, continued from page 1

The Stratix device family was specifically designed to address the increasing bandwidth requirements of high-speed systems.

Stratix devices include up to 28 embedded DSP blocks that eliminate the performance bottlenecks in DSP applications. Comprised of multiply and accumulate circuitry, the DSP blocks provide predictable performance and significant resource savings for complex applications that require high-data throughput. With up to 12 phase-locked loops (PLLs) and up to 40 system clocks for system-level clock management, support for many single-ended and differential I/O electrical standards, on-chip termination, and remote system upgrade circuitry, Stratix devices bring new levels of system integration for SOPC designs. Table 1 describes some of the highlights of the Stratix devices. Table 2 shows a family overview with the wide range of features and packages available.

High-Performance Architecture for Block-Based Design

The Stratix device family is based on a new architecture, built from the ground up to power complex designs to new levels of system integration. In combination with the Altera® Quartus® II LogicLock™ design methodology, Stratix devices simplify the difficult process of design integration, providing the basis upon which block-based designs can be developed and optimized for maximum performance.

Stratix Architectural Advances

The innovative, high-performance Stratix architecture is based on the MultiTrack™ interconnect with DirectDrive™ technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths used for inter- and intra-block connectivity. DirectDrive technology is a proprietary, deterministic routing technology that enables identical routing resource usage for any function regardless of placement within the device. DirectDrive technology simplifies the system integration stage of block-based design by eliminating the countless, time-consuming system re-optimization cycles that typically follow design changes and additions.

Table 1. Stratix Highlights

Feature	Benefit
High-Performance Architecture	New routing structure that facilitates block-based design for maximum system performance with minimum development time
TriMatrix Memory	Three sizes of embedded memory blocks with up to 10 Mbits of RAM, up to 12 terabits per second of memory bandwidth, and data transfer rates over 300 MHz per RAM block
DSP Blocks	Dedicated blocks run at up to 250 MHz for data throughput performance of up to 2.0 giga multiply-accumulate operations per second (GMACS) per DSP block
High-Speed I/O Standards and Interfaces	Support for high-speed I/O standards and high-speed interfaces such as 10-Gigabit Ethernet (XSBI), SFI-4, POS-PHY Level 4, HyperTransport™ technology, RapidIO™ standard, and UTOPIA Level 4 interfaces at up to 840 megabits per second (Mbps), as well as support for advanced external memory device interfaces
Clock Management Circuitry	Up to 12 PLLs and up to 40 system clocks plus features such as programmable bandwidth, clock switchover, PLL reconfiguration, spread-spectrum clocking, frequency synthesis, and programmable phase and delay shift
Terminator™ Technology	On-chip serial, parallel, and differential termination
Remote System Upgrades	Enables updates to PLDs in remote locations

High-Bandwidth Solutions

The Stratix device family was specifically designed to address the increasing bandwidth requirements of high-speed systems. All aspects of bandwidth are increased: overall memory bandwidth, arithmetic bandwidth for DSP applications, I/O bandwidth, and core performance.

Built on the performance-optimized and highly flexible MultiTrack interconnect routing structure, Stratix devices offer a dramatically

Table 2. Stratix Family Overview

Feature	EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80	EP1S120
Logic Elements (LEs)	10,570	18,460	25,660	32,470	41,250	57,120	79,040	114,140
M512 RAM Blocks (512 bits + parity)	94	194	224	295	384	574	767	1,118
M4K RAM Blocks (4 Kbits + parity)	60	82	138	171	183	292	364	520
MegaRAM™ Blocks (512 Kbits + parity)	1	2	2	4	4	6	9	12
Total RAM Bits	920,448	1,669,248	1,944,576	3,317,184	3,423,744	5,215,104	7,427,520	10,118,016
DSP Blocks	6	10	10	12	14	18	22	28
Embedded Multipliers *(1)*	48	80	80	96	112	144	176	224
PLLs	6	6	6	10	12	12	12	12
Maximum User I/O Pins	422	582	702	726	818	1,018	1,234	1,310
Available Packages	672-Pin BGA 672-Pin FineLine BGA™ 780-Pin FineLine BGA	672-Pin BGA 672-Pin FineLine BGA 780-Pin FineLine BGA	672-Pin BGA 672-Pin FineLine BGA 780-Pin FineLine BGA 1,020-Pin FineLine BGA	956-Pin BGA 780-Pin FineLine BGA 1,020-Pin FineLine BGA	956-Pin BGA 1,020-Pin FineLine BGA 1,508-Pin FineLine BGA	956-Pin BGA 1,020-Pin FineLine BGA 1,508-Pin FineLine BGA	956-Pin BGA 1,508-Pin FineLine BGA 1,923-Pin FineLine BGA	1,923-Pin FineLine BGA

Note to Table 2:

(1) Total number of 9 × 9 multipliers. To obtain the total number of 18 × 18 multipliers per device, divide the total number of 9 × 9 multipliers by a factor of 2. To obtain the total number of 36 × 36 multipliers per device, divide the total number of 9 × 9 multipliers by a factor of 8.

higher core performance than any previous architecture. Combined with performance and area-optimized embedded features such as TriMatrix memory, DSP blocks, and dedicated high-speed I/O interfaces, Stratix devices deliver optimal system integration to meet the requirements of high-bandwidth systems.

High-Memory-Bandwidth for Memory-Intensive Applications

Stratix devices feature the TriMatrix memory structure, made up of three sizes of embedded RAM blocks. TriMatrix memory includes M512 blocks, M4K blocks, and MegaRAM blocks, each of which can be configured to support a wide range of features. Each type of embedded RAM block in the TriMatrix memory structure targets a different class of applications: M512 blocks with 512 bits for small functions such as first-in first-out (FIFO) applications; M4K blocks with 4 Kbits to store incoming data from multi-channel I/O protocols; MegaRAM blocks with 512 Kbits for storage-intensive applications such as Internet protocol packet buffering or to store Nios™ embedded processor code. All memory blocks include extra parity bits for error control, embedded shift register functionality, mixed-width mode, and mixed-clock mode support. Additionally, the M4K and MegaRAM blocks support true dual-port mode and byte masking for advanced write operations.

Offering the highest memory-to-logic ratio and the highest memory bandwidth of any PLD family with up to 10 Mbits of RAM and up to 12 terabits per second of device memory bandwidth, the TriMatrix memory structure makes the Stratix family an ideal choice for memory-intensive applications.

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Altera Provides New Levels of System Integration with the Introduction of the Stratix Device Family, continued from page 5

DSP Blocks for Implementing Complex Systems

The DSP blocks in Stratix devices are high-performance embedded arithmetic units optimized for applications such as rake receivers, voice over Internet protocol (VoIP) gateways, orthogonal frequency division multiplexing (OFDM) transceivers, image processing applications, and multimedia entertainment systems. Flexible, efficient, and optimized for a variety of applications that require high data throughput, these DSP blocks can implement a variety of typical DSP functions, such as finite impulse response (FIR) filters, fast Fourier transform (FFT) functions, correlators, and encryption/decryption functions, and are ideal for the wireless communication, telecommunication, video, and image processing markets.

Stratix devices offer the True-LVDS circuitry to support the LVDS, LVPECL, PCML, and HyperTransport differential I/O standards with performance of up to 840 Mbps per channel.

DSP blocks eliminate performance bottlenecks in complex arithmetic applications, provide predictable and reliable performance, and result in resource savings. These attributes make DSP blocks ideal for implementing complex arithmetic functions while providing high-data throughput.

Stratix DSP blocks consist of hardware multipliers, adders, subtractors, accumulators, and pipeline registers. DSP blocks in Stratix devices can run at 250 MHz to provide data throughput performance of up to 2.0 GMACS per DSP block. Because Stratix DSP blocks can be implemented with dedicated circuitry, they offer optimal performance.

High-Bandwidth I/O & High-Speed Interface Capabilities

Stratix devices offer the True-LVDS™ circuitry to support the LVDS, LVPECL, PCML, and HyperTransport™ differential I/O standards with performance of up to 840 Mbps per channel. Each I/O channel includes dedicated serializer/deserializer (SERDES) circuitry for high-speed interface standards such as the 10-Gigabit Ethernet (XSBI), SFI-4, POS-PHY Level 4, HyperTransport, RapidIO™, and UTOPIA Level 4 standards. The fast PLLs in Stratix devices support clock rates over 600 MHz, which is required when designing with 10-Gigabit Ethernet (XSBI) and SFI-4 high-speed interfaces. The source-synchronous differential signaling capabilities are ideal for interface bridging, backplanes, chip-to-chip communications, or other subsystems. Stratix devices also support single-ended I/O standards, such as HSTL, SSTL, CTT, GTL+, PCI-X, AGP, LVTTL, and LVCMOS.

In addition to the on-chip TriMatrix memory, Stratix devices address increasing memory bandwidth requirements by providing customers with additional off-chip data storage, with support for external memory interfaces to the latest, industry-standard memory technologies such as double data rate (DDR) SDRAM, quad data rate (QDR) SRAM, QDRII SRAM, and zero-bus turnaround (ZBT) SRAM devices. Stratix devices are designed with timing-optimized I/O circuitry that ensures maximum data throughput.

Clock Management Circuitry for System-Level Clocking

Stratix clock management circuitry consists of a performance-optimized clock network and feature-rich PLLs for on- and off-chip clock management. With up to 12 PLLs and up to 40 system clocks per device, Stratix devices are built to function as the central clock manager to meet your system-timing challenges. Each Stratix device has up to 16 high-performance, low-skew global clocks that can be used for high-performance clocking or global control lines. Additionally, six localized clocks per region increase the total number of clocks for any region to up to 22 clocks.

Stratix PLLs offer advanced features such as external feedback, clock switchover, PLL reconfiguration, spread-spectrum clocking, and programmable bandwidth that provide the tools needed to manage the most complex timing challenges for high-speed designs. These devices are the first PLDs to offer on-chip PLL features for system-level clock management previously found only in high-end discrete PLL devices. This comprehensive timing solution eliminates the need for multiple discrete timing devices on a board, resulting in savings in real estate and overall system cost.

On-Chip Termination for Improving Signal Integrity & Board Benefits

The increasing demand for higher bandwidth in today's digital systems requires high-speed data transfer rates. At these high data rates, signal integrity is critical in meeting system performance requirements. In addition, I/O pin counts have increased dramatically, leading to even more board design challenges. Signal integrity is improved by terminating signals using on-board termination resistors. However, this further complicates board design, using up valuable engineering resources.

To address these challenges, Stratix devices provide Terminator technology, an on-chip termination resistor technology that supports on-chip serial, parallel, and differential termination (e.g., LVDS). On-chip termination is essential for reducing reflections and improving signal integrity in high-speed systems to maximize system performance. The on-chip termination resistors are placed adjacent to the buffers in the Stratix device, eliminating stub effects and helping to prevent reflections. In addition, Terminator technology on-chip termination simplifies board design and reduces board space by minimizing the number of external resistors required on the printed circuit board (PCB).

Remote System Upgrades

While using PLDs moves designs to market faster, using the remote system upgrade capability in Stratix devices can keep designs on the cutting edge. With the option of making real-time system upgrades from remote locations, Stratix devices can efficiently enable a host of new applications. A Stratix device's remote system upgrade can be transmitted through any communications network to keep products ahead of the competition.

Stratix devices also feature the industry's first dedicated recovery circuitry for remote system upgrades. Dedicated circuitry ensures that whenever an error occurs, whether during data transmission or device configuration, the Stratix device will always return to a known state to operate correctly, guaranteeing always operational functionality. Remote system upgrades provide both enhanced design flexibility and extended life cycles by allowing the design and shipment of a functional subset of your system now, giving you the ability to add features and enhancements at a later date from any remote location. Using Stratix devices, you can start your product design earlier and get your products to market faster with the assurance that they can be easily upgraded in the future.

Cost Reduction Path

System designers that require a low-risk cost-reduction path for high-volume production can migrate their Stratix designs to HardCopy™ devices. HardCopy devices preserve the functionality and timing of the design, providing a time-saving alternative to ASICs for high-volume production.

Quartus II Software Support

Stratix devices are supported by the Quartus II software version 2.0. The Quartus II software is the only PLD hardware design software that includes the LogicLock™ design flow for block-based design methodology. The LogicLock design flow allows designers to increase productivity and shorten design and verification cycles. Combined with the features of the Quartus II software, Stratix devices deliver SOPC solutions for high-bandwidth, high-performance applications.

While using PLDs moves designs to market faster, using the remote system upgrade capability in Stratix devices can keep designs on the cutting edge.

Nios Embedded Processor Support

Altera recently announced the release of the Nios embedded processor version 2.0. This new version includes support for Stratix devices and delivers significantly higher performance.

Conclusion

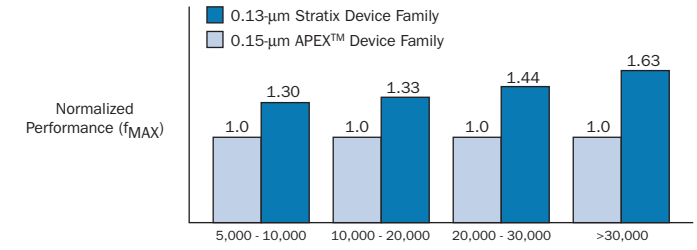
Together with the Quartus II software, Stratix devices enable block-based methodology and flexible system integration. These high-performance, high-density PLDs offer shorter design cycles, and faster time-to-market for complex designs, and they allow designers to integrate more and more complex functions into a single device. Visit the Altera® web site to learn more about the Stratix device family at **http://www.altera.com/stratix**.

Stratix Devices Combined with Quartus II Version 2.0 Provides Top Performance

The Altera® Quartus® II software version 2.0 is now shipping to all active subscribers. This release includes support for the new Stratix™ device family and new features and enhancements to boost system-on-a-programmable-chip (SOPC) design performance and productivity.

To offer optimal performance for the Stratix device family, the silicon and the performance algorithms embedded within the Quartus II software were designed in concert from start to finish. The result of this parallel device and software algorithm development is an performance improvement of 40% over the prior release and architecture. The greatest performance improvements are in the higher density devices in the family with up to 114,140 logic elements (LEs) and up to 10 Mbits of embedded memory. See Figure 1 for performance improvements by design density. The Quartus II software includes full support for advanced Stratix features including TriMatrix™ memory, digital signal processing (DSP) blocks, phase-locked loops (PLLs), and on-chip termination technology that can significantly reduce system-level bottlenecks and maximize system-level design performance.

Figure 1. Performance Improvements



Other benefits of combined silicon and software development are optimized support for incremental design flows and the introduction of advanced register packing algorithms that allow the placement of more logic in a given device. In addition to support for the new Stratix device family, the Quartus II software version 2.0 compiles designs up to 50% faster using the new fast fit compile option with minimum impact on design performance. The Quartus II software also supports selected MAX® devices and includes new features that improve system-level verification efficiency.

Increase Performance Using The LogicLock Block-Based Design Flow

By offering the LogicLock™ block-based design flow, the Quartus II software version 2.0 is the only programmable logic device (PLD) design software to include a block-based design methodology as a standard feature to shorten design and verification cycles. Using LogicLock constraints can increase design performance up to 25% (15% on average) compared to designs not using LogicLock constraints.

Stratix devices include DirectDrive™ technology to support and enhance the LogicLock block-based design methodology. DirectDrive technology ensures the same routing is available to a predefined design block regardless of where it is placed within a device, enabling fast, deterministic performance. This deterministic performance allows designers to use the LogicLock block-based design methodology to develop intellectual property (IP) libraries of data processing and I/O functions that designers can easily reuse in any project.

Register Packing Algorithms

The Quartus II software version 2.0 register packing algorithms result in an average of 15% fewer logic resources being consumed in Stratix devices than in previous Altera device families utilizing the same design. Using the Quartus II software version 2.0 with Stratix devices improves design performance while condensing silicon real estate, enabling integration of more system features.

Faster Compile Times & UNIX Performance

The new fast fit compile option delivers up to 50% faster compile times with only a minimal loss in f_{MAX} performance. You can use the fast fit option to quickly run multiple design iterations and then turn off the *Fast Fit* option to fine-tune the design. The Quartus II software

version 2.0 reduces compile times on UNIX-based distributed networks. Sophisticated compression techniques to optimize algorithms resulted in up to a 50% reduction in UNIX compile times compared to the Quartus II software version 1.1.

New Features Minimize System-Level Verification

Verification is typically the longest stage of any project. The Quartus II software version 2.0 adds several new features and enhancements to reduce verification times, including a new in-system verification technology, automatic testbench generation, and an interface to third-party signal integrity and electromagnetic compatibility (EMC) analysis tools.

SignalProbe™ in-system verification technology complements the SignalTap® embedded logic analysis feature, allowing you to incrementally route an internal node to an unused or reserved pin for analysis with an external scope or logic analyzer. The design's original routing, timing, and design files are fully preserved and any delays added in the routing from the internal nodes to the device pin are reported to provide an accurate representation of the captured signal's timing relationships.

The Quartus II software version 2.0 can output verification netlists for use in third-party HDL simulators, and create HDL testbench templates that can jump-start testbench development efforts. The Quartus II software can even create complete HDL testbenches from Quartus II software simulator Vector Waveform Files (**.vwf**).

The keys to developing systems with high-speed I/O are signal integrity and meeting stringent EMC requirements. The Quartus II software can output design-specific input/output buffer information specification (IBIS) models that can be exported to third-party signal integrity and EMC analysis tools. The IBIS models are customized based on the I/O standard settings for each pin in the design and simplify the analysis in third-party tools.

New Feature Summary

Table 1 shows a summary of the new features and enhancements in the Quartus II software version 2.0.

Table 1. Enhancements in the Quartus II Software Version 2.0

Functional Area	Change
Device Support	• New Stratix family, APEX II, Mercury, selected MAX® families (see Table 15 on page 16)
Design	• New MegaWizard® Plug-Ins to configure and parameterize new Stratix DSP, memory, and I/O functions • Tcl script template generation to run current project and to easily create custom scripts • New Stratix, LogicLock design methodology, and ARM®-based Excalibur™ on-line tutorials • Added device symbol generation for use in PCB schematic capture environments from Innoveda and Electronics Workbench
LogicLock Design Methodology	• Average of 15% faster f_{MAX} performance due to enhanced place-and-route algorithms • LogicLock enhancements for importing and exporting modules • Mentor Graphics® LeonardoSpectrum™ tool can produce separate EDIF files for modules and use tool command language (Tcl) commands for identifying LogicLock regions • Support for Synopsys FPGA Compiler II BLIS flow to generate separate EDIF files for modules • Synplicity® Synplify® tool uses LogicLock Tcl commands to group logic (equivalent to cliques)
Synthesis	• Exemplar Logic and Synplicity can now pass detailed timing constraints to the Quartus II software, including t_{SU} and t_{CO} for individual I/O pins (with respect to reference clocks) and t_{PD} for multi-cycle constraints
Place-and-Route	• New fast fit compile option to reduce compile times by 50%
Verification	• New SignalProbe in-system verification • Automatic testbench and testbench template generation • Capability to pass testbenches and macro files to third-party HDL simulation tools from within the Quartus II environment • New SignalTap user interface and enhancements including a log of captured data • IBIS model generation for export to third-party signal integrity and EMC analysis tools • Added support for Cadence NC-VHDL and Synopsys Scirocco VHDL simulators
Distributed Network and UNIX Performance	• Quartus II software version 2.0 reduces size of installation by 3× and decreases the amount of data sent over distributed networks to reduce compile time • Optimized Quartus II software user interface to start up faster on UNIX platforms
Programming	• IEEE 1532 programming support • Support for the Altera Programming Unit (APU)

Stratix

Quartus II Now Supports Stratix Devices

Stratix™ device support is currently available in the Altera® Quartus® II software version 2.0. The high-density, feature-rich Stratix devices range in density from 10,570 to 114,140 logic elements (LEs) and offer up to 10 Mbits of embedded RAM through its TriMatrix™ memory structure. Stratix devices include up to 28 digital signal processing (DSP) blocks for complex arithmetic functions that require high data throughput. Based on a leading-edge 0.13-µm all-layer-copper SRAM process, Stratix devices support high-speed data transfers through a wide range of high-speed differential and single-ended I/O standards and interfaces. Stratix devices offer up to 12 on-chip phase-locked loops (PLLs) for system-level clock management. In addition, the Terminator™ technology in Stratix devices supports on-chip serial, parallel, and differential termination and driver impedance matching. Stratix devices also offer remote system upgrade capabilities, allowing real-time updates to programmable logic devices (PLDs) from remote locations.

The first Stratix device, the EP1S25 device, will be available in Q2 2002, followed by the EP1S10 and EP1S80 devices. See Tables 1 and 2 for availability schedules and software support for Stratix devices.

Table 1. Stratix Device Availability

Device	Availability
EP1S10	Q3 2002
EP1S20	Q3 2002
EP1S25	Q2 2002
EP1S30	Q4 2002
EP1S40	Q3 2002
EP1S60	Q4 2002
EP1S80	Q3 2002
EP1S120	First half of 2003

Table 2. Stratix Devices & Quartus II Software Advanced Support Availability

Device	Package	Quartus II Software Advanced Support Availability
EP1S10	672-pin BGA *(1)*	Version 2.0 SP1 *(2)*
	672-pin FineLine BGA™	Version 2.0 SP1
	780-pin FineLine BGA	Now
EP1S20	672-pin BGA	Version 2.0 SP1
	672-pin FineLine BGA	Version 2.0 SP1
	780-pin FineLine BGA	Now
EP1S25	672-pin BGA	Version 2.0 SP1
	672-pin FineLine BGA	Version 2.0 SP1
	780-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP1S30	780-pin FineLine BGA	Version 2.0 SP1
	956-pin BGA	Now
	1,020-pin FineLine BGA	Now
EP1S40	956-pin BGA	Now
	1,020-pin FineLine BGA	Now
	1,508-pin FineLine BGA	Now
EP1S60	956-pin BGA	Now
	1,020-pin FineLine BGA	Now
	1,508-pin FineLine BGA	Now
EP1S80	956-pin BGA	Now
	1,508-pin FineLine BGA	Now
	1,923-pin FineLine BGA	Version 2.2
EP1S120	1,923-pin FineLine BGA	Version 2.2

Notes to Table 2:
(1) BGA: Ball-grid array.
(2) SP1: Service pack 1.

EXCALIBUR

Nios 2.0 Now Shipping

Building upon over a year and a half of overwhelming market success, Altera is now shipping the Nios™ embedded processor version 2.0. This new version of the popular Nios embedded processor delivers significantly higher performance and reduces the logic use of the core, while adding system performance features such as a simultaneous multi-master bus and custom instructions. These enhancements allow embedded systems developers to rapidly create custom system-on-a-programmable-chip (SOPC) solutions

optimized for high-throughput applications such as those found in networking, communications, and mass storage products. The definition and customization of Nios embedded processor-based systems is made possible with Altera's SOPC Builder system development tool.

New architectural features allow designers to optimize system performance by eliminating common data processing and throughput bottlenecks. The Nios embedded processor version 2.0 provides a set of five user-definable (custom) CPU instructions, allowing designers to easily integrate application-specific logic into the Nios arithmetic logic unit (ALU) to accelerate execution of time-critical software algorithms. You can increase data throughput dramatically with the new simultaneous multi-master Avalon™ bus and direct memory access (DMA) engine. Now multiple bus masters can transfer data simultaneously without CPU intervention, pushing Nios-processor-based systems into the realm of gigabit throughput performance.

The Nios embedded processor version 2.0 delivers a powerful solution for mainstream PLD designs. For example, a practical 32-bit Nios system with on-chip ROM, RAM, universal asynchronous receiver/transmitter (UART), interrupt controller, and bus logic running "hello world" consumes less than 1,800 logic elements (LEs) and can run at over 95 MHz in an APEX™ II device. A full-featured 32-bit system including an external memory interface, on-chip ROM, timer, four parallel I/O ports, UART, interrupt controller, and bus logic runs at over 80 MHz and consumes about 2,600 LEs.

SOPC Builder is an automated system development tool that dramatically simplifies the task of creating system-on-a chip (SOC) designs. The tool accelerates time to market by automating the system definition and integration phases of SOPC development. System designers can now define a complete system, from hardware to software, all within one tool and in a fraction of the time of traditional SOC design. SOPC Builder is included with the Nios embedded processor and integrated with the Quartus II software to give PLD designers immediate access to a revolutionary new development tool.

The Excalibur™ Development Kit featuring the Nios embedded processor, version 2.0, is available today for $995. For more information, go to **http://www.altera.com/nios**.

Nios Subscription Renewal

Annual subscription renewals are now available for the Nios embedded processor. With the Nios Subscription Renewal Program, you will receive automatic updates to the Nios embedded processor, the SOPC Builder tool, the GNUPro Toolkit, and Quartus II Limited Edition software for 1 year for only $495. Contact your local Altera sales representative for more details.

What Customers Are Saying about Nios

"For Telena's next generation product that integrates asynchronous transfer mode (ATM) and packet over SONET (Pos) capabilities, we use the Nios embedded processor to off-load tasks from the main, external CPU. We typically handle Level 2 and Level 3 processing in the Altera PLD, and it seems natural to integrate a Nios embedded processor alongside these functions," said Tony Porras, CTO and cofounder of Telena Communications. Porras continued, "External CPU performance is limited by bus throughput, while the Altera PLD architecture is excellent at fast data stream processing. We plan to implement more and more data stream processing functions with the Nios embedded processor inside the Altera PLD, and we look forward to using the Nios embedded processor as a central processing resource in Telena's future products."

ARM-Based Excalibur Device Family

Altera is now shipping all members of its ARM®-based Excalibur device family: low-cost EPXA1, mid-range EPXA4 and high-end EPXA10 devices. ARM-based Excalibur devices feature a 200-MHz ARM922T™ CPU in a performance-optimized hard core subsystem, which includes instruction and data caches, a memory management unit, on-chip SRAM and DPRAM, single data rate (SDR) and double data rate (DDR) controllers, flash memory, interrupt controllers, and a set of peripherals. This processor subsystem (PLD stripe) mates to the APEX-like architecture and supports from

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EXCALIBUR™

Devices & Tools, continued from page 11

4,160 up to 38,400 LEs, from 43,248 up to 327,680 RAM bits, and up to 711 user I/O pins as well as many of the high-speed I/O standards.

The EPXA10 Development Kit supports the Excalibur family, with a lower cost EPXA1 kit available soon. The Excalibur Solutions Pack, available in the kits or separately, covers the software support and utilities for ARM-based Excalibur platforms.

APEX II

APEX II EP2A70 devices, the first PLDs on 0.13-µm technology, began shipping at the end of 2001. Altera and TSMC partnered to bring this cutting-edge technology to market first. Altera continues to offer customers both increased core performance and a sustainable long-term low-cost model through HardCopy™ migration.

EP2A15, EP2A25, EP2A40, and EP2A70 devices are now shipping. APEX II devices range in density from 16,640 to 67,200 LEs and are memory-rich, offering 4 Kbits of memory per embedded system block (ESB), with total device memory ranging from 416 Kbits to 1.1 Mbits. The APEX II device family supports high-speed data transfers through a wide range of high-speed I/O standards such as the LVDS, PCML, LVPECL, HyperTransport™, HSTL, and SSTL standards. With True-LVDS™ circuitry, APEX II devices can achieve data transfer rates of up to 1 gigabit per second (Gbps) per channel. With these I/O features, you can use APEX II devices in the following applications:

- PHY-link layer interface applications (POS-PHY, Flexbus, and UTOPIA)
- Host-processor interface applications (HyperTransport technology, peripheral component interconnect (PCI), and PCI-X)
- Switch fabric interface (CSIX and LCS)
- External memory interfaces (double data rate (DDR), zero bus turnaround (ZBT), and quad data rate (QDR) memory devices)

See Tables 3 and 4 for availability schedules and software support for APEX II devices.

Table 3. APEX II Device Availability

Device	Production Availability
EP2A15	Now
EP2A25	Now
EP2A40	Q2 2002
EP2A70	Q2 2002

Table 4. APEX II Devices & Quartus II Software Support Availability

Device	Package	Software Support Availability
EP2A15	672-pin FineLine BGA 724-pin BGA	Now
EP2A25	672-pin FineLine BGA 724-pin BGA 1,020-pin FineLine BGA	Now
EP2A40	672-pin FineLine BGA 724-pin BGA 1,020-pin FineLine BGA	Now
EP2A70	724-pin BGA 1,508-pin FineLine BGA	Now

APEX II Board Offerings

An Altera development/demonstration board used to display the high-performance I/O channels of APEX II devices (e.g., the LVDS, LVPECL, PCML, and HyperTransport channels) is now available through Altera field application engineers. This board also has the capability of demonstrating the APEX II DDR interface with an external Micron DDR SDRAM DIMM module.

Additionally, an Altera APEX II I/O standard board is now available for purchase from Princeton Technology Group (PTG), allowing you to evaluate different high-speed communication I/O standards such as the LVDS, POS-PHY Level 4, RapidIO™, and HyperTransport standards. You can purchase this board directly from PTG at **http://www.ptgroupinc.com**.

APEX II IP Offerings

APEX II device-optimized IP functions now available for purchase include the POS-PHY Level 4, Flexbus Level 4, DDR SDRAM controller, and SDR SRAM controller cores.

Additionally, the ZBT SRAM and QDR SRAM controller reference designs are available for free. To obtain these functions, contact your local Altera sales representative or go to the IP MegaStore™ web site at **http://www.altera.com/ipmegastore.**

APEX II HardCopy Solution

Altera offers a migration solution from APEX II to HardCopy devices for system designers who need a low-risk cost-reduction solution for high-volume production. You can prototype time-sensitive applications using APEX II devices and migrate the design to HardCopy devices for high-volume production. HardCopy devices preserve the functionality and timing of the design and allow you to improve time-to-market at the lowest cost.

APEX II Industrial Offerings

Altera has proactively selected industrial-grade devices for the APEX II device family to further compress design cycles for the fastest possible time-to-market. A -8 speed grade will be available in the industrial-grade production versions of the device offerings. Table 5 shows the availability for industrial-grade offerings.

Table 5. APEX II Industrial Device Offering

Device	Package	Production Availability
EP2A15	672-pin FineLine BGA	Now
EP2A25	672-pin FineLine BGA	Now
	724-pin BGA	Now
	1,020-pin FineLine BGA	Contact Altera
EP2A40	1,020-pin FineLine BGA	Q2 2002

MERCURY

Mercury Silicon Available in Production Mode

All devices and all speed grades of the Mercury™ device family are now shipping in production mode, including industrial temperature offerings in both product lines (see Table 6). High-speed 1.25-Gbps serial links featuring clock-data recovery (CDR) circuitry and an embedded serializer/deserializer (SERDES) make these devices ideal for serial backplane applications.

Mercury I/O Performance Update

Based on extensive characterization of the Mercury silicon, the data rate specifications for CDR and source-synchronous mode have been updated. These new specifications illustrate the capabilities of the Mercury transceiver silicon across the range of the product's speed grades. See Table 7.

Table 6. Mercury Device Availability

Device	Package	Temperature Grade	Speed Grade	Availability
EP1M120	484-pin FineLine BGA	Commercial	-5, -6, -7	Now
		Industrial	-6	Now
EP1M350	780-pin FineLine BGA	Commercial	-5, -6, -7	Now
		Industrial	-6	Now

Table 7. Mercury Device I/O Performance

Speed Grade	Maximum CDR Performance (Gbps)	Maximum Source-Synchronous Performance (Mbps)
-5	1.25	840
-6	1.25/1.0 (1)	840
-7	1.0	840

Note to Table 7:

(1) EP1M350 devices in -6 speed grade (commercial and industrial) have a maximum CDR rate of 1.25 Gbps for a maximum of 8 channels, as long as the data rate of the other 10 channels does not exceed 1.0 Gbps. EP1M120 devices in -6 speed grade have a maximum CDR rate of 1.25 Gbps on all eight channels.

APEX

APEX 20KC Available in Production Mode

All APEX 20KC devices are now available with all parts and packages shipping in full production mode. These high-performance APEX devices address the high-bandwidth needs of SOPC applications. They combine the advanced features found in APEX 20KE devices with high-performance 0.15-µm all-layer-copper interconnect technology that provides performance improvements of 25% over aluminum-based devices. Table 8 on page 14 shows the availability schedule for APEX 20KC devices. All APEX 20KC devices are supported in the Quartus II software version 2.0, as shown in Table 9 on page 14.

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Table 8. APEX 20KC Device Availability

Device	Production Availability
EP20K200C	Now
EP20K400C	Now
EP20K600C	Now
EP20K1000C	Now

Table 9. APEX 20KC Devices & Quartus II Software Support Availability

Device	Package	Software Support Availability
EP20K200C	208-pin PQFP *(1)*	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K400C	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now

Note to Table 9:
(1) PQFP: Plastic quad flat pack.

Industrial-Grade APEX Offerings

Industrial-grade APEX devices are now available in a wide variety of package offerings. Refer to Tables 10, 11, and 12.

Table 10. APEX 20KC Device Industrial Offering

Device	Package	Speed Grade
EP20K200C	484-pin FineLine BGA	-8
EP20K400C	672-pin FineLine BGA	-8
EP20K600C	652-pin BGA	-8
	672-pin FineLine BGA	
EP20K1000C	1,020-pin FineLine BGA	-8

Table 11. APEX 20KE Device Industrial Offering

Device	Package	Speed Grade
EP20K60E	144-pin FineLine BGA	-2X *(1)*
	208-pin PQFP	
EP20K100E	144-pin FineLine BGA	-2X *(1)*
	324-pin FineLine BGA	
EP20K160E	484-pin FineLine BGA	-2X *(1)*
EP20K200E	240-pin PQFP	-2X *(1)*
	484-pin FineLine BGA	
EP20K300E	672-pin FineLine BGA	-2X *(1)*
EP20K400E	652-pin BGA	-2X *(1)*
	672-pin FineLine BGA	
EP20K600E	652-pin BGA	-2X *(1)*
	672-pin FineLine BGA	
EP20K1000E	652-pin BGA	-2X *(1)*
	672-pin FineLine BGA	

Note to Table 11:
(1) The "X" denotes PLL and LVDS support.

Table 12. APEX 20K Device Industrial Offering

Device	Package	Speed Grade
EP20K100	208-pin PQFP	-2V (1)
	240-pin PQFP	
EP20K200	240-pin PQFP	-2V (1)
	484-pin FineLine BGA	
EP20K400	652-pin BGA	-2V (1)
	672-pin FineLine BGA	

Note to Table 12:
(1) The "V" denotes 5.0-V tolerant I/O interfaces.

ACEX

ACEX 1K Availability

ACEX® 1K devices are available in quad flat pack (QFP) and FineLine BGA packages in the 10,000, 30,000, 50,000, and 100,000 gate densities. These cost-optimized devices are especially suited for low-cost, high-volume applications.

To reiterate Altera's commitment to the low-cost marketplace, Altera has aggressively reduced high-volume pricing on ACEX 1K devices and continues to provide the lowest-cost solution in the industry.

Full software support for all ACEX 1K devices is available in the Quartus II Web Edition version 2.0, which is available for free download at **http://www.altera.com**.

MAX

Altera Provides Complete Silicon & Software Support for the IEEE 1532 Standard

The IEEE 1532 standard was recently approved and allows for multi-vendor, multi-device concurrent programming and enables faster programming times. Altera was a major participant in the definition and approval of this standard.

Altera is the only PLD vendor shipping IEEE 1532-compliant devices in volume today. Table 13 lists the current IEEE 1532-compliant devices offered by Altera.

Table 13. Current IEEE 1532-Compliant Devices

Device Family	Compliant Devices
MAX® Devices	MAX 7000B, MAX 7000AE, MAX 3000A
Configuration Devices	EPC4, EPC8, EPC16

The Quartus II software version 2.0 provides support for the IEEE 1532 device files. Go to the Altera web site at **http://www.altera.com** and click **Devices** then **MAX 7000** to learn more about Altera's IEEE 1532 solution.

MAX Applications Web Page Update

A new application, "Use MAX Devices in Configuration Schemes," is posted on the Altera web site at **http://www.altera.com**. This application details how you can use the non-volatile MAX devices in conjunction with enhanced configuration devices or with flash memory to control and manage the configuration of SRAM-based lookup table (LUT) devices. It also references other relevant data sheets and technical specifications.

The MAX Applications section of the Altera web site is an excellent resource for detailed technical information, including white papers and application notes. This information allows you to quickly and efficiently implement specific functionality within MAX devices.

CONFIGURATION

Enhanced Configuration Devices

Altera introduces industrial-grade enhanced configuration devices, available today with the EPC4, EPC8, and EPC16 devices. These enhanced configuration devices provide a complete single-device solution for a wide range of density requirements. Vertical migration capability allows you to easily migrate from the EPC4 to the EPC8 to the EPC16 device in the same package, without having to change the board layout. Also, the commercial-grade EPC4, EPC8, and EPC16 devices are all available.

Enhanced configuration devices offer in-system programmability (ISP) through a built-in IEEE standard for a boundary-scan-based in-system configuration standard of programmable devices (IEEE 1532). The inclusion of ISP and reprogrammability provides a significant advantage over one-time programmable solutions by introducing flexibility and reusability to the configuration process.

Altera's enhanced configuration devices also introduce numerous features for specialized configuration needs. These features include a parallel configuration capability to accelerate configuration times, a new page mode that allows you to store multiple configurations, block protection for partial reprogramming support, and full clocking flexibility through the programmable clock and external clock features.

You can use portions of the flash memory as general-purpose memory via a built-in processor access feature. This advanced feature set enhances the overall PLD design experience while improving manufacturability for a high-volume environment.

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Design Software

Quartus II Version 2.0 Improves Performance & Reduces Compile Times

The Quartus II software version 2.0 is now shipping to all users with active subscriptions. Version 2.0 delivers 40% faster performance (f_{MAX}) with support for the new Stratix device family and up to 50% faster compile times than version 1.1. For more information on the Quartus II software version 2.0, refer to "Stratix Devices Combined with Quartus II Version 2.0 Provides Top Performance" on page 8. Table 14 shows a list of new device support in the Quartus II software version 2.0.

Download the Latest OEM Synthesis and Simulation Tools

All customers with active subscriptions can download the latest versions of the OEM synthesis and simulation tools from the Altera web site. These new versions include support for the new Stratix device family and will also be included in the Quartus II version 2.0 upgrade shipments. Table 15 shows the latest versions available.

Table 15. OEM Synthesis & Simulation Tools

Tool	Version
Exemplar Logic™ LeonardoSpectrum™-Altera Edition	2002a
Model Technology ModelSim®-Altera Edition	5.5e

New Adapters for EPC Configuration Devices

The following new adapters are now available for the Altera Programming Unit (APU) and Master Programming Unit (MPU) hardware (see Table 16).

Table 16. New Adapters

Ordering Code	Description
PLMUEPC-88	88-pin Ultra FineLine BGA package programming adapter for EPC16 configuration devices
PLMQEPC-100	100-pin PQFP package programming adapter for EPC4, EPC8, and EPC16 configuration devices

Table 14. Quartus II Software Version 2.0 Support for New Devices

Support	Family	Device	Package
Advanced compilation and simulation support	Stratix *(1)*	EP1S10	780-pin FineLine BGA
		EP1S20	780-pin FineLine BGA
		EP1S25	780-pin FineLine BGA, 1,020-pin FineLine BGA
		EP1S30	956-pin BGA, 1,020-pin FineLine BGA
		EP1S40	956-pin BGA, 1,020-pin FineLine BGA, 1,508-pin FineLine BGA
		EP1S60	956-pin BGA, 1,020-pin FineLine BGA, 1,508-pin FineLine BGA
		EP1S80	956-pin BGA, 1,508-pin FineLine BGA
	ARM®-Based Excalibur	EPXA1	484-pin FineLine BGA, 672-pin FineLine BGA
Full support, includes Programmer Object File (**.pof**) generation	APEX II	EP2A70	724-pin FineLine BGA, 1,508-pin FineLine BGA
	APEX 20KC	EP20K200C	240-pin PQFP, 484-pin FineLine BGA, 208-pin PQFP, 356-pin BGA
	MAX 7000B	All	All
	MAX 7000AE	All	All
	MAX 3000A	All	All
	Mercury	EP1M120	484-pin FineLine BGA

Note to Table 14:
(1) Stratix pin-out support will be included in a subsequent service pack.

SignalProbe Compilation Enables Fast System Debugging with the Quartus II Software

The SignalProbe™ feature, introduced with the Quartus II software version 2.0, enables you to quickly route signals to I/O pins without affecting the design. While taking advantage of incremental routing with a fully routed design, SignalProbe compilation allows you to select signals for easy debugging. These signals are then routed to either previously reserved I/O pins or currently unused I/O pins.

The SignalProbe feature reroutes signals in a fraction of the normal compilation time. The incremental routing process preserves results of the prior compilation, thereby preserving the signals' behavior and design operation. For guidelines on using the SignalProbe feature, see Table 17.

Keeping system-level debugging time to a minimum, SignalProbe compilation reduces the signal routing process to less than 5% of the time required for a full recompilation. This reduction in processing time grants quick access to internal design signals.

Table 17. SignalProbe Guidelines

Guidelines	Description
Devices Supported	APEX II, APEX 20KE, APEX 20KC, APEX 20K, ARM-based Excalibur.
Compiler Settings	Initial compilation must be performed with smart compilation turned on.
Internal Nodes for Analysis	Must be post compilation and cannot be groups, output signals, and neither carry-out nor cascade-out signals.
Pins for Routing Internal Nodes for Analysis	Must not already be assigned for design use. Must not be dedicated clocks, Excalibur stripe I/O pins, fast pins, PLLs, or dual-purpose pins used for second purpose (e.g., `INIT_DONE` or `DEV_OE`).

Quartus II Device Support

The Quartus II software supports the following device families:

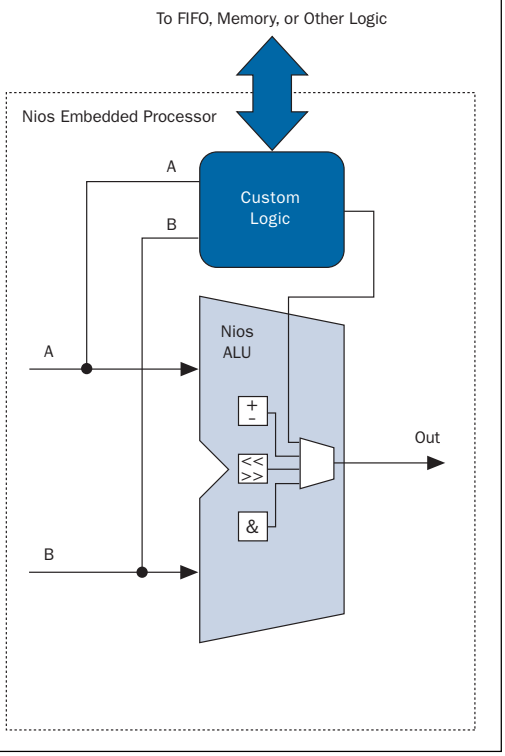
- Stratix
- APEX II
- APEX 20K (including APEX 20K, APEX 20KE, and APEX 20KC)
- ARM-Based Excalibur
- Mercury
- FLEX® 10KE
- ACEX 1K
- FLEX 6000
- MAX 7000B, MAX 7000AE, MAX 3000A

Optimizing Nios System Performance Using Custom Instructions

By creating custom instructions, designers can significantly increase system performance by targeting critical inner loops and cycle-intensive algorithms and reducing a complex sequence of instructions to a single instruction implemented in hardware.

With Altera's Nios™ embedded processor version 2.0, system designers can add custom-defined functionality directly inside the Nios CPU's arithmetic logic unit (ALU) using custom instructions (see Figure 1).

Figure 1. Custom Instruction Logic



Custom Instructions

Designers can use custom instructions to replace complex, cycle-intensive software routines with fast, cycle-efficient custom logic blocks. Up to five combinatorial or sequential custom logic blocks may operate in a single CPU, and may also access memory and/or logic outside of the Nios system module. Custom logic blocks perform their user-specified operation upon the contents of two registers, `Ra` and `Rb`. The resulting value is stored in register `Ra`. The functionality of these custom logic blocks is only limited by the number of logic elements (LEs) in the device and the imagination of the designer.

Custom hardware blocks are software-accessible through five user-definable opcodes in the Nios embedded processor instruction set. These opcodes are accessed using automatically generated C and Assembly language macros. The SOPC Builder creates the macros for any custom instructions during system generation.

Custom Instructions Use

Complex algorithms implemented in hardware are often faster and more efficient than software implementations. By creating custom instructions, designers can significantly increase system performance by targeting critical inner loops and cycle-intensive algorithms and reducing a complex sequence of instructions to a single instruction implemented in hardware. System designers use this feature for a variety of applications (e.g., to optimize their Nios embedded processor for digital signal processing (DSP), packet header processing, and other computation-intensive applications).

For example, a floating-point multiply operation executed by the Nios CPU can take over 2,800 clock cycles. A custom instruction implementation of this floating-point multiplication using a floating-point unit (FPU) hardware block is executed in only 19 clock cycles (see Table 1). This example is part of the Nios Custom Instruction Tutorial, and is available as a reference design in the *<Nios version 2.0-installation directory>* **\tutorials\Cust_Inst_Example1** directory.

Implementing Custom Instructions

You can implement custom instructions in the Nios embedded processor version 2.0 while creating or editing a Nios CPU by clicking the **Custom Instructions** tab (see Figure 2).

The **Custom Instructions** tab is the interface for system designers to connect their custom logic to the ALU of the Nios CPU. First, select the opcode used for the custom instruction. Five opcodes are available: USR0 through USR4. Next, import and scan the HDL files that will be represented as custom instructions. The Design Import Wizard scans the top-level module for ports (see Figure 3 on page 20) and makes the appropriate connections. The Design Import Wizard accepts files of the following type: Verilog HDL, VHDL, EDIF, VQM, and the Altera® Quartus® II schematic. After you import your design files, assign the number of CPU clock cycles needed by the custom instruction and the name of the custom instruction.

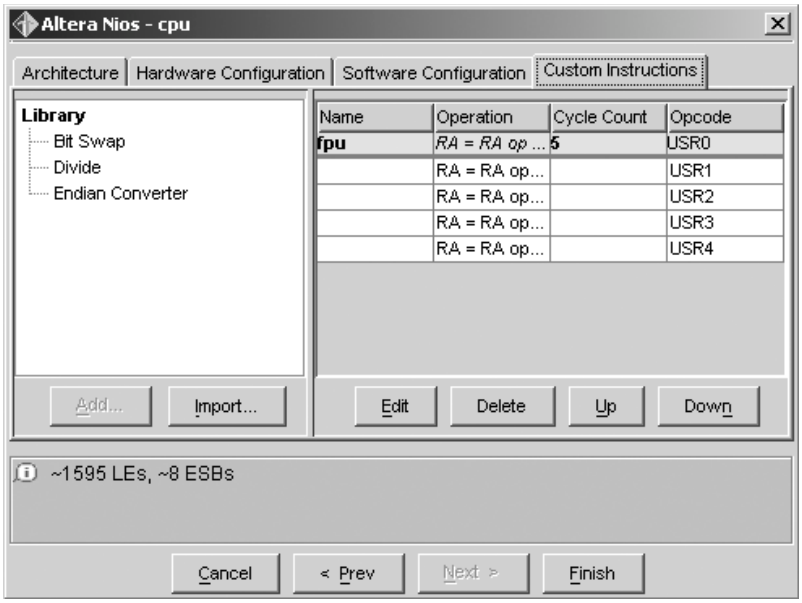
During system generation, the SOPC Builder tool builds the Nios CPU with the custom logic as part of the ALU, controlled by the opcode selected. Using the name of the custom instruction, the software development kit builds software macros that are used in C/C++ and Assembly language. These macros are included in the **nios.h** and **nios.s** files, respectively, located in the **inc** directory of the custom software development kit directory.

The software macros created give the designer access to the custom instruction. In C/C++, the macros are in-line and are used just like a function call. If the prefix port is used, a separate macro is created to use with the prefix. For example, the two C/C++ macros created for the floating-point unit (FPU) are:

```
result = nm_fpu (dataa, datab);
     //not using the prefix

result = nm_fpu_pfx (prefix,
     dataa, datab);
     //using the prefix
```

Figure 2. SOPC Builder: Nios CPU Configuration Interface



In Assembly language, the macro calls the USR opcode and is used as a standard Assembly instruction. If the prefix is used, the PFX instruction must precede the macro, since it only affects the following instruction. For more information on user-defined opcodes (USR0 through USR4), refer to the *Nios Software Development Reference Manual*.

Table 1. Custom Instruction vs. Software-Only Performance Comparison *Note (1)*

Floating-Point Operation	CPU Clock Cycles		Speed Increase
	Software Library	Custom Instruction (FPU)	
Multiplication a x b	2,874	19	151.26
Multiply and negate – (a x b)	3,147	19	165.63
Absolute |a|	1,769	18	98.28
Negate – (a)	284	19	14.95

Note to Table 1:

(1) These performance calculations are compiler-dependent. They were taken using the Cygnus compiler included in the Nios embedded processor version 2.0.

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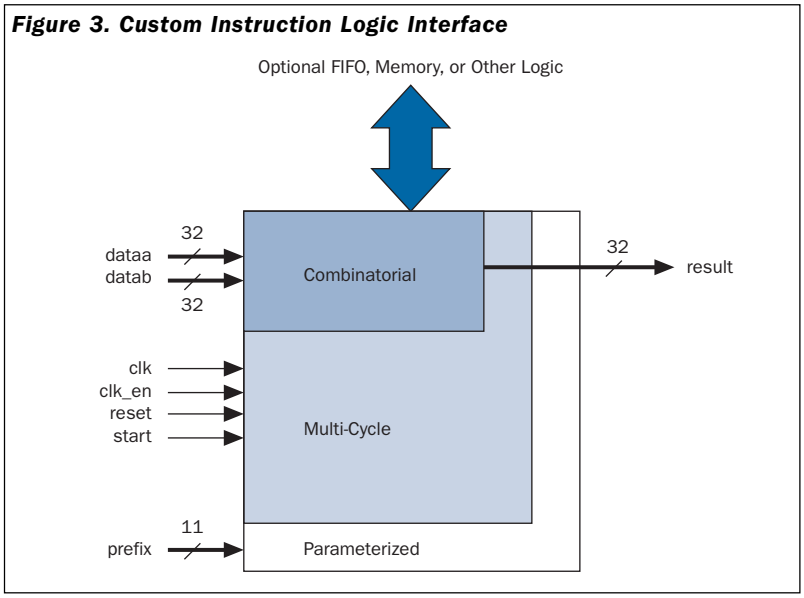
Using Custom Instructions in Nios Version 2.0, continued from page 19

Figure 3. Custom Instruction Logic Interface



Conclusion

By using the custom instruction feature in the Nios embedded processor, system designers have the ability to tailor their CPU to accelerate application-specific tasks.

For more information on custom instructions, refer to *AN 188: Custom Instructions for the Nios Embedded Processor*.

New Altera Publications

New publications are available from Altera Literature Services at **lit_req@altera.com**. When ordering, please specify the part number shown in parentheses. On-line documents are available on the Altera web site at **http://www.altera.com**.

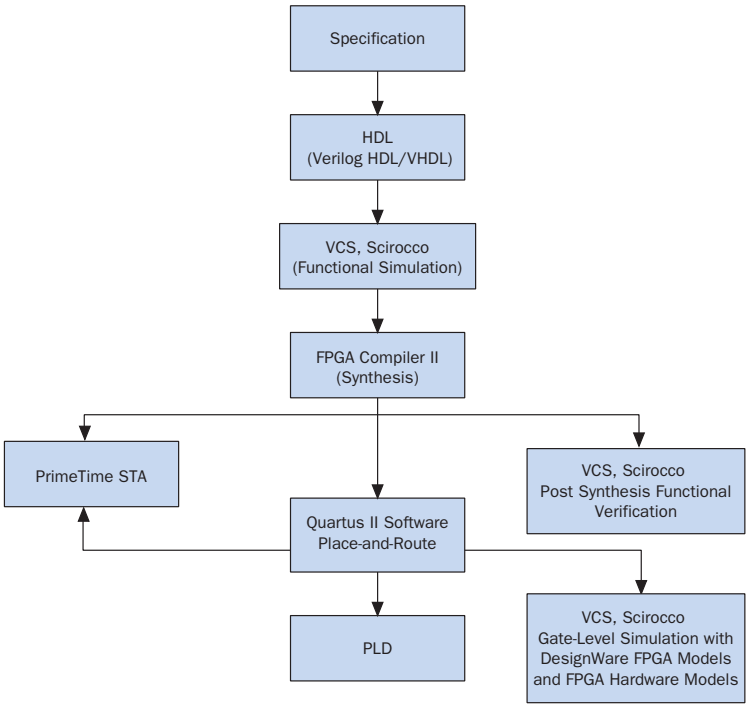
- *AN 200: Using PLLs in Stratix Devices (AN-200-1.0)*
- *AN 201: Using Selectable I/O Standards in Stratix Devices (AN-201-1.0)*
- *AN 202: Using High-Speed Differential I/O Interfaces in Stratix Devices (AN-202-1.0)*
- *AN 203: Using TriMatrix Embedded Memory Blocks in Stratix Devices (AN-203-1.0)*
- *AN 204: Using ModelSim-Altera in a Quartus II Design Flow (AN-204-1.0)*
- *AN 205: Understanding Altera Software Licensing (AN-205-1.0)*
- *AN 206: Understanding the Differences Between Stratix & APEX Memory Architecture (AN-206-1.0)*
- *AN 207: TriMatrix Memory Selection Using the Quartus II Software (AN-207-1.0)*
- *AN 208: Configuring Stratix Devices (AN-208-1.0)*
- *AN 209: Using Terminator Technology in Stratix Devices (AN-209-1.0)*
- *AN 210: Converting Memory from Asynchronous to Synchronous for Stratix Designs (AN-210-1.0)*
- *AN 211: QDR SRAM Controller Reference Design for Stratix Devices (AN-211-1.0)*
- *AN 212: Implementing Double Data Rate I/O Signaling in Stratix Devices (AN-212-1.0)*
- *AN 214: Using the DSP Blocks in Stratix Devices (AN-214-1.0)*
- *AN 217: Using Remote Configuration with Stratix Devices (AN-217-1.0)*
- *AN 225: LeonardoSpectrum & Quartus II Design Methodology (AN-225-1.0)*
- *AN 226: Synplify & Quartus II Design Methodology (AN-226-1.0)*
- *AN 229: Advanced Troubleshooting for Altera Software Licensing (AN-229-1.0)*
- *Stratix Programmable Logic Device Family Data Sheet (DS-STXFAMLY-1.0)*
- *The Need for a High-Bandwidth Memory Architecture in PLDs White Paper (WP-TriMatrix-1.0)*
- *Using PLDs for High-Performance DSP Applications White Paper (WP-STXDSP-1.0)*

Creating an ASIC-Like Flow Using Synopsys Tools & Stratix Devices

by Jackie Patterson,
Director of Marketing Programs,
Synopsys, Inc.

Altera® programmable logic devices (PLDs) have grown tremendously in size, speed, and complexity, allowing designers to use them as their system-on-a-programmable-chip (SOPC) solutions. For example, the new Stratix™ device family with embedded digital signal processing (DSP) blocks can handle DSP functions and complex arithmetic functions previously reserved for ASIC technologies. Stratix devices enable you to complete a difficult project in less time. Careful attention to the design flow is necessary to ensure that the device will work correctly and meet the project schedule. To address such concerns, programmable logic designers are applying techniques proven in ASIC design, as shown in Figure 1.

Figure 1. ASIC-Like Design Flow for Stratix Devices



High-Performance Simulation

The key to first-pass success in working with ASICs is ensuring that the design will work before it goes to silicon. This confirmation is also important with programmable logic, even though the device logic can be modified at no cost. Functional simulation of the design in register transfer level (RTL) is the generally accepted way to gain confidence that the end design meets the specifications. As the design grows, so does the size of the test vector set used for simulation. High-performance simulators such as the Synopsys VCS and Scirocco software are needed to run as many simulation cycles as possible before the device goes to the lab.

ASIC-Like Synthesis

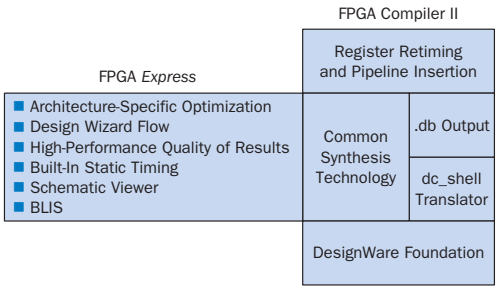
The synthesis tool you choose can greatly affect the outcome of a design project. The Synopsys FPGA Compiler II synthesis tool offers an easy-to-use ASIC-like synthesis design flow for designs targeting Stratix devices. Also, the FPGA Compiler II tool uses synthesis techniques originally proven on ASICs to optimize clock speed and area. One technique is register retiming, which finds the best location in a cone of logic for a register so the device runs at the fastest clock speed. Synopsys FPGA Compiler II can retime all types of logic (pipelining arithmetic operators, fine-tuning state machines, and even optimizing random logic), which is increasingly important as designs become more complex.

In addition, the Synopsys FPGA Compiler II tool offers ASIC-compatibility features (see Figure 2 on page 22). This tool can read and write Design Compiler scripts, giving you a starting point if you are reusing HDL code from a legacy ASIC project. Synopsys FPGA Compiler II is able to write out a Synopsys database file (**.db**), which is the database used by other high-performance tools such as the PrimeTime static timing analyzer.

If you are using a Stratix device to prototype an ASIC, Synopsys FPGA Compiler II can handle the DesignWare Foundation intellectual property (IP) used to speed the design of that

continued on page 22

Figure 2. Adding ASIC Capabilities to PLD Synthesis



ASIC. Another benefit is that you are prototyping the same logic that appears on the ASIC.

Static Timing Analysis

Both ASIC and programmable logic designers have long used static timing analysis. The advantages of a comprehensive timing check of all paths in the design are well known. However, as the devices grow larger, more emphasis is placed on quickly identifying and fixing the root cause of timing issues. Fixing timing issues is the strong point of the Synopsys PrimeTime software. The PrimeTime tool applies sophisticated analysis algorithms to the timing data, identifying bottlenecks in the design and pinpointing the logic operation which may cause violations on several critical paths.

For more information on an ASIC-like flow for your next programmable logic project, visit **http://www.synopsys.com/fpga**.

Conclusion

With the introduction of the Stratix device family, PLDs can now handle DSP functions and computationally complex arithmetic functions previously reserved for ASICs. For designs targeting Stratix devices, the Synopsys FPGA Compiler II offers an easy-to-use ASIC-like synthesis design flow. Combining Stratix devices with the Synopsys FPGA Compiler II allows designers to create an ASIC-like design flow to accelerate design cycles.

LeonardoSpectrum Supports Advanced Features in Stratix Devices

by Roger Do,
Technical Marketing Manager,
Mentor Graphics

Altera® Stratix™ devices are the industry's fastest programmable logic devices (PLDs), enabling higher levels of system integration. Stratix devices incorporate advanced features such as the TriMatrix™ memory, digital signal processing (DSP) blocks, versatile phase-locked loops (PLLs), and Terminator™ technology. The LeonardoSpectrum™ tool provides support for all of these advanced features. This article focuses on DSP block support in the LeonardoSpectrum software.

DSP Block Support

The DSP blocks in Stratix devices are high-performance embedded DSP units that are optimized for applications such as rake receivers, voice over Internet protocol (VoIP) gateways, orthogonal frequency division multiplexing (OFDM) transceivers, image processing applications, and multimedia entertainment systems.

To support the DSP functionality in the Stratix architecture, the LeonardoSpectrum software version 2002a is enhanced to detect DSP functions in register transfer level (RTL) code and map them appropriately to utilize the dedicated DSP blocks. You can use the following to map to the DSP block:

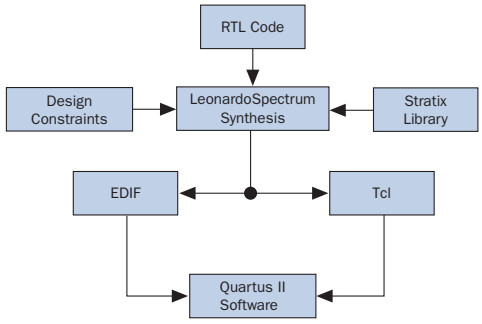
- Stand-alone multiplier
- Multiplier-accumulator (MAC)
- Multiplier adder or subtractor

The LeonardoSpectrum software detects these cases in the RTL code and maps the function to the appropriate Altera megafunction: `lpm_mult`, `altmult_accum`, and `altmult_add`.

LeonardoSpectrum & Quartus II Design Flow

For the designer, implementing functions in the dedicated DSP block does not differ from the normal LeonardoSpectrum design flow (see Figure 1). You can enter the RTL code, select the Stratix device as the target architecture, assign design constraints, synthesize, and output a structural netlist for place-and-route. The LeonardoSpectrum software and the structural EDIF netlist output a tool command language (**.tcl**) file used to set up an Altera Quartus® II project with the design constraints entered in the LeonardoSpectrum software.

Figure 1. LeonardoSpectrum & Quartus II Design Flow



Inferring DSP Functions

The LeonardoSpectrum tool infers three types of megafunctions: `lpm_mult`, `altmult_accum`, and `altmult_add`.

LeonardoSpectrum infers the `lpm_mult` for multiplier functions (see code below).

Verilog:

```
always @(posedge clk) begin
        a = b × c ;
end
```

To infer the `altmult_add` function, the result must come from the addition or subtraction of two multiplier functions. To infer the `altmult_accum` function, the result must come from the accumulation of two multiplier functions with the same source. You cannot use the accumulator/adder block without the multiplier block. Figure 2 shows an example construct that will infer `altmult_accum` and `altmult_add` MAC functions.

Instantiating Altera Megafunctions for DSP Blocks

With the LeonardoSpectrum software, you can include a library of parameterized modules (LPM) function in synthesis or have synthesis treat the LPM function as a black box.

With VHDL, you can choose to include an LPM function in the synthesis or just instantiate an empty component for synthesis to treat the function as a black box. To include the function in the synthesis, a generic value declaring the LPM type must be present.

If you do not add the LPM type generic, the Quartus II software will not be able to recognize the LPM function since the LeonardoSpectrum software will change the instance name to reflect the generic type.

Figure 2. Example Construct

```
ALTMULT_ADD:
Verilog:
    wire [35:0] multa = DATAAX × DATAAY;
    wire [35:0] multb = DATABX × DATABY;
    reg  [35:0] DATAOUT;

    always @(posedge clk) begin
          if (ADDnSUB)begin
                DATAOUT <= multa + multb;
          end
          else begin
                DATAOUT <= multa - multb;
          end
    end

ALTMULT_ACCUM:
reg  [31:0] dataout;
wire [15:0] multa;
wire  [31:0] adder_out;

assign multa = data × dataout;
assign adder_out = multa + dataout;

always @(posedge clk or posedge aclr)
begin
          if(altr)
          begin
               dataout <=0;
          end

          else if(clken)
          begin
               dataout <=adder_out;
          end
end
```

Conclusion

The LeonardoSpectrum software provides support for the advanced features of Stratix devices. This support enables easy design, debugging, and optimization of complex systems such as DSP applications. Along with the place-and-route capability of the Quartus II software, the LeonardoSpectrum tool provides excellent quality of results for programmable logic designers.

Synplicity's Advanced Support for Stratix Devices

by Steve Pereira,
Technical Marketing Manager,
Synplicity

With the recent release of Altera's new Stratix™ device family, the need for high-performance, fast synthesis is a definite requirement. Synplicity® engineers are working diligently with Altera to produce outstanding results for Stratix devices with the Synplify® and Synplify Pro® programmable logic device (PLD) synthesis software.

Stratix devices have dedicated digital signal processing (DSP) blocks that you can configure as multipliers, multiplier adders, or multiplier accumulators.

Several Stratix features will ensure that performance needs will be met. This article will discuss how the Synplify Pro software provides you with an exceptional synthesis solution using enhanced support for the ALTSYNCRAM megafunction and the Stratix digital signal processing (DSP) blocks.

Synplify Pro Software DSP Block Support

Stratix devices have dedicated DSP blocks that you can configure as multipliers, multiplier-adders, or multiplier-accumulators. The Synplify Pro synthesis software is ideal for DSP-type applications because it is able to extract and perform true timing-driven synthesis on mathematical functions. The DSP blocks are specified in the Verilog Quartus Mapping (**.vqm**) netlist file through the Altera® `altmult_add`, `altmult_accum`, and `lpm_mult` megafunctions. Structural VHDL and Verilog HDL simulation netlists also return these functions. The Altera Quartus® II software then maps these functions directly into the DSP blocks. Each DSP block consists of four 18-bit multipliers feeding into two-level adders. Depending on the device, the number of DSP blocks varies between 6 and 28. Both inputs are rounded up to the next highest multiple of 9 and the larger of the two is taken as the size of the multiplier. Unused most significant bits (MSBs) are automatically set to zero (sign extended).

Multiply Only Mode in DSP Blocks

The Synplify Pro software automatically recognizes and extracts multipliers through the `lpm_mult` megafunction. This function is inferred under three situations.

- One 36 × 36-bit multiplier, i.e., `x = a * b`
- Four independent 18 × 18 multipliers (less than or equal to 18-bit inputs), i.e., `x1 = a1 * b1, x2 = a2 * b2, x3 = a3 * b3, x4 = a4 * b4`
- Eight independent 9 × 9 multipliers (less than or equal to 9-bit inputs), i.e., `x = a * b`

The Synplify Pro software automatically selects the best operation mode for the DSP block. The width of `a` or `b` can be between 1 and 36.

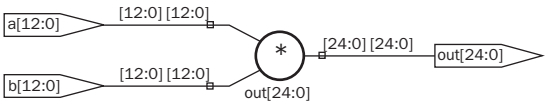
Figure 1 shows an example of a multiplier/adder combination and the output results from the Synplify Pro software.

Figure 1. Multiplier/Adder Combination

The following code maps to an `lpm_mult` megafunction generating one multiplier:

```
'define W 12
module mult4(out, a, b);
        output ['W*2:0] out;
        input ['W:0] a, b;
        assign out = a*b;
endmodule
```

This code produces the following implementation in the Synplify Pro HDL Analyst® software viewer:



Multiply-Add Mode in DSP Blocks

The Synplify Pro software automatically recognizes and extracts multiplier/adder combinations through the `altmult_add` megafunction. Both one- and two-level adders are supported. This function is inferred under two situations.

- Two 18 × 18-bit multipliers with an adder (less than or equal to 18-bit inputs), `x = a * b + c * d` (one-level adder)
- Four 18 × 18-bit multipliers with two level adder/subtractor followed by an adder,
  `x =(a * b + c * d)+(e * f + g * h)` (two-level adder)
  `x =(a * b - c * d)+(e * f + g * h)`
  `x =(a * b - c * d)+(e * f - g * h)`
  `x =(a * b + c * d)+(e * f - g * h)`

Performing DSP functions with the dedicated DSP block can significantly increase performance while decreasing debugging time.

You can register the input and outputs of the multipliers of the `altmult_add` function; you can also register the output of the final adder. These three registers can be brought into the DSP block.

Multiplier-Accumulator (MAC) Mode in DSP Blocks

The Synplify Pro software automatically recognizes and extracts the `altmult_accum` megafunction. This function is inferred under one situation:

`x = x + a × b` or `x = x - a × b`
(One multiplier with accumulator)

The size of inputs `a` and `b` must be between 4 and 18, and `x` is between 8 and 52.

Synplify Pro Software's Advanced Feature Support

Stratix devices incorporate the next generation of single- and dual-port RAM. The `altsyncram` megafunction supports ROM, single-port RAM, simple dual-port RAM, and true dual-port RAM. The Synplify software recognizes and extracts these new ROM and RAM modules and passes the optimized netlist through to the Quartus II software.

Attribute Support

Table 1 shows the user attributes for DSP inferencing that the Synplify Pro software recognizes.

Performing DSP functions with the dedicated DSP block has significantly increased performance while decreasing debugging time.

Table 1. Attribute Support

Attribute	Description
`syn_useioff`	Registers with these attributes will not be packed into DSP blocks.
`syn_preserve`	Registers with these attributes will not be packed into DSP blocks.
`syn_keep`	A `syn_keep` between the adder and multiplier prevents inferencing of `altmult_add` and `altmult_accum`, but not plain multipliers.
`syn_multstyle`	A multiplier with the attribute value "logic" will map to logic.

Conclusion

Altera's new Stratix devices are reaching performance and capacity points that are enabling designers to implement entirely new types of applications with programmable logic. Together, Synplicity and Altera are making it easy for designers to quickly reach aggressive performance goals, thereby bringing leading-edge electronics products to market on time.

Customer *Application*

Mercury Devices Enable Echotek's Software-Defined Radio

by Tom Winstead,
EnVision LLC

Echotek Corporation, located in Huntsville, Alabama, specializes in high-performance, high-speed data I/O products used in RADAR, digital radio, signal intelligence, and other data-acquisition applications. Echotek was incorporated in 1987 to address the needs of classified government programs, and their very first products contained Altera® programmable logic devices (PLDs). Echotek continues to use the fastest, largest Altera devices available in nearly every design.

After a few years of government programs, Echotek took their RADAR-centric, high-bandwidth products and ported the analog-to-digital (A/D) converters, intermediate-frequency portions, and receivers to conventional computer bus systems (primarily VME bus). These products are now used in many wideband applications, including commercial radar, magnetic resonance imaging (MRI), and digital imaging.

As the communications industry increased bandwidth, Echotek also found a natural fit in the signal intelligence area. A large portion of Echotek's products go into the communications industry, taking advantage of receiver products easily adaptable to applications on the receiver side of the digital radio. In this market segment, Echotek became involved in an effort to develop software-defined radio systems, which are designed to go beyond the limitations of existing and developing wireless standards by relying on a platform-neutral, multi-band, multi-protocol, configurable environment for commercial, government, and military applications. For example, software-defined radio systems can provide communication between various forces and/or agencies in times of war, allowing multiple groups (i.e., rescue, police, military, international) to communicate on a variety of hardware platforms.

Company:
Echotek Corporation

Industry:
High-Speed Data I/O Products

End Product:
Wideband Digital Transmitter/ Receiver

Altera Products:
Mercury EP1M350 & FLEX EPF10K50E Devices

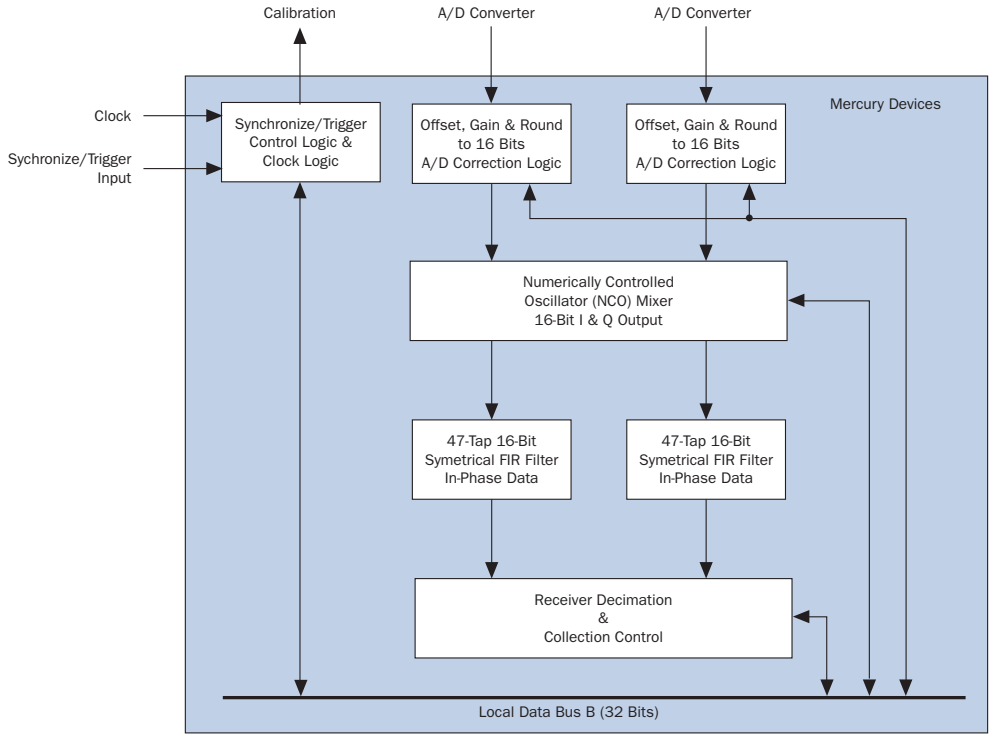
Echotek Uses Mercury Devices to Achieve DSP Performance Goals

Echotek's approach to designing their software-designed radio system was an extension of their legacy products, intellectual property (IP), and PLD expertise, but the software-defined radio program required a minimum of 50% more processing power than their previous designs. Since this program required an implementation on two system boards approximately five inches square, including the analog and high-speed digital sections, board real estate was a major concern. This implementation required a speed of 125 MHz in both directions, nearly three times the bandwidth achievable with commercially available digital signal processing (DSP) ASICs or ASSPs. Echotek's President, Ralph Kimball, decided that the best approach was to employ Altera Mercury™ devices to achieve the needed bandwidth.

Echotek evaluated Mercury devices using the Altera Quartus® II software, and concluded that they would easily meet their target performance. To ensure a comfortable performance margin, Echotek set as a target to meet their speed requirements the slowest Mercury device scheduled for release.

To help achieve the required performance, Echotek selected a new family of pre-release, high-performance A/D converters. Echotek's software-defined radio design uses the Mercury LVDS I/O interface for the A/D interface to achieve speed, noise, and power advantages. The LVDS channels feed four interleaved high-speed numerically controlled oscillators (NCOs) inside the Mercury device, generating 500 MHz I and Q channels. Each NCO runs at 125 MHz, or 2.5 times faster than the fastest commercially available NCO device. The I and Q channels are then filtered through a decimate by four, 125 MHz, 16-bit, 47-tap finite impulse response (FIR) filter, twice as fast as the fastest commercially available ASSP. The Mercury device multiplier mode helped achieve this performance, and the quad-port memory structure accommodated adaptive coefficients, key to implementing the software-defined radio

Figure 1. Block Diagram



"We wouldn't have been able to accomplish this project without Altera's Mercury devices. We needed 16-bit, 47-tap FIR filters running twice as fast as the fastest commercially available ASSP, and Mercury devices delivered," said Ralph Kimball, President of Echotek.

design. Multiplication speed is critical to successful software-defined radio applications and is often the limiting factor in NCO and FIR designs, but Echotek's tests show that Mercury devices can run 16 × 16 multipliers operating at above 300 MHz.

Mercury Devices Meet Performance Goals

Mercury devices met Echotek's performance goals on delivery. Echotek easily exceeded their minimum requirements; the system is capable of running at over 150 MHz in standard speed grades. The implementation uses four Mercury EP1M350 devices, which fit on the 5-inch square board along with three FLEX® 10KE EPF10K50E devices (for the dual high-speed Raceway interfaces) and other components. Implementing this system in such a small platform was a staggering accomplishment, considering that they provided the processing power that would have required several full-size VME boards just a few years ago.

As an early Altera adopter, Echotek is enjoying the benefits of spending a year and a half with the early releases of the Quartus software, as well as a successful transition to the Quartus II software. They have seen improvements across the board, from ease-of-use to shorter compile times to dramatic performance increases from the APEX™ 20K devices. By using the APEX II and Mercury device families, the Quartus II software, and IP cores such as Cordic and Arctan functions, FIR filters, NCOs, fast Fourier transform (FFT), and peripheral component interconnect (PCI) cores, Echotek remains focused on producing the best and fastest products in their field, and remaining on the leading edge of performance.

"We wouldn't have been able to accomplish this project without Altera's Mercury devices. We needed 16-bit, 47-tap FIR filters running twice as fast as the fastest commercially available ASSP, and Mercury devices delivered," said Ralph Kimball, President of Echotek.

Interfacing to External Memories Using Stratix Devices

With this external interface support, Stratix devices are easily connected to a wide range of the latest memory devices from leading vendors such as Micron Technology, Integrated Device Technology, and Cypress Semiconductor.

Due to the rapid escalation of bandwidth in modern-day systems, the need for high-speed memory to buffer signals has never been higher. Stratix™ devices address this bandwidth requirement by providing abundant on-chip memory resources using the TriMatrix™ memory structure and enabling high-speed support for external memory interfaces for additional off-chip data storage.

With this external interface support, Stratix devices are easily connected to a wide range of the latest memory devices from leading vendors such as Micron Technology, Integrated Device Technology, and Cypress Semiconductor. With a comprehensive, industry-leading solution, high-density memory devices are integrated into complex system designs without degrading data access performance or increasing development time. Furthermore, Stratix devices are designed to keep up with the proliferation of memory device types, each using different interface standards and protocols at varying transfer rates. Table 1 illustrates the rates at which Stratix devices can communicate with the industry's most advanced memory devices.

Table 1. Stratix Communication with Memory Devices

External Memory Device	Maximum Data Transfer Rate (Mbps)	Memory Clock Speed (MHz)
SDR SDRAM *(1)*	200	200
DDR SDRAM *(2)*	400	200
DDR FCRAM	400	200
ZBT SRAM *(3)*	200	200
QDR SRAM *(4)*	668	167
QDRII SRAM	668	167

Notes to Table 1:
(1) SDR: single data rate.
(2) DDR: double data rate.
(3) ZBT: zero-bus turnaround.
(4) QDR: quad data rate.

Architectural Features

Stratix devices contain the following individual I/O features specifically designed to aid in the implementation of external memory interfaces:

- Multi-register input/output elements (IOEs)
- Programmable input delays
- Programmable ZBT delay
- Dedicated data strobe (DQS) circuitry
- Positive-edge alignment circuitry

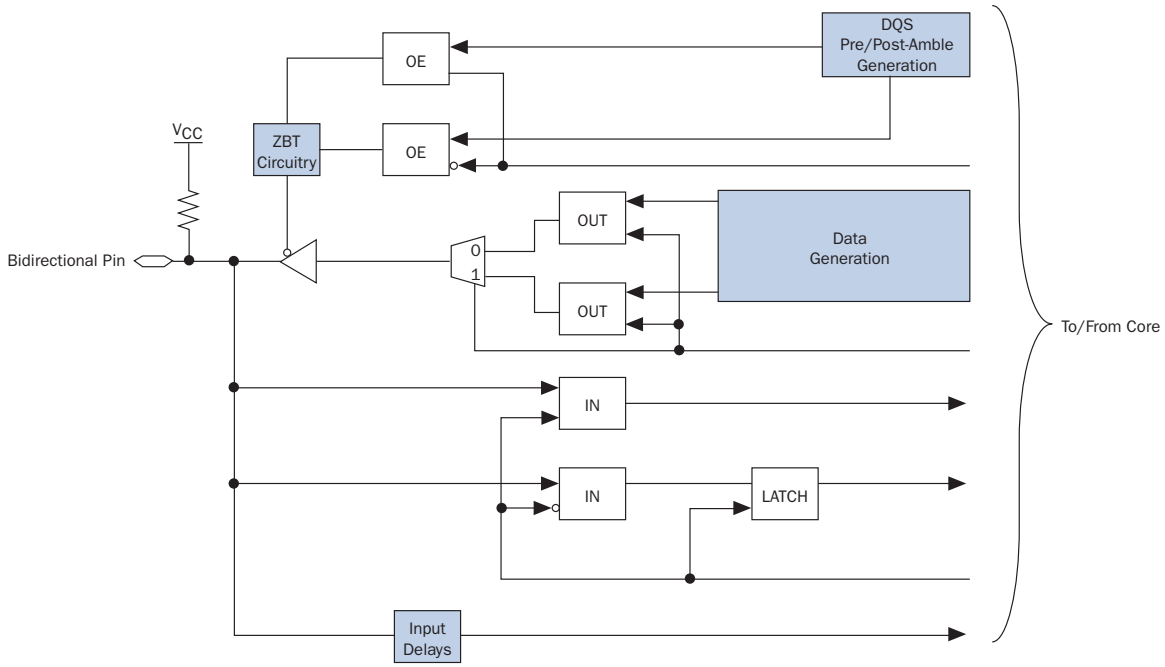
I/O Elements

Every Stratix IOE features six registers and a latch, as shown in Figure 1 on page 29. You can use the input registers to capture DDR inputs on the rising and falling edges of the clock. The latch holds the bit captured on the negative-edge triggered input register and sends it into the core on the same clock cycle as the bit captured on the positive-edge triggered register, thereby ensuring a positive-edge interface with the core. Similarly, for DDR outputs, both output registers interface with the core on the clock's positive edge. The falling-edge output at the pin is then generated by toggling the output multiplexer. Additional features in the IOE enhance support for ZBT and DDR memory interfaces.

Timing-Optimized Data & Data Strobe Pins

To increase data transfer rates, data strobe signals are driven into external memory devices along with regular data lines. This process ensures that data is captured within the data valid window and accounts for changes in temperature, voltage, or loading. To further enhance interfacing with DDR FCRAM and SDRAM memory devices, Stratix devices also feature two banks of optimized data (DQ) with corresponding data strobe (DQS) pins, as shown in Figure 2. Each DQS pin drives at least eight DQ pins in up to 20 groups on each device through a dedicated, balanced clock tree. The DQS pins are timing-optimized for a 90° or 72° phase shift, as specified by the user in the Altera® Quartus® II software.

Figure 1. Stratix IOE Block Diagram

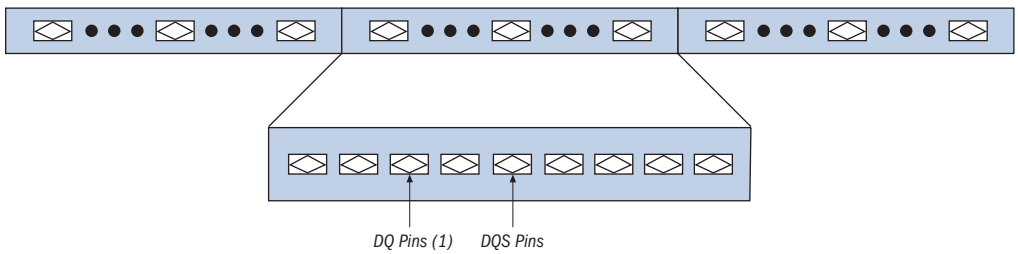


Intellectual Property

Altera offers fully customizable intellectual property (IP) memory controller functions developed and tested by Altera and Altera Megafunction Partners Program (AMPP℠) partners, available at the IP MegaStore™ web site. These functions include DDR SDRAM, SDR SDRAM, and DDR FCRAM controllers. Furthermore, Altera offers several memory controller design examples for users designing their own custom memory interfaces. If you use QDR and ZBT SRAM devices, you can download royalty-free reference designs from the Altera web site. These megafunctions allow you to quickly and easily incorporate the latest semiconductor memory technologies into your Stratix designs using an intuitive graphical user interface from within the Quartus II software.

This combination of dedicated circuitry and optimized IP ensures a seamless interface with high-speed external memory devices. When combined with the TriMatrix memory capability, Stratix devices provide a complete memory solution for systems on a programmable chip (SOPC).

Figure 2. Stratix Top or Bottom I/O Bank *Note (1)*



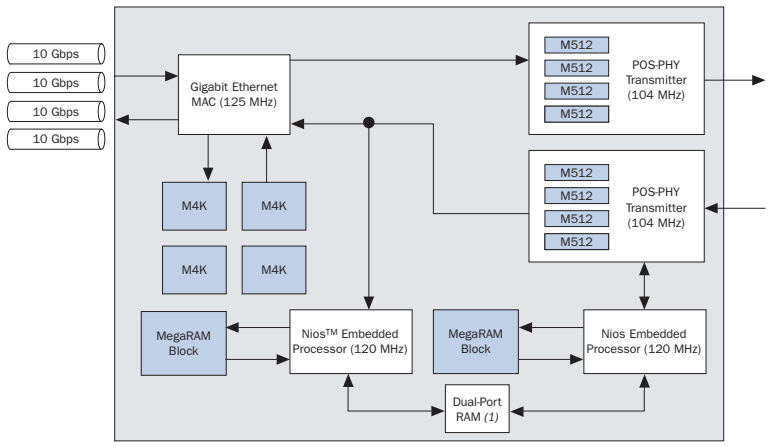
Note to Figure 2:
(1) In each I/O bank, there are at least eight DQ pins per group.

Stratix Devices Provide the Solution for High-Bandwidth Memory Architecture in PLDs

One of the challenges engineers designing communications equipment face is that memory devices were adopted from PC computer platforms. These devices, although inexpensive and easy to source, are suboptimal for communication systems because they were designed with a different end system in mind. SDRAM memory is a good example of a PC technology that was transferred by economies of scale into the communications world. Fundamentally, SDRAM memory was designed with storage for microprocessors in mind—not to accept TCP/IP packets travelling at 10 gigabits per second (Gbps) through high-performance switching equipment.

Although discrete memory suppliers introduced new architectures with increased bandwidth such as double data rate (DDR), zero-bus turnaround (ZBT), and quad data rate (QDR), they have not kept pace with the performance demands of transmission media standards such as OC-48 and OC-192. Since these discrete devices formerly were the only source of system memory, they defined the bottleneck in the system under design.

Figure 1. New Role of Embedded Memory Structures on PLDs in Communications Equipment



Note to Figure 1:
(1) M4K, M512, and MegaRAM blocks support dual-port RAM mode.

As an alternative to discrete memory devices, the industry adapted by developing sophisticated memory structures embedded within programmable logic devices (PLDs). Over the last several years, the complexity of memory structures in programmable logic devices has increased to the point of parity with many system ASIC designs, including application-optimized features such as dual-port, mixed-width, and parity bits.

The latest generation of high-bandwidth, multi-functional memory architectures available in programmable logic supports higher system speeds than the discrete memory devices that are available today. Furthermore, there are significant performance, time-to-market, and cost advantages associated with embedded memory in a multi-million gate programmable fabric. Figure 1 shows how embedded memory structures on PLDs can increase system performance by supporting various functions. Figure 1 also illustrates that although system bandwidth may be 40 Gbps, the memory bandwidth required to support clock domain translation may be significantly beyond that because each clock domain transaction is a memory transaction.

In its next-generation Stratix™ family of high-density PLDs, Altera has introduced the TriMatrix™ memory structure, a technology that bridges the expanding gap between the memory bandwidth requirements of emerging transmission and processing technologies, and what is currently available in discrete memory devices.

The TriMatrix memory structure consists of an array of three different-sized embedded RAM blocks:

- M512 (512 bits + parity)
- M4K (4 Kbits + parity)
- MegaRAM™ blocks (512 Kbits + parity)

You can configure these feature-rich memory resources to support a wide range of applications. The TriMatrix memory structure

in Stratix devices offers up to 10 Mbits of RAM and up to 12 terabits per second peak device memory bandwidth, which makes this family an ideal choice for memory-intensive applications. You can use the smaller M512 blocks of RAM for first-in first-out (FIFO) applications, the medium size M4K blocks for channelized functions (a channelized function consolidates smaller channels into a larger channel), and the large MegaRAM blocks with 512K bits of RAM for network processor cache.

High memory bandwidth is required at the intersection of microprocessor, memory, and transmission technologies, which is the programmable logic device.

One important metric for evaluating a memory architecture is its peak memory bandwidth. The peak memory bandwidth defines the upper limit of a device's capability to move data through memory.

To calculate the peak memory bandwidth of Stratix devices, assume that each TriMatrix memory block is at maximum clock frequency and in simple dual-port mode (simultaneous reads and writes are possible). The calculation used to determine the peak memory bandwidth in each memory block is as follows:

(maximum achievable frequency × maximum configurable bitwidth)/(number of clock cycles to write a word) × (number of write ports)

The calculation used to determine the peak memory bandwidth in each Stratix device is as follows:

(Peak bandwidth of M512 blocks × number of M512 blocks on device) + (peak bandwidth of M4K blocks × number of M512 blocks on device) + (peak bandwidth of the MegaRAM block × number of M512 blocks on device)

This formula calculates the memory architecture's bandwidth within the device. The calculation also assumes that the number of ports on each block type is in its default state (no special techniques for increasing number of ports are being utilized). See Tables 1 and 2.

Table 1. Peak Memory Bandwidth by Block Type

Block Type	Peak Memory Bandwidth per DSP Block
M512	6 Gbps
M4K	11 Gbps
MegaRAM	43 Gbps

Table 2. Peak Memory Bandwidth by Stratix Device

Device	M512 Resources	M4K Resources	MegaRAM Resources	Peak Memory Bandwidth
EP1S10	95	60	1	1 terabit per second
EP1S20	194	82	2	2 terabits per second
EP1S25	224	138	2	3 terabits per second
EP1S30	295	171	4	4 terabits per second
EP1S40	384	183	4	4 terabits per second
EP1S60	574	292	6	7 terabits per second
EP1S80	767	364	8	9 terabits per second
EP1S120	1,118	520	12	12 terabits per second

The PLD must manage the speeds of the packets and buffer them while the microprocessor and off-chip memories prepare themselves for more data. This management must occur on the device that has the I/O capabilities and that device must have enough wide memories to store the packets and manage them. For more information on Stratix I/O capabilities, see *Application Note 202 (Using High-Speed Differential I/O Interfaces in Stratix Devices)*.

Conclusion

Emerging technologies in PLDs, such as the TriMatrix memory architecture, address the need of next-generation communications systems. By incorporating high-density memory structures into devices with the I/O capabilities to receive and transmit data at high rates, Stratix devices are well suited for communications system designs.

Resolving Clock Management Issues Using Stratix Devices

As high-density PLDs incorporate more functions to avoid bottlenecks associated with board-level chip-to-chip communication, on-chip clock distribution becomes significantly important to the speed, integrity, and performance of the designs implemented in these devices.

Today's complex products feature high-speed signals that introduce various timing problems. It is difficult to detect and fix all board-level timing issues given the increasingly shorter design cycles and expedited production timelines. The issues associated with high-speed designs are forcing designers to alter their design approaches. These issues are typical of designs where high-speed clocks are generated from multiple sources and cross long interconnects to reach their destinations. Altera's new Stratix™ devices can address these issues by generating multiple clocks and managing them so that they satisfy the requirements of the system regardless of voltage, temperature, and process variations.

To increase continuously the clock frequency and maintain the integrity of the data transmitted, the transmitter must send a clock with the data (source-synchronous clocking). Source-synchronous design is gaining popularity because it simplifies timing relationships, allowing the designer to focus on the functionality of the circuits. The only performance concerns with source-synchronous designs are maximum clock frequency and input and output timing.

There are three main points of consideration when discussing clock management circuits: clock frequency, skew, and jitter.

One approach is to design systems that perform operations at very high speeds, but communicate with other devices at lower data rates. It is usually possible to increase the internal clock frequency of the integrated circuit (IC) by including a clock frequency multiplier such as a phase-locked loop (PLL) on-board. This technique is used in Stratix devices and allows the internal logic of the programmable logic device (PLD) to run at very high clock frequencies relative to the board clock frequency. In addition to up to 40 unique clock domains within the device, the Stratix device family offers up to 12 PLLs, which can be used to clock other devices on the board or for source-synchronous clocking. Therefore, Stratix PLLs provide designers with complete control of their clocks and system timing. Stratix PLLs also offer flexible system-level clock management that was only previously available in discrete PLL devices. Stratix PLLs meet and exceed the features offered by these high-end discrete devices, reducing the need for other timing devices in the system.

As high-density PLDs incorporate more functions to avoid bottlenecks associated with board-level chip-to-chip communication, on-chip clock distribution becomes significantly important to the speed, integrity, and performance of the designs implemented in these devices.

PLLs minimize skew and delay across the device. Also, you can operate Stratix PLLs in zero delay buffer (ZDB) mode so that the output clock from the PLL is exactly in phase with the input clock to the PLL. You can use Stratix PLLs in external feedback mode so that the feedback input pin is phase aligned with the clock input pin. By aligning these clocks, you can actively remove clock delay and skew between devices. The PLL also has the ability to multiply the incoming clock to the PLD, which allows the board-level clock to remain at low frequencies, which in turn reduces the probability of electromagnetic interference (EMI).

PLLs are used as an industry-standard circuit to achieve frequency synthesis and filter the extrinsic jitter. Stratix PLLs offer the programmable bandwidth feature that allows customization of PLL characteristics to better serve the end application. A "low" bandwidth setting filters out the high-frequency jitter whereas a "high" bandwidth setting allows the PLL to track high-frequency jitter.

PLLs use several divide counters and delay elements to perform frequency synthesis and phase shift functions. In Stratix PLLs, these counters and delay elements are configurable in real-time. User control of these PLL components allows output frequency and clock delay variation in real time, without the need to reconfigure the entire PLD.

The PLL reconfiguration feature is useful in applications that might operate at different frequencies. It is also useful in prototyping environments where you could easily sweep PLL output frequencies and adjust clock delay. For example, a system generating test patterns might be required to generate and transmit patterns at 50 or 100 MHz, depending on the unit under test. Real-time reconfiguration of PLL components allows you to switch between two such output frequencies within 20 µs. You can also use this feature to adjust clock-to-output (t_{co}) delays in real time by changing the output clock delay. This approach eliminates the need to regenerate a programming file with the new PLL settings.

Once these clock management issues are resolved, the next step is to build a reliable system that runs consistently. To ensure reliability, it is helpful to build redundancy into the system so that it always receives a clock. Clock switchover is a feature that allows the PLL to switch between two reference input clocks. You can use PLL switchover for clock redundancy or for a dual-clock domain application. You can use this Stratix PLL feature to develop a reliable system where the redundant clock can be switched on if the primary clock stops running for any reason. When the clock is no longer toggling or based on a user control signal, you can automatically perform clock switchover.

Today's digital clocks are generally square waves with short rise times. With these high-speed digital clocks, a significant amount of energy is concentrated in a narrow bandwidth at the target frequency and at the higher frequency harmonics. This concentration results in high-energy peaks, which lead to elevated EMI emissions. The radiated noise from the energy peaks, if not minimized, can lead to corrupted data and intermittent system errors, which can jeopardize system reliability. Not only could there be malfunctions within your own system, but excessive EMI causes interference with other electronic devices. For these reasons, regulatory agencies such as the Federal Communications Commission (FCC) set and enforce acceptable EMI emission levels. These agencies also test for the amount of peak energy radiated from electronic equipment. To comply with these regulations, designers have investigated various methods to either contain or reduce EMI emissions.

Traditional methods for limiting EMI include shielding, filtering, and multi-layer printed circuit boards (PCBs). However, sometimes these methods are not enough to meet EMI compliance. Spread-spectrum technology gives you a simple and very effective technique to reduce EMI emissions without the added cost or trouble of redesigning a board.

Stratix PLLs are equipped with spread spectrum technology to help reduce the EMI emitted from the device. The PLL provides up to a 0.5% down spread modulation.

Spread spectrum modulates the target frequency over a small range. Instead of concentrating the energy at the target frequency, the energy is redistributed across a wider band of frequencies. Spreading this energy over a range of frequencies results in a reduction of peak energy. Not only is there a reduction in the peak EMI, but there is an even greater reduction in EMI of the higher order harmonics. Because FCC regulations focus on peak EMI emissions and not average EMI emissions, spread-spectrum technology is a valuable method to meet FCC requirements.

Stratix PLLs are equipped with spread-spectrum technology to help reduce the EMI emitted from the device. The PLL provides up to a 0.5% down spread modulation.

Conclusion

With up to 12 PLLs and 40 unique system clocks per device, Stratix devices are built to function as the central clock manager to meet system timing challenges. Stratix devices are the first PLDs to offer on-chip PLL features previously found only in high-end discrete PLL devices. Stratix devices also offer PLL reconfiguration, allowing you to change the PLL configuration without reprogramming the entire device. Stratix PLLs increase system and device performance and provide advanced clock interfacing and clock-frequency synthesis.

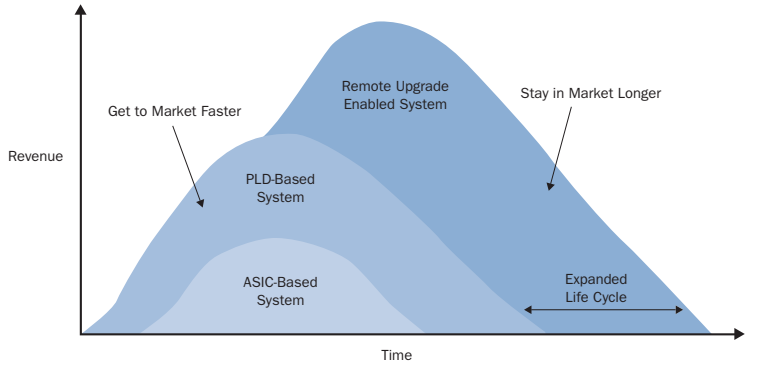
Remote System Upgrades with New Stratix Devices

As competitors battle for the same market share increases, the significance of being first-to-market is greater than ever. However, amid constant changes in market demands and emerging protocols there is a risk in introducing a product too early, rendering such systems obsolete within months. The remote system upgrade capability, featured in Altera's new Stratix™ devices, provides the ideal solution for these situations by allowing an in-place system upgrade from a remote location.

Programmable logic devices (PLDs) historically provide designers with a faster time-to-market option compared to ASICs. Remote system upgrades in Stratix devices allows designers to get their product to market even faster, to keep the product in the market longer, and to reduce future system costs. This feature is supported by dedicated circuitry built into the Stratix devices, including an error recovery module that ensures safe deployment of remote upgrades. Remote system upgrades let you keep your system-on-a-programmable-chip (SOPC) designs ahead of the competition more easily.

This article introduces the advantages of Stratix remote system upgrades and illustrates how you can quickly and efficiently implement this exciting new feature.

Figure 1. Remote System Upgrades with Stratix Devices



The Benefits of Remote System Upgrades

Remote system upgrades take the concept of re-programmable systems to a higher level. In the past, designers could only upgrade a system's software, but now they can upgrade both hardware and software remotely with greater design flexibility.

Fastest Time-to-Market

To maximize the full potential revenue of a product, it is imperative to get to market as soon as possible to secure the biggest market share possible. With the ability to remotely update a remote system upgrade-enabled system at anytime, you can ship a working subset of your system to enter the market in the shortest amount of time. This quick market entry allows you to take full advantage of the window of opportunity and reap the benefits of being first to market with your product, as seen in Figure 1.

Extend Marketplace Advantage

The remote system upgrade feature extends the life cycle of a product by allowing it to evolve with the market. In today's dynamic markets that welcome new advances in technology and emerging standards, a product that is cutting edge today can easily become obsolete in months. A system that is capable of evolving with the demands of the market can stave off obsolescence and extend its own revenue generation.

Bulletproof Remote Upgrades

Dedicated remote system upgrade circuitry, the first of its kind in the PLD industry, is built into the revolutionary Stratix device architecture to ensure correct system operation in case there are data transmission errors. Remote system upgrades to core system functionalities are deployed safely and reliably.

Implementing Remote System Upgrades

Dedicated Circuitry

Stratix devices feature dedicated circuitry to make designing for a remote system upgrade-enabled system simple and reliable. A series of remote system upgrade registers keep a record of updates that are received or programmed, the status of each update, and any errors that may have occurred, while the error recovery module ensures safe remote upgrades.

Components of Remote System Upgrade- Enabled System

The implementation of a remote system upgrade-enabled system consists of a Stratix device, memory, and a controller. As seen in Figure 2, the memory or configuration source can be any industry-standard flash memory, while the controller can be a microcontroller or other logic that handles the configuration data transmission. A remote system update occurs in three steps, as shown in Figure 3.

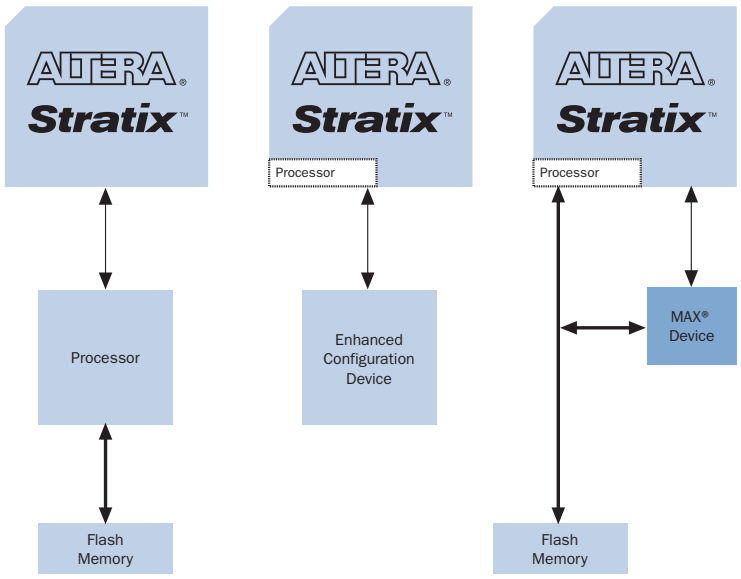
1. Send an update from the development location through any network to the Stratix device
2. Store the update in the memory
3. Update the Stratix device with the new data

For example, a complete remote system upgrade solution consists of a Stratix device with a Nios™ embedded processor and one of Altera's enhanced configuration devices. Since Altera provides a free software development kit that includes a remote system upgrade version of the Nios embedded processor, no other development systems are required.

Remote System Upgrades Enable State-of-the-Art Technology

Systems enabled by Stratix devices with the remote system upgrade capability are assured of the fastest possible time-to-market, helping you realize the maximum revenue benefits of being first to market. Future system upgrades can then be sent remotely, ensuring that the system meets the demands of the market and continues to generate revenue. Dedicated circuitry in Stratix devices provide you with peace-of-mind and unmatched ease of remote system upgrade implementation.

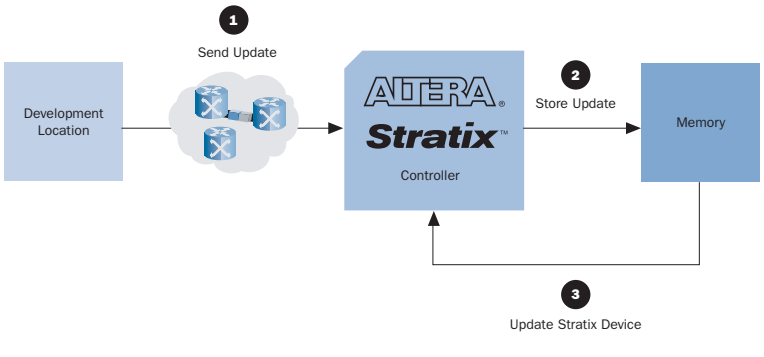
Figure 2. Options for Remote System Configuration



Conclusion

Realize the benefits of a remote system upgrades-enabled system and begin designing with Stratix devices. Stratix devices, Altera® Quartus® II software support, and the free remote system upgrade development kit are now available.

Figure 3. Steps to Remotely Upgrade Systems with a Stratix Device



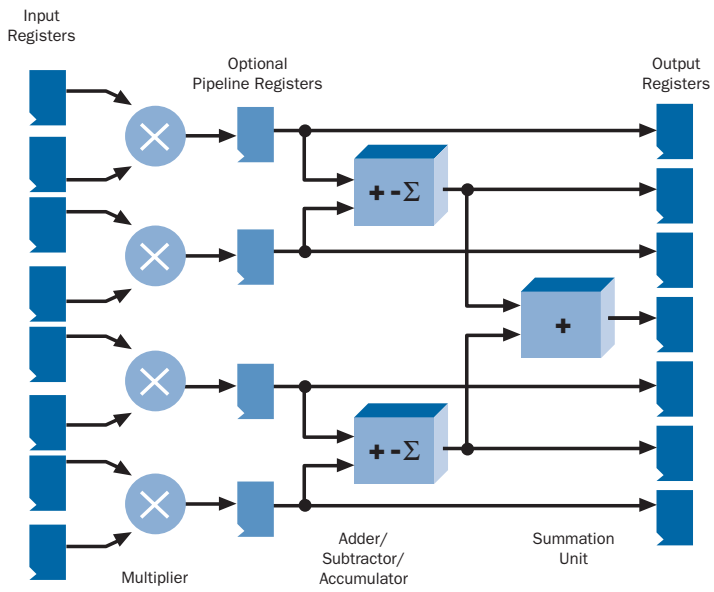
DSP Blocks in Stratix Devices Boost DSP Performance

The digital signal processing (DSP) blocks in Stratix™ devices are high-performance embedded DSP units that are optimized for applications such as rake receivers, voice over Internet protocol (VoIP) gateways, orthogonal frequency division multiplexing (OFDM) transceivers, image processing applications, and multimedia entertainment systems.

Stratix DSP blocks eliminate performance bottlenecks in DSP applications, provide predictable performance, and result in resource savings. This flexibility makes DSP blocks ideal for implementing complex DSP systems while providing high-data throughput at the same time.

Altera® Stratix devices use DSP blocks to achieve the high-data throughput necessary for computationally demanding applications. The DSP blocks in Stratix devices can run at 250 MHz to provide data throughput performance of up to 2.0 giga multiply-accumulate operations per second (GMACS) per DSP block. Additionally, the 28 DSP blocks of the largest Stratix device, the EP1S120 device, can provide a combined throughput of up to 56 GMACS—more than six times the data throughput available from leading digital signal processors.

Figure 1. DSP Block Architecture



DSP Block Architecture

Stratix DSP blocks consist of hardware multipliers, adders, subtractors, accumulators, and pipeline registers. Stratix DSP blocks provide optimal performance due to their dedicated circuitry, as shown in Figure 1.

Each DSP block is optimized for maximum performance of up to 2.0 GMACS per block with minimal routing congestion. Further, these DSP blocks are optimized to interface with the specialized memory structures in Stratix devices for memory-intensive DSP applications.

Each DSP block in a Stratix device can implement eight 9 × 9-bit multiplications, four 18 × 18-bit multiplications, or one 36 × 36-bit multiplication for different applications by choosing the appropriate DSP block operation mode in the Altera Quartus® II software. When configured in the 36 × 36 mode, the DSP block also performs floating-point arithmetic. The dedicated multiplier circuitry supports signed and unsigned multiplication operations, and dynamically switches between the two without any loss of precision.

You can configure the adder/subtractor/accumulator block as an adder, a subtractor, or as an accumulator, based on its operation mode. This block automatically switches between adder and subtractor functionality, acting as a 9-bit, 18-bit, or 36-bit adder as necessary. In accumulator mode, the unit acts as a 52-bit accumulator.

Higher DSP Performance than DSP Processors

Stratix devices offer higher data processing capacity than DSP processors and are more flexible and cost effective. Each Stratix device DSP block offers up to eight parallel multipliers that can run at 250 MHz and provide a data throughput of two GMACS per DSP block. The largest Stratix device, the EP1S120 device, offers 28 DSP blocks and can perform up to 224 parallel multiplication operations and provide a combined data throughput of 56 GMACS. Traditional DSP processors can perform only up to eight parallel multiplication operations and can provide only up to 8.8 GMACS. Figure 2 shows how Stratix devices can replace DSP processors in a high-performance communication system.

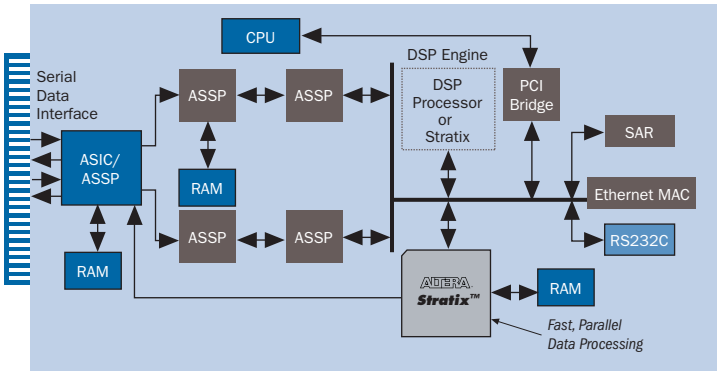
Further, with the availability of software tools such as the DSP Builder (an interface between the Quartus II software and MATLAB/Simulink), you can use Stratix devices for implementing entire DSP systems such as rake receivers and wideband code division multiple access (W-CDMA) transmitters. The DSP Builder combines the algorithm development, simulation, and verification capabilities of MathWorks MATLAB and Simulink system-level design tools with the HDL synthesis, simulation, and verification capabilities of the Quartus II software.

Using Logic Elements to Implement Multipliers

In addition to the dedicated multipliers inside the DSP blocks, you can implement multipliers and DSP functions in logic elements (LEs). For example, you can implement a 256-tap FIR filter using about 9,600 LEs in a Stratix device. The largest Stratix device, the EP1S120 device, which has about 114,140 LEs, can accommodate 11 such filters. Each filter would run at 200 MHz, which implies an overall device throughput of 563 GMACS arising from LE-based implementation. When combined with the 56 GMACS throughput from DSP blocks, Stratix devices offer 620 GMACS of data throughput.

Stratix devices provide higher performance, and are more efficient, flexible, and cost-effective than DSP processors. They offer the best alternative for system design needs while implementing DSP systems such as 3G wireless basestations, multimedia and VoIP applications, and image processing applications.

Figure 2. Stratix Device in a Communications Transceiver System

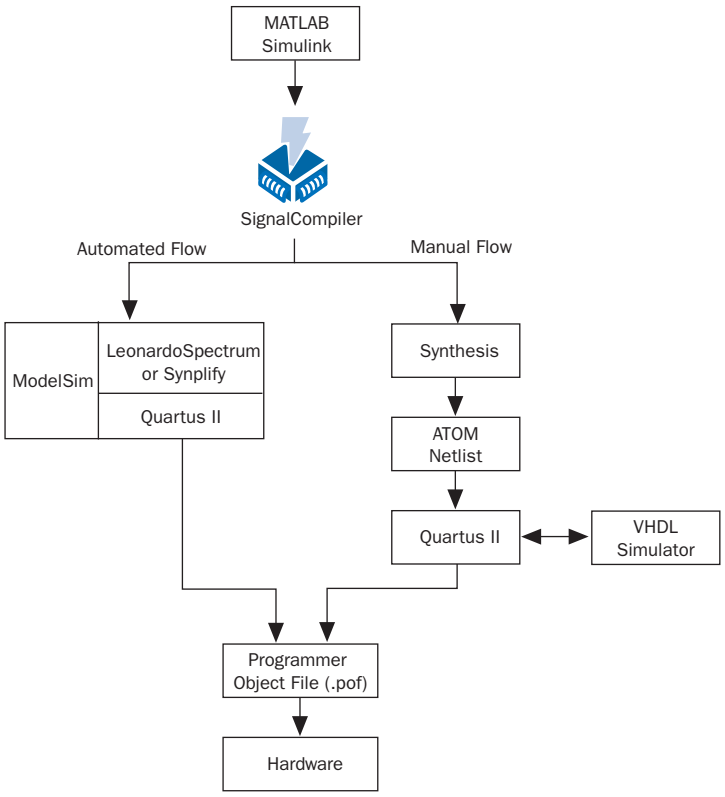


Altera Simplifies DSP Design with DSP Builder & Stratix Devices

By taking advantage of the new dedicated Stratix™ device digital signal processing (DSP) hardware circuitry at the system level, DSP Builder accelerates the design cycle of very high-speed data applications. Stratix DSP blocks offer higher data-processing capacity and are more flexible and cost-effective than discrete DSP processors.

The DSP Builder interfaces industry-leading, system-level design software with the Altera® Quartus® II software. The DSP Builder provides a seamless design flow, allowing DSP engineers to design algorithms in MATLAB, then enable system integration in Simulink, and port to hardware description language (HDL) for design in the Quartus II software. The DSP Builder enables users to harness the true capabilities of programmable logic for a variety of emerging high-performance DSP applications such as 3G base stations, local multi-point distribution service (LMDS), and multi-channel multi-point distribution services (MMDS). The DSP Builder provides a complete design environment in which users can go from system design to hardware implementation in a very short time period.

Figure 1. DSP Builder Design Flow



Using the DSP Builder, you can automatically generate a register transfer level (RTL) design and RTL testbench from Simulink. These pre-verified RTL output files are optimized for use in the Quartus II software for quick timing and simulation comparisons. The design flow also enables floating-point to fixed-point analysis.

This simple and intuitive development flow does not require extensive experience in designing with programmable logic design software. You can use the various intellectual property (IP) signal processing blocks provided with the DSP Builder to create a hardware implementation of a Simulink system model. The DSP Builder contains bit- and cycle-accurate Simulink fixed-point blocks, which cover basic operations such as arithmetic or storage functions as well as complex functions such as forward error correction, filtering, and modulation. Figure 1 shows the system-level design flow using the DSP Builder.

The DSP Builder consists of four key elements:

- SignalCompiler
- Primitive blockset
- DSP IP blockset
- DSP development board libraries

The SignalCompiler is the main component of the DSP Builder. It reads Simulink Model Files (**.mdl**) and generates VHDL files and tool command language (Tcl) scripts for synthesis, compilation, and simulation. Tcl scripts let you perform synthesis and compilation

automatically from within the MATLAB and Simulink environment.

The primitive blockset consist of four types of blocks: bus, arithmetic, storage, and gates. These libraries include basic building block functions such as adder-subtractors, gain, or product. The DSP IP blockset consists of complex functions such as FIR Compiler, Reed-Solomon Compiler, and Viterbi Decoder MegaCore® functions. All of these functions come with bit- and cycle-accurate C++ models.

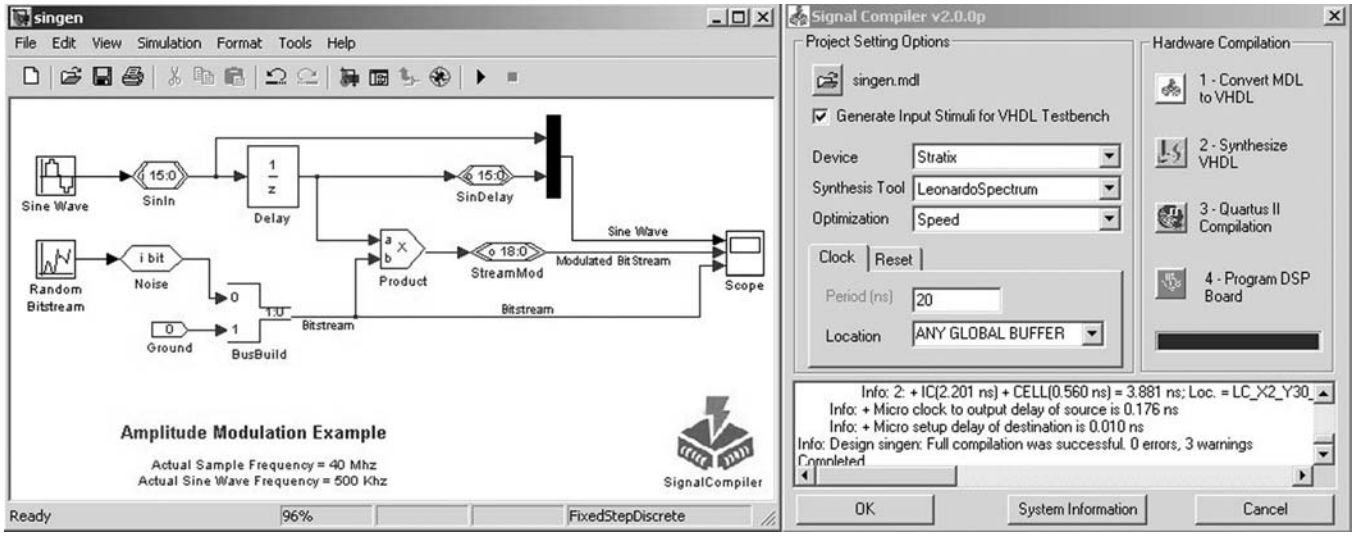
By integrating the various hardware features of the board such as switches, analog-to-digital (A/D) converters, and digital-to-analog (D/A) converters within the DSP Builder, you can rapidly prototype and test a design in hardware.

You can use the DSP Builder by creating a model in the MATLAB and Simulink environment and translating a floating-point algorithm into a fixed-point implementation by using functions from the provided blocksets. Figure 2 shows a simple amplitude modulation design in the Simulink environment and the resulting output as seen on a scope in the fixed-point domain. For more information about the DSP Builder, refer to the user guide.

The DSP Builder significantly reduces the overall design development time and enables designers to create high-performance DSP systems on programmable logic. DSP engineers with minimal programmable logic design experience can use the DSP Builder to develop their designs on PLDs.

With the availability of software tools such as the Altera DSP Builder, you can use Stratix devices to implement entire DSP systems such as rake receivers and wideband code division multiple access (W-CDMA) transmitters. The DSP Builder combines the algorithm development, simulation, and verification capabilities of MathWorks MATLAB and Simulink system-level design tools with the HDL synthesis, simulation, and verification capabilities of the Quartus II software. The combination of the DSP Builder software with the Stratix hardware brings DSP design to a higher level.

Figure 2. DSP Builder Translating Floating-Point Algorithm into Fixed-Point Implementation



Using Terminator Technology in Stratix Devices to Address System Design Challenges

An industry first, Terminator technology supports on-chip differential termination for the LVDS I/O standard.

To meet the requirements of today's high-performance, high-bandwidth systems, very high-speed data rate transfers are needed. At these speeds, maintaining signal integrity becomes increasingly critical. Termination is essential for reducing reflections and improving signal integrity for maximum system performance. To provide a clean signal, the designer needs to properly terminate both single-ended and differential signals by using on-board termination resistors. However, these resistors can take up significant board space. Also, as I/O pin counts for ball-grid array (BGA) packages increase, system designers must reduce external termination resistors in their design to save valuable board space.

Terminator™ technology in Stratix™ devices addresses these challenges by offering on-chip termination resistor technology that enables driver impedance matching and on-chip termination for serial, parallel, and differential signals.

An industry first, Terminator technology supports on-chip differential termination for the LVDS I/O standard. On-chip differential termination can be especially useful in system applications, requiring support for processor interface protocols, such as RapidIO, POS-PHY Level 4, SPI-4, SFI-4, 10-Gigabit Ethernet (XSBI), and CSIX streaming.

Terminator technology also supports on-chip series termination, where a resistor is placed in series with the output driver. You can use this termination when using SSTL-2 and SSTL-3 I/O standards while interfacing with double data rate (DDR) SDRAM and DDR FCRAM memories. In addition, you can use series termination resistors for output impedance matching in many general-purpose applications. In impedance matching, the impedance of the output driver is matched with the transmission-line impedance, resulting in improved signal integrity.

Additionally, you can use Terminator technology parallel termination when using HSTL I/O standards in system applications. HSTL I/O standards are used when interfacing with quad data rate (QDR) SRAM memories, network processors (CSIX L1), and 10-Gigabit Ethernet (XGMII) systems. When using the SSTL-2 and SSTL-3 I/O standards, on-chip parallel termination is useful when interfacing with DDR SDRAM and DDR FCRAM memories. You can also use on-chip parallel termination for backplane applications and processor interfaces which use GTL and GTL+ I/O standards.

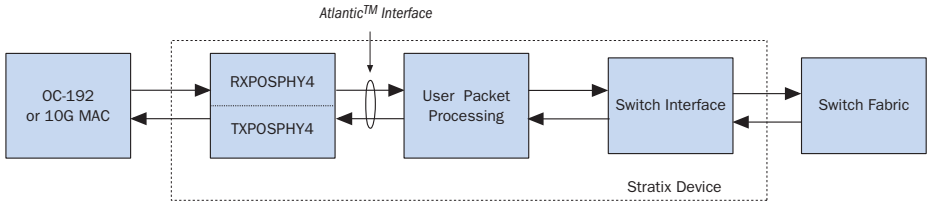
Differential Termination Simplifies POS-PHY Level 4 Interface

POS-PHY Level 4 interfaces cell and packet transfers between physical (PHY) and link layer devices. POS-PHY Level 4 enables 10-gigabits per second (Gbps) data rate transfers and is primarily used in OC-192 systems. The interface has a 16-bit data and 1-bit control bus that operates at 622 megabits per second (Mbps) on each LVDS channel to provide a 10-Gbps throughput. At these data rates, maintaining signal integrity is challenging. Putting the external termination resistor on the chip significantly simplifies this challenge by eliminating the reliability issues that arise with external resistors. Figure 1 shows a block diagram for a POS-PHY Level 4 interface.

Series Termination Simplifies Interface with DDR SDRAM Memories

DDR SDRAM memories are commonly used in low-cost applications requiring access to large amounts of memory at high speeds, such as digital access cards in voice over Internet protocol (VoIP) applications. The interface typically consists of a 72-bit data bus and uses the SSTL class II I/O standard at speeds of up to 200 MHz. The resistor network required to terminate all the lines in the interface consists

Figure 1. POS-PHY Level 4 Interface



of an extensive resistor network, which uses substantial board space and consumes valuable engineering resources to layout the board.

Terminator technology offers an excellent solution to these challenges. You can use the on-chip termination resistors to terminate the signals, thereby achieving the desired signal integrity while minimizing board space usage and engineering time. Figure 2 shows a physical DDR SDRAM interface.

Parallel Termination Simplifies interface with QDR SRAM Memories

To support the high-speed data throughput requirements of today's communication systems such as routers and asynchronous transfer mode (ATM) switches, QDR SRAM memories are especially useful because they provide up to four times the bandwidth as other static memories. The interface to the QDR SRAM requires a 36-bit data bus and uses the 1.5-V HSTL Class I I/O standard at speeds of up to 200 MHz. To maintain signal integrity on these data lines, each line must be properly terminated. Terminator technology on-chip parallel termination provides an ideal solution for this requirement. You can save valuable board space that would have been used by the termination resistors, while at the same time ensuring signal integrity. Figure 3 shows a block diagram for a QDR SRAM interface.

Figure 3. QDR SRAM Interface

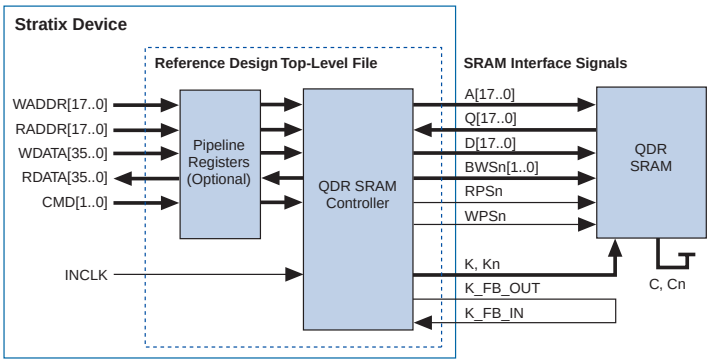
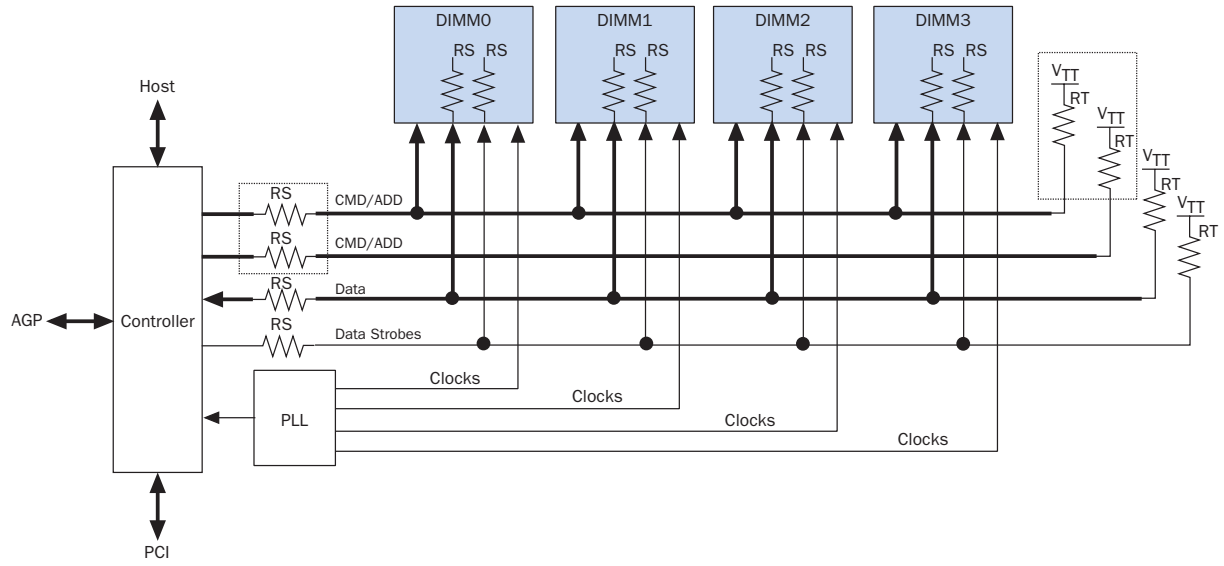


Figure 2. DDR PC266 PC Memory Subdivision



Stratix Devices Deliver the Features & Flexibility for High-Speed Interface Design

Altera continues its industry-leading support for high-speed differential I/O support with Stratix™ devices. The Stratix device family provides unprecedented high-speed differential I/O support with a maximum aggregate device bandwidth of up to 600 gigabits per second (Gbps). The source-synchronous differential signaling capabilities are ideal for interface bridging, backplanes, chip-to-chip communications, or other subsystems. Because of the large number of channels supported and the new differential signaling features, Stratix devices are designed to support up to four high-bandwidth interfaces such as the 10-Gigabit Ethernet XSBI, POS-PHY Level 4, HyperTransport™, RapidIO™, SPI-4, SFI-4, and UTOPIA IV standards in one device. The Stratix True-LVDS™ circuitry provides enhanced embedded serializer/deserializer (SERDES), multi-mode clocking, data realignment, on-chip termination resistors, and significantly more flexibility in the differential I/O blocks.

High-Speed Interface Support

Support for many of the leading interface standards was designed into Stratix devices. For the first time, Altera provides support for the SFI-4 and XSBI standards along with enhanced support for the HyperTransport, RapidIO, POS-PHY Level 4, and UTOPIA IV standards. See Table 1.

Bridging

Stratix differential I/O provides the features and the performance necessary when used as an interface-bridging platform. Stratix True-LVDS technology was designed to support the strict timing requirements of up to four high-speed differential I/O protocols, unmatched in any other programmable logic device (PLD). Altera's interface capabilities are strengthened through the Atlantic™ bus interface intellectual property (IP) function.

More Embedded Functionality

Some of the significant improvements in the True-LVDS channels are provided through the enhanced clocking capabilities and an exciting new feature called data realignment. Previously, designers would need to byte-align the parallelized data in logic to obtain meaningful data. The new data realignment feature enables byte alignment with few additional logic elements (LEs).

Table 1. Standard Interfaces Supported in Stratix Devices

Feature	10-Gigabit Ethernet XSBI	SFI-4	POS-PHY Level 4 (SPI-4 Phase 2)	HyperTransport	RapidIO	UTOPIA IV
Maximum Bandwidth (Gbps)	10	10	10	6.4	10	10
Data (Bus Width)	16	16	16	8, 16, 32	8, 16	8, 16, 32
Clocks	1	1	1	1, 2, 4	1, 2	1
Maximum Data Rate (Mbps)	644.53	622.08	840	800	500	415
Maximum Clock Rate (Mbps)	644	622	420	400	250	415
Electrical Standard	LVDS	LVDS	LVDS	HyperTransport	LVDS	LVDS

Stratix High-Speed Differential I/O Channels

The number of differential I/O channels available increases as device density increases. Larger devices have up to 116 high-speed differential I/O channels, with up to 80 channels optimized for 840-megabits per second (Mbps) operation. Not only does the large number of channels supported in the device provide a large aggregate bandwidth, but it can also provide you with the flexibility to place differential I/O channels in a wide range of locations.

To achieve high-data transfer rates, Stratix devices support True-LVDS differential I/O interfaces which have dedicated SERDES circuitry for each differential I/O pair. Stratix SERDES circuitry transmits and receives at up to 840 Mbps per channel. Stratix devices support many high-speed I/O standards, such as LVDS, LVPECL, PCML, and HyperTransport technology.

The SERDES transmitter is designed to serialize 4-, 8-, or 10-bit wide words and transmit them across either a cable or printed circuit board (PCB). The SERDES receiver takes the serialized data and reconstructs the bits into a 4-, 8-, or 10-bit-wide parallel word. The SERDES contains the necessary high-frequency circuitry, multiplexer, demultiplexer, clock, and data manipulation circuitry. You can use double data rate I/O (DDRIO) circuitry to transmit or receive differential data in by-one (×1) or by-two (×2) modes.

Enhanced Clocking Capabilities

Stratix boasts several exciting new additions to differential I/O clocking:

- You can make clock phase adjustments in increments of 45°. This feature allows the implementation of an edge-aligned or a center-aligned clock for interfaces such as the HyperTransport interface.
- High-frequency single data rate (SDR) transmitter clock output is supported, which is important for applications that require a 1-to-1 relationship between the clock and data. This 1-to-1 relationship is required when implementing SFI-4 and 10-Gigabit Ethernet XSBI.
- Transmitter clock outputs can now be routed to any of the differential I/O pins. This feature allows you to place the transmitter clock pair close to the data channels, thereby reducing clock-to-data skew and increasing overall system margins. Due to the large number of channels supported in Stratix devices, there are a wide variety of placement options for differential clock outputs.
- Fast phase-locked loop (PLL) enhancements allow for a wide variety of clock distribution to occur. For example, you can now send receiver and transmitter clocks into the local or global clocks in the core of the device.

10-Gigabit Ethernet (XSBI)

The 10-Gigabit Ethernet XSBI interface is a 16-bit LVDS interface used to connect the physical coding sublayer (PCS) and physical medium attachment (PMA) sublayers that are common to a family of 10-Gbps physical layer implementations, collectively known as 10GBASE-R. XSBI is based on the Optical Internetworking Forum (OIF) standard SFI-4. Stratix devices support the required data rates of up to 644.53 Mbps together with the 1-to-1 relationship required between clock frequency and data rate. The Stratix differential I/O PLL is designed to support the high-clock frequencies and 1-to-1 relationship needed for interfaces such as XSBI and SFI-4. Stratix devices also support the XGMII 10-Gigabit Ethernet interface standard through the use of the HSTL I/O standard.

To achieve high-data transfer rates, Stratix devices support True-LVDS differential I/O interfaces which have dedicated SERDES circuitry for each differential I/O pair.

SFI-4

SFI-4 is an OIF standard used in an OC-192 SONET system to link the framer and the SERDES. In a manner similar to XSBI, Stratix devices support the required data rates of up to 622.08 Mbps along with the 1-to-1 relationship required between clock frequency and data rate. For interfaces such as SFI-4 and XSBI that require this 1-to-1 relationship, the Stratix differential I/O PLL is designed to support high clock frequencies. Support for SFI-4 extends the reach of high-density programmable logic from the backplane to the physical layer devices.

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Stratix Devices Deliver the Features & Flexibility for High-Speed Interface Design, continued from page 43

POS-PHY Level 4 (SPI-4 Phase 2)

POS-PHY Level 4 provides an interface for cell and packet transfers between physical (PHY) and link layer devices. POS-PHY Level 4 enables 10-Gbps data transfer and is primarily used in OC-192 systems. Along with the Stratix family's advanced differential I/O capabilities, other features such as TriMatrix™ memory, advanced PLL technology, and DDRIO capabilities combine to deliver a 840-Mbps POS-PHY Level 4 solution.

Stratix differential I/O buffers are designed to support the specific requirements of the physical layer of HyperTransport technology, including the requirements for a center-aligned clock (with respect to the transferred data) and DDRIO buffers.

HyperTransport Technology

HyperTransport technology is a high-speed, high-performance, point-to-point link technology primarily used as a processor interface. Stratix differential I/O buffers are designed to support the specific requirements of the physical layer of HyperTransport technology, including the requirements for a center-aligned clock (with respect to the transferred data) and DDRIO buffers.

RapidIO Standard

The RapidIO interconnect architecture is designed to link network processors, digital signal processing (DSP) devices, and other peripheral devices. The RapidIO interconnect is a high-performance, packet-switched interconnect technology that can exceed 10-Gbps throughput using LVDS links. Stratix devices support the necessary 250-MHz clock frequency and 500-Mbps data rate through the DDRIO capabilities. With TriMatrix memory—the Stratix family's leading-edge embedded memory solution— implementing the buffering requirements for a RapidIO system in Stratix devices is easy.

Discontinued Devices Update

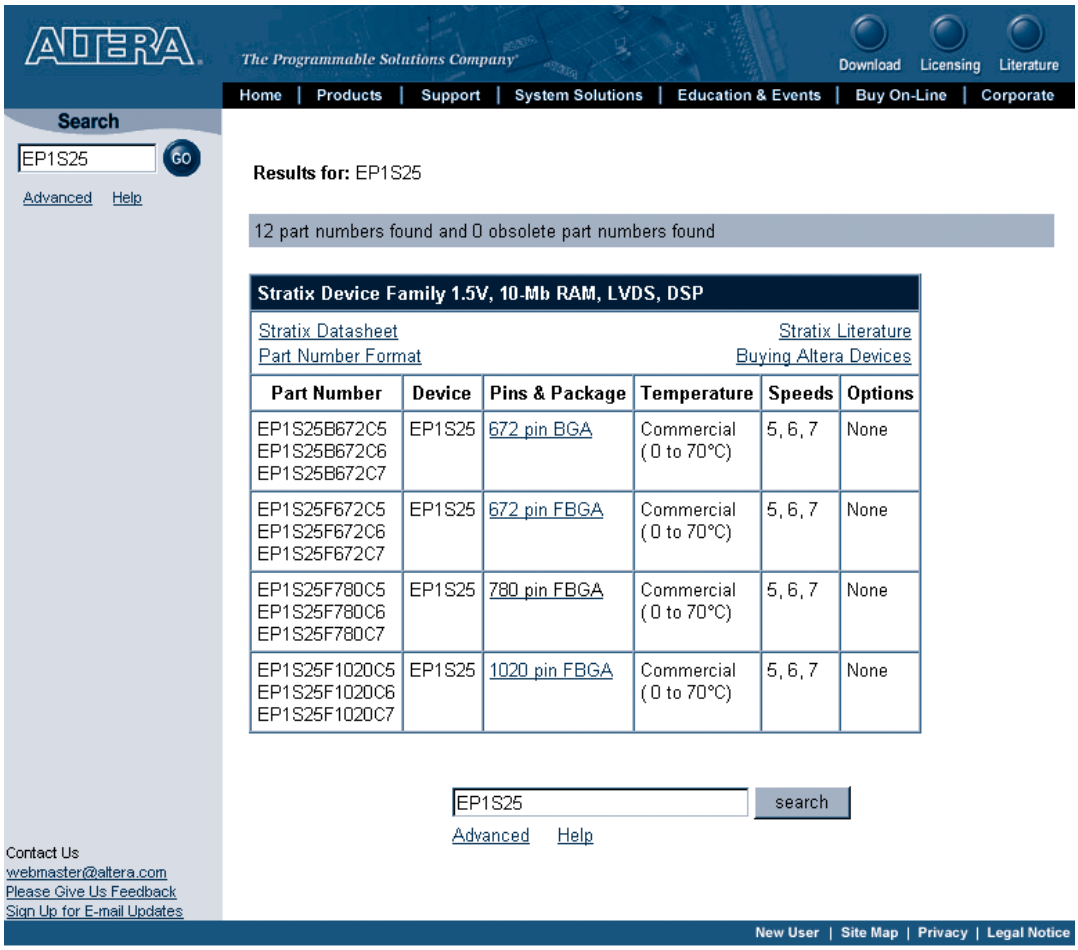
Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

Altera Improves Web Site by Integrating New Part Number Search

Altera improved its web site search engine by adding a quicker and easier Altera® device part number search feature. A significant number of searches submitted on the Altera web site are by users looking for technical information by entering full or partial device part numbers. Entering a partial or full device part number displays a list of all the relevant device part numbers, and technical information such as data sheets, application notes, pin-out tables, and package information. For example, Figure 1 displays the results of a search on a Stratix™ EP1S25 device.

Figure 1. EP1S25 Part Number Search Results



Stratix Frequently Asked Questions

In response to Stratix customer interest, Altera has compiled a list of questions and answers dedicated entirely to Stratix™ devices.

Q *Are Stratix devices drop-in compatible with any other device families?*

A Stratix devices are not drop-in compatible with other Altera device families. Because the Stratix device family is an entirely new architecture built from the ground up with brand new features, capabilities, and package offerings, new pin-outs were developed to support these enhancements. Designers can easily re-target their designs for Stratix devices using third-party EDA development tools and the Altera® Quartus® II software.

Q *How many system gates are available in Stratix devices?*

A It has become increasingly difficult to represent logic density, advanced features, and memory blocks using system gates as a single unit of measure because they do not follow a defined, PLD industry standard. Disproportionate growth in embedded memory and LEs leads to unbalanced weighting in gate enumeration and ultimately to misleading density representations. For example, the largest Stratix device has 43 million system gates when enumerated using traditional methodologies, with logic capacity only accounting for 2.4 million gates. An LE-based nomenclature facilitates better device selection and avoids confusion. Therefore, Stratix device densities are more appropriately represented using an LE-based nomenclature that accurately communicates the logic capacity of PLDs.

Q *What is the MultiTrack™ interconnect?*

A The MultiTrack interconnect is a continuous routing structure that provides high-speed connectivity between logic resources, TriMatrix memory, DSP blocks, and I/O structures using column- and row-based routing lines of varying lengths. These lines ensure fast, consistent signal propagation within and between design blocks. The Quartus II software intelligently prioritizes signals so that design-critical paths are routed on faster lines to accelerate performance.

Q *What is DirectDrive™ technology?*

A DirectDrive technology is a proprietary, deterministic routing technology that ensures identical routing resource usage for any function regardless of its placement within the device. This greatly simplifies the system integration stage of block-based designs by eliminating the often time-consuming system re-optimization process that typically follows design changes and additions. Designers can freely add, modify, and move various portions of their design without negatively affecting design performance, fittability, or functionality.

Q *Why are Stratix devices designed with so much memory in non-uniform block sizes?*

A Next-generation system speeds are steadily outpacing internal processing power, resulting in a growing need for buffering and on-chip storage. To address this issue, Stratix devices are designed with a 4× increase in the logic-to-memory ratio over previous-generation Altera architectures. This increase was achieved by integrating area-efficient MegaRAM™ blocks. However, the total number of data ports is as important as the total number of memory bits, as this parameter determines the maximum memory bandwidth in the device (an increasingly important measure of performance as system performance continues to accelerate). By adding a large number of M512 and M4K blocks, the effective number of ports is increased in the device, allowing greater movement of data in and out of the memory blocks for processing.

Q *What benefits are associated with the Stratix digital signal processing (DSP) block architecture?*

A Stratix DSP blocks provide designers with many benefits in both performance

and resource usage. The processing capabilities of programmable logic devices (PLDs) outperform industry-standard DSP processors in computation-intensive applications that require parallel operations or time-domain multiplexing (TDM). Resources for the various stages of the DSP block are not shared with the general-purpose portion of the device; therefore, whether the device is 99% or 10% consumed, performance of the blocks remains the same.

Q *How many clock networks are available in each device?*

A Each device has up to 16 global clock networks, representing a 100% increase over previous architectures. These low-skew clock networks are used anywhere in the device, including I/O elements (IOEs), logic elements (LEs), DSP blocks, and TriMatrix™ memory blocks. In addition to these resources, up to four regional and two fast regional clock networks are available for use within each device quadrant. Regional clocks are driven by either phase-locked loop (PLL) outputs or input pins (shared with global clock networks), whereas fast regional clocks are driven by either input pins or signals from the peripheral I/O bus. This results in up to 40 unique clock networks per device.

Q *How many types of PLLs are available in Stratix devices and what features are available?*

A Stratix devices support two types of PLLs: enhanced PLLs and fast PLLs. Each device has up to four enhanced PLLs, which are feature-rich, general-purpose PLLs that support advanced capabilities such as external feedback, clock switchover, phase and delay control, PLL reconfiguration, spread-spectrum clocking, and programmable bandwidth. Each device also has up to eight fast PLLs that offer high-speed outputs to manage the high-speed differential I/O interfaces, as well as other general-purpose clocking management capabilities such as clock multiplication and phase shifting.

Q *What high-speed differential I/O electrical standards are supported in Stratix devices?*

A With proven expertise in high-speed differential I/O design, Altera continues support for LVDS, PCML, HyperTransport, and LVPECL in Stratix devices. The Altera differential I/O solution, unlike any other in the programmable logic industry, uses dedicated, high-speed circuitry, thereby maximizing device throughput. Up to 116 channels are available on each device, 80 of which are optimized for 840-megabit per second (Mbps) performance.

Q *What high-speed I/O interfaces are supported in Stratix devices?*

A Stratix devices support many of the latest high-bandwidth bus protocols, including: SPI-4 Phase 2 (POS-PHY Level 4), SFI-4, 10-Gigabit Ethernet XSBI interface (16 bits), HyperTransport, RapidIO, common switch interface (CSIX), and UTOPIA IV.

Q *How many high-speed differential channels are available on each device?*

A Stratix devices have up to 116 input and 116 output channels with 80 optimized for 840-Mbps performance; however, support varies with device density and package. For more information, see *Application Note 202 (Using High-Speed Differential I/O Interfaces in Stratix Devices)*.

Q *Do Stratix devices support clock-data synchronization (CDS)?*

A Stratix devices do not support CDS for channel-to-channel bit alignment. Instead, you can use the phase shifting capabilities of the fast PLL and the data realignment feature for alignment. You can shift the output of the fast PLL to ensure that data capture occurs at the appropriate time in the data window for signals that are within the receiver skew margin. For subsequent byte alignment, you can use the data realignment feature to delay the parallel output from the SERDES to the core by a full bit period,

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essentially shifting the data byte by one bit. You can accomplish this alignment over several clock cycles until the correct byte window is established by the SERDES.

Q *What enhancements were made to external memory interfaces over previous-generation architectures?*

A To enhance strobe-based memory interfaces such as those used with double data rate (DDR) SDRAM devices, localized data strobe (DQS) signal clock networks are designed into Stratix devices that drive a predefined set of associated data (DQ) signals. To correctly align with incoming data, each DQS signal includes delay circuitry that precisely shifts the strobe signal by either 90° or 72° prior to reaching the DQ pins.

Q *Do I still need a 100-Ω termination resistor for LVDS?*

A No, an external termination resistor is no longer required when using LVDS. Stratix devices include Terminator™ technology that provides on-chip termination resistors for many I/O standards, including LVDS.

Q *Does the Stratix device family support migration to HardCopy™ devices?*

A HardCopy devices provide a low-risk, cost-effective, time-saving alternative to application-specific integrated circuits (ASICs) for Altera's largest density PLDs. HardCopy devices will support the Stratix device family, offering the same seamless, proprietary design conversion process that is currently available with other Altera device families. The HardCopy device architecture will offer identical functionality, supporting Stratix device family features such as TriMatrix memory, DSP blocks, high-speed interfaces, Terminator technology, and PLLs.

Q *What version of software will support Stratix devices?*

A Altera Quartus II software version 2.0 supports preliminary compilation for Stratix devices. With new features such as SignalProbe™ compilation, fast fit, and Linux support, you have a truly-integrated, single-platform development tool that minimizes overall development time. The advanced PowerFit™ technology optimally places and routes designs resulting in efficient resource usage and maximized performance. Programming file generation for Stratix devices will be supported in a subsequent service pack.

Q *Which third-party tools will support Stratix devices and when will they be available?*

A Altera, working with all major third-party EDA vendors, provides a truly seamless design flow for Stratix device designs. Exemplar™, Synplicity®, and Synopsys will all support the Stratix device family in their synthesis and simulation tools, ensuring the highest quality of results in Altera devices. Contact your local Altera representative for details on third-party software availability.

Q *What intellectual property (IP) cores will be available for Stratix devices?*

A Most of the existing Altera MegaCore® functions will make a transition to support Stratix devices. Altera and Altera Megafunction Partners Program (AMPP℠) functions will be specifically optimized for the Stratix architecture and will be fully verified, documented, and supported. These optimized cores include all signal processing, communications, and bus interface functions. For schedules, contact your Altera sales representative.

Q *Is the Nios™ embedded processor version 2.0 supported in Stratix devices?*

A Stratix devices support the Nios embedded processor, including the already available Nios embedded processor version 2.0, offering significant performance improvements over previous Altera architectures. Stratix devices feature continued support for current Nios features such as the simultaneous multi-master Avalon™ bus, custom instruction capabilities, and advanced debugging solutions. The Nios embedded processor version 2.0 is supported in the Quartus II software version 2.0.

Discontinued Devices Update

To increase operational efficiency in manufacturing flow, Altera will be discontinuing several products (see Table 1 for details). To ensure that customers may make lifetime buys, Altera will maintain shipments on many of these devices through the end of 2003; Table 1 shows the last order and last shipment dates for discontinued devices. For a detailed list of discontinued ordering codes, refer the Altera® document listed in the reference column.

Continued support for Altera devices beyond the phase-out period may be available through Rochester Electronics, an extended after-market supplier. Please contact Rochester Electronics at (508) 462-9332 for more information.

For additional information on discontinued devices, contact your local Altera representative.

Altera will maintain shipments on many discontinued devices through the end of 2003.

Table 1. Discontinued Device Update

Product Family	Device	Last Order Date	Last Shipment Date	Reference
MAX® 7000	Selected devices with a dry pack option	05/31/02	11/30/02	PDN0117
	EPM7192EGM160-15	05/31/02	11/30/02	PDN0117
MAX 7000S	Selected devices in plastic quad flat pack (PQFP) and thin quad flat pack (TQFP) packages	05/31/02	11/30/02	PDN0117
MAX 9000	Selected devices	02/28/02	08/31/02	PDN0106
	EPM9560BC356-20	05/31/02	11/30/02	PDN0117
	EPM9320RC208-15F	05/31/02	11/30/02	PDN0117
FLEX® 8000	Selected FLEX 8000 pin-grid array (PGA) packages	02/28/02	08/31/02	PDN0107
	Selected devices	02/28/03	08/31/03	PDN0107
	EPF8820ABC225-3	05/31/02	11/30/02	PDN0117
FLEX 10K	Selected FLEX 10K PGA packages	02/28/02	08/31/02	PDN0107
	Selected FLEX 10K PGA & ball-grid array (BGA) packages	02/28/03	08/31/03	PDN0107
	EPF10K10U84-4	05/31/02	11/30/02	PDN0117
FLEX 10KA	Selected FLEX 10KA PGA packages	02/28/03	08/31/03	PDN0107
	EPF10K30AFI256-2	05/31/02	11/30/02	PDN0117
FLEX 10KE	Selected FLEX 10KE PGA packages	02/28/03	08/31/03	PDN0107
APEX™ 20K	Selected APEX 20K PGA packages	02/28/03	08/31/03	PDN0107
	EP20K400BI652-2	05/31/02	11/30/02	PDN0117

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera.

Information Type	U.S. & Canada	All Other Locations
Product Literature	http://www.altera.com	http://www.altera.com
Altera Literature Services *(1)*	lit_req@altera.com	lit_req@altera.com
News & Views Information	http://www.altera.com/literature/nview.html n_v@altera.com	http://www.altera.com/literature/nview.html n_v@altera.com
Non-Technical Customer Service	(800) 767-3753	(408) 544-7000
Technical Support	https://www.altera.com/mysupport	(408) 544-7000 (7:30 a.m. to 5:30 p.m. Pacific Time) *(2)*
	(408) 544-6401	(408) 544-6401 *(2)*
FTP Site	ftp.altera.com	ftp.altera.com
General Product Information	(408) 544-7104	(408) 544-7104 *(2)*
	http://www.altera.com	http://www.altera.com

Notes:
(1) The ***Quartus Installation and Licensing*** and ***MAX+PLUS II Getting Started*** manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for the latest listing.