News & Views

Second Quarter 2002

Newsletter for Altera Customers

Power Up with New Quartus II Verification Features

As increasingly complex, team-based system-on-a-programmable-chip (SOPC) design becomes the norm, hardware, software, and systems designers grapple with new verification challenges in addition to the urgency of the usual time to market, cost, and performance goals. Verification is historically the longest and most critical portion of system-level design. To ease those verification blues, engineers can now power up with a comprehensive, multi-faceted suite of verification features in Altera's Quartus® II software.

The latest Quartus II software release (version 2.1) includes the SignalTap® II logic analyzer and the SignalProbe™ verification tool to provide deeper levels of analysis and greater visibility into the design's operation. These features leverage the generous memory and innovative MultiTrack™ routing resources of Altera's new Stratix™ device family, which is shipping today.

Inside This Issue:

ALTERA®

Message from *Software*

Quartus II—Altera's True Customer Experience

The Altera® Quartus® II design software is the foundation of Altera's system-on-a-programmable-chip (SOPC) design environment and is Altera's true customer experience. As the only product that most of you, our customers, get intimately involved with, the Quartus II software is designed and developed to deliver complete satisfaction, meeting your demands for ease-of-use, the fastest compile times, innovative design and verification features, and continual performance improvements.

Altera has reclaimed its title as the champion of design software solutions for programmable logic. By acting on the recommendations of hardware and software design engineers around the world, Altera has assembled an arsenal of software and development tools to accomplish a single goal: to give you a powerful yet easy-to-use environment in which to develop the next generation of SOPC solutions. The positive response to the Quartus II software version 2.0 proves that we are achieving that goal.

This issue of *News & Views* introduces the Quartus II software version 2.1, a fully integrated design platform that also embraces today's growing trend of embedded microprocessors and peripherals. Altera's SOPC Builder (now included as a standard part of the Quartus II software) and DSP Builder tools offer both hardware and software designers the ability to communicate the status of their specific portions of the system-under-development. In effect, the system definition and integration phases of the development are automated, saving time and money. The Quartus II software version 2.1 includes enhanced support for Altera Stratix™ devices, the industry's most advanced FPGAs—which are available today. The software includes enhancements to many industry-first developments such the LogicLock™ block-based design flow, native support for the Linux operating system, and the PowerGauge™ power analysis tool.

This issue focuses on sophisticated verification techniques—new to the Quartus II software version 2.1—that distinguish Altera's superior SOPC methodology as a powerful tool, helping you to meet the new challenges you face in design validation. As you confront the increasing obstacles of designing with high-performance devices, we place laser focus on quick and accurate verification of the design at every level. From formal verification and testbench generation to board-level verification, Altera's SignalTap® II logic analyzer and other features in the Quartus II software version 2.1 discussed in this issue deliver increased insight into the powerful tools now available to help you go from concept to system in less time than ever.

Tim Southgate,
Vice President of Software
& Tools Marketing

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Figure 1. Quartus II & Third-Party Verification Tools

time. In team environments, designers can easily pass Quartus II-generated simulation netlists to other engineers or directly to third-party software tools for further analysis. For example, board-level designers can perform other signal integrity analysis on high-speed I/O signals or board-level simulations using Quartus II software-generated simulation files, and PLD designers can pass Quartus II PowerGauge power consumption estimates to board-level designers before board design and layout.

Hardware-Software Co-Simulation

The Quartus II software and the SOPC Builder system development tool can output complete system simulation models and testbenches that let you simulate hardware and software at the same time. This feature includes simulating your embedded processor code, operating system code, PLD hardware, and internal and external memory. Wizards initialize the memory models and create sample universal asynchronous receiver/transmitter (UART) character streams for simulation. PLD designers can use traditional third-party HDL simulators while software engineers can simultaneously run HDL simulators and software debugging tools to interactively control the simulation. See Figure 2.

Comprehensive SOPC Verification Solution

The Quartus II software now provides the most comprehensive verification solutions available for traditional programmable logic device (PLD) hardware design and complete SOPC solutions. Table 1 provides an overview of the verification solutions available to Quartus II designers, and which stage of the design process relies on each solution. The table order is arranged in approximate order of use in the design flow.

As shown in Table 1, Quartus II users have several verification options available. Some solutions are supported by both the Quartus II software and third-party tools. You can select the flow to get a design completed in the shortest possible

To optimize this flow, Altera has developed an Excalibur™ stripe simulator (ESS), which is a fast, functional stripe simulator and an instruction set simulator for the ARM922T™ processor. The ESS enables you to simulate systems in minutes instead of days. For example, an Excalibur EPXA10 device booting the WindRiver VxWorks operating system can be simulated in just three minutes.

Figure 2. ESS: Co-Simulation Tool
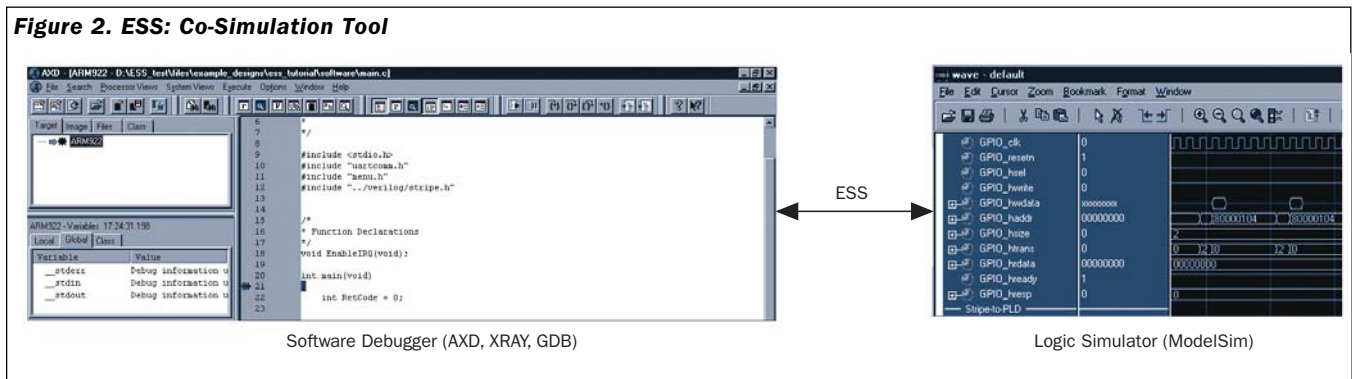
Verification Method	**Description**	**Quartus II Software or Subscription Support**	**Third-Party Support**	**Stage Used**
		Table 1. Quartus II Software Verification Solutions		
Design rule checking	Checks designs for coding styles that will cause synthesis, simulation, or design migration problems later	Quartus II software design assistant	Atrenta (SpyGlass) Synopsys (Leda)	PLD design
Functional verification	Checks if a design meets functional requirements before you perform place-and-route	Quartus II software simulator ModelSim®-Altera	Cadence (NC-Verilog, NC-VHDL) Mentor Graphics® (ModelSim) Synopsys (VCS, Scirocco)	PLD design
Testbench generation	Reduces the number of hand-generated test vectors	Waveform-to-testbench converter Testbench template generator		PLD design
Static timing analysis	Analyzes, debugs, and validates a design's performance after place-and-route	Quartus II software static timing analyzer	Synopsys (PrimeTime)	PLD design
Timing simulation	Performs a detailed gate-level timing simulation after place-and-route	Quartus II Simulator ModelSim-Altera	Cadence (NC-Verilog, NC-VHDL) Mentor Graphics (ModelSim) Synopsys (VCS, Scirocco)	PLD design
Hardware-software co-simulation	Quickly simulates interaction between PLD hardware, embedded processors, memory, and peripherals	ModelSim-Altera	Mentor Graphics (ModelSim)	PLD design Board design Software design
In-system debug	Enables you to see the behavior of internal nodes in-system and at system speeds	Quartus II SignalTap II logic analyzer Quartus II SignalProbe technology	Bridges 2 silicon	PLD design Software design
Board-level timing analysis	Verifies that the PLD and the entire board meets system timing requirements		Innoveda (Blast) Mentor Graphics (Tau)	Board design
Signal integrity analysis and electromagnetic compatibility (EMC)	Verifies that the high-speed I/O signals will be transmitted reliably and within EMC guidelines	Quartus II software design-specific input/output buffer information specification (IBIS) model generation	Cadence (SPECCTRAQuest) Innoveda (XTK, Hyperlynx) Mentor Graphics (Interconnectix)	Board design
Formal verification	Identifies differences between source register transfer level (RTL) netlists and post place-and-route netlists without creating any test vectors		Synopsys (Formality) Verplex (Conformal LEC)	PLD design
Power estimation	Estimates the power consumption of your device using your design's operating characteristics	Quartus II Simulator ModelSim-Altera	Mentor Graphics (ModelSim)	PLD design Board design

The following sections describe the verification tools available in the Quartus II software.

Design Rule Checking

Design rule checking tools contain a set of customized rules that designers can apply to a design to initially check if the design can be synthesized, simulated, and migrated to a particular device technology. The upcoming Quartus II software version 2.1 contains design rule checking for designs targeted for an Altera HardCopy™ device. Altera is working closely with Atrenta and Synopsys to develop customized rule sets for their design rule checking tools. Customized rule sets help you optimize designs targeting Altera devices early in the design process.

The upcoming Quartus II software version 2.1 contains design rule checking for designs targeted for an Altera HardCopy device.

Testbench Generation

In addition to outputting verification netlists for use in third-party HDL simulators, the Quartus II software version 2.0 and later can create HDL testbench templates that can jump-start verification efforts. The Quartus II software can also create complete HDL testbenches from Quartus II software simulator waveform files. The Altera SOPC Builder and DSP Builder software tools can also generate complete system simulation models and testbenches.

Static Timing Analysis

You can use static timing analysis to analyze, debug, and validate a design's performance. Static timing analysis measures the delay of every path in the design and reports the design's performance. The Quartus II software provides advanced timing analysis features such as multi-cycle and multi-clock analysis. The Quartus II software also outputs industry-standard Standard Delay Format Output files (**.sdo**) and STAMP format files for further analysis by third-party chip-level or board-level timing analysis tools.

Excalibur Simulation

Excalibur embedded processor solutions include HDL designs as well as embedded software that is executed by the embedded processor. The only way to verify that the hardware and software portions of the design are working together correctly before building a prototype is to co-simulate the hardware and software at the same time.

The Quartus II software outputs Excalibur simulation models that designers can use with ModelSim-Altera and other third-party simulation products to simulate complete systems, including embedded processors, embedded processor software, memory, and custom programmable logic systems. Excalibur simulation models included with Altera design software subscriptions include bus-functional models for peripheral development, fast-functional simulation and instruction set simulation models for quick hardware-software co-simulation (simulates up to 500K instructions per second), and cycle-accurate models to verify the processor and PLD system's exact operation.

Formal Verification

Formal verification is a relatively new verification technology that uses mathematical algorithms to verify that a post-place-and-route netlist provides the same functionality as a pre-place-and-route netlist. Formal verification tools do not require the user to create any test vectors and can significantly accelerate verification efforts for large designs. The upcoming Quartus II software version 2.1 will support the Verplex Conformal LEC formal verification tool flow. Support for the Synopsys Formality software is under development for a future release of the Quartus II software.

In-System Verification

Altera developed two in-system verification methods that utilize the programmable nature of SOPC designs to help designers analyze their devices' internal nodes or I/O pins while operating in-system and at system speeds. These methods are the SignalTap II logic analyzer and SignalProbe debugging technology. The SignalTap II and SignalProbe technologies fit seamlessly into any third-party synthesis flow and do not require any modifications to the HDL design source files.

SignalTap II Logic Analyzer for Hardware Verification

The SignalTap II logic analyzer is Altera's next-generation embedded logic analyzer verification tool included in the upcoming Quartus II software version 2.1. The SignalTap II logic analyzer facilitates the verification process by integrating the functionality of one or more logic analyzers within the Quartus II software. The SignalTap II logic analyzer allows the design team to capture the state of any internal node or I/O pin on a device in real time, operating at system speeds. The SignalTap II logic analyzer does not require any external probes or changes to user design files. Data is filtered, captured, and stored in the device's embedded RAM block. Captured data is sent to the Quartus II software waveform viewer via a download cable. For more information on The SignalTap II logic analyzer, refer to "Introducing the SignalTap II Logic Analyzer" on page 8.

SignalProbe Debugging Technology

The SignalProbe hardware debugging technology, is available in the Quartus II software version 2.0 and later, lets designers incrementally route an internal node to an unused or reserved pin for analysis with an external scope or logic analyzer. Because SignalProbe technology can incrementally route paths from the node(s) of interest to device pin(s), compile times are typically less than 5% of a full compilation. Furthermore, the design's original routing and timing are fully preserved. As the SignalProbe technology reports any delays added in the routing from internal nodes to the device pin (where the external signal capture occurs), designers have an accurate picture of the captured signal's timing relationships. For more information, refer to *TB 82: SignalProbe Compilation Enables Fast System Debugging with the Quartus II Software.*

Signal Integrity & EMC Analysis

The keys to developing systems with high-speed I/O are signal integrity and meeting stringent EMC requirements. The Quartus II software can generate design-specific IBIS models that designers can export to third-party signal integrity and EMC analysis tools such as Cadence SPECCTRAQuest, Innoveda XTK and Hyperlynx, and Mentor Graphics Interconnectix software.

PowerGauge Power Analysis

The Quartus II software includes PowerGauge technology, the industry's first integrated power analysis tool. The PowerGauge analysis tool uses the designer's simulation files to link the power consumption estimate with customer-specific design files and operating parameters. Integrated power analysis using the Quartus II Simulator or third-party simulators enables Altera designers to identify and optimize system-level power consumption early in the design cycle.

ModelSim-Altera

Altera software subscriptions include the Mentor Graphics ModelSim-Altera HDL simulator. For large designs requiring multiple design iterations, the ModelSim-Altera software supports behavioral RTL simulation for pre-place-and-route functional verification of HDL code. The ModelSim-Altera software also gives Quartus II users full support for VHDL and Verilog HDL testbenches so they can perform automated and fully repeatable testing of large and complicated designs.

Conclusion

Altera's Quartus II software now provides access to the most comprehensive verification solution available for SOPC designs. The Quartus II software provides verification methodologies for each design team member and for each stage of a project including PLD hardware design, board-level design, and embedded software design.

The SignalTap II logic analyzer facilitates the verification process by integrating the functionality of one or more logic analyzers within the Quartus II software.

Introducing the SignalTap II Logic Analyzer

Available exclusively in the Altera® Quartus® II software, the SignalTap® II logic analyzer supports the highest number of channels and sample depths and the fastest acquisition clocks of any embedded logic analyzer in the programmable logic market.

Similar to the original SignalTap logic analyzer, the SignalTap II logic analyzer does not require any external probes or changes to user design files to capture the state of internal nodes or I/O pins in your design. The SignalTap II analyzer also provides the following new features:

- Includes support for multiple devices in a single Joint Test Action Group (JTAG) chain
- Allows multiple logic analyzer megafunctions in each device in a JTAG chain
- Supports up to 1,024 channels and up to 128K samples per channel
- Supports up to 200-MHz acquisition clocks
- Features new user interface with separate triggering and data-acquisition windows
- Includes up to 10 trigger levels to filter captured data
- Customized display options to make captured data more useful
- Supports Stratix™ devices

SignalTap II Overview

Running at speed under "real-world" system conditions is the ultimate testbench if you want to monitor the active processes within your design as it operates. The SignalTap II logic analyzer allows you to capture the state of internal nodes or I/O pins while the device is running in-system and at system speed. The following components are required to use the SignalTap II logic analyzer to perform logic analysis:

- The Quartus II software
- The megafunctions that are inserted into the device:
    - SignalTap II logic analyzer megafunction
    - SignalTap II hub
- The download cable:
    - ByteBlasterMV™ cable
    - MasterBlaster™ cable
- The design under test

You can store captured data in the Altera device's memory blocks and stream out the data to the Quartus II software waveform display using a ByteBlasterMV or MasterBlaster communications cable (see Figure 1).

Table 1 summarizes the features and benefits of the SignalTap II embedded logic analyzer.

Multiple Logic Analyzers in a Single Device

The SignalTap II logic analyzer includes support for multiple instances of the logic analyzer megafunction in each device. This support allows you to create a unique embedded logic analyzer (ELA) megafunction for each clock domain present on the device. Additionally, by "reserving" a free node in a particular ELA , you can add an internal register or node to the ELA for data capture without having to recompile later (this feature will be supported in a future release of the SignalTap II logic analyzer).

Logic analyzer megafunctions are defined in SignalTap files (**.stp**). Each **.stp** can contain multiple logic analyzer megafunctions. Each **.stp** file's scope is limited to a single device in the JTAG chain.

Figure 1. SignalTap II Logic Analyzer Implementation
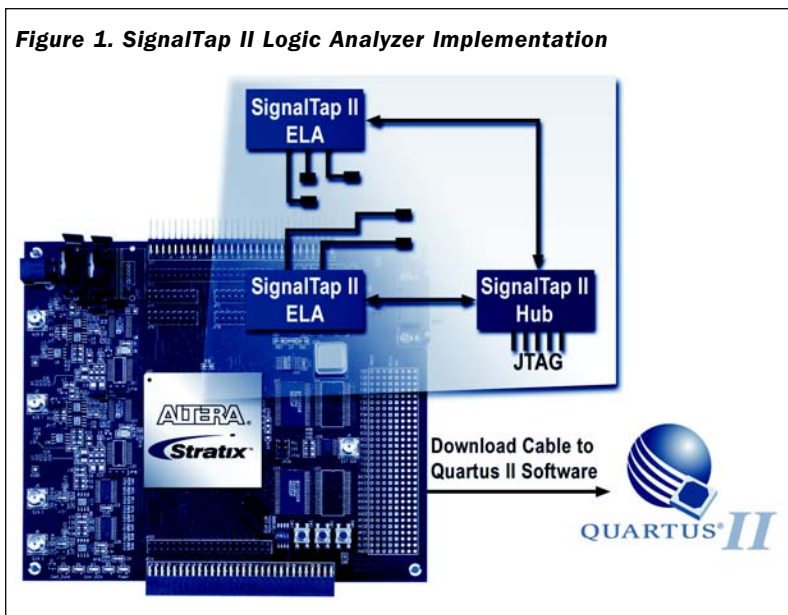
The Instance Manager is available in the top portion of the new interface and shows all recognized logic analyzers in the design that you can use to capture and store data (see Figure 2).

Figure 2. Instance Manager

Multiple Logic Analyzers in Multiple Devices in a Single JTAG Chain

The SignalTap II logic analyzer allows multiple devices in a single JTAG chain in combination with multiple logic analyzer megafunctions in each device in that JTAG chain.

Up to 10 Levels of Trigger Conditions for Each Analyzer

Trigger conditions instruct the SignalTap II analyzer when to start capturing data. Ten levels of trigger conditions offer a great deal of flexibility to set up complex triggering conditions that assist the engineer in isolating reasons for failures or problems.

To set up multiple levels of trigger conditions, use the setup tab in the SignalTap II user interface. You can trigger-out signals to trigger external logic analyzers or oscilloscopes.

Four Different Trigger Positions

The SignalTap II logic analyzer supports four trigger positions, allowing you to have more control over what data is captured and displayed when a trigger condition is satisfied.

The "pre" trigger position tells the software to save and store 12% of the samples that occurred before the trigger condition was met, and 88% of the samples that occurred after the trigger condition was met.

The "center" trigger position tells the software to save and store 50% of the samples that occurred before the trigger condition was met, and 50% of the samples that occurred after the trigger condition was met.

Table 1. SignalTap II Features & Benefits

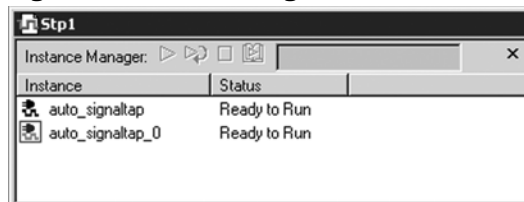| Feature	Benefit
Multiple logic analyzers in a single device	Supports multiple clock domains in a single device
Multiple logic analyzers in multiple devices in a single JTAG chain	Allows multiple devices with multiple clock domains to be analyzed
Up to 10 levels of trigger for each analyzer	Allows for more complex data capture commands, providing greater accuracy and problem isolation
Four different trigger positions	Sets up each trigger to sample at different ranges relative to the triggering event, allowing more accurate data collection
Up to 1,024 channels in each device	Samples many signals and wide-bus structures, allowing for a great deal of data collection to locate problems
Up to 128K samples in each device	Provides more than enough samples than you would normally use for practical applications
Supports clocks up to 200 MHz	Samples design data at system frequency
Vendor-independent application program interface (API) for source level debug tools	Allows third-party software to utilize SignalTap II resources
Add nodes, change signal selection, and change trigger conditions without recompilation *(1)*	During analysis, if you want to add an internal register to the analyzer, you can add it and capture data without recompiling your design
Mnemonic and radix tables	Labels signals with true signal names from software source to assist in identification of problem source
Auto-detect devices in JTAG chain	Confirms connection to device before attempting to initiate data capture
Auto-detect programming hardware	Confirms connection to device before attempting to initiate data capture
Print waveforms	Allows you to print the waveforms you have captured for reporting
New, user-friendly interface	Easier to use and less cluttered display
Price	Free with Altera software subscription

Note to Table 1:
(1) This feature will be supported in a future release of the SignalTap II logic analyzer.

The "post" trigger position tells the software to save and store 88% of the samples that occurred before the trigger condition was met, and 12% of the samples that occurred after the trigger condition was met.

The "continuous" trigger position tells the software to save samples continuously in a circular buffer fashion, until terminated by the user.

Introducing the SignalTap II Logic Analyzer, continued from page 9

Up to 1,024 Channels in Each Device

The number of channels that can be supported in a specific design is largely a function of the available device resources (logic elements (LEs) and RAM). The SignalTap II logic analyzer is capable of managing up to 1,024 channels from one or more logic analyzer megafunctions in each device.

Up to 128K Samples Per Channel

The SignalTap II logic analyzer is capable of managing up to 1,024 channels from one or more logic analyzer megafunctions in each device.

The number of samples the embedded memory of an Altera device can store is a function of the surplus memory resources on the device that are not consumed by the design under test. The SignalTap II logic analyzer can support up to 128K samples per channel.

Supports Clocks Up to 200 MHz

Many complex digital systems with FPGAs include clocks that are faster than 100 MHz. With support for clocks at frequencies as high as 200 MHz, the SignalTap II analyzer samples your data at system speeds.

Add a Node, Change Signal Selection & Change Trigger Conditions Without Recompilation

The SignalTap II logic analyzer enables you to add nodes, change which signals are under sample, and change trigger conditions without recompiling your design.

To add a node, you must reserve a channel on the embedded logic analyzer megafunction before compilation. After capturing data, the reserved channel may then be incrementally connected to a node in the device by use of the SignalProbe™ feature. This feature will be supported in future release of the SignalTap II logic analyzer.

Mnemonic & Radix Tables

The SignalTap II software includes both a mnemonic feature (to associate names with bit patterns) and selectable radices (binary, octal, hexadecimal, 8-bit ASCII, two's complement, unsigned, and signed). You can associate a mnemonic table with a group of signals in the data waveform view or define a mnemonic table based on the number of bits in the group. If you define multiple mnemonic tables with the same bit-width, you can choose the table from a drop-down list.

SignalTap II Device Support

You can use the SignalTap II embedded logic analyzers with the following Altera devices:

- Stratix™ devices
- Excalibur™ devices
- APEX™ II devices
- APEX 20K devices
- Mercury™ devices

Conclusion

The SignalTap II logic analyzer supports the highest number of channels, highest sample depth, and fastest acquisition clocks of any embedded logic analyzer in the programmable logic market. By combining the ability to capture large amounts of high-speed data with powerful trigger-condition filters and data display features, you can focus on the most critical data to quickly solve your design problems.

SOPC Builder—From Concept to System in Minutes

SOPC Builder is an automated system development tool that simplifies the task of creating high-performance system-on-a-programmable-chip (SOPC) designs. The tool accelerates time-to-market by automating the system definition, integration, and verification phases of SOPC development.

SOPC Builder encompasses all aspects of embedded system design, including software design and verification, within one tool. You can generate embedded systems in a fraction of the time of traditional system-on-chip (SOC) designs. SOPC Builder is integrated within the Altera® Quartus® II software to give programmable logic device (PLD) designers immediate access to this revolutionary new development tool.

With the introduction of million-gate FPGAs, complex intellectual property (IP) cores, and Altera's Nios® and Excalibur™ embedded processors, the individual technologies are in place to enable true SOPC-level design. SOPC Builder ties all these technologies together in one flow. SOPC Builder, combined with Altera's core technologies, gives you a complete solution for implementing entire embedded systems in programmable logic.

SOPC Builder Feature Overview

SOPC Builder allows you to create SOPC designs in a fraction of the time traditionally required for embedded SOC designs. SOPC Builder saves design time by significantly simplifying engineering effort in four key areas (see Figure 1).

System Definition & Customization

SOPC Builder provides an intuitive graphical user interface (GUI) that simplifies the definition and customization of your system. Because you do not have to edit HDL code to customize the system, SOPC Builder can save weeks of design time. SOPC Builder presents a wizard tailored for each component, allowing you to easily customize functionality. For example, you can launch wizards to configure the ARM® CPU in Excalibur devices to add a Nios® processor, or to customize each peripheral and memory interface in your system.

Figure 1. SOPC Builder System Overview

System Customization	System Integration
Using wizard-based interfaces, you can configure: ■ Excalibur and/or Nios processors ■ Memory map, interrupt priority, boot address, vector table location ■ Peripherals and on-chip memory ■ Off-chip memory interfaces ■ Component connection, bus architecture, and arbitration priority	SOPC Builder accelerates system integration by: ■ Automatically connecting all components ■ Creating multi-master bus architecture with arbitration logic ■ Connecting user-defined blocks of logic to system
Software Generation	**System Verification**
SOPC Builder jump-starts software development by automatically creating: ■ Header files that define the memory map, interrupts and hardware-specific data structures ■ Libraries of routines to access each hardware peripheral ■ Software components, such as an OS kernel, drivers and/or protocol stack, to match the target hardware	Simulation can start immediately, because SOPC Builder creates a full simulation environment, including: ■ Register transfer level (RTL) simulation model ■ System testbench ■ ModelSim® project with pre-formatted waveforms Prototype can start immediately, using one of the many development boards available for programmable logic

You can select and parameterize intellectual property (IP) blocks from SOPC Builder's extensive list of communication, digital signal processing (DSP), microprocessor, and bus interface IP cores. SOPC Builder-Ready IP cores are available both from Altera and third-party IP vendors (see Figure 2 on page 12). Altera certifies that these IP blocks are SOPC Builder Ready, ensuring seamless integration with the SOPC Builder design flow. If you are designing custom modules, SOPC Builder offers an application programming interface (API) so that you can include and configure any block of IP (either proprietary or purchased) similar to standard SOPC Builder components.

SOPC Builder's GUI allows you to specify the memory map, interrupt priorities (see Figure 3 on page 12), CPU boot address, interrupt vector table location, and program and data memory locations.

EXCALIBUR™

Figure 2. Available SOPC Builder-Ready Components

If a system contains multiple masters (e.g., two processors, or a processor and a direct memory access (DMA) peripheral), SOPC Builder automatically generates the bus arbitration logic to connect these masters to shared slave peripherals and memories. SOPC Builder uses a technique called slave-side arbitration that allows multiple masters to transfer data simultaneously. The arbitration logic never stalls a master unless multiple masters are attempting to access the same slave at the same time. Using the SOPC Builder GUI, you can easily specify arbitration priorities.

Software Generation

SOPC Builder automatically generates a software development environment that matches the target hardware. You save days or weeks of design time by using the software components generated by SOPC Builder:

- Header files that define the memory map, interrupt priorities, and data structures corresponding to each hardware peripheral
- Software routines to access system hardware peripherals
- Operating system or real-time operating system (RTOS) kernels with the appropriate drivers to control the system hardware

By guaranteeing that the software components always match the hardware, SOPC Builder can save weeks of debug time especially when the hardware design changes.

System Integration

SOPC Builder saves weeks or months of design time by automating mundane, error-prone tasks of writing the system. After you customize the system architecture, SOPC Builder automatically generates all necessary logic to integrate processors, peripherals, memories, IP cores, on-chip buses, and bus arbitrators. To connect the system components together, SOPC Builder takes system specifications from the system customization step and creates the appropriate VHDL or Verilog HDL code. The result is an HDL description of the entire system.

System Verification

SOPC Builder provides an environment for the simulators of hardware and software. SOPC Builder automatically generates a simulation model of the system, a testbench for it, and a full environment for immediate system simulation. This includes ModelSim® project files, formatted bus-interface waveforms, and a testbench to simulate user software executing on the custom hardware.

Furthermore, Altera development boards provide a means for immediate prototyping of hardware and software. Using development boards, designers can verify their system in hardware, at full system speed, using real-world stimuli. Because the target hardware is programmable, the hardware design can be developed incrementally

Figure 3. Memory Map & Interrupt Priorities for Active Components

Use	Module Name	Description	Bus Type	Base	End	IRQ
✔	⊞ ARM_Stripe	ARM-based Excalibur Stripe	AHB			
✔	⊞ amba_pci_bridge	PLDApplications - AMBA-P...	AHB	0x80000000	0x80003FFF	16
✔	⊞ ahb_avalon_bridge	AHB To Avalon Bridge	AHB | avalon	0x00000000	0x000003FF	
✔	⊞ nios_cpu_0	Altera Nios 2.1 CPU	avalon			
✔	⊞ nios_cpu_1	Altera Nios 2.1 CPU	avalon			
✔	⊞ uart_0	UART (RS-232 serial port)	avalon	0x00000000	0x0000001F	17
✔	⊞ uart_1	UART (RS-232 serial port)	avalon	0x00000020	0x0000003F	18
✔	⊞ ssram_offchip	SSRAM (Micron MT58L256...	avalon_tristate	0x00080000	0x000FFFFF	
✔	⊞ sdram_controller	SDRAM Controller	avalon	0x00800000	0x00FFFFFF	
✔	⊞ pio_7seg	PIO (Parallel I/O)	avalon	0x00000040	0x0000004F	
✔	⊞ pio_ide_interface	PIO (Parallel I/O)	avalon	0x00000050	0x0000005F	19
✔	⊞ timer_0	Interval timer	avalon	0x00000060	0x0000007F	20
✔	⊞ timer_1	Interval timer	avalon	0x00000080	0x0000009F	21
✔	⊞ timer_2	Interval timer	avalon	0x000000A0	0x000000BF	22
✔	⊞ custom_peripheral	Interface to User Logic	avalon	0x00000100	0x0000017F	23
✔	⊞ tri_state_bridge	Avalon Tri-State Bridge	avalon | avalon_trist...			

and downloaded to the board at each phase. Software can be verified and optimized to work on the exact target hardware, rather than just a simulation model.

Evolution of Embedded Design Methodology

SOPC Builder enables very complex systems to be customized, integrated, and verified in much less time than a traditional embedded design. This increased productivity can be attributed to a few fundamental shifts in embedded design methodology.

True Design Automation

Many of the tasks of embedded design are systematic, mundane, and error-prone. SOPC Builder can simplify the design process by automating such tasks as wiring together complex buses or creating software header files. SOPC Builder is more than just a tool that helps you design; it is a tool that creates designs, outputting HDL and software.

Incremental Design

Programmable hardware allows subsystems to be created incrementally, and tested in hardware at each step. Incremental design allows software and hardware developers to work in parallel through much more of the design cycle than in an ASIC-based design flow. For example, the hardware team creates the processor subsystem and passes it to the software team. The software team begins prototyping software immediately. In parallel, the hardware team incrementally develops additional logic.

Performance Optimization & Resource Allocation

Customizable hardware allows you optimize performance by allocating the most appropriate hardware and/or software resources to a given task. Time-critical software tasks can be accelerated with custom hardware much more easily in FPGAs than in traditional processor systems. For example, you can integrate SOPC Builder-Ready IP cores with the CPU to optimize the system's processing and throughput performance. Alternately, you can add application-specific custom instructions to a configurable processor such as the Nios processor, drastically improving performance for software algorithms that use the custom instruction.

Closed-Loop Design

Programmable logic allows the hardware design to evolve to meet the needs of software, thus closing the loop between desired software performance and the actual hardware implementation. You can observe software performance executing on real hardware. If the software needs greater performance for a specific task, you can augment the CPU with hardware acceleration logic.

Software is Integral

In the SOPC Builder methodology, software is viewed as a system component, allowing protocol stacks, OS/RTOS, and other software components to be easily added to a system.

SOPC Builder-Ready IP Cores Now Shipping

SOPC Builder-Ready IP functions are megafunctions that integrate seamlessly into the SOPC Builder development flow. Over 25 SOPC Builder-Ready IP cores are available today from Altera and the Altera Megafunction Partners Program (AMPP℠) partners, which include companies such as Alcatel, Eureka Technology Inc., Mentor Graphics Inventra, and PLD Applications. For a complete list of SOPC Builder-Ready IP and to request a free evaluation copy of the SOPC Builder, visit the Altera web site at **http://www.altera.com/sopcbuilder**.

Availability

SOPC Builder is included in the Quartus II design software, in the Nios Development Kit, and in the Excalibur Solutions Pack.

Stratix

Stratix Devices Now Available

The first Stratix™ device, the EP1S25 device, is available now and is shipping in the packages shown in Table 2. Pin-out tables are now available at **http://www.altera.com**. See Tables 1 and 2 for Stratix availability schedules and software support.

More Stratix Devices Supported by Quartus II Version 2.0 Service Pack 1

Support for the Stratix EP1S10, EP1S20, and EP1S25 devices in the 672-pin ball-grid array (BGA) and FineLine BGA® packages is currently available in the Altera® Quartus® II software version 2.0 service pack 1.

The feature-rich Stratix devices range in density from 10,570 to 114,140 logic elements (LEs) and offer up to 10 Mbits of embedded RAM through its TriMatrix™ memory structure. Stratix devices include up to 28 digital signal processing (DSP) blocks for complex arithmetic functions that require high data throughput. Based on a leading-edge 0.13-μm all-layer-copper SRAM process, Stratix devices support high-speed data transfers through a wide range of high-speed differential and single-ended I/O standards and interfaces. Stratix devices offer up to 12 on-chip phase-locked loops (PLLs) for system-level clock management. In addition, the Terminator™ technology in Stratix devices supports on-chip serial, parallel, and differential termination and driver impedance matching. Stratix devices also offer remote system upgrade capabilities, allowing real-time updates to programmable logic devices (PLDs) from remote locations.

Table 2. Stratix Devices & Quartus II Software Advanced Support Availability

Device	Package	Quartus II Software Advanced Support Availability
EP1S10	672-pin BGA	Now
	672-pin FineLine BGA	Now
	780-pin FineLine BGA	Now
EP1S20	672-pin BGA	Now
	672-pin FineLine BGA	Now
	780-pin FineLine BGA	Now
EP1S25	672-pin BGA	Now
	672-pin FineLine BGA	Now
	780-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP1S30	780-pin FineLine BGA	Version 2.1
	956-pin BGA	Now
	1,020-pin FineLine BGA	Now
EP1S40	956-pin BGA	Now
	1,020-pin FineLine BGA	Now
	1,508-pin FineLine BGA	Now
EP1S60	956-pin BGA	Now
	1,020-pin FineLine BGA	Now
	1,508-pin FineLine BGA	Now
EP1S80	956-pin BGA	Now
	1,508-pin FineLine BGA	Now
	1,923-pin FineLine BGA	Version 2.2
EP1S120	1,923-pin FineLine BGA	Version 2.2

Stratix Support in the Nios Embedded Processor Version 2.1

The Nios® embedded processor version 2.1 includes support for the Stratix device family. Designed to maximize the performance benefits of the Nios embedded processor, the advanced architectural features of Stratix devices combined with the enhanced Nios embedded processor improve the overall system performance of the embedded SOPC Builder to over 125 MHz, offering unparalleled processing power that meets the needs of high-bandwidth systems.

Table 1. Stratix Device Availability

Device	Device Availability	Pin-Out Availability
EP1S10	September 2002	Now
EP1S20	Q4 2002	Now
EP1S25	Now	Now
EP1S30	Q4 2002	Now
EP1S40	Q4 2002	Now
EP1S60	First half of 2003	Now
EP1S80	October 2002	Now
EP1S120	First half of 2003	TBD

EXCALIBUR

Nios Processor Version 2.1 Now Shipping

Altera is now shipping version 2.1 of the Nios embedded processor. This upgrade to the highly successful Nios embedded processor version 2.0 provides optimized compilation support for Altera's new Stratix device family. Version 2.1 of the Nios processor takes advantage of the Stratix architecture, achieving even higher f_{MAX} performance while consuming fewer LE resources. A fully functional Nios embedded processor system in Stratix devices consumes 500 fewer LEs than other Altera architectures and can reach up to 125 MHz. This performance boost, combined with custom instructions and the simultaneous multi-master bus architecture, gives the industry's most powerful configurable processor for programmable logic an even greater performance lead.

This upgrade ships only to customers with a Nios subscription. Customers who purchased the Excalibur™ Development Kit, featuring the Nios embedded processor longer than one year ago must purchase a Nios subscription renewal to receive this upgrade.

Nios Subscription Renewal

Annual subscription renewal is now available for the Nios embedded processor. With the Nios Subscription Renewal Program, you will receive automatic updates to the Nios embedded processor, SOPC Builder, GNUPro® Toolkit, and the Quartus II Limited Edition software for one year for only $495. Contact your local Altera sales representative or visit the Altera web site at **http://www.altera.com/niosrenewal** for more details.

SOPC Builder Now Supports Both Nios & Excalibur Embedded Processors

Altera is now shipping SOPC Builder including support for the Excalibur embedded stripe. Designers can use SOPC Builder to create custom system-on-a-programmable-chip (SOPC) designs based on the Nios embedded processor. Version 2.1 of the SOPC Builder now supports both the Nios and Excalibur processors in the same easy-to-use design flow. SOPC Builder en-

ables designers to easily combine the Excalibur embedded stripe, multiple Nios embedded processors, any of the SOPC Builder-Ready IP functions, and user-defined logic into a single system. SOPC Builder automatically generates on-chip bus logic for both the advanced high-performance bus (AHB) and the Avalon™ bus. Designers gain productivity by avoiding the task of creating bus bridges or multi-master arbitration logic.

You can download evaluation versions of SOPC Builder at **http://www.altera.com/sopcbuilder**. For more information on SOPC Builder, see "SOPC Builder—From Concept to System in Minutes" on page 11.

Excalibur Solutions Pack

The Excalibur Solutions Pack provides software designers with access to Altera utilities and offers a suite of the industry's leading development tools, debugging solutions, and operating system support for building SOPC solutions.

The Excalibur Utilities and Resources CD version 1.4 features the Excalibur stripe simulator (ESS). The ESS facilitates the integration of hardware and software on the Excalibur architecture. Reference designs and updated documentation for the EPXA10 development board and Excalibur devices are also included in the CD.

The third-party tools include evaluation and demonstration versions of system integration tools, debug tools, and operating system support for Excalibur devices:

- Nucleus Plus real-time operating system (RTOS) from the Accelerated Technologies division of Mentor Graphics®
- OSE RTOS from OSE Systems
- Embedded Linux operating system from Red Hat.
- XRAY Debugger for Excalibur Devices from Mentor Graphics
- EASI_Integrator—System Integration tools from Beach Solutions

The Excalibur Solutions Pack is shipped as an upgrade to owners of the Excalibur EPXA10 development kit.

EXCALIBUR™

APEX II

APEX II Availability

All members of the APEX™ II device family are shipping. This family includes the EP2A70 device, which is the industry's first PLD on a 0.13-μm process. APEX II devices range in density from 16,640 to 67,200 LEs and are memory-rich, offering 4 Kbits of memory per embedded system block (ESB), with total device memory ranging from 416 Kbits to 1.1 Mbits. The APEX II device family supports high-speed data transfers through a wide range of high-speed I/O standards such as the LVDS, PCML, LVPECL, HyperTransport™, HSTL, and SSTL standards. With True-LVDS™ circuitry, APEX II devices can achieve data transfer rates of up to 1 gigabit per second (Gbps) per channel. With these I/O features, you can use APEX II devices in the following applications:

- PHY-link layer interface applications (POS-PHY, Flexbus, and UTOPIA)
- Host-processor interface applications (HyperTransport technology, peripheral component interconnect (PCI), and PCI-X)
- Switch fabric interfaces (CSIX and LCS)
- External memory interfaces (double data rate (DDR), zero bus turnaround (ZBT), and quad data rate (QDR) memory devices)

See Tables 3 and 4 for availability and software support for APEX II devices.

APEX II HardCopy Solution

Altera offers a migration solution from APEX II to HardCopy™ devices for system designers who need a low-risk, cost-reduction solution for high-volume production. You can prototype time-sensitive applications using APEX II devices and migrate the design to HardCopy devices for high-volume production. HardCopy devices preserve the functionality and timing of the design and allow you to improve time-to-market at the lowest cost.

APEX II Industrial Offerings

Altera has proactively selected industrial-grade devices of the APEX II device family to further compress design cycles for the fastest possible time-to-market. Industrial-grade production versions of the device offerings are available in a -8 speed grade. Table 5 shows the availability for industrial-grade offerings.

Table 3. APEX II Device Availability

Device	Production Availability
EP2A15	Now
EP2A25	Now
EP2A40	Now
EP2A70	Now

Table 4. APEX II Devices & Quartus II Software Support

Device	Package	Software Support
EP2A15	672-pin FineLine BGA 724-pin BGA	Now
EP2A25	672-pin FineLine BGA 724-pin BGA	Now
EP2A40	672-pin FineLine BGA 724-pin BGA 1,020-pin FineLine BGA	Now
EP2A70	724-pin BGA 1,508-pin FineLine BGA	Now

Table 5. APEX II Industrial Device Offering

Device	Package	Production Availability
EP2A15	672-pin FineLine BGA	Now
EP2A25	672-pin FineLine BGA	Now
	724-pin BGA	Now
EP2A40	1,020-pin FineLine BGA	Now

ACEX

ACEX 1K Availability

ACEX® 1K devices are available in quad flat pack (QFP) and FineLine BGA packages in 576-, 1,728-, 2,880-, and 4,992-LE densities. These cost-optimized devices are specially suited for low-cost, high-volume applications.

To reiterate commitment to the low-cost market-place, Altera has reduced high-volume pricing on ACEX 1K devices and continues to provide the lowest-cost solution in the industry.

Free software support for all ACEX 1K devices is available in the Quartus II Web Edition software version 2.0, which is available for download at **http://www.altera.com**.

MERCURY

Mercury Silicon Available in Production Mode

All devices and all speed grades of the Mercury™ device family are now shipping in production mode, including industrial temperature offerings in both product lines (see Table 6). High-speed 1.25-Gbps serial links featuring clock data recovery (CDR) circuitry and an embedded serializer/deserializer (SERDES) make these devices ideal for serial backplane applications.

Table 6. Mercury Device Availability

Device	Package	Temperature Grade	Production Availability
EP1M120	484-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now
EP1M350	780-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now

APEX

APEX 20KC Available in Production Mode

All APEX 20KC devices are now available with all parts and packages shipping in full production mode. These high-performance APEX devices address the high-bandwidth needs of SOPC applications. They combine the advanced features found in APEX 20KE devices with high-performance 0.15-μm all-layer-copper interconnect technology that provides performance improve-

ments of 25% over aluminum-based devices. Table 7 shows the availability schedule for APEX 20KC devices. All APEX 20KC devices are supported in the Quartus II software, as shown in Table 8.

Table 7. APEX 20KC Device Availability

Device	Production Availability
EP20K200C	Now
EP20K400C	Now
EP20K600C	Now
EP20K1000C	Now

Table 8. APEX 20KC Devices & Quartus II Software Support Availability

Device	Package	Software Support Availability
EP20K200C	208-pin PQFP *(1)*	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K400C	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now

Note to Table 8:
(1)   PQFP: Plastic quad flat pack.

Industrial-Grade APEX Offerings

Industrial-grade APEX devices are now available in a wide variety of package offerings. Refer to Tables 9, 10, and 11.

Table 9. APEX 20KC Device Industrial Offering

Device	Package	Speed Grade
EP20K200C	484-pin FineLine BGA	-8
EP20K400C	652-pin BGA	-8
	672-pin FineLine BGA	
EP20K600C	652-pin BGA	-8
	672-pin FineLine BGA	
EP20K1000C	1,020-pin FineLine BGA	-8

A P E X ™

Table 10. APEX 20KE Device Industrial Offering

Device	Package	Speed Grade
EP20K30E	144-pin FineLine BGA	-2X *(1)*
EP20K60E	144-pin FineLine BGA	-2X *(1)*
	208-pin PQFP	
EP20K100E	144-pin FineLine BGA	-2X *(1)*
	324-pin FineLine BGA	
	356-pin BGA	
EP20K160E	484-pin FineLine BGA	-2X *(1)*
EP20K200E	240-pin PQFP	-2X *(1)*
	356-pin BGA	
	484-pin FineLine BGA	
	672-pin FineLine BGA	
EP20K300E	652-pin BGA	-2X *(1)*
	672-pin FineLine BGA	
EP20K400E	652-pin BGA	-2X *(1)*
	672-pin FineLine BGA	
EP20K600E	652-pin BGA	-2X *(1)*
	672-pin FineLine BGA	
EP20K1000E	652-pin BGA	-2X *(1)*
	672-pin FineLine BGA	

Note to Table 10:
(1)   The "X" denotes PLL and LVDS support.

Table 11. APEX 20K Device Industrial Offering

Device	Package	Speed Grade
EP20K100	208-pin PQFP	-2V *(1)*
	240-pin PQFP	
EP20K200	240-pin PQFP	-2V *(1)*
	484-pin FineLine BGA	
EP20K400	652-pin BGA	-2V *(1)*
	672-pin FineLine BGA	

Note to Table 11:
(1)   The "V" denotes 5.0-V tolerant I/O interfaces.

MAX

MAX Applications Web Page

MAX® devices can help you integrate various functions in your systems. The MAX Applications web site offers detailed technical information on how to implement specific functionality

within MAX devices. Currently the web site details the following applications:

- Using MAX devices in configuration schemes
- Integrating multiple I/O transceivers and buffers into a single MAX device
- Integrating multiple LED driver chips into a single MAX device
- Interfacing with multiple I/O voltages with a single MAX device
- Implementing digital switch matrices using MAX devices

The web site also includes references to white papers and application notes to allow you to quickly and efficiently implement desired functionality within MAX devices. See the MAX Applications web site at **http://www.altera.com** under the MAX 7000 section.

MAX Process Transition

All MAX 7000AE and MAX 3000A devices are being transitioned from the existing 0.35-µm process to an advanced 0.30-µm process. All timing and reliability characteristics for the devices remain within the data sheet specifications. Altera provides a comprehensive Process Transition Report (also referred to as the data pack) for each device that compares the key characterization and reliability data for the two processes. The transition is expected to be complete by the end of June 2002.

For more details, contact your local Altera sales representative.

CONFIGURATION

Enhanced Configuration Devices

Altera enhanced configuration devices support the external flash interface, allowing unused portions of the flash memory to be used as general-purpose memory. This feature is now supported in both the EPC4 and EPC16 devices.

Enhanced configuration devices provide a complete single-device solution for a wide range of density requirements. Vertical migration capability allows you to easily migrate from the EPC4 to the EPC8 to the EPC16 device in the same

package without having to change the board layout. Commercial and industrial grade EPC4, EPC8, and EPC16 devices are all now available.

Enhanced configuration devices offer in-system programmability (ISP) through a built-in IEEE standard for boundary-scan-based, in-system configuration standard of programmable devices (IEEE 1532). The inclusion of ISP and re-programmability provides a significant advantage over one-time programmable solutions by introducing flexibility and reusability to the configuration process.

Altera's enhanced configuration devices also introduce numerous features for specialized configuration needs. These features include parallel configuration capability to accelerate configuration times, a new page mode that allows you to store multiple configurations, block protection for partial reprogramming support, and full clocking flexibility through the programmable clock and external clock features. This advanced feature set enhances the overall PLD design experience.

Design Software

Quartus II Version 2.0 For Linux Now Available

The Quartus II software version 2.0 is now available for the Red Hat Linux version 7.1 operating system, making it the first design software from a programmable logic vendor to run natively on the Linux operating system. The Quartus II software for Red Hat Linux offers a key benefit to UNIX users who prefer the power and flexibility of a UNIX environment and want to take advantage of high-speed, low-cost PC hardware. You can order the Quartus II software for Red Hat Linux version 7.1 by using the following two ordering codes:

- FLOATLNX—multiple-user network licensing for PC and Linux clients
- ADD-FLOATLNX—additional Linux or PC client for a FLOATPC, FLOATNET, or FLOATLNX-based network

Customers with FLOATNET or FLOATPC subscriptions can purchase ADD-FLOATLNX licenses to add support for Red Hat Linux version 7.1 clients to their existing subscriptions.

Introducing the SignalTap II Embedded Logic Analyzer

The Quartus II software version 2.1 will include the SignalTap® II embedded logic analyzer. The SignalTap II logic analyzer includes many enhancements and new features that facilitate debugging complex SOPC designs in-system and at system speeds. For more information, see the "Introducing the SignalTap II Logic Analyzer" article on page 8.

Quartus II Version 2.0 SP1 & SP2 Now Available

The Quartus II software version 2.0 service pack 1 adds advanced and pin-out support for several Stratix devices, adds full support for several Excalibur and APEX II devices, includes final timing models for APEX EP20K200C, EP20K1000C, and Mercury EP1M120C devices, and includes many software enhancements. The Quartus II software version 2.0 service pack 2 includes all of the enhancements of SP1 plus final timing models for Excalibur EPXA1 and EPXA4 devices, full support for APEX II EP2A70 devices, and additional software enhancements. Table 12 includes a complete list of new device-package combination support included in service pack 2.

You can now download the Quartus II software version 2.0 service pack 2 from the Altera web site at **http://www.altera.com**. The web site also includes a form where you can request a CD-ROM version of the service pack by mail.

Table 12. Quartus II Software Version 2.0 Service Pack 2 Support for New Devices			
Support	**Family**	**Device**	**Package**
Advanced compilation and simulation support	Stratix	EP1S10	672-pin BGA, 672-pin FineLine BGA
		EP1S20	672-pin BGA, 672-pin FineLine BGA
		EP1S25	672-pin BGA, 672-pin FineLine BGA
	Excalibur	EPXA1	484-pin FineLine BGA, 672-pin FineLine BGA
Full support, includes Programmer Object File (**.pof**) generation	APEX II	EP2A40	672-pin FineLine BGA, 724-pin FineLine BGA, 1,020-pin FineLine BGA
		EP2A70	1,508-pin FineLine BGA

Contributed *Articles*

El Camino Develops Application to Embed Digital Data into Analog Video Signals

by Wolfgang Loewer,
El Camino GmbH

With digital video and time shifters now available, the needs for transmitting data across analog video channels are changing. To provide electronic or intelligent program guide data to these digital devices, a digital data link based on existing analog channels is needed. For example, service providers could supply TV program guides on the Internet, allowing you to program your VCR at home from the PC in your office. You would register with a unique VCR ID and select the program you want to record. Your service provider could then transmit the information through a normal video channel to all VCRs in the network. Only your VCR with the correct ID would recognize and process the programming information.

El Camino, an Altera® Certified Design Center partner, developed an application that allows designers to embed digital data into a video stream. When analyzing customer design concepts, they discovered mostly analog implementations, which led to tolerance- and temperature-sensitivity issues. Knowing that a data-insertion system must operate on a video stream just before broadcasting, additional requirements like high availability, signal quality, and fallback into a known state become important concerns. As a result, El Camino outlined a digital concept that used a high degree of integration to boost both stability and reliability.

This digital concept required a complete redesign of existing systems, going far beyond minor modifications. A simple prototype was necessary to demonstrate and prove the new system-on-a-programmable-chip (SOPC) approach. Considering the project's schedule and budget, an expensive design of a custom prototyping system was impossible. El Camino decided to partner with Andimedes, an experienced design house in analog and video applications. Andimedes developed a universal analog add-on module, the ANDILAB 76. You can use this module with the Altera Nios® Development Board and the El Camino DIGILAB 1K×208 board. Figure 1 shows the system block diagram.

The design shown in Figure 1 must embed data waveforms on available, blank video lines with a well-defined timing and shape. The design must also receive the embedded data from a host computer and manage the data flow. In this case, all digital signal processing (DSP) is done inside the Altera FPGAs, except the interpolation filter just before the digital-to-analog converter (DAC). The baseband video signal is acquired by the analog-to-digital converter (ADC) on the ANDILAB 76 board and is then sent to the FPGA.

Incorporating embedded data into a video stream requires the partial substitution of video information with data information. Existing video information at locations where data is inserted must be reduced to its neutral blank level. This "clamping" action is usually handled by special video ADCs in the analog domain. A digital clamp replaces analog clamping, taking advantage of the ANDILAB 76 module's 12-bit resolution. The clamping control logic, located inside the block's blank-level capture, compares samples of the incoming video signal to a reference level and sets a

Figure 1. System Block Diagram
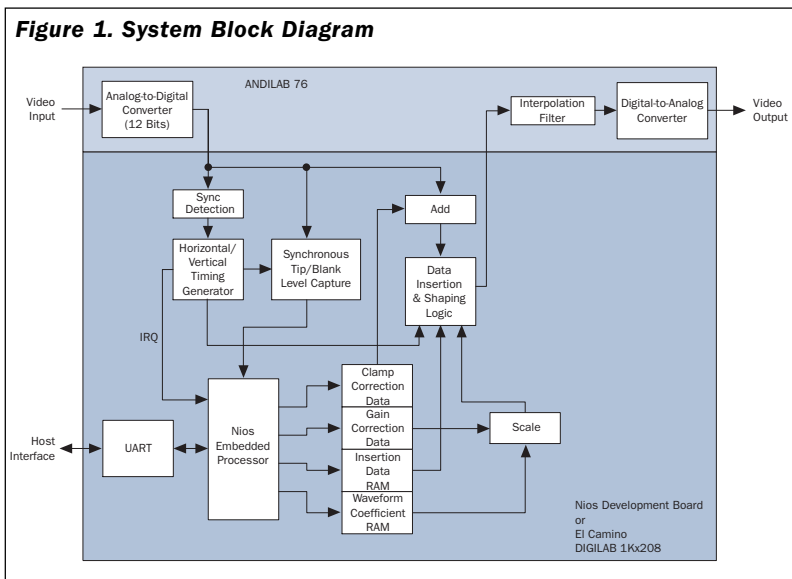
compensation value (clamp correction data). You can add this value to the video signal whenever blanking is active. Blanking control is performed by the Nios embedded processor, which is synchronized by an interrupt at the video-line rate.

The design must also scale the inserted waveform so that it fits the received video level. The video level is extracted by determining the difference between the blank level and the sync-tip level, both provided by their respective capture modules.

The inserted waveform, not the video output, is then scaled to match the video level by weighting the waveform data with the gain-correction data. The "sync-tip and blank-level capture" block smoothes both values and removes noise by averaging two samples.

To make the video timing accessible to other logic modules, a synchronization detection unit together with a horizontal and vertical timing generator is implemented. This block triggers the sync-tip and blank-level capture modules, as well as the data insertion and shaping modules, and generates an interrupt to the Nios embedded processor at the video-line rate.

A major benefit of this digital insertion concept is the absence of the huge filters to shape the inserted data signal. These filters are typically found in analog solutions. The shape of the digital signal is a trade-off between bandwidth occupied and data rate (a square cosine or Gaussian shape is usually preferred). A small shaping state machine fed with waveform coefficients calculated by either the Nios embedded processor or the host is a flexible approach and ensures that the requirements are met.

The data is inserted into the video signal within the module data insertion and shaping logic, which generates the waveforms according to both the waveform shape and the data to be inserted. Finally, the video signal is fed back to the ANDILAB 76 module. The integrated interpolation filter reduces the reconstruction filter's effort.

In general, digital video systems mostly lock their sampling rate to the video signal. Due to the programmable on-board clock generator and the well-defined video timing specification combined with a high sampling rate, this was not necessary during prototyping. The data to be inserted is sent to the Nios embedded processor through the universal asynchronous receiver/transmitter (UART) shown in Figure 1. The Nios embedded processor manages the insertion data RAM and ensures that it neither underflows nor overflows by requesting data from the host system.

Conclusion

By working closely with competent partners, the customer was able to implement the target system in a new and innovative manner, based on an SOPC approach. Key achievements of this project include:

- Switched main implementation from an analog to digital concept, including an embedded processor
- Increased reliability with fewer components
- Better stability and control by using a digital approach
- More flexibility for future enhancements through embedded computing power
- Utilized off-the-shelf and newly developed prototyping systems to initially proof the concept and reduce the overall risk

About El Camino GmbH

El Camino GmbH was founded in 1999 and is a fast-growing competence center focusing on design, training, and consultation related to PLDs. With its background in system-on-chip (SOC) design, El Camino GmbH is a key partner in creating SOPC solutions. For more information on El Camino GmbH and its prototyping systems, visit their web site at **http://www.elca.de**.

About Andimedes GmbH

Andimedes GmbH was founded in 2001 and provides design services and prototyping on general digital and analog signal processing techniques as well as system design. As part of a close cooperation with El Camino GmbH, the ANDILAB 76 analog add-on module was developed and introduced. More information on Andimedes is available at **http://www.andimedes.de**.

A major benefit of this digital insertion concept is the absence of the huge filters to shape the inserted data signal.

Princeton Technology Group Partners with Altera to Provide High-Speed I/O Evaluation Board

"Our evaluation boards will be extremely beneficial to Altera customers involved in designing next-generation SONET, wireless, and data networking applications," said Ted Altman, partner at PTG.

Design engineers implementing telecom systems with high-speed I/O interfaces can now reduce product design cycles and speed time-to-market with Princeton Technology Group's (PTG) high-speed evaluation board. Through the Altera® Consultants Alliance Program (ACAP®) partnership, PTG will provide Altera customers with a Megalogic Apex2A15 evaluation board (see Figure 1) to test APEX™ II FPGA designs that use high-speed protocols such as LVDS, POS-PHY Level 4, RapidIO™, and HyperTransport™ standards.

"The design of the Megalogic evaluation board ensures that the unique competitive features of the APEX II devices, such as support for multiple, cutting-edge bus protocols and standards as well as numerous processing-intensive data path functions, will be evaluated thoroughly," said Hugh Durdan, Vice President of Technical Services at Altera.

"Our evaluation boards will be extremely beneficial to Altera customers involved in designing next-generation SONET, wireless, and data networking applications," said Ted Altman, partner at PTG. "As an ACAP partner, our experience and knowledge of Altera devices allows us to provide a leading-edge evaluation board."

About the Megalogic Apex2A15 Evaluation Board

PTG's Megalogic Apex2A15 evaluation board contains an Altera APEX II EP2A15-7 device in a 672-pin FineLine BGA® package. Future boards will be available for EP2A25 and EP2A40 devices in the 672-pin FineLine BGA package. The board allows designers to test both the true and flexible differential signaling available on the APEX II

Figure 1. Megalogic Apex2A15 Evaluation Board
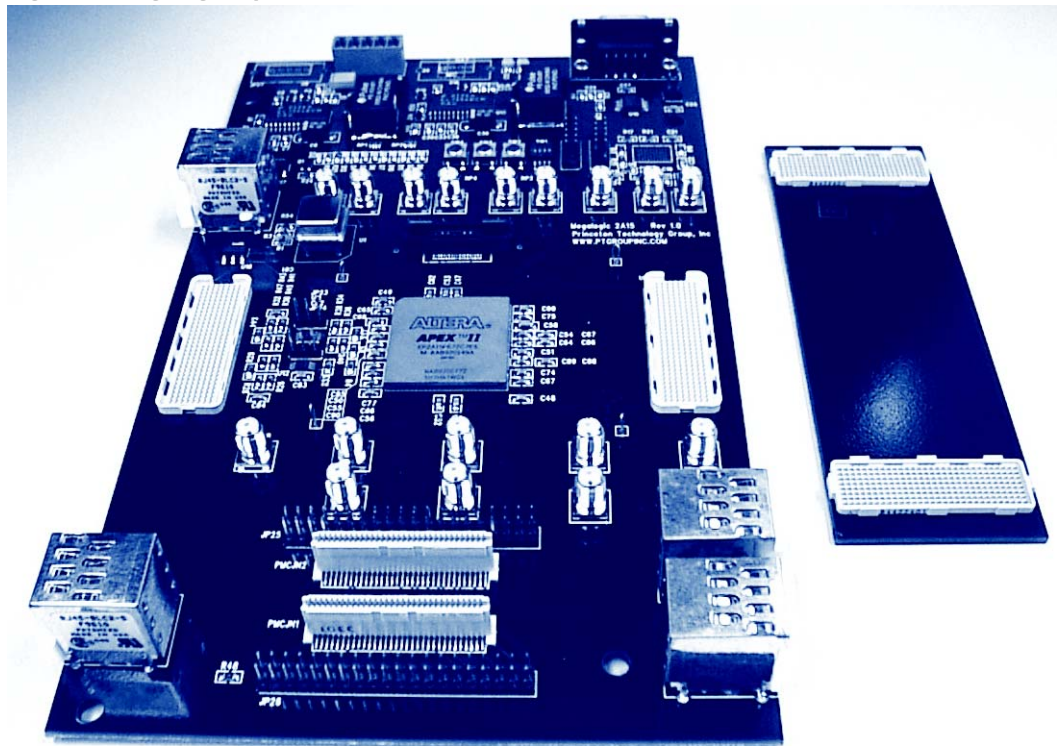
device with speeds up to 1 gigabit per second (Gbps). Other board features include:

- Two high-frequency connectors: transmit and receive
- Transmit and receive RJ45 connectors supporting three True-LVDS™ pairs plus clock
- Transmit and receive RJ45 connectors supporting three Flexible-LVDS™ pairs plus clock
- Numerous SMA connectors
- Eight on-board True-LVDS transmit and receive pairs
- Mictor connector for logic analyzer
- PMC Mezzanine connector shared with 75-pin I/O on 0.1 inch header
- Three push-button and four slide switch inputs
- RS232 I/O port
- Ten LEDs showing board status
- EPC16 configuration device and Joint Test Action Group (JTAG) programmability
- Voltage regulation for single-voltage input

About ACAP

The ACAP partnership is specifically designed to provide expert design assistance to users of Altera FPGAs and help them quickly get their products to market. Additionally, ACAP consultants specialize in niche areas, which makes them particularly effective at solving specific problems and facilitating time-to-market needs.

ACAP partnerships identify consultants based on their knowledge of Altera device architectures and tools, and refer their services and expertise to designers through Altera's broad marketing and sales channel. ACAP consultants are required to attend training sessions provided by Altera, and are encouraged to attend future training sessions.

About Princeton Technology Group

PTG is a closely-knit team of experienced hardware and software engineers committed to the principle that understanding and satisfying clients' needs are the keys to operating a successful business. Two such needs are rapid development cycles and cost-effective designs. PTG believes Altera FPGAs help meet both these goals, and the company has focused business around Altera devices. PTG has worked with Altera devices for more than five years and has successfully implemented a wide variety of designs ranging from motion picture expert group (MPEG) encoders to embedded microcontroller interfaces.

Customer *Applications*

ROWE Engineering Announces Stratix FPGA Development Board

by Sam Trapani,
Director of Marketing,
ROWE Engineering

Company:
ROWE Engineering

Industry:
Communications & DSP Intellectual Property Development

End Product:
Cable & xDSL Modem Physical Layer in VHDL, Communications & DSP Functions, QAM Systems, FPGA Development Boards

Altera Products:
Stratix™ (EP1S25), APEX™ 20KE (EP20K600E) Devices

ROWE Engineering specializes in digital communications and digital signal processing (DSP) intellectual property (IP) development. Typically, ROWE customers are Fortune 100 companies who choose to acquire technology rather than develop it themselves. For several years, ROWE has designed and developed high-end solutions, utilizing high-speed and high-density FPGAs. ROWE's latest products include VHDL code for the physical layer (PHY) of a DOCSIS-compatible cable modem, very high speed digital subscriber line (VDSL) and asynchronous digital subscriber line (ADSL) modems, and local-area network (LAN)/wide-area network (WAN) communications systems development.

With the tremendous growth of the Internet and the need for increased bandwidth, ROWE developed customer-driven solutions geared toward increased bandwidth utilization and efficiency. As a result, the need for real-time processing requiring high-density, high-speed FPGAs interconnected in a way that would easily accommodate such communications development was a concern. ROWE designed an FPGA development board featuring APEX 20KE devices to meet these needs. This first generation was called the Q4 series.

A main design goal was to produce a highly versatile, easy-to-use product. Figure 1 shows that each FPGA has multiple I/O ports that support interfacing with external boards (e.g., analog conversion devices or additional Q4 boards). There are dedicated ports between each FPGA to communicate with neighbor FPGAs as well as a broadcast port that can be used to simultaneously communicate with all other FPGAs. Coupling these ports with the FPGA's fast I/O registers, makes the entire board operate as one large FPGA/ASIC with up to six million gates. Furthermore, you can use this feature to partition your algorithms into pieces, allocating previously integrated work into a single FPGA, while allocating the small incremental part under test into another FPGA. The advantage is quicker system compilation times. Instead of rebuilding the entire function (which could take hours), you can build all the known working functions and then just rebuild the new function under test multiple times.

The Q4 board was designed primarily for digital communications systems design. ROWE has written VHDL code (for the Q4 board) for such complex communications functions as adaptive equalization, timing recovery, carrier recovery, automatic gain control, square root Nyquist pulse shaping filters, and receiver-matched filters designed for quadrature amplitude modulation (QAM) systems with high-density constellations.
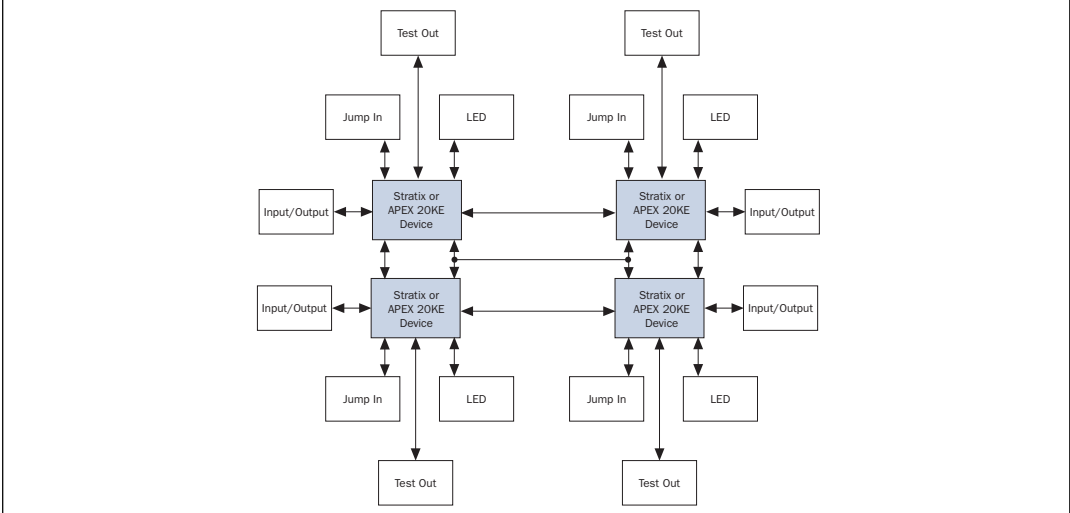
Figure 1. Q4/Q5 Block Diagram

All of these systems fit easily onto one Q4 board equipped with four EP20K600E devices. The Q4 board interfaces easily to analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), allowing the possibility of an integrated transceiver.

With the ever-increasing need for speed, ROWE recently announced the introduction of the new Q5 series of FPGA development boards, featuring Altera's new Stratix devices. These new boards possess significant speed increases over the Q4 series, while providing significantly more logic elements (LEs) and LVDS I/O ports. The Q5 board is intended for communications and optical systems design. The inclusion of LVDS interfaces allows for an 840 megabits per second (Mbps) transfer rate on a multitude of inputs. Stratix devices allow even higher sampling rate support than APEX 20KE devices. Also, the Q5 board supports a dual-independent clocking rate generation for systems designed for synchronization experiments. Thus, a single Q5 board is capable of implementing both sides of a transceiver with separate clocking for the transmitters and receivers. The Q4 and Q5 block diagrams are similar, except that the Q5 board includes LVDS ports. The first production Q5 boards will feature Stratix EP1S25 devices. There are three different versions of the Q5 boards, Q5.V1, Q5.V2, and Q5.V4 boards, which will have one, two, and four Stratix FPGAs, respectively. As Altera releases oth-er Stratix devices, ROWE will include them in the Q5 family of boards. Figure 2 shows the Q4.V4 board. The new Q5 series of boards will be similar.

Figure 2. Q4 Development Board
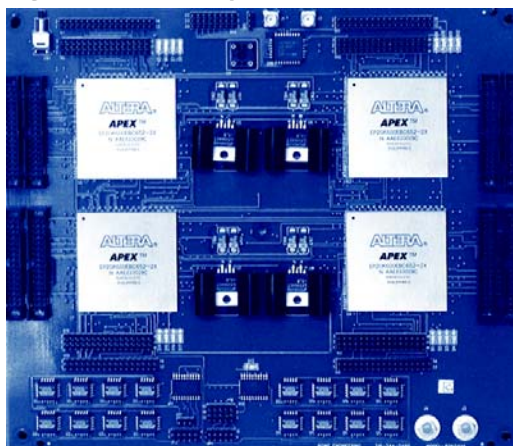
One of the new design applications for ROWE's Q5 Stratix-based boards will be implementation of a 50 megabits per second (Mbps) symmetrical DSL modem PHY in VHDL. In addition to the Q5 board, ROWE will market the sale of the IP and source VHDL that accompanies the algorithms used to implement the DSL transceiver.

For more information, visit the ROWE web site at **http://www.roweengineering.net**.

ROWE has written VHDL code (for the Q4 board) for such complex communications functions as adaptive equalization, timing recovery, carrier recovery, automatic gain control, square root Nyquist pulse shaping filters, and receiver matched filters designed for QAM systems with high-density constellations.

Altera's EP20K30E Device Cornerstone for PCMCIA-Based Camera

In the summer of 2001, MediaWorks Technology Corporation developed a PCMCIA-based color VGA video camera compatible with the Compaq iPAQ (or any other Pocket PC device that supports a PCMCIA interface).

At COMDEX 2001, PocketMultimedia, a division of Anteon Corporation, won awards based on their presentation of a camera that plugs into a Compaq iPAQ and allows the wireless transmission of video images to other iPAQ devices. The camera that PacketMultimedia used was the MediaWorks camera (see Figure 1).

This color VGA camera is a unique motion camera with a maximum image of 640×480. It utilizes a sensor capable of generating 320×240 (QVGA) images at the rate of 60 frames per second in the YCrCb 4:2:0 format. This format is the starting point for various compression algorithms such as MPEG-4. This camera allows you to develop various wireless video applications such as video e-mail and video conferencing. The Y portion of the YCrCb data can be used alone to generate black and white images if desired. The camera can also capture still images.

The risk and cost of trying to design the PCMCIA camera starting with an ASIC was too high, especially given the need to generate a prototype in three months. MediaWorks decided to use the Altera APEX™ EP20K30EF324 device as the cornerstone of its design solution. Altera was selected because of its HardCopy™ solution that offer a seamless migration from prototype to volume production.

The Design

This PCMCIA-based camera accepts inputs from a digital video interface and allows interfacing to a standard 3.3-V PC card bus. The card is powered from the 3.3-V PC card bus and provides a DC-to-DC conversion for +5.0-V power to the video interface and 1.8-V internal power for the FPGA.

The FPGA design was straightforward. The logic contained in the EP20K30EF324 device performs the following functions:

- PC card interface which utilized PCMCIA intellectual property (IP) from Mentor Graphics®)
- Card information structure (CIS) memory
- Extended attribute memory for I²C camera control
- EEPROM microwire interface
- I/O interface (16 bits) for video data
- Image frame buffer control and timing
- Image format conversion (4:2:2) to (4:2:0) and image banding

Due to the height requirements of the Type II PCMCIA slot, the FPGA needed to be a FineLine BGA® package.

The time from project start to completion was three months. PocketMultimedia would not have met this schedule without the capabilities of the APEX EP20K30EF324 device, the availability of cost-effective MegaCore® IP, and the help of Altera's technical support team.

Future Direction

MediaWorks' camera has been used and seen by other companies, and a reduced-cost version will be available during Q4 2002.

The product roadmap for the camera has several branches besides the previously mentioned low-cost production version. A second path is a development platform for advanced security and camera development. This version would keep the FPGA, and use a larger FPGA with room for multiple Nios® processors or an Excalibur™ embedded processor to allow various encode, decode, and blob-detection algorithms to be implemented on the PCMCIA card. A third path is the integration of wireless communications with the camera functionality. This wireless communication will be in the form of cellular modem or 802.11 technology.

Besides these PCMCIA versions of the design, MediaWorks is in the process of translating the design to a stand-alone remote presence/security camera. This camera will utilize IP to encode the image, which would then be sent to a central location via a hardwired or wireless network.

About MediaWorks Technology Corporation

MediaWorks Technology Corporation, an Altera Consultants Alliance Program (ACAP®) member, specializes in multimedia system-on-chip (SOC) architectures and design services. MediaWorks Technology Corporation is a Illinois-based company that is defining the "appliance era" of computing.

MediaWorks delivers the performance of a custom processor design to go "beyond DSP" at the cost of a generic microprocessor. MediaWorks' unique knowledge of cutting-edge tools, proven design processes and methodologies, combined with their precision-re-targetable architecture, delivers results fast.

MediaWorks is a chip design company that also does system-level service work. Current and previous projects besides the camera and its variations include telematics devices, audio, and audio/visual chips and systems along with related IP.

For more information on MediaWorks Technology Corporation, visit their web site at **http://www.mwsoc.com**. You can also contact MediaWorks at their web site for information on how to get these PCMCIA cameras.

MediaWorks delivers the performance of a custom processor design to go "beyond DSP" at the cost of a generic microprocessor.

Figure 1. MediaWorks PCMCIA Camera

ETAS Improves Automotive Control System with Excalibur Devices

Company:
ETAS GmbH

Industry:
Automotive

End Product:
Tools for Embedded
Control Systems

Altera Products:
Excalibur™ Devices

ETAS GmbH produces flexible, integrated tools for all phases of automotive embedded control systems development—from design and rapid prototyping, to hardware-in-the-loop testing, production code generation, documentation, and in-vehicle calibration. ETAS' ES1000.2 monitors various car sensor outputs. It can be used to develop motor ignition and camshaft angle patterns, and develop a complete motor management system.

ETAS included the Excalibur™ EPXA4F1020C2 device into its ES1303.1 high-speed analog-to-digital converter (ADC) interface. The VME-card ES1303.1 is a new ADC interface for the ES1000.2 system. A maximum of four ES1303.1 ADC conversion interfaces can work together in one ES1000.2. The ADC interface card has 16 analog inputs with galvanic isolation between each ADC channel. The advantage of this design is high common mode rejection. Simultaneous analog-to-digital conversion of all 16 channels at a maximum sampling rate of 100K samples per second is possible. Figure 1 shows the ES1000.2 system board.

Figure 1. ES1000.2 System Board

Altera's Design Win Advantages

Altera has provided the following key advantages in this design:

- Excalibur EPXA4 device
- High-performance embedded processor
- Embedded SDRAM controller
- Embedded trace module
- Flexible programmable logic device (PLD) area
- Large number of general-purpose I/O pins
- Sophisticated software and tool flow
- Sales support

These advantages allowed the customer to reduce this specific ADC-module from a four VME-card system down to a one VME-card system. ETAS was also able to put more ADC channels in the module and achieve a much more flexible system that allows more customization.
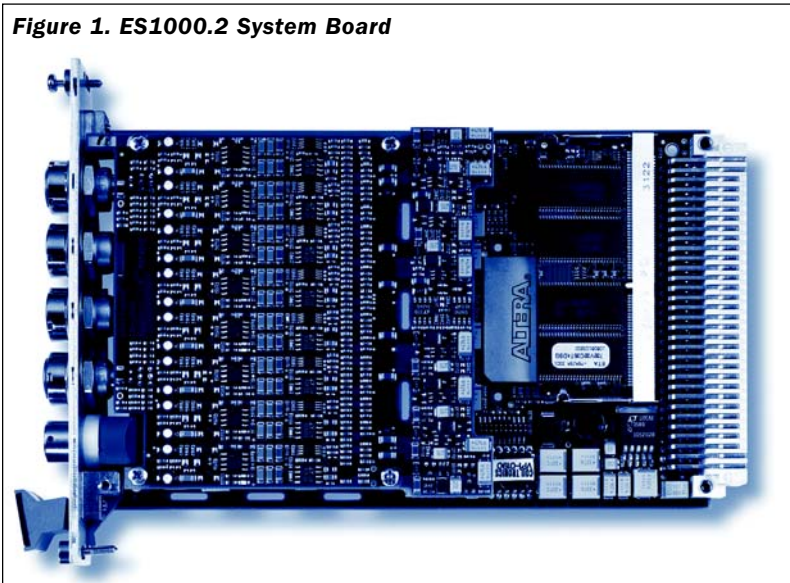
Conclusion

In combination with excellent sales support and Altera's dedication to customer satisfaction, this design win illustrates the higher flexibility and integration that is possible with Excalibur devices.

About ETAS

ETAS GmbH was founded in 1994 as a subsidiary of Robert Bosch GmbH and has its head office in Stuttgart, Germany. Robert Bosch GmbH supplies the automotive industry with fuel injectors, ABS, alternators, starters, and other electronic car equipment. ETAS manufactures a complete spectrum of engineering tools for embedded control systems in the automotive industry.

Implementing a Barrel Shifter Using Stratix DSP Blocks

Stratix™ devices feature high-performance digital signal processing (DSP) blocks that consist of embedded multipliers, adders, subtractors, accumulators, and summation units. While DSP blocks are traditionally viewed as functional units that can implement complex arithmetic operations, you can also use DSP blocks to implement certain commonly found non-arithmetic operations such as barrel-shifting, wide multiplexers, and cross-bars. This article outlines the implementation of barrel shifters using DSP blocks. Barrel shifters are found extensively in communication applications such as asynchronous transfer mode (ATM) switches and 10-Gigabit Ethernet.

Barrel Shifters

Barrel shifters can shift data by a specified number of bits, and can be unidirectional (left shift only or right shift only) or bidirectional (shift in either direction). Barrel shifters can also perform a left rotate or a right rotate of the data bits. Figure 1 shows examples of the various shift operations.

Relation Between Multiplication & Shift

Performing a left-shift operation is the same as multiplying the data by 2^n where n is the number of bits that the data shifts. Performing a right-shift operation is the same as dividing the data by 2^n where n is the number of bits that the data shifts, as shown in Figure 2.

Implementing a Barrel Shifter Using DSP Blocks

Since DSP blocks feature multipliers, you can implement a barrel shifter in Stratix devices using DSP blocks (see Figure 3). The decoder converts the distance (number of bits the data has to be shifted) to an appropriate multiplicand. For example, if the distance is two bits, the decoded multiplicand will be $2^2 = 4$. This decoded multiplicand and the data are then multiplied using the DSP block. The DSP block returns a product that has full precision. Therefore, if the data is 16 bits wide, the output will be 32 bits wide. For left-shift operations, only the 16 least significant bits (LSBs) are needed, which are then tapped off to the output.


Figure 1. Types of Shift Operations
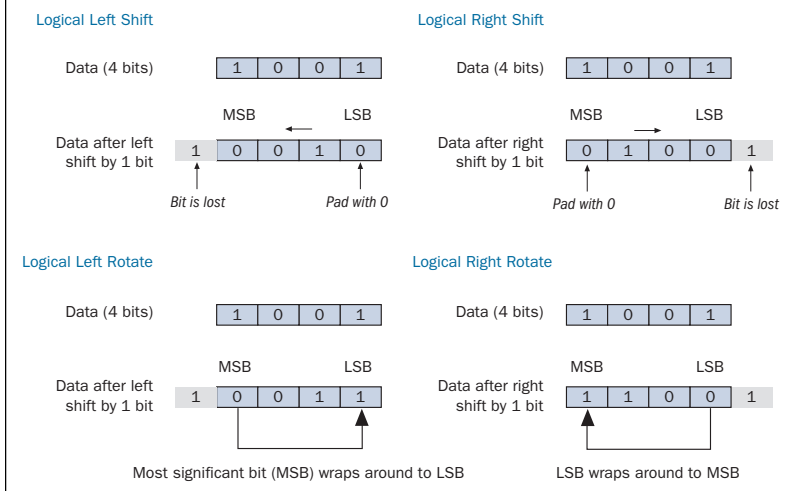
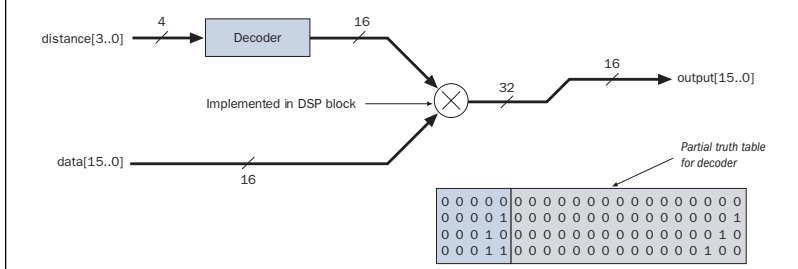## Implementing a Multi-Word Barrel Shifter Using DSP Blocks

You can also use DSP blocks for implementing barrel shifters that shift multiple data inputs by the same distance, as shown in Figure 4 on page 30. The multi-word barrel shifter implementation provides excellent logic element (LE) savings since only the decoder requires LEs, while the multipliers fit into the DSP blocks.

Figure 2. Relationship Between Shift Operations & Multiply
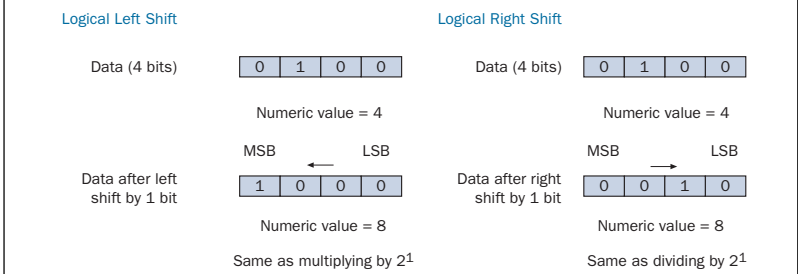
Figure 3. Left-Shift Barrel Shifter Using DSP Blocks

Performance & Implementation Results

The performance of the barrel shifter is determined mainly by the speed of the multipliers. For Stratix devices, the multipliers in the DSP block offer a frequency of more than 250 MHz. Therefore, the performance of the barrel shifter will also be very high. The size of the decoder determines how many LEs are used. The multipliers required by this implementation are mapped to the DSP block and do not impact the LE count. Table 1 shows the results for an implementation of a 16-word barrel shifter where each word is 8 bits wide. The design has a latency of two clock cycles arising from the input registers and uses pipeline registers inside the DSP block for higher performance.

For Stratix devices, the multipliers in the DSP block offer more than 250 MHz of performance.

Table 1. 16-Word Left Barrel Shifter Implementation Results

Bit Width	LE Count	Number of DSP Blocks	Performance (MHz)
8	8	2	280
16	16	4	230

Conclusion

Stratix DSP blocks offer an efficient implementation of barrel shifters. The performance of such barrel shifters is dependent on the speed of the high-performance multipliers inside the DSP blocks. This implementation offers significant LE savings over a pure LE-based barrel-shifter implementation.
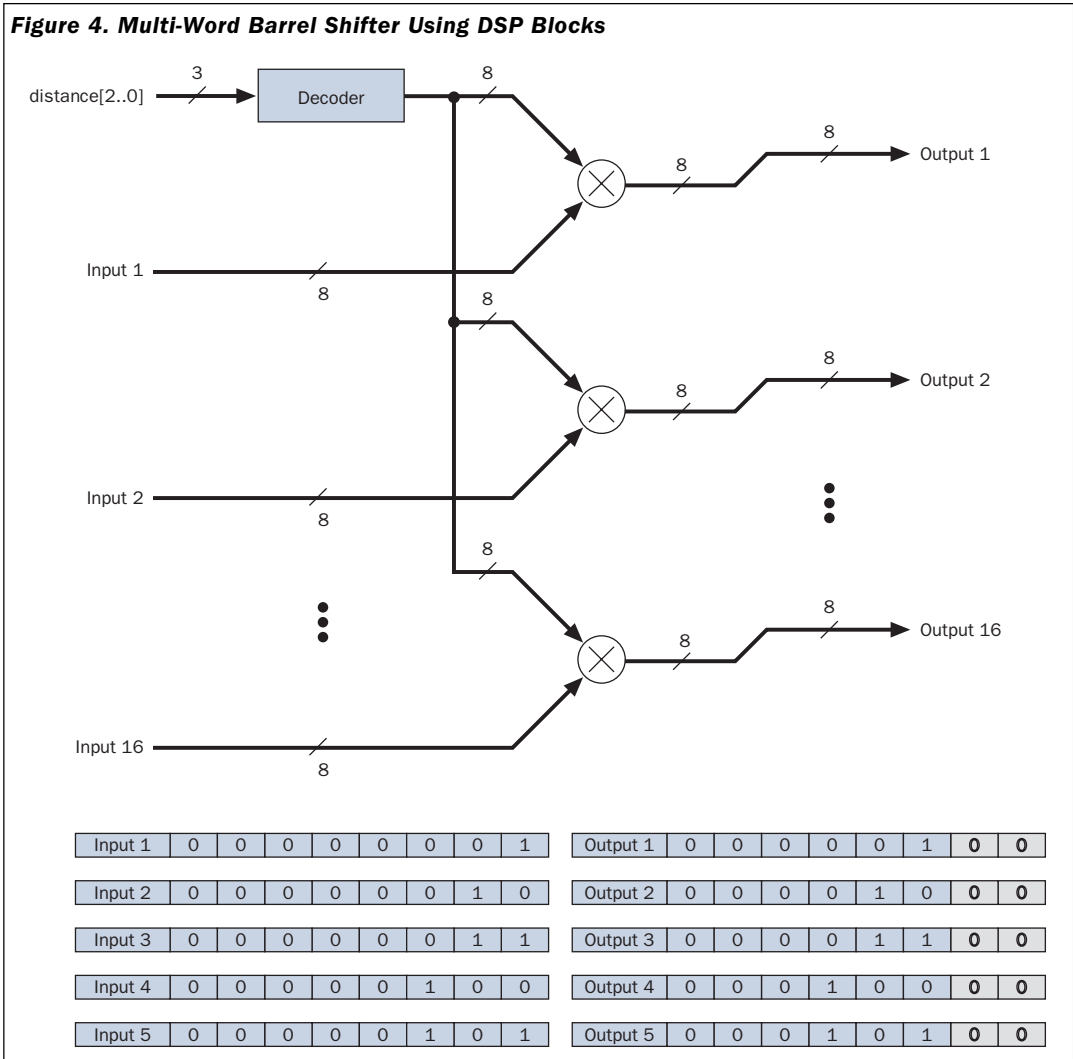
Figure 4. Multi-Word Barrel Shifter Using DSP Blocks

Input 1	0	0	0	0	0	0	0	1
Input 2	0	0	0	0	0	0	1	0
Input 3	0	0	0	0	0	0	1	1
Input 4	0	0	0	0	0	1	0	0
Input 5	0	0	0	0	0	1	0	1

Output 1	0	0	0	0	0	1	**0**	**0**
Output 2	0	0	0	0	1	0	**0**	**0**
Output 3	0	0	0	0	1	1	**0**	**0**
Output 4	0	0	0	1	0	0	**0**	**0**
Output 5	0	0	0	1	0	1	**0**	**0**

Stratix Devices Provide Unprecedented Performance & Area Utilization for DSP Applications

Stratix™ devices embed digital signal processing (DSP) functionality through the DSP block. The DSP block is a highly efficient and flexible feature that provides high-performance arithmetic computation capability such as multiplication, addition, subtraction, accumulation, and summation. Offering up to 10 Mbits of RAM and up to 12 terabits per second of device memory bandwidth, the Stratix TriMatrix™ memory structure caters to the memory needs of DSP applications.

The performance of most DSP applications is limited by the multipliers. Embedded hardware multipliers (such as the multipliers inside DSP blocks) not only run at high speeds but also provide area savings. The DSP block has its own dedicated routing resources between the various arithmetic units. The dedicated routing ensures predictable high performance that is essential for DSP applications. For example, the multipliers inside the DSP block can run as fast as 250 MHz. Therefore, DSP blocks can eliminate performance bottlenecks in 3G wireless basestations and voice over Internet protocol (VoIP) gateway applications.

Performance Improvements for DSP Algorithms in Stratix Devices

Finite impulse response (FIR) filters, fast Fourier transforms (FFT), numerically controlled oscillators (NCOs), and Reed-Solomon encoders/decoders are the most commonly used functions in DSP applications. These functions rely heavily on the multiply or the multiply-accumulate operations that often become the performance-limiting factor in a system. Stratix DSP blocks can improve performance due to the high-speed embedded multipliers and other arithmetic units. The following sections highlight the benefits of the Stratix architecture by using three key DSP functions: FIR, FFT, and NCO.

FIR Filter

The FIR filter is the most commonly used DSP function and is based on summation of product terms where each product term is calculated by multiplying a coefficient and a delayed data input. DSP blocks feature dedicated multipliers and

adders that are optimized for calculating such a summation of product terms. The dedicated multipliers reduce logic element (LE) count as well as improve overall clock speeds. Altera's FIR filter MegaCore® function takes advantage of Stratix DSP blocks to increase performance and logic utilization (see Table 1).

FFT

The basic computation unit of an FFT is the butterfly unit. The butterfly unit performs a complex multiplication of data points with sine and cosine values, which are referred to as twiddle factors. Stratix DSP blocks, which contain four 18-bit multipliers and adder blocks, are ideally suited to perform the complex multiplication operation in a single-clock cycle.

Multipliers are the main contributor to the size of an FFT, and are also the performance bottleneck. The clock frequency depends on the performance of the place-and-route tool. DSP blocks reduce the number of LEs and guarantee optimal timing for this timing-critical component due to the dedicated routing resources inside the DSP block. Table 2 shows the results of the Stratix device FFT implementation.

Table 1. FIR Implementation Results

	EP20K100EBC356-1	EP1S10F780C6	Stratix Advantage	Parameter
LEs	6,400	2,450	62%	37 taps, 8-bit input, 8-bit coefficient, fully pipelined
f$_{MAX}$ (MHz)	180	210	17%	

Table 2. FFT Implementation Results

	EP20K100EBC356-1	EP1S10F780C6	Stratix Advantage	Parameter
LEs	3,301	1,227	63%	Float width = 5, Data width = 16
f$_{MAX}$ (MHz)	98	202	52%	Twiddle width = 18
Transform Time (μsec)	53.11	25.78	51%	Points = 1,024, Radix = 4

Stratix Devices Provide Unprecedented Performance & Area Utilization for DSP Applications, continued from page 31

NCO

Altera's NCO Compiler generates high-precision sinusoidal waveforms for use in communication systems as intermediate frequency (IF) mixer oscillators and as reference generators in carrier recovery circuits (e.g., all-digital phase-locked loops (PLLs)).

The architectural features of the Stratix family resources allow you to obtain a high-performance NCO that can produce high-precision output waveforms and continue to provide resource savings.

You can use the high-performance dedicated multipliers to generate low-latency IF carriers at sample rates in excess of 200 million samples per second (MSPS). A new multiplier-based architecture utilizes the Stratix DSP blocks to implement high-precision, high-performance NCOs. This architecture requires fewer memory resources for a given spectral purity. A variable-pipeline-depth parallel CORDIC architecture generates sinusoidal waveforms by successive approximation implemented as shifters, comparators, and signed adders/subtractors in LEs. The enhanced arithmetic mode of the Stratix LE favors this algorithm leading to savings in LE counts over previous device families and yielding tremendous performance enhancements for high-quality oscillators. In ROM-based architectures, the Stratix blocks support high-precision NCO implementation. The high-speed synchronous memory enables generation of high-frequency carriers.

The Stratix architecture allows you to obtain a high-performance NCO that can produce high-precision output waveforms and continue to provide resource savings. Table 3 shows the results of such an NCO implementation.

Stratix devices lead to higher performance and area savings for many DSP functions, which are reflected as higher system-level performance and efficiency of implementation. The following case study for a digital down converter (DDC) provides an example of the kind of efficiency you can see with Stratix devices.

Case Study: Digital Down Converter

DDC is commonly used in 3G wireless systems for translating signals from a broadband frequency to baseband frequency. A typical DDC implementation consists of an NCO, mixer, cascaded integrator comb (CIC) filter, and a pulse-shaping decimator filter, as shown in Figure 1.

Figure 1. DDC Block Diagram
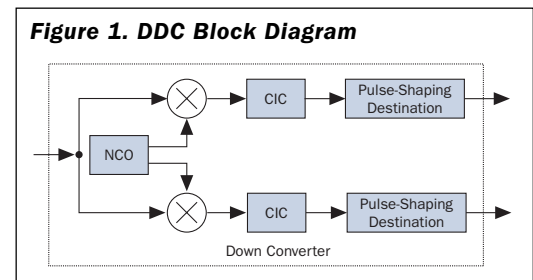
You can implement a DDC in an APEX™ 20KE device by designing a single-channel DDC using an NCO, two 18-bit multipliers, a decimate by eight CIC, a decimate by two 21-tap FIR filter, and a decimate by two 63-tap FIR filter. This solution could achieve 110+ dB spurious free dynamic range (SFDR) and achieve 125 MHz in APEX 20KE devices. A single channel would require an EP20K200E device for this type of implementation.

With this same implementation, you can fit four channels in Stratix EP1S10 devices by using the DSP blocks and TriMatrix™ memory to achieve performance of over 200 MHz. This implementation represents nearly a 4× channel density increase and nearly a 2× performance increase.

Conclusion

The advanced high-performance features of Stratix devices such as DSP blocks and TriMatrix memory provide unprecedented performance as well as resource savings in DSP applications. Stratix architecture simplifies DSP design to meet the needs of emerging DSP applications.

Table 3. NCO Implementation Results

	EP20K100EBC356-1	EP1S10F780C6	Advantage	Parameter
LEs	321	189	41%	Small ROM, 32-bit accumulator precision, 14-bit angular precision, 16-bit magnitude precision
f_MAX (MHz)	161	255	57%	

Configuring Altera's FPGAs Using the MicroBlaster Source Code & the Motorola MCF5206e (ColdFire) Embedded Processor

The MicroBlaster is a software driver that allows you to configure Altera's FPGAs in passive serial mode and is targeted to embedded configuration. As a proof-of-concept study, the source code was customized and implemented in a Motorola ColdFire embedded processor, using Motorola's MCF5206e Design Matrix Evaluation System. This article discusses the implementation of the MicroBlaster source code on the Motorola MCF5206e development board.

Figure 1. MicroBlaster Implementation Block Diagram

MicroBlaster on ColdFire

This design implements the MicroBlaster source code on the Motorola MCF5206e evaluation board. The on-board memory is a 4-Mbyte ADRAM SIMM. The targeted FPGA is an APEX™ 20KE EP20K200E device. The code size of the MicroBlaster is less than 20 Kbytes.

Block Diagram

Figure 1 shows the implementation block diagram of the MicroBlaster configuration on the ColdFire development board.

There are three main blocks in the implementation process: the parallel port, the ColdFire development board, and the FPGA test board. Among those blocks, there are three interfaces that involve different stages of the implementation process, which will be discussed in the following sections.

Instruction Download

The original and the customized MicroBlaster source code are written in C language. The source code is compiled and linked using the Metrowerks CodeWarrior software. The raw binary file (**.rbf**) is downloaded into the ColdFire development board using the software through the program and evaluation background debug mode interface cable. Once the instruction download is complete, the ColdFire processor starts executing the instructions and will keep reading at its parallel port (general-purpose I/O) for data.

Download (.rbf)

While the ColdFire processor is reading at its parallel port, the PC will start to dump the contents of the **.rbf** bit by bit to the parallel port. The bit stream is then processed and stored in the memory. There are two signals that are involved in this process: DATA and CLOCK.
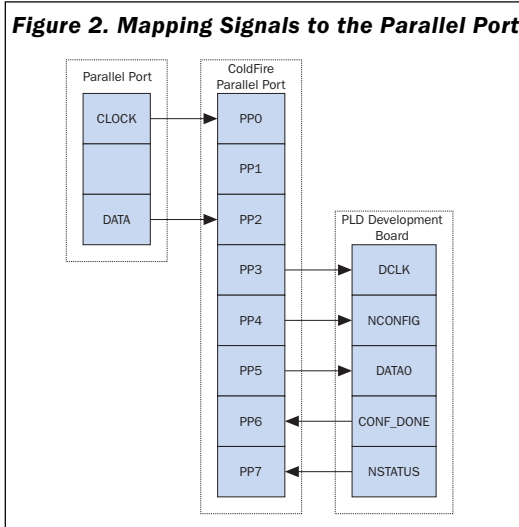
Configuration

At this stage, the on-board ADRAM is loaded with the configuration data, but the FPGA is not configured yet. The FPGA is configured in passive serial mode and involves five configuration signals (DCLK, DATA0, nCONFIG, nSTATUS, and CONF_DONE). These signals are mapped to five pins of the ColdFire parallel port where three pins are set as output and two pins are set as input, with reference to the ColdFire development board. Figure 2 on page 34 shows the pin mapping.

During the **.rbf** download stage, when catching a positive-edge-trigger signal at the CLOCK, the value of the DATA signal is processed and written into the on-board ADRAM. The DATA signal is processed by putting its data bit in the appropriate parallel port registers (PP0-PP7) before writing to the ADRAM. As shown in Figure 2, the PP5 register holds the data that will be dumped to the DATA0 signal of the FPGA development board during configuration. Therefore, the data bit read from the PP2 register (DATA signal from PC par-

The MicroBlaster is a software driver that allows you to configure Altera's FPGAs in passive serial mode and is targeted to embedded configuration.

Configuring Altera's FPGAs Using the MicroBlaster Source Code & the Motorola MCF5206e (Cold-Fire) Embedded Processor, continued from page 33

Figure 2. Mapping Signals to the Parallel Port

The customized MicroBlaster driver allows fast and easy configuration and requires no extra boards or components between the embedded system and the PLD test board.

allel port) is shifted to the PP5 register. Meanwhile, the PP3 register (map to the DCLK signal) is set to 0, and the byte (PP0-PP7) is written to the ADRAM.

When you initiate the FPGA configuration by driving a transition of LOW to HIGH signal on the nCONFIG pin, the first byte is loaded from the on-board ADRAM and then dumped to the ColdFire parallel port registers. The byte is then bit-wise OR'd with 0×08 to set the PP3 register (map to the DCLK signal) to a bit 1. The modified byte is then dumped to the ColdFire parallel port registers again. This process produces a positive transition (from a bit 0 to a bit 1) of the DCLK signal for every DATA0 bit sent to the FPGA development board.

The following examples only involve the DATA0 and DCLK signals.

Bytes loaded from the ADRAM (PP7-PP0):

```
Byte 1: XX1X0XXX
Byte 2: XX0X0XXX
...
```

Sequential dumps as observed on the ColdFire Parallel Port (PP7-PP0):

```
Dump 1: XX1X0XXX
Dump 2: XX1X1XXX
Dump 3: XX0X0XXX
Dump 4: XX0X1XXX
...
```

This process speeds up the configuration time but requires more memory space.

Occasionally, the nSTATUS pin senses to check for a configuration error. Once the configuration is done, the CONF_DONE signal is sensed to determine if the configuration process is successful. Depending on the parameter set in the MicroBlaster source code, the ColdFire embedded processor may reinitiate the configuration process if the configuration is not successful.

Conclusion

The MicroBlaster is a software driver developed for embedded passive serial configuration. You can easily customize the MicroBlaster source code to fit in different embedded systems. The system in this case is a Motorola MCF5206e Design Matrix Evaluation System. The customized MicroBlaster driver allows fast and easy configuration and requires no extra boards or components between the embedded system and the FPGA test board. In addition, the source code development and customization cycle is short. All of these features make the MicroBlaster an ideal solution for embedded passive serial configuration. The original and customized MicroBlaster source code is available at **http://www.altera.com**.

Altera Features On-Line Solution Centers

Altera Corporation recently launched its on-line solution centers to help you with your system-on-a-programmable-chip (SOPC) applications. Each solution center features design information on Altera devices, software, intellectual property (IP), and design examples. With all information in one location, the Altera solutions centers are "one-stop shops" for design help.

Memory Solutions Center

Altera offers programmable logic solutions with the latest memory technologies, abundant on-chip memory resources, and off-chip data storage with support for external memory interfaces.

DSP Solutions Center

Altera provides a comprehensive DSP solution consisting of complete design software environment, performance-optimized devices, and DSP-related IP. See Figure 1.

I/O Standards & Interfaces Solutions Center

Altera provides a comprehensive I/O interface solution with support for a variety of single-ended and differential I/O standards, external memory interfaces, and high-speed interfaces.

Networking, Wireless & Telecom Solutions Centers

Altera SOPC solutions allow system implementation of networking functions such as quality of service (QoS), multiprotocol label switching (MPLS), and voice-over-Internet-protocol (VoIP); implementation in third-generation (3G) wireless systems, local multi-point distribution service (LMDS), and multi-channel multi-point distribution services (MMDS); and implementation of telecommunications functions such as SONET/SDH systems.

For more information, visit the Altera web site at **http://www.altera.com/solutioncenters.com**.

Altera offers programmable logic solutions with the latest memory technologies, abundant on-chip memory resources, and off-chip data storage with support for external memory interfaces.

Figure 1. DSP Solutions Center

Costs of Using PLDs vs. ASICs

The Altera® web site now offers a tool to help you determine whether a programmable logic device (PLD) is more profitable to use than an ASIC. The PLD vs. ASIC Project Cost Calculator helps you make a decision by modeling a detailed revenue analysis. This model includes variables such as cost of software tools and engineering salary, projected gross margin, and product selling price. After entering the parameters of a project, the calculator shows a quarter-by-quarter breakdown of the revenue and costs of a project.

The calculator is designed to analyze different scenarios for a project, and immediately shows

The calculator is designed to analyze different scenarios for a project, and immediately shows the impact on the profitability of the project.

the impact on the profitability of the project. For example, one project scenario may involve migrating a design for high-volume production to a HardCopy™ device. The other scenario may not include a migration to a HardCopy device. You can simulate both scenarios, and you can immediately determine the impact on profitability.

You can try out the PLD vs. ASIC Project Cost Calculator on the Altera web site at **http://www.altera.com/pldvsasic.**

Figure 1. PLD vs. ASIC Cost Calculator

Discontinued Devices Update

Altera will be obsoleting select devices from product-term and FPGA families (see Table 1). Most of the devices will have longer than usual last-time buy (18 months) and last-time ship dates (an additional 6 months) to allow customers to gradually transition to using alternative ordering codes.

Select ordering codes from mature families such as MAX® 7000S are being obsoleted to increase the operational efficiency in the manufacturing flow. On mainstream product families such as the MAX 7000A, FLEX® 10KE, APEX™ 20K and newer product families, such as the MAX 7000B, ACEX® 1K, and APEX 20KE, ordering codes have been consolidated to offer a limited set of codes that will cover the various package / speed grade options.

Continued support for devices beyond the phase out period may be available through Rochester Electronics, an extended after-market supplier. For more information, contact Rochester Electronics at (508) 462-9332 or your local Altera sales office.

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Table 1. Discontinued Device Update				
Product Family	**Device**	**Last Order Date**	**Last Shipment Date**	**Reference**
MAX 7000	Selected devices with a dry pack option	05/31/02	11/30/02	PDN 0117
	EPM7192EGM160-15	05/31/02	11/30/02	PDN 0117
MAX 7000S	Selected devices in plastic quad flat pack (PQFP) and thin quad flat pack (TQFP) packages	05/31/02	11/30/02	PDN 0117
	Selected devices with fixed-pulse width programming option	10/31/03	04/30/04	PDN 0203
MAX 7000A	Selected devices in micro ball-grid array (BGA), FineLine BGA™, and TQFP packages	10/31/03	04/30/04	PDN 0203
MAX 7000B	Selected devices	10/31/03	04/30/04	PDN 0203
MAX 9000	EPM9560BC356-20	05/31/02	11/31/02	PDN 0117
	EPM9320RC208-15F	05/31/02	11/31/02	PDN 0117
FLEX 8000	Selected FLEX 8000 pin-grid array (PGA) packages	02/28/02	08/31/02	PDN 0107
	Selected devices	02/28/03	08/31/03	PDN 0107
	EPF8820ABC225-3	05/31/02	11/31/02	PDN 0117
FLEX 10K	Selected FLEX 10K PGA packages	02/28/02	08/31/02	PDN 0107
	Selected FLEX 10K PGA & BGA packages	02/28/03	08/31/03	PDN 0107
	EPF10K10LI84-4	05/31/02	11/31/02	PDN 0117
FLEX 10KA	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	EPF10K30AFI256-2	05/31/02	11/31/02	PDN 0117
FLEX 10KE	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	Selected devices	10/31/03	04/30/04	PDN 0204
APEX 20K	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	EP20K400BI652-2	05/31/02	11/31/02	PDN 0117
	Selected devices	10/31/03	04/30/04	PDN 0204
APEX 20KE	Selected devices	10/31/03	04/30/04	PDN 0204
ACEX 1K	Selected devices	10/31/03	04/30/04	PDN 0204

How to Contact Altera

It is now easier than ever to get information and services from Altera. The table below lists some of the ways you can reach Altera.

Information Type	U.S. & Canada	All Other Locations
Product Literature	http://www.altera.com	http://www.altera.com
Altera Literature Services *(1)*	lit_req@altera.com	lit_req@altera.com
News & Views Information	http://www.altera.com/literature/nview.html n_v@altera.com	http://www.altera.com/literature/nview.html n_v@altera.com
Non-Technical Customer Service	(800) 767-3753	(408) 544-7000
Technical Support	https://www.altera.com/mysupport	https://www.altera.com/mysupport
	(408) 544-6401	(408) 544-6401 *(2)*
FTP Site	ftp.altera.com	ftp.altera.com
General Product Information	(408) 544-7104	(408) 544-7104 *(2)*
	http://www.altera.com	http://www.altera.com

Notes:
(1) The *Quartus Installation and Licensing* and *MAX+PLUS II Getting Started* manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for the latest listing.

News & Views On-Line Survey

Altera is evaluating delivery options for News & Views. Along with the printed version of News & Views, we are considering an HTML-based e-mail version. Please take a moment and go to **http://www.altera.com/nv_survey** and tell us which method you prefer.