News & Views

Fourth Quarter 2002

Newsletter for Altera Customers

We Heard You

NV-2002-Q4

ALTERA®

Message from *Product Planning*

Message Received—Loud & Clear

For nearly twenty years, Altera has excelled at developing revolutionary programmable logic device (PLD) technology. Leading the industry from its infancy to today's complete system-on-a-programmable-chip (SOPC) methodology, we continue to focus our development engineering resources on first-to-market programmable logic innovations. Our primary objective is to provide our customers with powerful, cost effective, easy-to-use programmable solutions that leverage world-class silicon technology. This, we believe, will empower our customers to accelerate the delivery of innovative new products to their end markets.

The recent economic downturn has forced us all to take a hard look at business and focus our resources on our core competencies. At Altera, we've spent the past two years continuing our aggressive investment in research and development, but with significantly increased customer interaction toward the definition of our new products. We now have groups that analyze detailed product requirements in our focus markets, such as computer, consumer, industrial, networking, and wireless.

Additionally, several focused programs are in place to ensure that we communicate clearly with our customers and accurately gather the knowledge gained for future product requirements. For example, Altera's target team of product planning experts, dubbed the Blue Angels, are a select group tasked with spending valuable hours with customers sharing technology roadmaps and future plans. During these Blue Angel visits, we found that many customers were interested in taking this open relationship further. Hence, the creation of our customer advisory board, where development engineers and system architects are invited to our San Jose headquarters for private meetings with our key development engineers across chip design, software, and intellectual property (IP). As a result, not only can our customers plan their future product development based on our technology leadership and future product plans, but we at Altera gain valuable feedback that helps us tune our products to meet our customers' sweet spots. One engineer commented "it's like having Altera develop their products custom-made for my future needs."

Feedback from these programs drove home your message loud and clear: Programmable logic is the foundation of future system design—make it flexible, fast, and low cost. While flexibility is in our DNA, cost and performance is where Altera is placing laser focus.

With the full featured, digital signal processing (DSP) capable Stratix™ family, the designed for low cost Cyclone™ FPGAs, and the integration of transceivers in Stratix GX devices—not to mention the continued enhancement of our Nios® embedded processor and the powerful, easy-to-use new Quartus® II design software—you now have at your disposal a powerful design platform that will get your system from concept to production on time and on budget. Our new generation of SOPC solutions are your competitive edge, as your success means our success. You can read all about it in this issue.

2002 was dedicated to you, our customer. Not only do you now help define your products, you also define our company. We are committed to delivering you programmable technology that will meet and exceed your technology and business needs.

Robert Blake
Vice President, Product Planning

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Printed on recycled paper.

I.S. EN ISO 9001

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Curing the ASIC Headache: Introducing Altera's New Cyclone Device Family

Altera designed its new Cyclone™ FPGA family specifically to deliver the benefits of programmable logic to markets and applications driven by cost pressures to standard products or ASICs. By optimizing the Cyclone architecture with cost in mind, Altera offers a powerful FPGA device family at ASIC prices a first for the programmable logic industry.

Tom Williams, Editor-in-Chief of RTC Magazine said, "Like most species, the ASIC is not going extinct because of internal flaws, but because it cannot survive in a changing environment—an environment increasingly dominated by programmable logic."

New market trends and challenges such as evolving standards, shrinking product introduction opportunities, accelerated obsolescence, intense competition, and changing requirements call for flexible digital logic products that minimize time-to-market yet provide designers with a low-risk path to product differentiation. While the traditional strengths of FPGAs make them the ideal solution for these volatile market conditions, price has been a barrier to acceptance in cost-sensitive applications. Programmable logic suppliers have previously attempted to address this problem by introducing lower-cost FPGA families, but these devices have either lacked the functionality to support end-application requirements, or missed the required threshold price points. Despite the significant design risks and up-front charges, designers of high-volume applications have traditionally turned to ASICs, due to their low device cost. Until now, no programmable logic device (PLD) company has successfully filled the void in the low-cost, FPGA-addressable space.

The Cyclone FPGA family fills this void in two ways. First, Cyclone devices are priced at or near parity with ASIC devices. Second, Cyclone devices extend system-on-a-programmable-chip (SOPC) solutions into new applications beyond that of any other low-cost programmable product in history, providing an optimized feature set and abundant on-chip resources targeted at high-volume applications.

The Symptoms: NREs, MOQs & Long Development Cycles

In general, the average selling price (ASP) of a product is inversely proportional to the number of units sold. For example, a DVD player/recorder sells in volumes in excess of 100,000 units per year at an ASP below $200, whereas a high-end networking box sells in volumes in hundreds to thousands of units per year with end-market prices that range from $10,000 to $100,000. Designers of high-volume, low-ASP systems have historically chosen ASICs over FPGAs. Despite the clear time-to-market and flexibility advantages of FPGAs, designers have chosen to pay the up-front, non-recurring engineering (NRE) charges associated with ASIC development and accepted the risk of multiple design re-spins that could potentially cause product-completion delays and ultimately jeopardize delivery to market.

For example, the rapid proliferation of DVD capabilities and the integration with other products such as progressive-scan DVD players, high-definition (HD)-DVD, and DVD/digital television create countless new challenges for designers. Often, the market acceptance of new features or product combinations is initially unclear, creating high risk for application-specific standard product (ASSP) vendors that venture to support them. Nevertheless, ASSP vendors strive to keep up with the changes and new options, when justified, but have lengthy development cycles that parallel ASIC development cycles. As a result, leading-edge ASSPs can be up to one year behind current requirements of the DVD product. Historically, DVD manufactures have been forced to go to market without the latest features, or delay their product while a small ASIC is developed to support the new function or bridge between ASSPs.

Changes in the economics of ASICs and significant advancements made in programmable technology have turned the tables in favor of FPGAs. Tom Williams, Editor-in-Chief of RTC Magazine said, "Like most species, the ASIC is not going extinct because of internal flaws, but because it cannot survive in a changing environment—an environment increasingly dominated by programmable logic." With the introduction of low-cost Cyclone devices, FPGAs now have price points on par with ASIC devices, without the NRE charges and without the delay to market. Rising development costs for cutting-edge ASIC technologies—in the form of growing NREs and huge minimum-ordering quantities (MOQs)—are now difficult to justify, particularly in difficult economic conditions where there is lower visibility into end-product demand. "Once an attractive option for getting just the right functionality for a reasonable price, the custom ASIC will no longer be able to keep up with the alternatives," continued Tom Williams. Older ASIC technologies, although they have very low NREs, do not support the performance requirements of the latest digital systems.

These issues pose significant problems for the ASIC designer and call into question the economics of undertaking an ASIC project.

The Cure: Cyclone Devices

The Cyclone device architecture, low cost by design, was built specifically for designers wanting the reprogrammability of an FPGA at the cost of an ASIC. Packed with logic resources and features unmatched by any other low-cost FPGA, Cyclone devices are equipped with a targeted feature set that facilitates the integration of many complex, system-level functions.

Cyclone devices dramatically increase the low-cost FPGA density range while supporting performance levels previously seen only in high-end FPGA families. As a result, Cyclone devices move low-cost FPGAs from glue logic and peripheral activities, such as LED driver control, into critical system functions, such as color space conversion (CSC) and display processing in video display and projector systems.

The four Cyclone device family members, shown in Table 1, are available in multiple packages tailored for many system and price requirements.

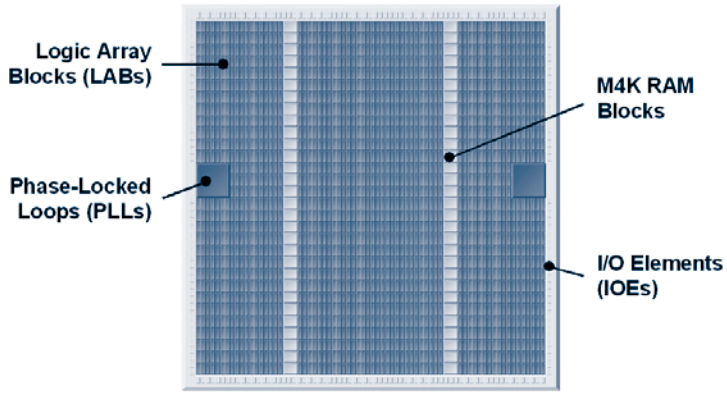
Table 1. Cyclone Device Family Overview

Feature	EP1C3	EP1C6	EP1C12	EP1C20
Logic Elements (LEs)	2,910	5,980	12,060	20,060
Embedded Memory Bits	59,904	92,160	239,616	294,912
Phase-Locked Loops (PLLs)	1	2	2	2
Maximum User I/O Pins	104	185	249	301
Package Options	100-Pin TQFP *(1)* 144-Pin TQFP	144-Pin TQFP 240-Pin PQFP *(2)* 256-Pin FineLine BGA® *(3)*	240-Pin PQFP 256-Pin FineLine BGA 324-Pin FineLine BGA	324-Pin FineLine BGA 400-Pin FineLine BGA

Notes to Table 1:
(1) TQFP: thin quad flat pack.
(2) PQFP: plastic quad flat pack.
(3) BGA: ball-grid array.

The Cyclone embedded memory structure (Figure 1) consists of multiple columns of 4,608-bit memory blocks, providing fast access to localized data storage resources. Each memory block supports multiple configurations, including true dual-port and single-port RAM, ROM, and first-in first-out (FIFO) buffers. For added flexibility, each block's input and output ports can be configured to different widths and can support independent clocking. Additional parity bits are included for error control.

Figure 1: Cyclone EP1C20 Device Floorplan



Cyclone devices are designed to communicate with double data rate (DDR) SDRAM and fast-cycle RAM (FCRAM) devices through a dedicated interface that ensures fast, reliable data transfer at up to 266 megabits per second (Mbps). As FPGAs are used in more critical system func-

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tions, it becomes increasingly important that they have the ability to exchange data quickly with external storage devices.

DDR SDRAM devices have become popular in low-cost applications, beginning with personal computers. These devices are now widely used across a broad spectrum of other applications requiring low-cost, moderate-performance memory modules, ranging from networking and communications to set-top boxes and home entertainment systems. DDR SDRAM devices are expected to cost less than single data rate (SDR) SDRAM devices with similar storage resources within the next two years. FCRAM devices, based on the same fundamental architecture, have also gained popularity, providing SRAM-like performance while consuming less power.

The combination of a Cyclone device with a Nios embedded processor provides an ideal solution for digital video applications in high-end DVD player/recorder systems.

Single-ended I/O standard support for basic data transmission includes the LVTTL, LVCMOS, PCI, SSTL-2, and SSTL-3 I/O standards. For more robust data transmission in noisy environments, Cyclone devices include support for LVDS at up to 311 Mbps. LVDS is a differential I/O standard that offers greater electromagnetic interference (EMI) protection and faster data transmission rates.

Cyclone devices feature eight low-skew, global clock networks that span the entire device, fed by four dedicated input clock pins. Cyclone PLLs, each with three output taps, feature frequency synthesis, and phase-shifting capabilities for complete system clock management, both on- and off-chip. Additionally, Cyclone PLLs offer advanced skew resolution capabilities for simplifying the printed circuit board (PCB) design process and reducing manufacturing difficulties of the end product.

Nios Embedded Processor & Cyclone Devices

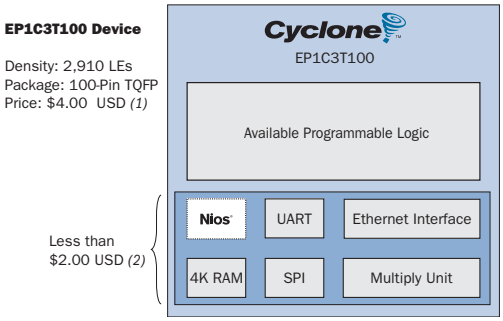
One of the most compelling uses for Cyclone devices is processor-based applications using Altera's Nios® embedded processor, the FPGA industry's most widely used soft embedded processor. A Nios processor and a Cyclone FPGA together offer comparable processing power, and much greater flexibility than many stand-alone embedded processors, at significantly lower cost.

The Nios embedded processor is a general-purpose RISC processor that can be combined with user logic and programmed into any Cyclone device. Featuring a 16-bit instruction set and a user-selectable 16- or 32-bit data path, the Nios processor is configurable for a wide range of applications. Nios processor users can optimize their system data flow using the simultaneous multi-master Avalon™ bus and increase their data-processing abilities by utilizing custom instructions. These features allow designers to easily increase system performance without requiring a higher operating frequency (f_{MAX}). The scalable nature of the Nios embedded processor means that it can be instantiated multiple times in a single Cyclone device for multi-processor applications. System updates can be easily performed by reprogramming the Cyclone device without incurring additional costs or development time, staving off obsolescence and extending usability beyond that of most off-the-shelf microprocessors and microcontrollers.

Consider a 32-bit Nios processor with the following peripherals: a fixed baud rate universal asynchronous receiver/transmitter (UART), serial peripheral interface (SPI), an Ethernet interface, a multiplication unit, and 4 Kbits of on-chip RAM. This well-equipped processor consumes approximately 1,400 LEs, or roughly 50% of the logic resources available on the smallest Cyclone device (EP1C3). In high-volume production quantities, the EP1C3 device costs $4 USD, meaning that the effective cost of the processor is less than $2 USD (see Figure 2). Designers "build to requirements" each time they use the Nios processor, meaning that unused peripherals are not wasted (and more importantly not paid for), as may be the case with discrete devices.

The combination of a Cyclone device with a Nios embedded processor provides an ideal solution for digital video applications in high-end DVD player/recorder systems. High-end DVD player/recorder systems play back decompressed and record compressed high-quality digital video and audio and include advanced audio and video processing capabilities. Most of the functional blocks in these systems are connected together with LVTTL I/O and the memory currently used is SDRAM, expected to transition to DDR SDRAM in the near future. Cyclone devices offer the functionality, density, I/O standards, and memory needed for these systems at ASIC prices.

Figure 2. Nios Embedded Processor & Cyclone Devices



Notes to Figure 2:
(1) Pricing for 250,000 units in 2004.
(2) Nios processor and peripherals use about 1,400 LEs.

Figure 3 shows an example of a DVD player/recorder system that uses a Cyclone device. When a DVD player/recorder system includes a CD-ROM read/write drive, a Cyclone device is used to perform the integrated drive electronics (IDE) conversion needed to interface with the video bus. In addition, a Nios processor acts as the DVD player/recorder microcontroller to perform a number of system functions, including control panel management and on-screen display (OSD). The total number of logic resources used for this application is approximately 4,500 LEs, meaning that you can integrate all functions into one Cyclone EP1C6 device with enough resources left for other functionality.

Cyclone devices, with embedded Nios processors, provide the industry's most cost-effective programmable solution for audio/video processing control.

More than Just Silicon

With Cyclone devices, Altera introduced more than just an FPGA family at lower price points. A cost-reduced solution makes the difference, starting with development software tools and ending with device configuration.

Altera offers Cyclone support in the free Quartus® II Web Edition design software that is available for download from the Altera web site at **www.altera.com**. Cyclone designs can be taken from concept to configuration entirely within the Quartus II Web Edition software environment, using schematic- and text-based design entry, HDL synthesis, place-and-route, verification, and programming tools. Cyclone devices are also supported in Altera's flagship Quartus II software, which offers advanced capabilities such as the LogicLock™ block-based design methodology and hardware verification tools.

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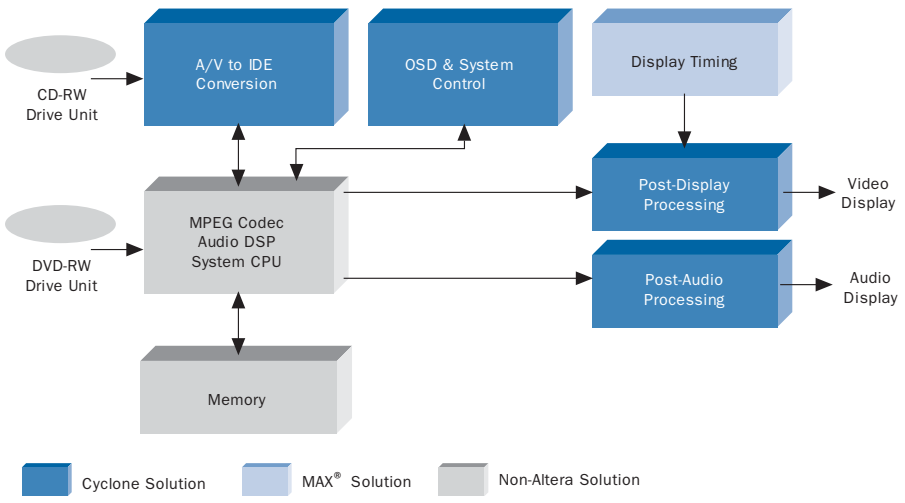
Cyclone devices, with embedded Nios processors, provide the industry's most cost-effective programmable solution for audio/video processing control.

Figure 3. Cyclone Usage Example for DVD Player/Recorder System



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Altera's new serial configuration device family complements the low prices of the Cyclone device family.

SOPC Builder

Available from the Altera web site free-of-charge (**www.altera.com/processorportfolio**), SOPC Builder streamlines the process of integrating large blocks of intellectual property (IP) and accelerates development of complex SOPC designs. Designers can use the tool to quickly combine system-level components, including the Nios embedded processor, memories, peripherals, and user-developed IP blocks to create their own custom SOPC solution. SOPC Builder automatically generates custom software development environments for each Nios processor included in the system.

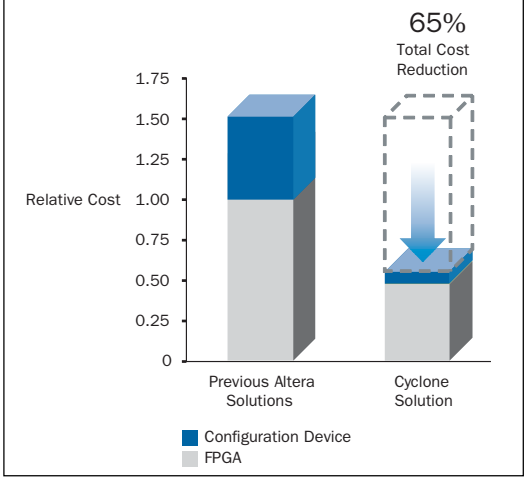
Serial Configuration Devices

Altera's new serial configuration device family complements the low prices of the Cyclone device family. They are priced on average at 10% of the target Cyclone device versus the 30% to 50% price seen with older configuration devices. These devices help reduce the total solution cost by up to 65% from previous low-cost FPGA offerings (see Figure 4). Available in 1-Mbit and 4-Mbit densities, these devices can store configuration data while making remaining resources available for general-purpose storage.

The Possibilities Are Endless

Cyclone devices clear the way for many exciting opportunities for FPGAs, opening non-traditional application spaces in new and existing markets, including consumer, communications, storage, automotive, and industrial. Companies in these cost-driven markets can now rapidly introduce competitive and innovative products, saving time and money while imparting their core competencies and value-adding functions to the end product.

Figure 4. Serial Configuration Device Savings



The introduction of Cyclone devices could not have happened at a more opportune time. In a cost-conscious economy where every expenditure is scrutinized, designers finally have access to a programmable logic solution at ASIC-level pricing, without the risks associated with MOQs and NREs. According to Tom Williams, "The emergence of programmable logic will not only spell the doom of the ASIC; it will also profoundly affect the way systems are designed."

Stratix GX Device Family Delivers a Low-Risk 3.125 Gbps Transceiver Option to the Programmable Market

Altera is proud to introduce the newest product in its high-performance FPGA product portfolio, the Stratix™ GX family. Stratix GX devices integrate 3.125 gigabit per second (Gbps) transceiver technology with the industry-leading Stratix FPGA architecture to provide a comprehensive solution for high-speed transceiver implementation. Drawing on valuable experience gained as the first FPGA company to embed high-speed transceivers in FPGAs with the Mercury™ device family, Altera designed Stratix GX devices to provide a truly low-risk path to flexible, multi-gigabit transceiver solutions.

High-speed transceivers have become a key requirement in all industries, as the need for high-speed communication and high-bandwidth data transfer pushes the boundaries of existing technology. Along with this rapid growth is a proliferation of standards, protocols, and approaches to handling data that has created a mixture of interfaces.

Introducing the Stratix GX Family

The Stratix GX family provides a powerful fusion of the industry's fastest FPGA architecture with a high-performance multi-gigabit transceiver. The seven devices in the family offer from 4 to 20 full-duplex transceivers, up to 40,000 logic elements (LEs), and up to almost 3.4 million bits of embedded RAM. To complement the high-speed transceiver channels, up to 45 channels of source-synchronous differential signaling are provided, featuring support for skew-reducing dynamic phase alignment (DPA) embedded in the device silicon. By designing the Stratix GX family around the ground-breaking Stratix architecture, Stratix GX devices provide the same revolutionary features, such as TriMatrix™ memory, optimized digital signal processing (DSP) blocks, advanced clock management circuitry, and on-chip termination with Terminator™ technology (see Table 1).

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Table 1. Stratix GX Device Family Overview

Device	LEs	Full-Duplex Transceiver Channels with DPA	Source-Synchronous Channels	Total RAM Bits	DSP Blocks	Phase-Locked Loops (PLLs)	Maximum User I/O Pins
EP1SGX10C	10,570	4	22	920,448	6	4	330
EP1SGX10D	10,570	8	22	920,448	6	4	330
EP1SGX25C	25,660	4	39	1,944,576	10	4	426
EP1SGX25D	25,660	8	39	1,944,576	10	4	542
EP1SGX25F	25,660	16	39	1,944,576	10	4	542
EP1SGX40D	41,250	8	45	3,423,744	14	8	544
EP1SGX40G	41,250	20	45	3,423,744	14	8	544

Stratix GX Device Family Delivers a Low-Risk 3.125 Gbps Transceiver Option to the Programmable Market, continued from page 9

Second-Generation Design Expertise

Stratix GX FPGAs represent the latest step in Altera's commitment to high-speed signaling products. As early as the original APEX™ 20KE devices, Altera identified the challenges of datapath design, and incorporated LVDS signaling and an embedded serializer/deserializer (SERDES) as key differentiating features. With the Mercury device family, Altera introduced the first full implementation of a complete clock data recovery (CDR) transceiver in a quality FPGA product. The experience gained from designing, shipping, and supporting these complex products is a key contributor to the evolution of the Stratix GX family. In creating an effective combined FPGA and transceiver architecture, it is the details that make the difference in ensuring that the device is suitable for your system-integration needs.

Stratix GX devices contain embedded gigabit transceiver blocks that feature four full duplex channels that serialize or deserialize data for high-speed transmission at a maximum data rate of 3.125 Gbps using CDR technology.

A successful FPGA/transceiver integration requires far more than simply combining the two disparate items, the layout and architecture of the channels is very important. Arranging the channels into tightly bound, integrated blocks consisting of four channels apiece ensures that each block maintains its own independence while still providing adequate flexibility for multi-block designs (see Figure 1). This block-based design also provides significant power consumption advantages, resulting in less than one third the power consumption of competing products. To enable the high-performance portions of the data transmit/receive process, many functions are implemented in hard intellectual property (IP). This provides designers with functionality capable of supporting high data rates, and also increased flexibility in the form of multiple SERDES factors, user-programmable pattern detection, channel alignment, and 8B/10B encoding and decoding. Optimized channel count to logic ratios and minimal power consumption—along with customer-based requirements for extended drive strength and input receiver equalization—further enhance the Stratix device family's capabilities.

Stratix GX Transceiver Blocks

Stratix GX devices contain embedded gigabit transceiver blocks that feature four full duplex channels that serialize or deserialize data for high-speed transmission at a maximum data rate of 3.125 Gbps using CDR technology. Each channel features dedicated circuitry that implements various stages of the data recovery/transmission, decoding/encoding, and synchronization process. A seamless interface with the programmable logic array ensures reliable data transfer, maximized data throughput, and simplified timing analysis.

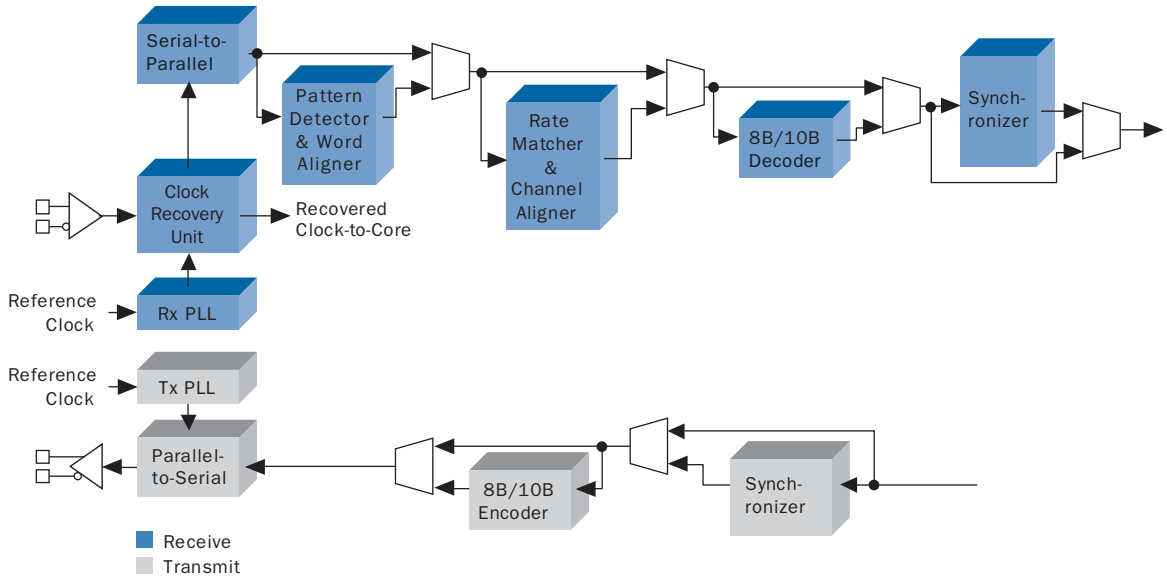
Stratix GX gigabit transceiver block highlights include:

- Support for many transceiver protocols, including 10 Gigabit Ethernet XAUI, SONET/SDH, Gigabit Ethernet, Fibre Channel, InfiniBand, the Serial RapidIO™ standard, PCI Express, SMPTE 292M, SFI-5, and SPI-5
- Low power consumption per channel (175 mW) and transceiver block (450 mW), results in reduced overall device power consumption
- Programmable pre-emphasis, equalization, and differential output voltage settings

Each gigabit transceiver block has circuitry that ensures smooth, seamless data transfer from the block to the rest of the device for processing and manipulation. This circuitry prevents data bottlenecks that can degrade performance and reduce data bandwidth. The logic array and gigabit transceiver blocks can exchange data as an 8-, 10-, 16-, or 20-bit-wide bus.

The gigabit transceiver block has SERDES and multiplexing/demultiplexing circuitry that translates the high-speed serial input stream to a width and frequency suitable for processing within the logic array. Additionally, each gigabit transceiver block has PLLs that multiply or divide the incoming reference clock to serialize or deserialize the outgoing or incoming data. The PLLs are also available for use in the functional blocks within the gigabit transceiver block. The architecture resolves small differences between the phase and frequency of the logic array and external reference clock entirely within the gigabit transceiver block. Table 2 shows the supported Stratix GX protocols.

Figure 1. Stratix GX Channel Block Diagram



Dynamic Phase Alignment

Stratix GX devices feature embedded silicon for implementation of DPA on the source-synchronous LVDS channels (see Figure 2). This feature enables the dynamic elimination of channel-to-channel skew, improving I/O performance and enabling source-synchronous signaling across backplane and connector media. This DPA capability is an important complement to the Stratix GX transceivers, providing access to the large bandwidth of data brought onto the transceiver side of the device. DPA is increasingly being adopted in protocol definition, and is currently a stated requirement for SPI-4.2.

Figure 2. Dynamic Phase Alignment

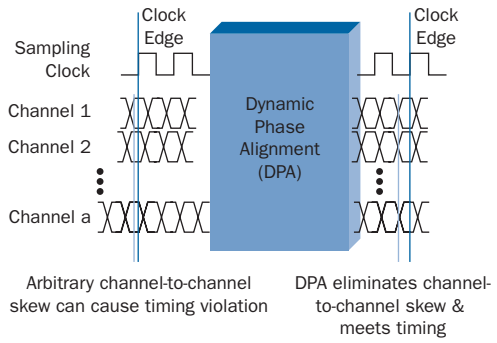


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Table 2. Stratix GX Transceiver Protocols

Feature	10 Gigabit Ethernet XAUI	Serial RapidIO	Gigabit Ethernet	InfiniBand	Fibre Channel	SPI-5	SFI-5	SMPTE 292M	PCI Express
Maximum Bandwidth (Gbps)	12.500	50	1.25	30	2.125	50	50	1.485	40
Channel Bus Width	4	1, 4, 8, 16	1	1, 4, 12	1	17 to 18	17 to 18	1	16
Maximum Channel Data Rate (Gbps)	3.125	3.125	1.25	2.5	2.125	3.125	3.125	1.485	2.5

Stratix GX Device Family Delivers a Low-Risk 3.125 Gbps Transceiver Option to the Programmable Market, continued from page 11

DPA uses Stratix GX fast PLLs and is an optional feature of the dedicated source-synchronous circuitry. Using one of eight phase-shifted clocks generated by the fast PLL, the dynamic phase aligner samples the incoming data and aligns the data by choosing the clock phase that is closest to the center of the incoming data. This alignment is continuous and can compensate for dynamic changes in the real-time timing variations between the clock and data signals.

Stratix GX Devices in Your System

High-speed transceiver technology is appearing in all types of systems; Stratix GX devices can assist by providing a flexible, low-risk, integrated solution for many diverse systems. Stratix GX devices are ideal for a variety of applications, including bridging applications, switch fabrics, traffic-management functions, wireless, storage, and high-definition television (HDTV) broadcast applications.

Stratix GX devices extend beyond the silicon to include software tools, IP, a capable and extensive support infrastructure, documentation, board-design guidelines, product interoperability testing, and development kits and boards.

Typical applications for Stratix GX devices might include:

- *Backplane transceivers*. The 40-inch drive strength, receiver equalization feature, hot-socketing capability and low power consumption of Stratix GX devices allow them to serve as backplane transceivers, integrating transceiver functionality with additional processing. See Figure 3.
- *Bridging functions*. Through the flexibility provided by the FPGA fabric, Stratix GX devices can serve as an effective bridging function between two devices that would not otherwise be able to communicate, whether they serve as a link between a XAUI backplane and an SPI-4.2 line card, or any group of relevant protocols.
- *System switch fabric*. Stratix GX devices can serve as system switch fabrics, managing the movement of traffic around a system either on a dedicated switch fabric card or by incorporating the capabilities of a distributed switch fabric onto each line card.
- *Storage switches*. Storage switches place a high importance on the ability to transfer data around the system, and the integration of logic with high-quality transceivers make Stratix GX devices a good fit.
- *HDTV applications*. HDTV applications are rapidly turning towards higher frequency signaling, and the large channel count requirements make highly integrated Stratix GX devices with their 20-channel capability a natural fit.
- *Test equipment*. High-speed signaling test equipment must always possess the flexibility to accommodate the newest and the most fluid protocols and standards, while maintaining the time-to-market advantages only available from FPGAs.

High-speed signaling is becoming increasingly important in system designs. Stratix GX devices address that need and reduce your design risk.

Assembling the Whole Product

While delivering a top-notch silicon device is a key requirement for the product family's success, Stratix GX devices are not just about silicon. To succeed with a complex, high-performance device, you need a whole product solution to complement the FPGA. Stratix GX devices extend beyond the silicon to include software tools, IP, a capable and extensive support infrastructure, documentation, board-design guidelines, product interoperability testing, and development boards and kits.

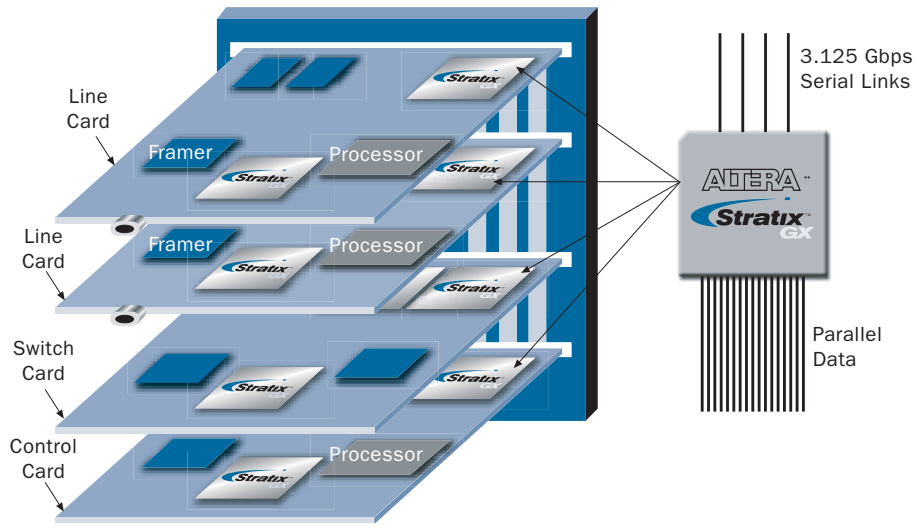
Altera's experience with Mercury devices means that the details of transceiver implementation in Stratix GX devices are well understood. With a dedicated team of high-speed I/O-focused applications engineers, Altera has the resources and capability in place to ensure that you have a successful design experience.

The Stratix GX development kit (available shortly after the first silicon release) will provide a comprehensive design experience incorporating all the necessary elements for high-speed design into one box.

Stratix GX: Multi-Gigabit Design Made Easy

Many systems require high-speed signaling. With Stratix GX devices, Altera provides a 3.125 Gbps transceiver option combined with the industry's premier FPGA product, allowing you full time-to-market and flexibility advantages of FPGAs combined with superior I/O performance.

Figure 3. Backplane Application



Altera Stratix Devices Available Now for Production

Announced in February 2002, Stratix™ FPGAs are the industry's highest performance, highest-density FPGA family. Since May 2002, Altera has rapidly rolled out six different devices within a span of six months, placing Stratix devices in the hands of customers in record time. You can now realize the benefits of this full-featured family, including shorter time-to-market combined with design flexibility, when implementing complex systems such as network test equipment, wireless basestation infrastructure equipment, and storage area networks.

EP1S20, EP1S25 & EP1S30 Production Devices Now Available

Stratix EP1S20, EP1S25, and EP1S30 devices have passed reliability tests and qualify for production status. All three devices are available from Altera's distribution channels for volume production applications.

Altera's prior experience in the advanced all-layer-copper 0.13-µm process technology, and our close working relationship with best-in-class fabrication supplier TSMC, have ensured availability and lower costs. Altera has been shipping devices based on the all-layer-copper 0.13-µm process for more than a year starting with the APEX™ II EP2A70 device in December of 2001.

In addition to a fast rollout, Stratix devices also show better-than-expected performance results. To deliver the benefit of higher performance to the customer, Altera announced a new, faster -5 speed grade that runs 15% faster than -6 speed grade devices. Table 1 on page 14 shows typical performance numbers for key Stratix features as seen in the Quartus® II software version 2.1 service pack 1.

Altera has also invested in a new package offering that extends the package options for the Stratix device family. The EP1S10 and EP1S20 devices will be offered in the 23 × 23 mm FineLine BGA® 484-pin package that offers a smaller footprint and provides board-area savings.

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Altera Stratix Devices Available Now for Production, continued from page 13

Table 1. Stratix Feature Performance

Feature	-5 Speed Grade	-6 Speed Grade	-7 Speed Grade
DSP block (8 x 8 simple multiplier mode)	336 MHz	294 MHz	256 MHz
M512 memory block (32 x 18 bits)	318 MHz	278 MHz	242 MHz
M4K memory block (128 x 36 bits)	291 MHz	256 MHz	228 MHz

Engineered for Success

Stratix devices are causing quite a buzz in the FPGA community, generating healthy demand from many customers.

Multiple Stratix devices have entered the market in record time, and the scalability of their modular design architecture ensures the on-time availability of the remaining members. The modular architecture of Stratix devices allows multiple design teams to simultaneously simulate and verify device functionality. The extensive design verification process prior to tape-out minimizes design errors and has led to fully functional Stratix devices delivered ahead of schedule.

Table 2. Stratix Device Availability

Device	ES Device Availability	Production Device Availability
EP1S10	Now	Q1 2003
EP1S20	Use Production Device	Now
EP1S25	Use Production Device	Now
EP1S30	Use Production Device	Now
EP1S40	Now	Q1 2003
EP1S60	Use Production Device	Q2 2003
EP1S80	Now	Q1 2003
EP1S120	2003	2003

Multiple Family Members Available Today

Production versions of three members of the Stratix family (EP1S20, EP1S25, and EP1S30 devices) are available today in all package configurations. Also available are engineering samples of three additional family members (EP1S10, EP1S40, and EP1S80 devices). See Table 2.

Altera's Stratix Commitment

Stratix devices are causing quite a buzz in the FPGA community, generating healthy demand from many customers. Altera plans to leverage the next-generation process technology based on 300-mm wafer sizes to improve overall device yields.

Cyclone

Cyclone: The Lowest-Cost FGPA Ever

The Cyclone™ device family has the perfect mix of features, density, and performance at less than $1.50 per 1,000 logic elements (LEs)—half the cost of competing FPGAs. System designers building high-volume applications in the consumer, communications, computer peripheral, automotive, and industrial markets have access to the flexibility, economic efficiencies, and time-to-market advantages of programmable logic. For more information on Cyclone devices, see "Curing the ASIC Headache: Introducing Altera's New Cyclone Device Family" on page 4.

Table 1 shows Cyclone device availability.

Table 1. Cyclone Device Availability

Device	Availability
EP1C3	April 2003
EP1C6	February 2003
EP1C12	April 2003
EP1C20	January 2003

Stratix

Six Stratix Devices Now Shipping

Production devices for Stratix™ EP1S20, EP1S25, and EP1S30 devices, and engineering samples of EP1S10, EP1S40, and EP1S80 devices are now available. Altera has rapidly rolled out six different devices within a span of six months, placing Stratix devices in the hands of several customers in record time. You can now realize the performance and advanced feature benefits of Stratix devices. For more information on Stratix devices, see "Altera Stratix Devices Available Now for Production" on page 13.

Stratix GX

Quartus II Software Now Supports Stratix GX Devices

Altera continues to provide its customers with advanced design support on leading-edge products. Stratix GX devices are currently supported in the Quartus® II software version 2.2. Building on the widely accepted Stratix architecture, the Stratix GX family features up to 20 low-power, full-duplex transceiver channels capable of operating at up to 3.125 gigabits per second (Gbps) per channel combined with minimal power consumption. Stratix GX devices offer the same features as Stratix devices, including TriMatrix™ memory, digital signal processing (DSP) blocks, and advanced clock management circuitry for intensive data path processing functions.

Each transceiver channel features dedicated circuitry that implements various stages of the data recovery/transmission, decoding/encoding, and data alignment process. A seamless interface with the programmable logic array ensures reliable data transfer, maximized data throughput, and simplified timing analysis.

You can achieve balanced data transfer through the device with source-synchronous I/O channels capable of 1-Gbps performance. Altera has also incorporated a new dynamic phase alignment (DPA) feature into Stratix GX devices. This feature dramatically simplifies printed circuit board (PCB) design, eliminating signal alignment issues introduced by skew-inducing effects when using source-synchronous signaling techniques.

The first group of Stratix GX devices, the EP1SGX25C, EP1SGX25D, and EP1SGX25F devices, will be available in Q1 2003, followed by the EP1SGX40D, EP1SGX40G, EP1SGX10C, and EP1SGX10D devices.

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See Tables 2 and 3 for device availability schedules and software support for Stratix GX devices. For more information on enabling Stratix GX support in the Quartus II software version 2.2, contact your local Altera® sales representative.

Table 2. Stratix GX Device Availability

Device	ES Availability
EP1SGX10C	Q3 2003
EP1SGX10D	Q3 2003
EP1SGX25C	Q1 2003
EP1SGX25D	Q1 2003
EP1SGX25F	Q1 2003
EP1SGX40D	Q2 2003
EP1SGX40G	Q2 2003

Table 3. Stratix GX Devices & Quartus II Software Advanced Support Availability

Device	Transceiver Channel Count	Package	Quartus II Software Advanced Support Availability
EP1SGX10C	4	672-pin FineLine BGA®	Now
EP1SGX10D	8	672-pin FineLine BGA	Now
EP1SGX25C	4	672-pin FineLine BGA	Now
EP1SGX25D	8	672-pin FineLine BGA 1,020-pin FineLine BGA	Now Now
EP1SGX25F	16	1,020-pin FineLine BGA	Now
EP1SGX40D	8	1,020-pin FineLine BGA	Now
EP1SGX40G	20	1,020-pin FineLine BGA	Now

Excalibur

EXCALIBUR™

EPXA1 Development Kit

Based on the Excalibur™ EPXA1 device, the EPXA1 Development Kit is the ideal platform for developing prototype designs for a wide range of applications, such as industrial control, automotive, and consumer markets. An external 10/100 Ethernet MAC PHY allows Ethernet connectivity without the need for an Ethernet intellectual property (IP) core. Two UART port connectors are present, one connected directly to the UART pins on the embedded processor subsystem, and one to the general-purpose I/O pins in the programmable logic.

EPXA1 development board features include:

- EPXA1 FineLine BGA device in the 484-pin package
- 10/100 Ethernet MAC/PHY with full- and half-duplex modes
- Two RS232 ports (DTE)
- 8-Mbyte flash memory (boot from flash supported)
- 32-Mbyte SDR SDRAM on board
- Three clock sources for system design
- ByteBlasterMV™ download cable
- IEEE Std. 1149.1 Joint Test Action Group (JTAG) connector
- Multi-ICE® connector for ARM® debug tools
- Two Altera expansion-headers for daughter cards (one standard and one long)
- One user-definable 8-bit DIP switch block
- Four user-defined, push-button switches
- Ten user-defined LEDs

The EPXA1 Development Kit includes:

- EPXA1 development board
- Power supply
- Smart LCD module
- Documentation
- Software, drivers, and application examples on CD
- Connection cables
- Quartus II Web Edition software
- SOPC builder and GNUPRO tools

The ordering code for the development kit is EPXA-DEVKIT-XA1, and the resale price is $1,195. There is a development kit promotion running until 12/20/02. Contact your local Altera sales representative for more information. Mention the promotion code 102102-U8.

Customer Feedback

"In our work to produce machine-vision-based automotive intelligence systems, it was necessary to quickly measure the performance of a range of different silicon implementation technologies against performance metrics for the embedded CPU, I/O, and memory subsystem," said Rainer Gutzmer, Manager of System Development at Aglaia-Gesellschaft für Bildverarbeitung und Kommunikation GmbH. "The EPXA1 Development Kit contained everything we needed for this benchmarking, including a series of reference designs that illustrated the EPXA1 device's flexibility and helped us to accelerate the development of our first prototypes."

MontaVista Linux & Excalibur Devices Deliver Reconfigurable SOPC Solutions

Altera and MontaVista have released the Linux Support Package (LSP) for the EPXA1 development board. The LSP unleashes the power of Excalibur devices combined with Linux to enable remote dynamic reconfiguration of the FPGA without resetting the processor, and remote loading of device drivers to the kernel-mode module.

The combination of these two features allows you to remotely upgrade the product, which includes changing the peripheral set of the embedded systems and loading device drivers using a standard communications channel (e.g., Ethernet). This reconfiguration feature is equally capable of loading locally stored FPGA images and dynamically loading the appropriate device's drivers to the kernel. By unleashing these capabilities, you can create a single board to build highly flexible and scalable system-on-a-programmable-chip (SOPC) solutions.

Shipping with the EPXA1 Development Kit is a demonstration application based on MontaVista Linux that demonstrates these capabilities. The demonstration is an Apache Web Server application running under Linux and the Linux file system. The web server application hosts pages that allow you to upload configuration files to the EPXA1 development board. Contained in the configuration file is all of the information needed by the operating system to identify the peripherals and the associated device drivers, along with the FPGA image. You do not need to reload applications already installed on the system.

With this powerful solution, you can deliver timely product enhancements with minimal user intervention.

MontaVista Linux Professional Edition

MontaVista Linux Professional Edition is fully open source and royalty free, with a full complement of tools designed to help you design, develop, and deploy your applications.

You need in-depth hardware support, a powerful development environment, and maximum scalability to deploy your embedded designs. MontaVista Linux Professional Edition delivers these capabilities, and allows you to streamline your development project and accelerate your time-to-market in a cost-efficient manner.

MontaVista Linux Professional Edition 2.1 includes:

- Source and binary files for Linux kernel
- Development tools
- KDevelop IDE
- Scaling and configuration tools to size kernel and file systems to suit your memory footprint
- Detailed documentation
- Product updates
- Technical support, including access to MontaVista Zone, a support and developer portal
- Training and customer education

Host operating system support includes Red Hat Linux, Solaris, VMWare/Linux on Windows, Yellow Dog Linux, Suse, and Mandrake.

Availability

The MontaVista LSP for the EPXA1 development board is available with the MontaVista Linux Professional Edition.

For further details about the MontaVista and Linux support for Excalibur devices, contact MontaVista at **sales@mvista.com** or visit the MontaVista web site at **www.mvista.com**.

SOPC Builder

SOPC Builder Supports Cyclone & Stratix GX Devices

Altera is now shipping SOPC Builder with support for Cyclone and Stratix GX devices. System designers can take advantage of SOPC Builder to automatically generate custom embedded systems for the industry's lowest-cost FPGA family and the Stratix GX family. Included in shipments of the Quartus II software version 2.2, the SOPC Builder version 2.7 system design tool also supports all of Altera's recent FPGA families, including Stratix devices.

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SOPC Builder enables designers to easily combine an embedded processor (one or more Nios® processors and/or the high-performance ARM922T™ processor in Excalibur devices), any SOPC Builder Ready IP functions, and user-defined logic into a complete system. SOPC Builder automatically generates both AMBA™, AHB, and Avalon™ on-chip bus logic to connect system components. Designers gain productivity by eliminating the task of manually creating bus bridges or multi-master arbitration logic.

For more information on SOPC Builder, visit the Altera® web site at **www.altera.com/sopcbuilder**. SOPC Builder is available free with the Embedded Processor Portfolio CD-ROM, which can be requested on-line at **www.altera.com/processorportfolio**.

Nios Processor

Nios Embedded Processor Rides High-Performance, Low-Cost Curve

The Nios embedded processor, based on Altera's advancing device and tool technology, continues to achieve higher performance and lower prices. Because the Nios processor is a soft IP core, gains in device and tool technology translate to an instant gain for systems integrating a Nios embedded processor. In addition, steady improvements to the Nios processor design provide a constant stream of performance and productivity gains.

Table 4. Performance & Size Data for Average Nios System Targeting Stratix, Cyclone & APEX 20KE Devices

Device	Third-Party Synthesis		Quartus II Integrated Synthesis	
	LEs	f_{MAX} (MHz)	LEs	f_{MAX} (MHz)
Stratix	2,002	135	1,861	133
Cyclone	1,965	120	1,858	113
APEX 20KE	2,782	55	2,668	58

Table 4 shows performance and size data for an average Nios system targeting the Stratix, Cyclone, and APEX™ 20KE families. CPU performance (f_{MAX}) improves by over 200% based on advances in device technology alone. System size (LE utilization) is reduced based on improved integrated synthesis in the Quartus II software. Reduced size translates to lower price—in addition to the dramatic price reduction available with Cyclone devices.

At 135 MHz, a Nios processor in a Stratix device offers the industry's highest-performance soft processor. Or, consuming only half of a $4 USD Cyclone device, a 32-bit Nios processor offers a price that is competitive with discrete 32-bit microprocessors. For the most recent news on the Nios processor version 2.2, visit the Altera web site at **www.altera.com/nios**.

APEX II

APEX II Availability

All members of the APEX II device family are shipping. APEX II devices range in density from 16,640 to 67,200 LEs and are memory-rich, offering 4 Kbits of memory per embedded system block (ESB), with total device memory ranging from 416 Kbits to 1.1 Mbits. The APEX II family supports high-speed data transfers through a wide range of high-speed I/O standards such as LVDS, PCML, LVPECL, HSTL, SSTL, and HyperTransport™ technology. With True-LVDS™ circuitry, APEX II devices can achieve data transfer rates of up to 1 Gbps per channel. With these I/O features, you can use APEX II devices in the following applications:

- PHY-link layer interface applications (POS-PHY, Flexbus, and UTOPIA)
- Host-processor interface applications (HyperTransport technology, peripheral component interconnect (PCI), and PCI-X)
- Switch fabric interfaces (CSIX and LCS)
- External memory interfaces (double data rate (DDR), zero bus turnaround (ZBT), and quad data rate (QDR) memory devices)

See Table 5 for APEX II device availability.

Table 5. APEX II Device Availability

Device	Package	Production Availability
EP2A15	672-pin FineLine BGA 724-pin BGA	Now
EP2A25	672-pin FineLine BGA 724-pin BGA	Now
EP2A40	672-pin FineLine BGA 724-pin BGA 1,020-pin FineLine BGA	Now
EP2A70	724-pin BGA 1,508-pin FineLine BGA	Now

APEX II HardCopy Solution

Altera offers a migration option from APEX II to HardCopy™ devices for system designers who need a low-risk, cost-reduction solution for volume production. You can prototype time-sensitive applications using APEX II devices and migrate the design to HardCopy devices for high-volume production. HardCopy devices preserve the functionality and timing of the design and allow you to improve time-to-market at the lowest cost.

APEX II Industrial Offerings

All the industrial-grade devices for the APEX II device family are now available to further compress design cycles for the fastest possible time-to-market. Industrial-grade production versions of the device offerings are available in a -8 speed grade. Table 6 shows the availability for industrial-grade offerings.

Table 6. APEX II Industrial Device Offering

Device	Package	Production Availability
EP2A15	672-pin FineLine BGA	Now
EP2A25	672-pin FineLine BGA	Now
	724-pin BGA	Now
EP2A40	724-pin BGA	Now
	1,020-pin FineLine BGA	Now

Mercury

Mercury Available in Production Mode

All devices and all speed grades of the Mercury™ device family are shipping in production mode, including industrial-grade offerings in both product lines (see Table 7). High-speed 1.25-Gbps serial links featuring clock data recovery (CDR) circuitry and an embedded serializer/deserializer (SERDES) make these devices ideal for serial backplane applications.

Table 7. Mercury Device Availability

Device	Package	Temperature Grade	Production Availability
EP1M120	484-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now
EP1M350	780-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now

APEX

APEX 20KC Available in Production Mode

All APEX 20KC devices are available with all parts and packages shipping in full production mode. Table 8 shows the availability schedule for APEX 20KC devices.

Table 8. APEX 20KC Device Availability

Device	Package	Production Availability
EP20K200C	208-pin PQFP *(1)*	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K400C	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now

Note to Table 8:
(1) PQFP: Plastic quad flat pack.

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Industrial-Grade APEX Offerings

Industrial-grade APEX devices are now available in a wide variety of package offerings. Refer to Tables 9, 10, and 11.

Table 9. APEX 20KC Device Industrial Offering

Device	Package	Speed Grade
EP20K200C	484-pin FineLine BGA	-8
EP20K400C	672-pin FineLine BGA	-8
EP20K600C	652-pin BGA 672-pin FineLine BGA	-8
EP20K1000C	1,020-pin FineLine BGA	-8

Table 10. APEX 20KE Device Industrial Offering

Device	Package	Speed Grade
EP20K30E	144-pin FineLine BGA	-2X *(1)*
EP20K60E	144-pin FineLine BGA 208-pin PQFP 324-pin FineLine BGA	-2X *(1)*
EP20K100E	144-pin FineLine BGA 240-pin PQFP 324-pin FineLine BGA 356-pin BGA	-2X *(1)*
EP20K160E	484-pin FineLine BGA	-2X *(1)*
EP20K200E	240-pin PQFP 356-pin BGA 484-pin FineLine BGA 672-pin FineLine BGA	-2X *(1)*
EP20K300E	240-pin PQFP 652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K400E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K600E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K1000E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*

Note to Table 10:

(1) The "X" denotes phase-locked loop (PLL) and LVDS support.

Table 11. APEX 20K Device Industrial Offering

Device	Package	Speed Grade
EP20K100	208-pin PQFP 240-pin PQFP 324-pin FineLine BGA	-2V (1) -2V (1) -2XV (1)
EP20K200	240-pin PQFP 484-pin FineLine BGA	-2V (1)
EP20K400	652-pin BGA 672-pin FineLine BGA	-2V (1)

Note to Table 11:

(1) The "X" denotes PLL support. The "V" denotes 5.0-V tolerant I/O interfaces.

ACEX

ACEX 1K Availability

ACEX® 1K devices are available in quad flat pack (QFP) and FineLine BGA packages in 576-, 1,728-, 2,880-, and 4,992-LE densities. These cost-optimized devices are specially suited for low-cost, high-volume applications. For mid- and high-density designs, see Altera's newest and lowest-cost Cyclone FPGA family on page 4.

Free software support for all ACEX 1K devices is available in the Quartus II Web Edition software version 2.2, which is available for download at **www.altera.com**.

MAX

Re-Designed MAX Pages on the Web

The MAX® complex programmable logic device (CPLD) web pages have been re-designed on the Altera web site. The MAX web pages now have an easier-to-use format and simpler navigation, allowing you to efficiently access information about the MAX family offerings, device architecture and features, related literature, and much more.

Compile MAX Designs Using the Quartus II Software

Support for MAX 3000A, MAX 7000AE, and MAX 7000B devices is now provided with the easy-to-use Quartus II software, including the free downloadable Web Edition software. The Quartus II software integrates the support of leading-edge CPLDs and FPGAs into one single platform, and significantly improves second-time fitting for MAX designs. A presentation has been posted to show how you can compile a MAX design step-by-step, from design entry to compilation and simulation. A tutorial file is also available to work alongside the presentation. For more details, visit the MAX section of the Altera web site at **www.altera.com**.

Configuration

New Serial Configuration Devices

Altera's new serial configuration devices are the lowest-cost configuration devices in the industry, and provide the ideal complement to Cyclone FPGAs in addressing high-volume, price-sensitive applications. Engineered for maximum efficiency, serial configuration devices deliver features such as in-system programmability (ISP) and re-programming capabilities at a cost even lower than one-time programmable (OTP) solutions.

Enhanced Configuration Devices

Enhanced configuration devices provide a complete single-device solution for a wide range of density requirements. Vertical migration capability allows you to easily migrate from the EPC4 to the EPC8 to the EPC16 device in the same package without having to change the board layout. Commercial and industrial grade EPC4, EPC8, and EPC16 devices are all now available.

Enhanced configuration devices offer ISP through a built-in IEEE standard for boundary-scan-based, in-system configuration standard of programmable devices (IEEE 1532). The inclusion of ISP and re-programmability provides a significant advantage over one-time programmable solutions by introducing flexibility and reusability to the configuration process.

Altera's enhanced configuration devices also introduce numerous features for specialized configuration needs. These features include an external flash interface that allows unused portions of the flash memory to be used as general-purpose memory, parallel configuration capability to accelerate configuration times, a new page mode that allows you to store multiple configurations, block protection for partial reprogramming support, and full clocking flexibility through the programmable clock and external clock features. This advanced feature set enhances the overall FPGA design experience.

Design Software

Quartus II Software Version 2.2 Simplifies SOPC Design

The Quartus II software version 2.2 simplifies SOPC design by including a new user interface, support for Stratix GX devices, and new incremental routing features in the SignalTap® II embedded logic analyzer to reduce verification cycles. The Quartus II software version 2.2 is now shipping to all customers with active subscriptions. For more information, refer to "Quartus II Software Version 2.2 Simplifies SOPC Design & Increases Productivity" on page 34.

New Device Support

The Quartus II software version 2.2 adds programming support for Stratix EP1S80 devices and adds advanced compilation and simulation support for new Cyclone and Stratix GX devices.

For more information on enabling Stratix GX support in the Quartus II software version 2.2, contact your local Altera sales representative.

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The Quartus II software version 2.2 includes full compilation, simulation, and programming support for new Altera devices as shown in Table 12.

Table 12. New Quartus II Device Support

Device Family	Device	Package
Stratix *(1)*	EP1S20	672-pin BGA
		672-pin FineLine BGA
		780-pin FineLine BGA
	EP1S30	780-pin FineLine BGA
		956-pin BGA
		1,020-pin FineLine BGA
	EP1S40	956-pin BGA
		1,020-pin FineLine BGA
		1,508-pin FineLine BGA
	EP1S80	956-pin BGA
		1,508-pin FineLine BGA
Cyclone *(2)*	EP1C6	256-pin FineLine BGA
	EP1C12	256-pin FineLine BGA
Stratix GX *(2)*	EP1SGX10C	672-pin FineLine BGA
	EP1SGX10D	672-pin FineLine BGA
	EP1SGX25C	672-pin FineLine BGA
	EP1SGX25D	672-pin FineLine BGA
		1,020-pin FineLine BGA
	EP1SGX25F	1,020-pin FineLine BGA
	EP1SGX40D	1,020-pin FineLine BGA
	EP1SGX40G	1,020-pin FineLine BGA

Notes to Table 12:

(1) Support includes compilation, simulation, and programming.

(2) Support includes compilation and simulation.

Quartus II Web Edition Supports All Cyclone Devices

The Quartus II Web Edition software is a free entry-level version of the Quartus II design software supporting all devices in the new Cyclone family. Also supported are selected Stratix, APEX II, APEX 20KE, Excalibur, MAX 7000AE, MAX 7000B, MAX 3000A, FLEX® 10KE, ACEX 1K, and FLEX 6000 devices.

The Quartus II Web Edition software includes a complete environment for FPGA design including schematic- and text-based design entry, HDL synthesis, place-and-route, verification, and programming. The Quartus II Web Edition software allows you to experience at no charge the performance and compile time benefits of the Quartus II software and eliminates all barriers to designing in high-performance FPGA and CPLD devices.

The Quartus II Web Edition software now supports devices from all mainstream Altera device families:

- Cyclone (all devices) New
- Stratix (EP1S10)
- APEX II (EP2A15)
- Excalibur (EPXA1)
- APEX 20KE (EP20K30E, EP20K60E, EP20K100E, EP20K160E)
- ACEX 1K (all devices)
- FLEX 10KE (EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, EPF10K200S)
- FLEX 6000 (all devices)
- MAX 7000AE (all devices)
- MAX 7000B (all devices)
- MAX 3000A (all devices)

The Quartus II Web Edition software includes integrated VHDL and Verilog HDL synthesis. The Exemplar Logic™ LeonardoSpectrum™-Altera synthesis tool is also available from the Altera web site for use in conjunction with the Quartus II Web Edition software. The Quartus II Web Edition software can also be used with third-party synthesis tools from Mentor Graphics®, Synopsys, and Synplicity®.

Introducing ByteBlaster II Cable

The ByteBlaster™ II programming cable is a direct replacement for the ByteBlasterMV™ programming cable. The ByteBlaster II cable offers all of the features of the ByteBlasterMV cable and adds the following new features:

- Support for active serial configuration mode to support the new low-cost EPCS1 and EPCS4 serial configuration devices
- Support for 1.8-V programming and configuration

The ByteBlaster II cable can be ordered today. It will begin shipping in January 2003 and is supported in the Quartus II software version 2.2 and higher.

Mentor Graphics' Precision Synthesis: The Next-Generation FPGA Synthesis Platform

by Tom Hill
Mentor Graphics

A major transformation is occurring in the area of electronic system design. The Altera® Stratix™ and Cyclone™ device families are providing designers with an environment to develop circuits with densities of 10 million plus system gates, frequencies over 300 MHz, and embedded processors and intellectual property (IP), enabling complete system integration. This technology leap is driving a shift in the design process by providing a comprehensive implementation platform outside the ASIC arena.

In the fast-moving world of programmable logic, the challenge that EDA vendors face is creating design tools and methodologies that keep pace with the increasing complexity and capacity of the silicon. For example, in the ASIC world, it took 15 years to merge the silicon process with a design methodology based on reliable and functional EDA software. ASICs have historically provided a cost-effective solution for the electronics industry which led to growth and innovation. ASICs popularity provided the driving force in the EDA industry and dictated the direction for software development. However, ASICs are moving out of the reach of many mainstream designers due to high upfront non-recurring engineering (NRE) costs and longer time-to-market. FPGAs are filling this void and will become the dominant approach for designers and the new driving force in the EDA industry.

FPGA design has many advantages over ASIC design. The user controls the entire design and layout process. Design cycle times are faster, photo-to-mask costs are nonexistent, and there are no minimum order restrictions. Historically, however, the low performance, comparatively smaller densities and high unit costs of FPGAs have relegated them to small, low-volume designs, with ASICs claiming the remainder of the market.

Altera is overcoming these market barriers by developing reconfigurable, system-level FPGAs, such as Stratix and Cyclone devices, offer high density and performance, and are bundled with IP support, including the Nios® embedded processor. These cores provide significant benefits to the designer such as: reduced system development time, improved power consumption, increased volume, expanded board space, and the flexibility to make changes right up to production time. These dramatic technological breakthroughs add design and verification challenges, and require new methodologies.

Altera is overcoming these market barriers by developing reconfigurable, system-level FPGAs, such as Stratix and Cyclone devices, offer high density and performance, and are bundled with IP support, including the Nios embedded processor.

For designers to take full advantage of these new capabilities, the supporting software tools must be prepared to handle any and all new issues a designer will face. Mentor Graphics® introduced its Precision Synthesis environment to solve this new set of problems.

Precision Synthesis Concepts

The architecture for Precision Synthesis had three major development themes:

- Intuitive user interaction
- Excellent quality of results
- Advanced analysis

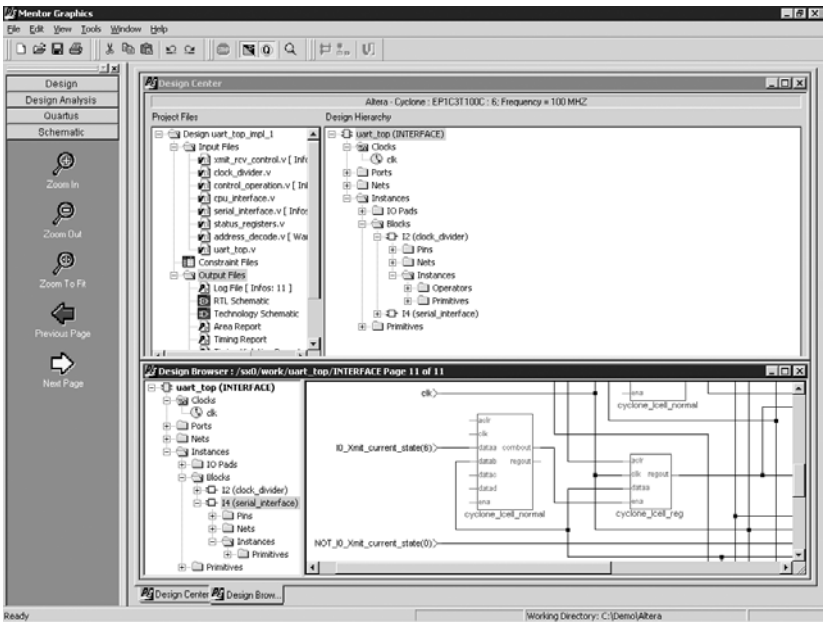
Intuitive Use

An EDA software product should be a tool that aids in the development, analysis, and debug of a design. It must drive the design process, but must also adapt to each user's design style. Precision Synthesis was designed with these requirements in mind. Designers only see the tasks and data that are relevant at a particular point in the design process, that is, data is not presented until it is needed. This focused view allows the designer to concentrate on the task at hand and provides an intuitive approach to synthesis (see Figure 1 on page 24).

continued on page 24

Mentor Graphics' Precision Synthesis: The Next-Generation FPGA Synthesis Platform, continued from page 23

Figure 1. Mentor Graphics' Precision Synthesis Interface



Focusing on critical path logic identified through timing analysis, Precision Synthesis automatically restructures logic to reduce logic levels and increases performance.

Precision Synthesis provides users a push-button synthesis flow without compromising results or flexibility. This flow was achieved by replacing user-configured synthesis options with automation. Optimization algorithms are automatically configured based on an analysis of a design against its constraints, eliminating the need to specify effort levels or optimization goals.

Intuitive use was also achieved by leveraging industry standards and knowledge whenever possible. For timing constraints, the industry standard Synopsys design constraint (SDC) format was adopted. As many ASIC designs are now being completed in FPGAs, the SDC format helps facilitate design reuse and increases productivity.

Excellent Quality of Results

Precision Synthesis includes a suite of unique algorithms called architecture signature extraction (ASE) optimization that automatically focuses specific optimizations on areas of the design that are most likely to hinder overall performance, such as finite state machines, cross-hierarchical paths, or paths with excessive combinational logic. ASE uses an automated, heuristic approach to deliver smaller and faster designs without the need for iterative user intervention.

Finite State Machine

New finite state machine optimization technology performs semantics-based analysis and state optimization. Finite state machine structures are reduced to mathematical models where all unnecessary states, such as terminal and redundant states, can be quickly identified and removed.

Retiming

A powerful new retiming algorithm is capable of pushing logic across register boundaries. In addition, Precision Synthesis is capable of retiming across entire operators and hierarchy boundaries to ensure optimal synthesis results.

Restructuring

Focusing on critical path logic identified through timing analysis, Precision Synthesis automatically restructures logic to reduce logic levels and increases performance. Precision Synthesis logic restructuring is automatically applied to portions of the design identified as critical.

Signature Analysis

A design's "signature" refers to its most abstract structures. Precision Synthesis begins the optimization process at the highest level of abstraction possible by identifying, extracting, and minimizing entire structures. Common examples include arithmetic logic, filters, data encryption, and DSP structures.

Module Generation

Precision Synthesis fully exploits the rich feature sets of the Stratix and Cyclone architectures through module generation and library of parameterized modules (LPM). Regular structures such as arithmetic and logic operators and memory elements are extracted and implemented using hand-crafted architectures.

Precision Synthesis' ASE technology is designed to take full advantage of Altera® device features by providing the smallest design that meets your target frequency, saving time by reducing design iterations and money by helping you fit into smaller devices or lower speed grades in the process.

Advanced Analysis

FPGAs have moved into the technology range where accuracy is paramount, and timing closure and high performance are now the design goals. The detailed timing and clocking requirements of the large systems now being designed into these devices combine to create complex requirements. The timing complexity can lead to excessive design iterations or even undetected timing problems affecting printed circuit board (PCB) debug.

To solve these new timing issues and to guarantee a reliable design, Precision Synthesis includes an advanced timing engine and enhanced design-analysis capabilities. Precision Synthesis' timing engine, PreciseTime, can handle the most complicated clocking schemes with speed and accuracy. Precision Synthesis provides valuable design debug capabilities beyond timing analysis, including:

- Reports of internal clocks including clock propagation information through simple gates, dividers, and phase-locked loops (PLLs).
- Reports of missing constraints that prevent comprehensive timing analysis.
- Reports of timing paths that cross asynchronous clock domains, allowing you to verify clock isolation or the existence of metastable-safe synchronization logic.
- Powerful schematic viewing with schematic fragment generation capabilities.

First-time success on your PCB requires a fully and accurately constrained design during synthesis—Precision Synthesis PreciseTime is designed to do just that.

Precision Synthesis: The Synthesis Platform

Precision Synthesis is designed to solve the entire synthesis problem. The synthesis domain is expanding from just the register transfer level, to the architectural and physical realm. Architectural synthesis provides you increased productivity; physical synthesis provides increased performance. Designers require tools with strong algorithms for optimization at each level of abstraction, plus a seamless methodology that allow easy migration throughout each phase of design.

The Precision Synthesis platform shares common GUI, schematic viewing, project management, database and timing analysis technology.

The Precision Synthesis platform shares common GUI, schematic viewing, project management, database and timing analysis technology. You can seamlessly move between abstractions while benefiting from a consistent user interface.

Conclusion

Precision Synthesis is the premier tool for doing the next generation of FPGA designs. With an intuitive user interface, excellent quality of results, and unparalleled analysis capabilities, Precision Synthesis can handle the toughest FPGA designs. The Precision Synthesis platform was designed to keep pace with the ever-changing landscape of programmable logic design. Mentor Graphics is committed to providing designers with the best EDA tools available to enable electronics design innovation. For more information about Mentor Graphics' Precision Synthesis platform or complete FPGA design product family, visit **www.mentor.com/fpga**.

BDTI Benchmarking FPGAs for DSP

by Jeff Bier
General Manager & Co-Founder
Berkeley Design Technology, Inc. (BDTI)

The latest digital signal processing (DSP)-enhanced FPGAs boast huge gate counts, ample supplies of hard-wired SRAM, and an abundance of hard-wired multipliers. These attributes hint at the potential for phenomenal performance in DSP applications, but the difference between potential performance and actual performance can be huge.

Simplified Metrics

Performance claims surrounding new devices must be viewed skeptically, especially when evaluating the DSP performance of FPGAs. For example, FPGA vendors sometimes quote the DSP performance of their devices in terms of multiplier-accumulators (MACs) per second. On the surface, this seems to be a reasonable approach since many DSP algorithms make heavy use of MACs, and DSP processor vendors are also fond of quoting processor performance in terms of MACs per second.

Similar to other overly simplified performance metrics, such as million instructions per second (MIPS), MACs per second suffer from a number of flaws (e.g., there is no universal definition of exactly what comprises a MAC operation). When FPGA vendors quote MACs per second numbers for their devices, their figures are often based on distributed-arithmetic implementations of finite impulse response (FIR) or non-recursive filters. Distributed arithmetic is a very natural way to implement a FIR filter on an FPGA. The problem is that in a distributed arithmetic FIR filter, the MAC operators rely on the fact that the coefficients of the filter are constants. If the MAC operations in your algorithm do not use constant coefficients (e.g., if you are building an adaptive filter or a correlator), the number of MACs per second that you can achieve with a particular FPGA will be lower. Even if there is a reliable way to assess the MAC performance of various devices, another serious problem arises—typical DSP applications do much more than MACs. As a result of these questions, the engineers at BDTI set out to determine the true DSP application performance of the current market's FPGAs.

For years, BDTI has been benchmarking the signal processing performance of DSPs and general-purpose processors using the BDTI Benchmarks™. BDTI Benchmarks are a suite of DSP algorithm kernels (e.g., fast Fourier transform (FFT) and Viterbi decoder) coupled with a methodology designed to ensure fair comparisons. This approach is very well suited for evaluating processors because of the way in which DSP applications are typically implemented on processors. On a processor, the most effective way to develop an optimized application is to find the parts of the application that burn most of the processor's time, and then aggressively optimize these sections. The optimized sections (algorithms) can then be used to create a well-optimized application. If you know a processor's performance on the key constituent algorithms, you can make pretty good predictions of the processor's overall performance in the application.

Over the last eight years, BDTI used this approach to evaluate over 50 processors. Using the same benchmarks for FPGAs would have had the advantage of allowing BDTI to quickly compare FPGAs to these previously benchmarked processors. Unfortunately, BDTI realized early on that this approach would not provide meaningful performance comparisons for FPGAs.

Holistic Optimization

In examining how high-capacity FPGAs are likely to be used in real DSP applications, BDTI reached the conclusion that individual algorithm kernels simply are not suitable as benchmarks for FPGAs. On a processor, when a particular algorithm is running, it has exclusive use of all of the processor's execution units. For this reason, it is useful to aggressively optimize each individual algorithm to make maximum use of all of the processor's computing resources. With an FPGA, you have the flexibility to trade off parallelism (and hence performance) against resource usage (in terms of logic blocks and multipliers). Unlike using a processor, it does not make sense to use all of the FPGA's available resources for a single

algorithm (that would leave no resources for the rest of the application). Instead, you must optimize the application as a whole, allocating the available hardware among each of the constituent algorithms.

To evaluate the DSP performance of FPGAs, BDTI needed a benchmark that looked more like a complete application and less like a single algorithm kernel. BDTI then considered what kind of application to use as the basis of the benchmark. BDTI's informal market research indicated that the new DSP-enhanced FPGAs were of strong interest to developers of communications systems, leading BDTI to develop a benchmark based on a communications receiver.

Cost Per Channel is Key Metric

For the initial benchmarking of DSP-enhanced FPGAs, BDTI decided to evaluate how many channels of their communications receiver each of the benchmarked devices could support. This decision allowed BDTI to measure the cost per channel, a key metric in the multi-channel applications that DSP-enhanced FPGAs are targeting.

The new benchmark consists of a simplified orthogonal frequency division multiplexing (OFDM) receiver, as shown in Figure 1. OFDM is a complex technique that is finding increasing use in a variety of high-speed data communications applications such as fixed wireless systems. All of the key parameters of the benchmark receiver, such as sample rates, filter lengths, and channel-code constraint lengths, are explained in a detailed benchmark specification. BDTI used a simplified receiver to make benchmark implementation more practical. For example, BDTI omitted the symbol deinterleaver and tone derandomizer ordinarily found in an OFDM receiver. Achieving an optimized implementation of this benchmark requires squeezing as many channels of the receiver as possible into a single device.

Implementing the Benchmark

BDTI invited Altera and Xilinx to implement the BDTI OFDM Benchmark on their DSP-enhanced FPGAs. BDTI also invited Motorola and Texas Instruments to implement the benchmarks on their high-end DSPs, which target communications infrastructure equipment. Altera and Motorola agreed to participate in BDTI's benchmark challenge, and each delivered a highly optimized implementation of the benchmark.

Some details of Altera's implementation of the benchmark are shown in Figure 1 and Table 1. Altera's Stratix™ family of DSP-enhanced FPGAs, which are now shipping, was used for this benchmarking effort (Q2 2002). The Motorola MSC8101 DSP, based on the StarCore SC140 core, was used. BDTI scrutinized both Altera's and Motorola's benchmark implementations for correct functionality and conformance to BDTI's specification.

Figure 1. BDTI Benchmarking Block Diagram

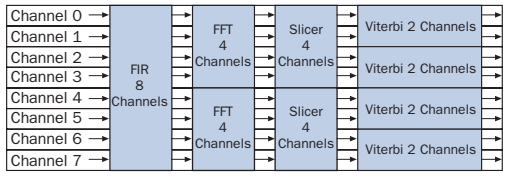


Table 1. Allocation of Key Hardware Resources

	LEs	DSP Units
FIR	15%	0%
FFT	35%	100%
Viterbi	50%	0%

continued on page 28

BDTI Benchmarking FPGAs for DSP, continued from page 27

Surprising Results

It is clear that the new DSP-enhanced FPGAs, with dozens of hardwired multipliers, RAM blocks, and tens of thousands of configurable logic blocks are capable of vast parallelism where applications are amenable to parallelization. However, as with a processor, an FPGA's throughput in an application depends not only on how much work it can perform in one clock cycle, but also on how high a clock speed it can attain. For processors, the maximum clock speed is easy to ascertain. For a given FPGA, the clock speed you can attain depends on what you are doing with it.

While BDTI expected the DSP-enhanced FPGAs to perform well, BDTI was surprised by just how well they did. For example, the Altera® Stratix EP1S20-6 device supports well over a dozen channels of BDTI's OFDM receiver benchmark. In contrast, the 300 MHz Motorola MSC8101 is only able to support about one-fifth of one channel.

On a cost/performance basis, the advantage of the FPGAs over the DSP is reduced somewhat compared to their throughput advantage. The latest DSP-enhanced FPGAs are expensive compared to DSPs: the Stratix EP1S20-6 device is priced at $325 (quantity 1,000), and the most expensive Stratix family members cost thousands of dollars per chip. In comparison, the Motorola MSC8101 currently sells for $140 in like quantities.

Full details on the results of our FPGA vs. DSP benchmarking work appear in our just-published report, *FPGAs for DSP*. (For details about the report, visit **www.bdti.com**.)

Other Factors Often Decisive

BDTI's initial benchmarking work suggests that the new DSP-enhanced FPGAs can indeed achieve impressive performance in certain types of DSP applications. BDTI's experience with these new devices, and discussions with users, indicate that factors other than performance are often important in decisions regarding the use of an FPGA. For example, one key challenge facing DSP developers using FPGAs is the relative complexity of the design process and the limited availability of DSP-specific features in the development tools compared to what is available for the best-supported digital signal processors.

Clearly, as with most technology, the decision of whether to use an FPGA for a DSP application requires a sophisticated, multi-dimensional evaluation—one that depends on a large number of specifics of the target application. In the research for BDTI's recently completed report, a framework to guide developers in this challenging process was created. BDTI will continue their benchmarking and analysis, tracking the new generations of DSP-enhanced FPGAs, processors, and other emerging technologies.

About the Author & BDTI

Jeff Bier is general manager and cofounder of BDTI, the DSP technology analysis and software development firm based in Berkeley, California. BDTI provides free information for developers of DSP systems on its web site (**www.bdti.com**). A version of this article first appeared in EDN magazine.

GIDEL Selects Stratix FPGAs for New DSP & Imaging Platform

by Reuven Weintraub
GIDEL

The ever-growing need for more cost-effective digital signal processing (DSP) and imaging solutions fuel innovation. The Altera® Stratix™ FPGA, combined with GIDEL's system design expertise, creates an ultra high-performance, yet flexible and cost-efficient DSP platform. With GIDEL's user-friendly development kit, you can prototype a DSP system in an extremely short time.

GIDEL's DSP solution is comprised of a PCI card containing up to three Stratix devices with a five-matrix memory architecture (see Figure 1), including the Stratix TriMatrix™ memory and two additional SDRAM memory levels for large amounts of data. The performance results from several initial test runs have been amazing. GIDEL observed a system which previously ran at only 50 MHz, operating flawlessly on the Stratix device at 133 MHz.

The performance of the Stratix-based DSP board is further enhanced by incorporating Altera's Nios® embedded processor with Stratix M-RAM blocks as program/data memory. The DSP blocks process the numbers in the Stratix logic, while the sophisticated real-time processing is accomplished by the Nios processors. The Stratix DSP board with the Nios embedded processor enables you to meet the performance challenge of DSP applications in more cost-effective FPGA boards where previous DSP device systems had an advantage.

In 1997, GIDEL completed development of a custom algorithm hardware-acceleration platform. Having expertise in hardware acceleration systems, GIDEL's next task was to create a highly customizable platform that could be utilized for a wider array of applications. At that time, a custom architecture had to be established for each and every algorithm. GIDEL used Altera FLEX® 10KE devices, along with a unique GIDEL memory controller intellectual property (IP), to accomplish this task.

The challenge was to build a singe flexible architecture that would address a range of complex tasks. A development board with FLEX 10KE devices, combined with dual-port memories, enabled simultaneous read and write cycles that were crucial for many algorithms. GIDEL augmented the board with dynamic memories controlled by an innovative memory controller IP—the PROC MultiPort. The memory controller enabled immediate access to Mbytes of DRAM beyond what common applications required. The IP also facilitated a virtual increase of the internal memory size and eliminated the need for external elements or devices. SRAM memories were then added to make random access possible.

Recently, GIDEL realized another technological leap was possible with Stratix devices. GIDEL initially set a new goal to replace a complete embedded architecture with a single customiz-

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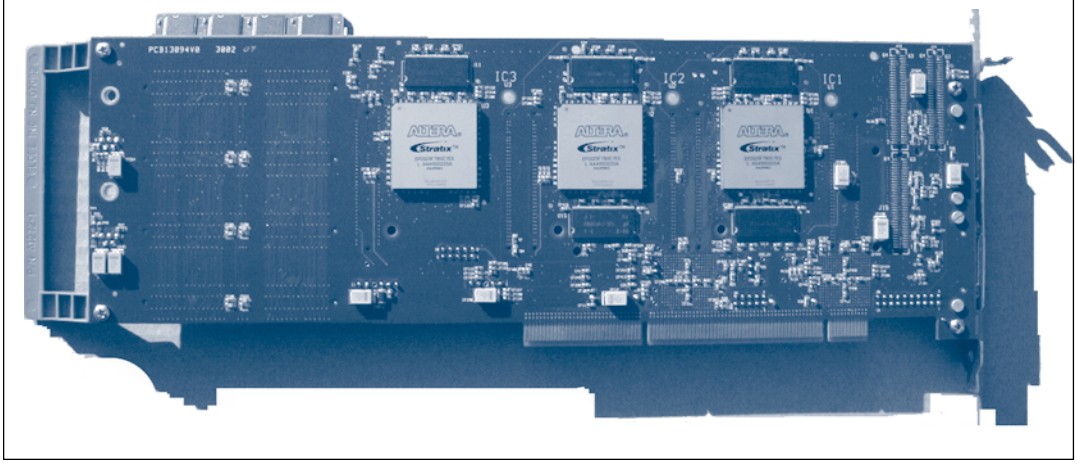
GIDEL's DSP solution is comprised of a PCI card containing up to three Stratix devices with a five-matrix memory architecture (see Figure 1), including the Stratix TriMatrix memory and two additional memory levels of SDRAM for large amounts of data.

Figure 1. Gidel PCI Card Containing Three Stratix Devices



Gidel Selects Stratix FPGAs for New DSP & Imaging Platform, continued from page 29

able board. However, when GIDEL began to design the Stratix-based PROCStar board, their intent became more ambitious. GIDEL used a Stratix-based board to carry out applications that until that point required the exclusive use of DSP processors. GIDEL knew that the main challenge was to achieve an aggressive cost-performance target.

Some of the challenges were:

- Developing higher computing capabilities.
- Creating a resource to operate sophisticated on-board logic.
- Building an advanced memory architecture to support the computing capabilities.

The solution GIDEL developed was based on several key elements:

GIDEL's customers utilize the Stratix-based PROCStar as a universal FPGA development platform for a wide range of embedded applications.

- The combination of DSP blocks and Stratix logic cells accompanied by a high device clock-speed to enable extremely high computing power, even for applications requiring simultaneous multiplication operations.
- Sophisticated logic carried out by a host via the board's PCI interface.
  - Using a dedicated Nios embedded processor offered an enhanced real-time connection with number crunching being carried out by the DSP blocks and logic cells.
- Up to 364 I/O pins available for system connections.
- An advanced five-matrix memory architecture to enable the needed on-board computing tasks.
  - The large number of Stratix M512 and M4K memory blocks allows parallel access to memories attached to the processing units. The memories are used as look-up tables (LUTs), delay lines, filters, coefficients, first-in first-out (FIFO) buffers, and mediating memories for butterfly calculations. A segmented mode option facilitated by PROC MultiPort IP enables virtual magnification of the memory depth.
  - The Stratix M-RAM blocks complement the attached memory array for computing when large LUTs and random access are required.
- The PROCStar board includes up to five blocks of 32/64 Mbytes of memory.
  - These memory blocks operate with access speed of 3 to 4 Gbytes per second and may be operated with dozens of parallel channels using the PROC MultiPort. These memory blocks allow different tasks, each operating at their own speed. The PROC MultiPort wrapper is automatically generated to your requirements by Gidel's CoreWizard.
- The memory array is complemented by a memory block up to 2 Gbytes in size.
  - It can store a complete data set for repeated use inside the card to significantly decrease traffic on the PCI bus. The two large memories often eliminate the need for real-time host software.

The complexity of the algorithms performed on the PROCStar board requires a firm, stable connection between the host code and the Stratix device. GIDEL developed the PROCWizard software to manage this task. The software performs automatic code integration between the host and FPGA. The PROCWizard software tool has been utilized successfully for over four years and has a record of reducing non-recurring engineering (NRE) costs while enabling a fruitful, synergic cooperation between project teams.

GIDEL's customers utilize the Stratix-based PROCStar board as a universal FPGA development platform for a wide range of embedded applications. Customization is a simple task that minimizes NRE costs and development time.

Conclusion

The drive for cost-efficient DSP and imaging solutions, along with inevitable technological advances, will keep producing flexible, ultra-high-performance DSP systems such as the Stratix PROCStar board offered by GIDEL. Using Stratix devices, GIDEL is able to offer a powerful, yet flexible development platform that meets the cost-performance needs for the most demanding applications.

Developing Flexible, High-Performance Inspection Systems for Flat-Panel Displays

by Brian Tithecott
Development Manager
Avvida Systems

The popularity of flat-panel displays (FPDs), including plasma display panels (PDPs) and liquid-crystal displays (LCDs), has forced companies to streamline their production. FPDs are increasingly replacing cathode-ray tube (CRT) screens, and are at a critical juncture where high availability and lower prices will drive further customer adoption. As a result, FPD manufacturers such as Pioneer, NEC, Fujitsu, Matsushita, and Sony are currently making major steps to drive their costs down. One of the most important, potentially time-consuming, and costly phases of FPD production is the inspection process, in which automated optical inspection and image processing techniques are used to identify production defects. Historically, the digital signal processing (DSP) functions required by this application would be implemented in DSP processors. However, much higher speed DSP functions can be built using programmable logic, which retains the needed flexibility of DSP processors while maintaining the performance advantage over normal multi-DSP processor systems.

If performed efficiently and economically, the FPD inspection process can reduce manufacturing costs significantly. For example, in the case of PDPs, an inspection is performed on two glass panels before they are bonded together to form a single complete panel. If defects are found in either of the two panels, they can often be repaired and reintroduced to the manufacturing process, resulting in yield recovery. If a defective panel is bonded to a good panel, the resulting complete panel must be scrapped.

During the prototyping and early manufacturing stages of PDP products, inspections were generally performed by a single charge-coupled device (CCD) sensor moving snake-like across the surface of the panel, taking as long as 60 seconds to complete. This kind of inspection produced a data stream of about 160 Mbytes per second. Currently, these types of inspections are being replaced with multiple parallel sensors inspecting a panel in a single pass. Further, the resolution of the optical inspections is being increased to identify smaller defects and increase the quality of the resulting product. Whereas earlier PDP inspections had a resolution of 5 to 7 microns, current inspections on LCD panels are being done at 1-micron resolution. These factors are increasing the bandwidth of visual data that must be processed to several gigabytes per second.

Early FPD inspection systems relied on DSP and other special-purpose processors to implement the inspection algorithms. An early system developed by Avvida consisted of 21 function-specific boards in a VME chassis using discrete logic, transporters, and DSP processors, and cost over $100,000 USD. As the inspections grew more demanding and data bandwidths increased beyond the capability of DSP processors, Avvida turned to programmable logic and a new processing architecture called JEDI to accelerate the DSP functions. The system Avvida developed was based on 12 Altera® FLEX® 10K FPGAs occupying three boards, and as a result benefited from a 50% reduction in the amount of hardware complexity and corresponding cost. In addition, the move to programmable logic allowed Avvida to develop a product with which they could focus on developing the algorithms as opposed to recreating the hardware with each new generation or version of the product. This reliance on hardware reconfigurability makes investment in algorithm and application development easily transferable to the next generation of programmable logic.

In Avvida's latest image processing system (called Tsunami), one Altera Stratix™ FPGA resides on a Tsunami board, but you can add more Stratix FPGAs for additional processing power via JEDI II daughter card modules. Using the higher-speed Stratix FPGAs allows an input bandwidth of over 3 Gbytes per second and processing speed in the teraops range at a total system cost of less than $10,000 USD. The algorithms involved in FPD inspection require large amounts of rapid-

continued on page 32

Company:
Avvida Systems

Industry:
Industrial Imaging

End Product:
Industrial Imaging Development Systems

Altera Products:
Stratix Devices
FLEX 10K Devices

Developing Flexible, High-Performance Inspection Systems for Flat-Panel Displays, continued from page 31

access integrated memory and several high-speed image processing functions such as convolution, erosion, dilation, and comparison. A next-generation FPD inspection algorithm implemented with the on-board Stratix FPGA and another Stratix FPGA on a JEDI II module is shown in Figure 1.

Elements of a Next-Generation FPD Inspection Algorithm

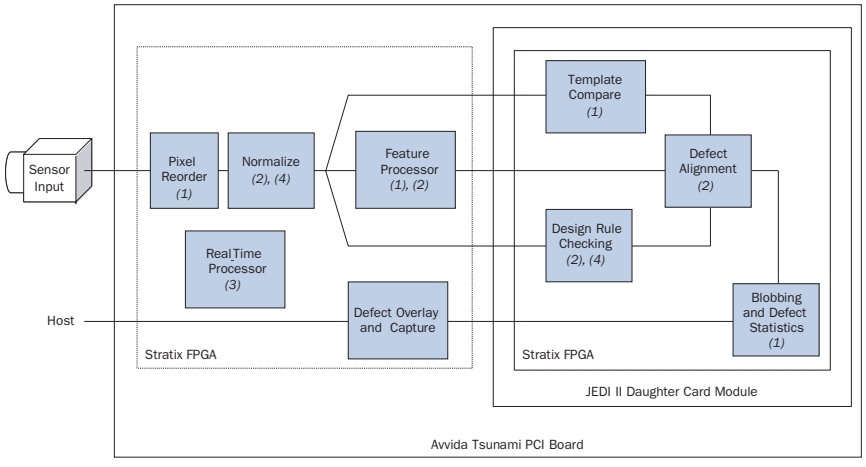
The output of the Feature Processor, Template Compare, and DRC blocks is then fed into the Defect Alignment block, which aligns the data streams using Stratix M-RAM blocks and compares them to further identify defects.

In the Pixel Reorder block, data from multiple digital cameras is brought into the system in many independent streams called "camera taps." The individual taps are re-formatted to produce a single contiguous image. This block relies on high-speed data storage and uses the Stratix M4K memory blocks. To compensate for irregularities in optical configuration, the Normalization block performs individual pixel correction, gain, and offset. Normalization uses the Stratix DSP blocks as well as the large on-board M-RAM blocks for look-up tables (LUTs) and correction curves. Next, the Feature Processor identifies the location of certain features (end points, crosses, and T-junctions) in the structure of the fine line conductors linking each pixel to the driver circuitry. This technique, called "skeletonization," uses a Stratix M4K block, an M-RAM block, and an external DRAM memory bank to store feature data that the host can read from and write to. The Feature Processor then flags additional or missing features as defects.

In parallel with the Feature Processor, the data also undergoes a template comparison, in which the individual display cells are compared. Any cell-to-cell irregularity is flagged as a defect. The comparison algorithm uses Stratix M4K blocks and two external DRAM memory banks to store and delay the image data corresponding to the prior cell. In the Tsunami system, this template comparison can also be performed using a known good or "golden" template. Also, in parallel with the Feature Processor and Template Comparison is the Design Rule Checking (DRC) stage. The DRC stage uses Stratix DSP blocks to gauge the interconnect trace dimensions to predefined minimum and maximum limits. Features smaller or larger than the design rule are considered defects.

The outputs of the Feature Processor, Template Compare, and DRC blocks are then fed into the Defect Alignment block, which aligns the data streams using Stratix M-RAM blocks and compares them to further identify defects. The resulting defect data is then routed to the Blobbing and Defect Statistics block, where a blobbing function extracts detailed statistics about identified defects. Defect type, location, orientation, and size are passed on to the host application for defect

Figure 1. Next-Generation FPD Inspection Algorithm



Notes to Figure 1:
(1) Uses Stratix M4K memory blocks.
(2) Uses Stratix M-RAM memory blocks.
(3) Uses the Nios® embedded processor.
(4) Uses Stratix DSP memory blocks.

analysis and reporting. The identified defects are also passed on to the Defect Overlay and Capture block, which allows the equipment operator to quickly identify defective areas on the panel under inspection. Captured defect images are also sent to the host and stored with the defect statistical data for further review and analysis.

Overseeing the real-time operation of the Tsunami board is the Nios embedded processor. A local controller such as the Nios processor is needed since the host processor operating system in a PCI-based system may not be able to respond in real time. The Nios processor controls the overall image processing portions of the inspection process and is responsible for initiating, idling, or stopping the process as needed. The Nios processor also handles passing the data to the host. Integrating the processor into the on-board FPGA eliminates the need for an external processor, saves on-board development and other engineering costs, and keeps the system complexity in check.

Reconfigurability Critical to In-Field Operation, Reduces Development Costs

The reconfigurability of Avvida's inspection systems allows them to be optimized to a high degree for specific applications. In the case of FPD inspection, the algorithms in the FPGAs are developed to correspond to the specific requirements of the environment at the manufacturer's inspection site. These algorithms are further tuned iteratively until the desired results are obtained. Designers can address differences in CCD sensors, emphasis on detecting different types of defects, and variations resulting from process changes with refinements to the algorithms programmed into the FPGAs. Further, designers can modify the system via FPGA reconfiguration to handle inspection of different sizes or types of panels, allowing the end user a high degree of flexibility with respect to the system's application. By building a modem into the system, Avvida can also reconfigure their systems remotely, addressing customer needs for upgrades, system adjustments, enhanced functionality, or completely new functions.

Building reconfigurability into these systems also decreases their associated development costs. Avvida can focus research and development investment on algorithm development rather than hardware development. Avvida can then take advantage of the next generation of FPGAs by building new daughter boards rather than rebuilding the whole system. Designers can easily migrate the algorithms from one FPGA design to the next, and you can develop new applications in a matter of days or weeks, allowing Avvida to reduce their engineering costs. Avvida estimates that they are saving 70% of the engineering resource time using this approach compared to past hardware design approaches.

Altera's Stratix FPGAs are ideal for high-bandwidth image processing tasks in terms of their feature set and density.

Conclusion

Altera's Stratix FPGAs are ideal for high-bandwidth image processing tasks in terms of their feature-set and density. With large amounts of flexible, on-board memory, and dedicated structures for implementing DSP functions, the latest generation of programmable logic technology allows hardware designers to be more creative in tackling DSP-related tasks. With the availability of mature embedded processors for programmable logic, DSP designers can continue enjoying the benefits of a software-based design flow while taking advantage of the hardware acceleration traditionally offered by FPGAs. These advantages, currently enjoyed by FPD inspection systems, can easily be extended to other image processing and DSP applications. DSP designers will increasingly need to consider programmable logic if they want to deliver best-in-class solutions.

Quartus II Software Version 2.2 Simplifies SOPC Design & Increases Productivity

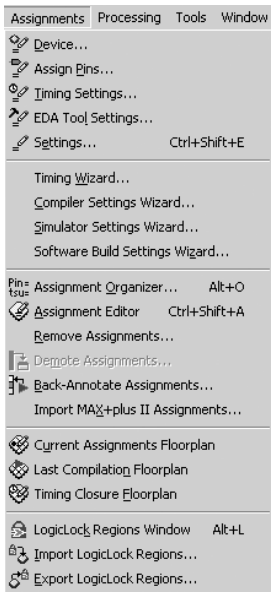
The Quartus II software user interface has been redesigned based on user feedback and extensive usability testing to provide a more intuitive and user-friendly experience.

The Quartus® II software version 2.2 simplifies system-on-a-programmable-chip (SOPC) design by including a simplified user interface, an integrated wizard interface to implement the latest high-speed transceiver protocols—up to 3.125 gigabits per second (Gbps)—and new incremental routing features in the SignalTap® II embedded logic analyzer to reduce verification cycles. For an overview of the new features and enhancements in Quartus II software version 2.2, refer to Table 1 and Altera's web site at **www.altera.com**. The Quartus II software version 2.2 is now shipping to all customers with active subscriptions.

Simplified Quartus II User Interface

The Quartus II software user interface has been redesigned based on user feedback and extensive usability testing to provide a more intuitive and user-friendly experience. The Compile, Simulate, and Software Build mode selections have been removed; all modes of operation are now available from the same menu structure. The new Assignments menu organizes all settings and assignments commands for the project in one convenient location (see Figure 1). The **Settings** command (Assignments menu) provides a tree-type display with access to all Quartus II settings options. The Assignments menu also includes an **Import MAX+plus II Assignments** command to facilitate migrating a design from the MAX+PLUS® II to the Quartus II software. The File, Project, and Processing menus have all been reorganized and restructured to make the user interface more intuitive.

Figure 1. Assignments Menu



Memory Compiler MegaWizard

You can now use a new Memory Compiler MegaWizard® Plug-In to create and instantiate all types of memory in all device families. In previous versions of the Quartus II software, different MegaWizard Plug-Ins were used to implement different types of memory or to target a specific device family.

New Spreadsheet Assignment Editor

The Quartus II software version 2.2 includes a new Assignment Editor. You can use the new Assignment Editor to view and make assignments for all device families; however, location assignments can only be made for Stratix™, Stratix GX, and Cyclone™ devices in this release. The new Assignment Editor displays assignments made by the Assignment Editor or the Assignment Organizer in a spreadsheet display. The new Assignment Editor interface is very intuitive. For example, after an assignment option is selected, the source and destination fields are enabled or disabled and the value field changes to a pull-down menu selection or text entry box based on the requirements of the selected option. Using the category field, you can view all assignments made in a project or just a particular type of assignment, and then edit those assignments directly in the spreadsheet display (see Figure 2).

The explicit source and destination fields make it easy to use the new Advanced Assignment options, such as Manual Logic Duplication. To duplicate a register, you can select a source register to duplicate, select the destination entity you want to connect to, and assign a name for the duplicate value in the value field.

Place-&-Route & Timing Closure Enhancements

Refined place-and-route algorithms deliver 5% faster push-button performance and over 10% faster compile times for the fastest speed grade Stratix devices compared to the previous Quartus II software release. A new push-button optimization option can use fitter timing information to increase design performance as much as 20% faster. The Quartus II software version 2.2 now delivers the best push-button performance available for MAX® 3000A, MAX 7000AE, and MAX 7000B device families. You can use a new routing congestion floorplan view to guide manual placement of logic and LogicLock™ regions to further optimize design performance (see Figure 3).

Figure 3. Routing Congestion Floorplan View

SignalTap II Analyzer Gets Incremental Routing & Usability Enhancements

The SignalTap II embedded logic analyzer allows you to capture the state of any internal node or I/O pin on a device in real time, operating at system speeds. The Quartus II software version 2.2 adds the ability to incrementally add or change which nodes are being monitored without performing a full recompile, saving valuable debug time. For more information on the new SignalTap II features, refer to "The Solution for Hardware Verification at Real System Speeds" on page 37.

Figure 2. Assignment Editor

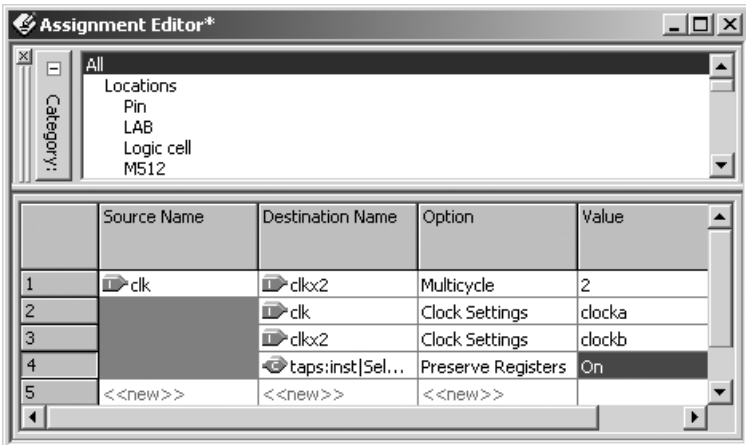


Table 1 on page 36 lists the new features in the Quartus II software version 2.2.

Easily Implement High-Speed Transceiver Protocols

The Quartus II software version 2.2 includes full design flow support for Stratix GX transceivers by providing behavioral simulation models along with an integrated wizard interface to implement the latest high-speed transceiver protocols (e.g., 10 Gigabit Ethernet XAUI and SONET) or your custom protocols in Stratix GX devices. The wizard interface asks you to select parameters such as protocol, operation mode (duplex, receiver, or transmitter), number of channels, channel width, optional input and output ports, and data rates to fully configure the Stratix GX transceivers for backplane applications and high-speed chip-to-chip communications. Contact your local Altera® sales office to enable Stratix GX support in the Quartus II software.

The SignalTap II embedded logic analyzer allows you to capture the state of any internal node or I/O pin on a device in real time, operating at system speeds.

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Quartus II Software Version 2.2 Simplifies SOPC Design & Increases Productivity, continued from page 35

Table 1. New Features in the Quartus II Software Version 2.2

Design	■ Redesigned User Interface ○ Removal of modes: Compile, Simulate, and Software Build menus are now available at all times ○ New Assignment menu provides access to all device, pin, and other assignment options as well as access to all settings, windows, and floorplan editors ○ New Settings window includes all settings options ○ New Assignment Editor provides spreadsheet like interface to view assignments (all families) and make assignments (location assignments for Cyclone, Stratix, and Stratix GX devices only) ■ New Memory Compiler MegaWizard Plug-In Manager provides single interface to instantiate all types of memory in all device families ■ Includes Stratix GX behavioral simulation models along with an intuitive MegaWizard Plug-In Manager interface to implement the latest high-speed transceiver protocols such as 10 Gigabit Ethernet XAUI, SONET, or custom protocols in Stratix GX devices ■ Remove Assignments dialog box allows obsolete assignments and categories of assignments to be removed from a design easily ■ The MegaWizard Plug-In Manager now includes a *Return to this page for another create operation* option to easily create multiple megafunction variations and a new copy function to copy existing megafunctions ■ Area estimates are included for `ALTMEMMULT`, `ALTMULT_ADD`, and `LPM_ADD_SUB` megafunctions; estimates for other megafunctions will be included in future Quartus II software releases
Synthesis	■ Synplicity® Synplify® added a new multipoint synthesis option that supports the LogicLock design flow and full DSP block inferencing for Stratix family designs ■ Support for new pragmas to guide synthesis results when using the Quartus II software's integrated synthesis
LogicLock Block-Based Design Flow	■ Added ability to flip LogicLock regions horizontally for Stratix designs ■ Added virtual I/O support for Mercury™ designs ■ Added option to ignore LogicLock region back-annotated location contents so you can experiment with different settings without deleting assignments
Place-and-Route	■ The *Limit to one fitting attempt* option allows you to get a quick estimate of timing before you perform a full place-and-route ■ Reporting enhancements ○ Mid-compilation reporting of estimated delay from placement ○ Improved peripheral signal table reporting for APEX™ 20K, APEX II, Excalibur™, FLEX® 10KE, ACEX® 1K, and MAX device families ○ Delay chain summary added for older families ○ New report panels display user settings ■ New netlist optimization option uses fitter timing information to re-synthesize and optimize a design ■ Preserve register assignment available to define which registers should not be touched by the register retiming netlist optimization feature ■ Timing closure floorplan improvements ○ Now can be used for all device families (not all features are available for all device families) ○ Now displays user-assigned pin labels ○ Enhanced critical path display by enabling you to filter by source and destination node names, display delay for path components, and display a slack-based critical path report ○ You can use a new routing congestion floorplan view to guide manual placement and assignment decisions ○ Significantly reduced launch time when loading large designs ■ Ability to manually duplicate logic for Stratix, Stratix GX, and Cyclone designs using an assignment ■ Improved MAX 3000A, MAX 7000B, and MAX 7000A performance by an average of 10% while reducing the average number of macrocells used to implement a design
Verification	■ SignalProbe™ support for Cyclone and Stratix GX devices ■ SignalTap II embedded logic analyzer (ELA) Enhancements ○ Incremental routing capability allows you to incrementally add/change nodes monitored without performing a full recompile ○ Ability to export captured data in **.vwf**, **.tbl**, **.vec**, **.csv**, and **.vcd** file formats for display and analysis in other tools ○ Resource usage estimator displays how many logic and memory resources are required for a given SignalTap II ELA configuration ○ New status bars guide you through tasks of configuring and using the SignalTap II ELA ■ You can now perform PowerGauge™ power estimation for given start and stop times ■ You can now use the Design Assistant to identify design problems for all device families ■ EDA Netlist Writer improvements ○ Automatically bring out device wide set/reset signals as ports ○ Option to maintain design hierarchy in simulation netlists ○ Generate simulation netlists with or without SDF files so behavioral simulation netlists can be generated at any stage of the design process ■ Stratix IBIS model generation ■ Synopsys PrimeTime static timing analysis support for Cyclone and Stratix GX devices

The Solution for Hardware Verification at Real System Speeds

Verification issues that occur late in the design cycle require a great deal of time and effort to debug. These functional errors can significantly affect production schedules, which inevitably increases the time-to-market of the product.

Altera has developed two in-system verification features that utilize the programmable nature of system-on-a-programmable-chip (SOPC) designs to help designers analyze their system at the board level. These methods are the SignalTap® II embedded logic analyzer and SignalProbe™ debugging technology. The SignalTap II and SignalProbe technologies fit seamlessly into any third-party synthesis flow and do not require any modifications to the HDL design source files.

The Design Verification Dilemma

It is common for a designer to power up their PCs and see unexpected results. This result is due in part to the lack of functional verification done on the front-end of the design cycle, and largely dependent on the stimulus provided to test the design. Many times a complete set of test vectors is not available, leading to unexpected behavior when the design is tested in a real environment.

Verification Difficulties Using BGA packages

A traditional verification method that many designers employ is to manually route internal signals to unused I/O pins. The designer can then connect the test pins to an external logic analyzer where the internal signals can be monitored. This method works well where the printed circuit board (PCB) is relatively small and access to I/O pins is not an issue. However, this debugging technique is not always practical. Access to ball-grid array (BGA) pins can be difficult and can potentially require changes to the PCB. These changes are expensive to make and ultimately delay design production. Manually adding debug signals to I/O pins requires changes to the design files and can change design performance.

The SignalTap II Embedded Logic Analyzer Solution

The SignalTap II embedded logic analyzer is a second-generation, system-level debug tool that captures and displays real-time signal behavior in an SOPC design, giving designers the ability to observe interactions between hardware and software in their system design. The SignalTap II embedded logic analyzer is comprised of a soft intellectual property (IP) core, programming hardware, and analysis software. See Table 1 for SignalTap II features.

Table 1. SignalTap II Logic Analyzer Features

Feature	Description
Up to 1,024 channels	Allows you to capture a wide variety of signals including internal nets, input pins, output pins, and data buses.
Up to 128K samples per channel	A large sample depth allows you to capture infrequent events.
Multiple analyzers within one FPGA	Supports analysis of signals from multiple clock domains.
Real-time data capture	Supports data capture of signals of up to 200 MHz.
Incremental routing	Allows you to incrementally change signal selections without performing a full design recompile.
Data log	Allows you to store captured data and compare results to previous runs.
Up to 10 trigger levels	Allows you to apply complex filters to signals, thereby capturing only relevant data.
Multiple trigger settings	Allows data capture of complex events that occur infrequently.
Four separate trigger positions	Allows data capture of different ranges relative to the trigger event.
Included with the Quartus® II software at no additional cost	Available for free with an active Altera subscription.

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The Solution for Hardware Verification at Real System Speeds, continued from page 37

You can compile the SignalTap II logic analyzer by enabling a switch within the Quartus II design environment, resulting in a programming file that embeds the logic analyzer in the design.

A SignalTap II File (**.stp**) contains all of the SignalTap II configuration settings. During the Quartus II compilation, the logic analyzer is automatically placed with the rest of the design. The resulting programming file is then used to configure the target FPGA.

Once the target FPGA is properly configured, you start the SignalTap II logic analyzer by clicking **Run**. Data capture commences once the user-specified trigger conditions are satisfied.

The SignalProbe feature allows you to route user-specified signals to output pins without affecting the existing fitting in a design.

The SignalTap II logic analyzer uses the FPGA's internal memory to store captured data. The captured data is then transferred from internal memory to the SignalTap II interface in the Quartus II design environment via an Altera programming cable.

New SignalTap II Features in Quartus II Version 2.2

Several new features are included with the release of the Quartus II software version 2.2.

Incremental Routing

The incremental routing feature allows you to change the nodes that are monitored without having to perform a full recompile.

Waveform Export Utility

This feature allows users to export the acquired data to industry-standard formats that could be used with third-party simulation tools. The export file types are:

- Comma Separated Values (**.csv**)
- Table File (**.tbl**)
- Value Change Dump (**.vcd**)
- Vector Waveform File (**.vwf**)

Resource Usage Estimator

This feature allows users to determine SignalTap II resource usage before compilation. This feature is important when FPGA resources are limited. The verification engineer can tailor the SignalTap II settings based on the available resources. As the SignalTap II configuration is modified, the resource usage estimator values dynamically update to show estimated logic element (LE) and memory usage.

SignalTap II Health Monitor

This feature provides useful information on the status of the SignalTap II logic analyzer.

The SignalProbe Solution

The SignalProbe feature allows you to incrementally route user-specified signals to output pins without affecting the existing fitting in a design and without performing a full compilation.

You can use the SignalProbe feature with I/O pins that are reserved prior to compilation, or I/O pins that are unused in a post-compilation design. You must assign a SignalProbe source from a post-compilation design; the source cannot be an Excalibur™ stripe I/O pin, a dedicated clock or a `DDIO` output pin, and it cannot have a carry or cascade chain fan-out.

Conclusion

As the device geometry of FPGAs decreases in size, verification engineers will find it increasingly difficult to access device I/O pins for debugging purposes. With the aid of the SignalTap II logic analyzer, this problem becomes virtually non-existent.

If FPGA resources are limited, verification engineers can use the SignalProbe feature in conjunction with external debug equipment to monitor internal signals.

Both the SignalTap II logic analyzer and the SignalProbe feature offer a variety of configurations, making them ideal tools for debugging FPGA designs.

Altera's Embedded Processor Portfolio Offers Designers Over 100 Free Ready-Made Processor Designs

The Altera® Embedded Processor Portfolio is a collection of pre-built processor configurations targeting a wide variety of microcontroller and embedded processor applications. Altera solidifies its position as the industry leader in embedded configurable processors by offering the Embedded Processor Portfolio at no cost to designers who are targeting Altera's Cyclone™, Stratix™, Excalibur™, and APEX™ device families. You can freely design and ship products containing Embedded Processor Portfolio designs. There are no license or royalty fees required.

The Embedded Processor Portfolio is based on the popular Nios® embedded processor architecture, Excalibur devices, and Red Hat's GNUPro Toolkit, providing an industry-proven development environment. The processor selection process for an Embedded Processor Portfolio design is very similar to the selection process for a traditional microcontroller unit. Simply select from a table the processor design that best meets peripheral and performance requirements. The processor hardware design is pre-compiled and ready to download to an Altera FPGA for prototyping in hardware. With all the tools at hand, you can begin developing software immediately.

The Embedded Processor Portfolio contains designs compiled for Cyclone devices, Altera's new low-cost device family, targeting price-sensitive applications such as digital entertainment boxes, low-end routers and switches, industrial motor and servo controllers, and automotive telematics. A 32-bit Nios embedded processor in a Cyclone device is cost-competitive with discrete 32-bit microcontrollers available today. The Embedded Processor Portfolio also includes designs compiled for high-performance, high-density Stratix devices in addition to Excalibur and APEX devices. Stratix processor designs take advantage of the vast on-chip Stratix device memory resources and utilize digital signal processing (DSP) blocks. The Embedded Processor Portfolio offers over 100 processor designs that cover a wide range of applications, several of which are shown in Table 1 on page 40.

The Embedded Processor Portfolio lowers the barrier for developers interested in exploring custom embedded-processor solutions. All of the Embedded Processor Portfolio processor designs were generated with SOPC Builder, Altera's system development and integration tool. If an Embedded Processor Portfolio design does not meet the needs of a particular application, you can use SOPC Builder to modify and re-generate a processor system, creating a custom solution to fit the exact needs of the application.

The Embedded Processor Portfolio CD-ROM is available today, free of charge. Designers can request the portfolio on-line at **www.altera.com/processorportfolio**. The CD-ROM contains over one-hundred pre-built processor designs, documentation, and development tools. In addition to the Red Hat GNUPro Toolkit C/C++ compiler and utilities, each processor design contains a software development kit (SDK) with example source code and libraries. The free Quartus II Web Edition software and the SOPC Builder development tool are also included, enabling you to modify existing designs or create new, custom system-on-a-programmable-chip (SOPC) designs.

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The Embedded Processor Portfolio contains designs compiled for Cyclone devices, Altera's new low-cost device family, targeting price-sensitive applications such as digital entertainment boxes, low-end routers and switches, industrial motor and servo controllers, and automotive telematics.

Altera's Embedded Processor Portfolio Offers Designers Over 100 Free Ready-Made Processor Designs, continued from page 39

Table 1. Selected Subset of the Embedded Processor Portfolio

Family	Cyclone								Stratix			Excalibur		
Device	EP1C3				EP1C20				EP1S25			EPXA1		EPXA10
Processor Name	Nios32_1C3_C	Nios16_1C3_D	Nios16_1C3_E	Nios16_1C3_G	Nios32_1C20_D	Nios32_1C20_E	Nios32_1C20_F	Nios32_1C20_J	ios32_1S25_C	Nios32_1S25_G	Nios32_1S25_K	ARM_XA1_F	ARM_XA1_J2	ARM_XA10_H
CPU Speed (MHz)	50	50	50	50	50	50	50	50	50	50	50	166	200	200
CPU Data Width (Bits)	32	16	16	16	32	32	32	32	32	32	32	32	32	32
JTAG Debug												Y	Y	Y
Multiply Instruction					Y	Y		Y	Y	Y	Y			
DSP Extensions (Divide, FIR, and FFT hardware acceleration)						Y								
On-Chip RAM (Kbyte)	4	4	4	4	28	22	28	24	128	128	128	16	16	32
On-Chip ROM (Kbyte)	1	1	1	1	1	1	1	1	1	1	1			
Max. Off-Chip SRAM (Byte)	256K	32K	32K	32K	256K	256K	256K	256K		256K		8M	8M	8M
Max. Off-Chip Flash (Byte)	256K	16K	16K	16K	256K	256K	256K	256K		256K		8M	8M	8M
SDRAM Controller						Y		Y	Y				Y	Y
Serial UART Channels	4	1	7	2	6	2	6	4	4	20	2	16	2	2
SPI Channels (Master)	1			1			2			2			1	
SPI Channels (Slave)	2			2			2			4			2	
Internal Ethernet MAC								1						1
External Ethernet MAC/PHY Interface							1				2		2	
General-Purpose I/O (GPIO) Pins with Edge-Sensitive IRQ	48	48	24	32	176	48	56	48	24		40	16		32
Edge-Sensitive IRQ Pins	4	4	4	4	16	8	8	8	8	8	4	8		8
DMA Controller	Y				Y			Y	Y		Y		Y	Y
PWM Channels				6			8							
Timer	4	2	1	4	4	4	6	4	4	4	4	2	2	2
Watchdog Timer	1	1		1	1	1	1	1	1	1	1	1	1	1

Discontinued Devices Update

Altera will be obsoleting select devices from product-term and FPGA families (see Table 1). Most of the devices will have longer-than-usual last-time buy (18 months) and last-time ship dates (an additional 6 months) to allow customers to gradually transition to using alternative ordering codes.

Select ordering codes from mature families such as MAX® 7000S are being obsoleted to increase the operational efficiency in the manufacturing flow. On mainstream product families such as the MAX 7000A, FLEX® 10KE, APEX™ 20K and newer product families, such as the MAX 7000B, ACEX® 1K, and APEX 20KE, ordering codes have been consolidated to offer a limited set of codes that will cover the various package and speed grade options.

Continued support for devices beyond the phase-out period may be available through Rochester Electronics, an extended after-market supplier. For more information, contact Rochester Electronics at (508) 462-9332 or your local Altera sales office.

Continued support for devices beyond the phase out period may be available through Rochester Electronics, an extended after-market supplier.

Table 1. Discontinued Device Update

Product Family	Device	Last Order Date	Last Shipment Date	Reference
MAX 7000	Selected devices with a dry pack option	05/31/02	11/30/02	PDN 0117
	EPM7192EGM160-15	05/31/02	11/30/02	PDN 0117
MAX 7000S	Selected devices in plastic quad flat pack (PQFP) and thin quad flat pack (TQFP) packages	05/31/02	11/30/02	PDN 0117
	Selected devices with fixed-pulse width programming option	10/31/03	04/30/04	PDN 0203
MAX 7000A	Selected devices in micro ball-grid array (BGA), FineLine BGA®, and TQFP packages	10/31/03	04/30/04	PDN 0203
MAX 7000B	Selected devices	10/31/03	04/30/04	PDN 0203
MAX 9000	EPM9560BC356-20	05/31/02	11/31/02	PDN 0117
	EPM9320RC208-15F	05/31/02	11/31/02	PDN 0117
FLEX 8000	Selected FLEX 8000 pin-grid array (PGA) packages	02/28/02	08/31/02	PDN 0107
	Selected devices	02/28/03	08/31/03	PDN 0107
	EPF8820ABC225-3	05/31/02	11/31/02	PDN 0117
FLEX 10K	Selected FLEX 10K PGA packages	02/28/02	08/31/02	PDN 0107
	Selected FLEX 10K PGA & BGA packages	02/28/03	08/31/03	PDN 0107
	EPF10K10LI84-4	05/31/02	11/31/02	PDN 0117
FLEX 10KA	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	EPF10K30AFI256-2	05/31/02	11/31/02	PDN 0117
FLEX 10KE	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	Selected devices	10/31/03	04/30/04	PDN 0204
APEX 20K	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	EP20K400BI652-2	05/31/02	11/31/02	PDN 0117
	Selected devices	10/31/03	04/30/04	PDN 0204
APEX 20KE	Selected devices	10/31/03	04/30/04	PDN 0204
ACEX 1K	Selected devices	10/31/03	04/30/04	PDN 0204

How to Contact Altera

It is now easier than ever to get information and services from Altera. The table below lists some of the ways you can reach Altera.

Information Type	U.S. & Canada	All Other Locations
Product Literature	**http://www.altera.com**	**http://www.altera.com**
Altera Literature Services *(1)*	**lit_req@altera.com**	**lit_req@altera.com**
News & Views Information	**http://www.altera.com/literature/nview.html** **n_v@altera.com**	**http://www.altera.com/literature/nview.html** **n_v@altera.com**
Non-Technical Customer Service	(800) 767-3753	(408) 544-7000
Technical Support	**https://www.altera.com/mysupport**	**https://www.altera.com/mysupport**
	(408) 544-6401	(408) 544-6401 *(2)*
FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	(408) 544-7104	(408) 544-7104 *(2)*
	http://www.altera.com	**http://www.altera.com**

Notes:

(1) The ***Quartus Installation and Licensing*** and ***MAX+PLUS II Getting Started*** manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.

(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for the latest listing.