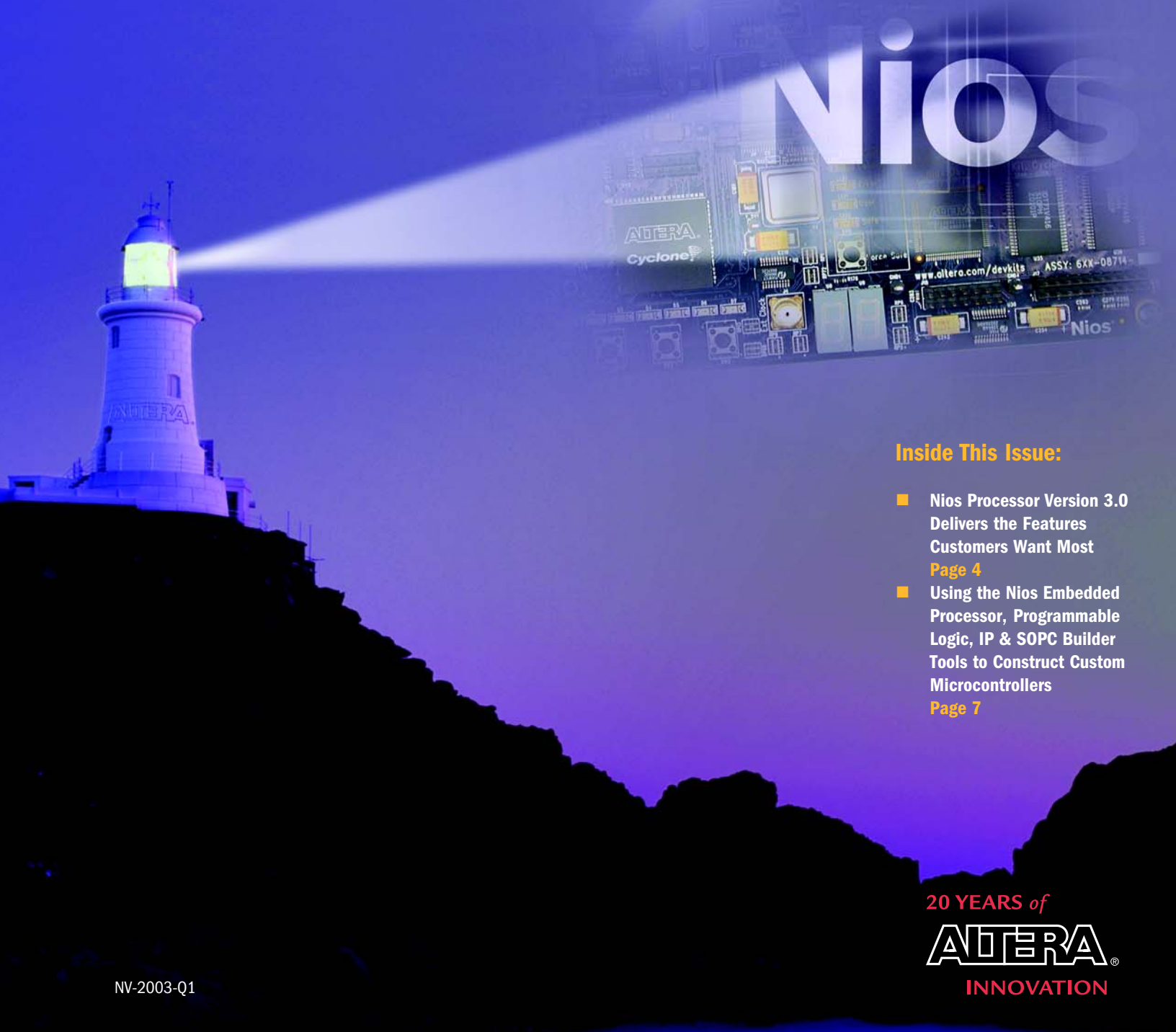
News & Views

First Quarter 2003

Newsletter for Altera Customers



Inside This Issue:

20 YEARS *of*
ALTERA®
INNOVATION

NV-2003-Q1

Executive *Viewpoint*

Not Your Father's PLDs

With 20 years of innovation behind us, we at Altera find ourselves at a very exciting point in time, in full view of new territories we are set to conquer. Today's FPGAs, far from their original versions, have reinvented themselves into powerful chips that are the heart of our customers' systems. Driven by our steadfast objective of giving our customers what they need, we have reached the crossroads where the benefits and cost structure of our FPGAs now meet the strict demands of customers who want to slash system costs, without sacrificing features or performance.

Consequently, a paradigm shift is occurring, not just for Altera, but for the semiconductor industry as a whole. System architects and designers are increasingly using programmable logic devices (PLDs) to replace other technologies. Our markets have expanded far beyond our original comfort zone—communications—as other markets clamor louder than ever for flexibility with no price penalty. Stratix™ devices have presented themselves as a viable alternative to digital signal processors (DSPs) for imaging applications, for example. Replacing microcontrollers with a Nios® processor embedded into a Cyclone™ device is creating quite a storm as a highly flexible, low-cost processor solution. (To date, Nios embedded processors have been sold to over 10,000 users and that community continues to grow at an exponential rate.) Stratix GX devices, with embedded serializer/deserializer (SERDES), are facing-off with ASSPs in the digital broadcast space, where applications such as high-definition TV require faster data rates and faster logic to process the burgeoning amount of information. HardCopy™ devices are now finding their way into storage systems, as the cost and performance equation is far too tempting to resist. These are not your father's PLDs.

So hang on to your hat, FPGAs are the next big thing. As George Gilder wrote in the December 2002 edition of his newsletter, "the innovative digital architecture of the coming era will be realized in dynamically programmable logic devices, which jettison the cumbersome complications of CPU architectures while reaping all their flexibility."

This issue of *News & Views*, the first to celebrate our twentieth anniversary, highlights customer applications of Altera FPGAs. Now sitting at the heart of systems that are part of our daily lives, FPGA products from Altera will continue to be a result of our on-going dialog with you, our customers.

Hugh Durdan,
Vice President, Computer, Consumer
& Industrial Business Group

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Nios Processor Version 3.0 Delivers the Features Customers Want Most

Since its introduction in the fall of 2000, Altera's Nios® embedded processor has become the soft core processor solution of choice for developers worldwide, with over 10,000 hardware kits shipped. The design community has chosen the Nios processor as their standard FPGA processor because it is easy to use and provides solid, reliable performance.

Created with the Nios Developer in Mind

The community of Nios developers has provided a wealth of feedback over the past year, helping our design team focus on the most useful features and enhancements. With the Nios processor version 3.0, Altera delivers the latest collection of product enhancements based on developer feedback. This feedback ensures the Nios processor will be even easier to use and addresses a wider range of embedded applications.

Altera's Stratix™ devices, with over 7 Mbits of on-chip memory, make it possible to run an entire real-time operating system (RTOS) and application code from internal memory.

Altera gathered feedback that clearly indicated that developers want even faster memory access to low-cost SDRAM memory, better software development and debugging tools, faster access to product updates, new intellectual property (IP) cores, enhanced timer functions, and faster floating-point mathematical operation. Altera listened, incorporating many of these features in version 3.0, and providing an Internet-based delivery method for rapid deployment of the remaining and future enhancements.

Choosing the Right Memory

Developers will always get the best system performance when executing code from FPGA internal memory blocks. Altera's Stratix devices, with over 7 Mbits of on-chip memory, make it possible to run an entire real-time operating system (RTOS) and application code from internal memory. While this strategy provides performance benefits, using internal memory for program and data storage is usually not economically practical. Typically, system designers choose external SDRAM for its low cost and high capacity advantages, even though they pay the price of additional latency that is inherent in SDRAM devices.

New Optimized SDRAM Controller

The new SDRAM controller included in the Nios processor version 3.0 is optimized to deliver efficient access to single data rate (SDR) SDRAM devices while maintaining a small FPGA resources footprint. Enhancements to the Avalon™ switch fabric that connects the Nios processor and associated peripherals provide pipelined data transfers, allowing posted read and posted write operations to minimize the latency effects. Coupled with the new, configurable on-chip cache, designers can achieve single-cycle access to SDRAM at speeds in excess of 100 MHz, dramatically boosting system performance.

New On-Chip Instruction & Data Cache

Version 3.0 of the Nios processor enables fast, sustained access to SDRAM with the new instruction and data caches included. Among available FPGA processor solutions, on-chip cache is an Altera® advantage provided by the availability of large dual-port RAM blocks on Stratix and Cyclone™ devices. Designers can configure the cache buffers from 1 to 16 KB in depth, allowing them to adjust the size to fit application requirements.

The direct-mapped instruction cache and write-through data cache provide an effective performance boost with minimal impact on logic element (LE) usage. The usefulness of the SDRAM controller and on-chip cache span a wide array of applications, from high-speed networking equipment to cost-sensitive consumer products. For example, an automotive electronics developer relies on the new SDRAM controller to store graphical data. A high-speed image processing engine within the FPGA fabric then processes this data. This example is typical of many applications in which designers use custom logic within the FPGA to provide high-speed data processing in hardware. The combination of the new SDRAM controller and on-chip cache delivers the data transfer speeds needed to achieve aggressive system performance goals.

Tools to Accelerate Software Development

The Nios development kits include a compiler and debugger based on the industry-standard GNUPro Toolkit. The GNU debugger (GDB) and the Insight graphical user interface (GUI) provide a powerful set of software debugging tools that rely on a piece of software (the debugging "stub") running on the target system. While this method is useful for debugging most applications, it is not an effective solution for debugging real-time code due to the intrusive nature of the debugging stub at run time.

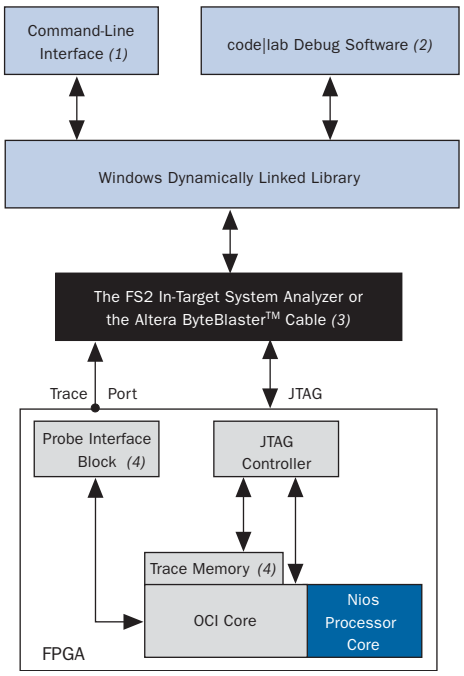
The Nios processor version 3.0 provides real-time code debugging capabilities with the new JTAG-based, on-chip instrumentation (OCI) module from FS2. This on-chip debugging tool eliminates the need to run debugging software on the target system. Instead, it monitors and controls processor activity directly in hardware based on commands received through the FPGA's JTAG port. The OCI core is supported by the Altera ByteBlasterMV™ download cable, providing the most essential debugging facilities, including software download, run control, memory examination, modification, and software breakpoints.

For more advanced debugging requirements such as hardware breakpoints and processor trace, two development kits are available separately from the Accelerated Technology, the embedded systems division of Mentor Graphics® Corporation and FS2. These products extend the baseline Nios processors debugging capabilities and add a robust software development environment. Figure 1 highlights the different levels of debugging support available in the Nios development kits.

The following products are available for purchase from Mentor Graphics and FS2:

- ISA-NIOS ($7,000): Includes Accelerated Technology's code|lab EDE debug software and FS2's debugging hardware. This hardware/software kit combines support for hardware breakpoints and on-chip program trace with a powerful development environment and source-level debugger.
- ISA-NIOS/T ($9,000): Same features as ISA-NIOS plus an external trace buffer in the FS2 debugger hardware for deep trace capture.

Figure 1. FS2's ISA & OCI Core



Notes to Figure 1:

(1) Command-line interface included in the Nios development kits.
(2) Evaluation version included in the Nios development kits.
(3) FS2 ISA sold separately. The ByteBlaster cable does not support trace or hardware breakpoints.
(4) Probe interface and on-chip trace memory are optional and are only supported with the FS2's ISA product for use with the Nios processor.

Fast Product Updates

Nios developers will always demand the latest peripherals, interfaces, custom instructions, hardware acceleration units, software, documentation, and reference designs. In the past, these new features were delivered a few times a year in Nios processor updates. The SOPC Builder development tool version 2.8, included with Nios processor version 3.0, now checks the Altera update server and notifies developers when new components, custom instructions, hardware accelerators, documentation, and software are available for download.

The Nios processor version 3.0 provides real-time code debugging capabilities with the new JTAG-based, on-chip instrumentation (OCI) module from FS2.

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Nios Processor Version 3.0 Delivers the Features Customers Want Most, continued from page 5

Several new components will be available in Q2 2003, including:

- *Streaming Parallel Output*: This configurable output port provides continuous, cycle-accurate output of digital data with minimal intervention required by the CPU. It operates in periodic, event-driven, and "time-scripted" modes.
- *Pulse Width Modulator*: This modulator can be connected directly to the Nios CPU, or to the output of the streaming parallel output peripheral to generate continuous, cycle-accurate pulse-width modulated signals.
- *One-Bit Digital-to-Analog Converter (DAC)*: This 1-bit DAC can be connected directly to the Nios CPU, or to the output of the streaming parallel output peripheral to generate continuous, cycle-accurate DAC signals.
- *Input Capture/Event Counter*: This configurable input port provides continuous, cycle-accurate time stamping of logic events with minimal CPU intervention.
- *Floating Point Custom Instruction*: This small footprint custom instruction provides floating point multiply, add, and subtract operations to accelerate math-intensive software routines.
- *Nucleus PLUS RTOS Software Component*: This software component automatically generates an ATI Nucleus PLUS RTOS kernel specific to a designer's system configuration during system generation.

One of the most compelling reasons why developers choose the Nios processor is avoiding product obsolescence.

New Stratix Development Kit

The Nios processor version 3.0 is available in the Nios Development Kit, Stratix Edition. Available from Altera and authorized distributors for $995, this kit comes with everything a designer needs to immediately begin development of Nios-based designs on the new Stratix EP1S10 development board, which is included. Support for the 10/100 Ethernet port on the EP1S10 board is included with the addition of Altera's network protocol software library providing support for ICMP, TCP, UDP, IP, ARP, and raw Ethernet protocols.

Also included in the Stratix development kit are evaluation versions of several tools, including:

- *code|lab Debug*: A 30-day evaluation version of the code|lab debug software from Accelerated Technology allows software engineers to debug their software, connecting to their target system via an Altera ByteBlaster download cable or optional FS2 In-System Analyzer.
- *Nucleus Plus LV*: An evaluation version of this royalty free, source-available RTOS lets software developers create embedded applications and run them for a limited time on the Stratix development board.
- *IAR visualSTATE*: An evaluation version of this powerful software design tool allows Nios developers to automatically generate C/C++ code from state machine models created within a graphical user interface.

Future-Proof Your Next Design with the Nios Processor

One of the most compelling reasons why developers choose the Nios processor is avoiding product obsolescence. In the past, many designers ran into problems when their processor suddenly became obsolete. Not only did this require a hardware redesign, but it also put their software investment at risk, potentially requiring a complete re-write.

The Nios processor and associated peripherals come with a royalty-free, perpetual license, giving developers the right to create and deploy Nios designs indefinitely in any Altera device. Because the Nios processor is a soft core processor, it can be compiled to target a wide range of Altera FPGAs, from the high-performance Stratix devices, to the low-cost Cyclone devices.

More to Come

As the Nios processor continues to grow in popularity, Altera continues to create tools, IP, and software to maintain the Nios processor's leadership in FPGA-based processor technology. The Nios processor version 3.0 is here today, delivering the most desired enhancements to the Nios design community.

Using the Nios Embedded Processor, Programmable Logic, IP & SOPC Builder Tools to Construct Custom Microcontrollers

Microcontrollers are the original system-on-chip (SOC) devices. In the last few years, programmable logic manufacturers have proffered the term system-on-a-programmable-chip (SOPC), which captures the idea of using programmable logic to create system-level custom hardware including microcontrollers. The elements required for this include: full-featured, 32-bit RISC microprocessors, available peripherals and options for building custom peripherals, intellectual property (IP), and complete development tools. These elements are now available, and in combination with low-cost Cyclone™ FPGAs, designers have attractive alternatives to off-the-shelf microcontrollers.

With microprocessor systems in FPGAs, the designer can code specific software blocks as hardware that can be called as "single custom instructions" from the microprocessor. From the software engineer's perspective, this is simply a function call in C or assembly language, but rather than a set of instructions being called, hardware is used to execute the algorithm. Similarly, a designer can change the system architecture to match the problem, including adding multiple arbitrated slave-peripherals on a multi-master bus, custom peripherals, or direct memory access (DMA) controllers. This article gives a detailed example and performance numbers of an MP3 player optimized using custom instructions.

Detailed Example: MP3 Player

Custom instructions can increase system performance by adding custom logic to the arithmetic logic unit (ALU) of the Nios® embedded processor. An MP3 player design was created to show the potential performance enhancements of using a custom instruction in a real-world, compute-intensive application. By adding two custom instructions, this design was able to increase system performance by approximately three times. Figure 1 shows a block diagram of the MP3 system design.

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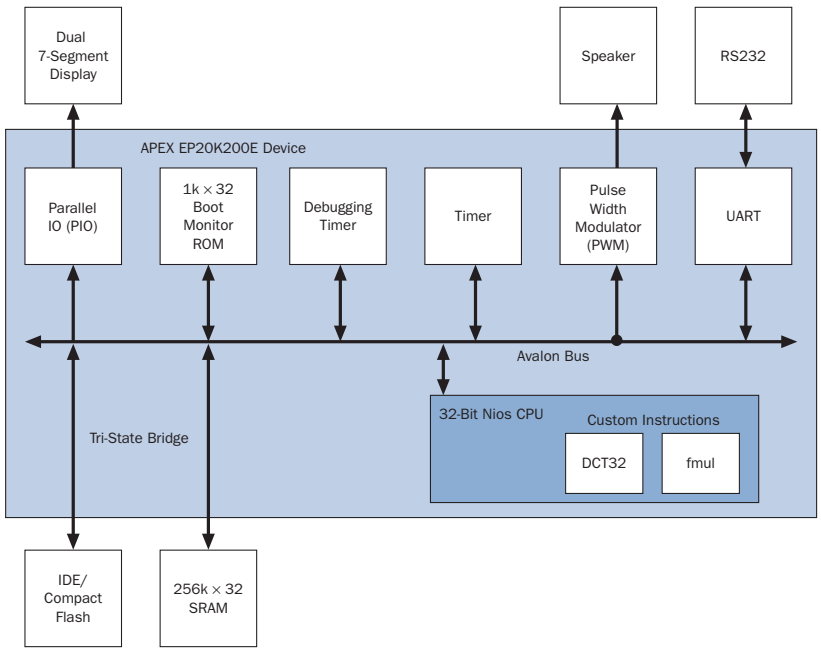
Figure 1. MP3 System Design Diagram



Using the Nios Embedded Processor, Programmable Logic, IP & SOPC Builder Tools to Construct Custom Microcontrollers, continued from page 7

MP3 Decoder

In many MP3 players, the processor is used for control functions and moving data. A specialized MP3 decoder ASIC is used to perform the compute-intensive decode and send data to the sound device[1]. In Altera's design example, the Nios processor handles control signals, transferring data, and MP3 decoding.

In general, Altera's MP3 decoder:

- Reads the MP3 data from CompactFlash controller through an IDE interface
- Buffers the MP3 data in SRAM
- Decodes the MP3 data
- Synthesizes the MP3 subbands into pulse code modulation (PCM) data
- Sends the PCM data to the PWM

The player uses MPEG Audio Decoder (MAD) for MP3 decoding because of the following special features:

- 100% fixed-point (integer) computation
- Available as source-code on the web
- Distributed under the terms of the GNU General Public License (GPL)

References to functions found in the source-code will be used throughout this article.

Custom Instructions

The majority of the execution time for MP3 decoding takes place in the synthesis of the subbands. Therefore, the Altera MP3 design focuses on a function called `mad_synth_frame`, which contains two functions that could be optimized using the custom instructions `f_mul` and `DCT32`.

f_mul

`f_mul` and `mad_f_mul` are macros used by MAD to emulate floating-point multiplication using integer multiplication. These macros are defined as:

```
#define mad_f_mul(x, y)
      ((((x) + 0x00002000L)>> 14) ×
      (((y) + 0x00002000L)>> 14))
#define f_mul(x,y)(((x)| 0x0001FFFFL) ×
      ((y)| 0x0001FFFFL))
```

These functions are a set of shifts, adds, multiplies, and logical `OR` operations, which are easy to implement in hardware. The Altera MP3 design uses a hardware custom instruction called `f_mul` which performs the software macro previously mentioned. By using the prefix option, this design was able to incorporate both macros into a single custom instruction. Below is the code used to define `f_mul` and `mad_f_mul` using Altera's custom instruction:

```
#define f_mul(x,y) nm_fmul((x),(y))
#define mad_f_mul(x,y) nm_fmul_pfx
      (1,(x),(y))
```

DCT32

`DCT32` performs the discrete cosine transform (DCT) in the MP3 decode. The MAD software uses an optimized DCT to increase performance. From a software perspective, this optimized algorithm provides a significant performance improvement over the general DCT, using only 80 multiplies, while the standard DCT equation requires 1,024 multiplies.

The hardware used for the `DCT32` custom instruction was provided by Celoxica[2], a provider of reconfigurable computing solutions with their Handel-C-based design tools. Altera's `DCT32` custom instruction was designed with the following features:

- Stores 32 inputs and 32 outputs
- Works independently of the CPU during DCT calculation
- Uses the prefix instruction to receive commands:
  - Load/unload
  - Start DCT calculation
  - Poll if complete

Because the custom instruction can be polled, other code can run in parallel until the DCT output is needed. At that time, the custom instruction is polled to see if the calculation is complete. If complete, the Nios processor unloads the output data while loading the next group of inputs. Figure 2 shows a flow diagram illustrating how a designer can use the DCT32 custom instruction.

MP3 Example: Performance Versus Size[3]

Altera measured the number of cycles needed to complete a single mad_synth_frame function using a hardware multiply instruction as well as the custom instructions f_mul and DCT32. Performance improvement comes with a cost; custom instructions generally require additional hardware resources (e.g., logic elements (LEs) and memory). Table 1 shows the hardware requirements and results for the three example designs using the mad_synth_frame function.

Table 1. Number of Cycles to Compute a MP3 Frame

Hardware Used	Number of Cycles	Logic Elements	Memory (Bits)
Hardware multiply only	1,279,000	3,542	26,624
f_mul	293,000	3,642	26,624
f_mul and DCT32 parallel	231,600	4,331	30,528

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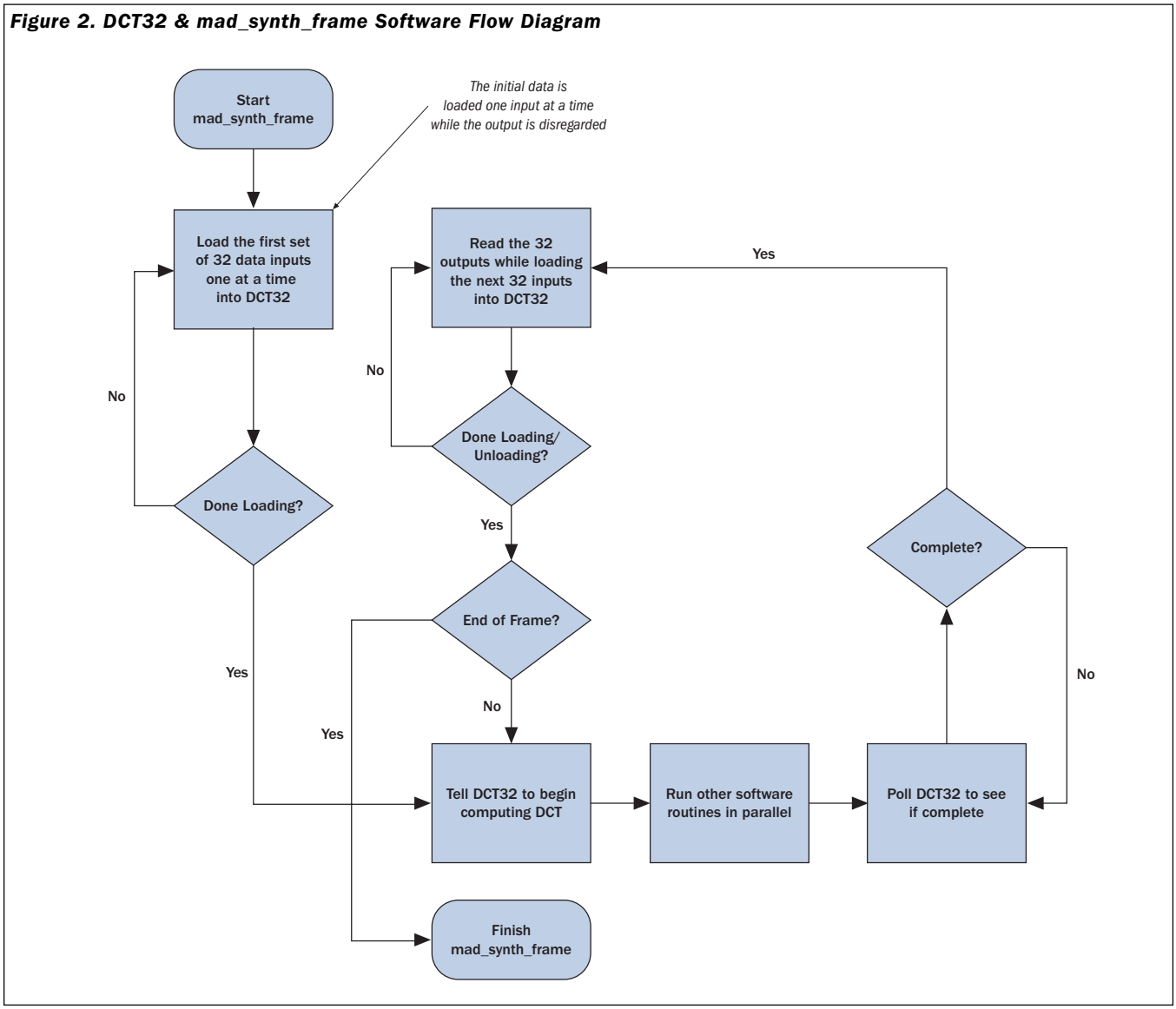
Figure 2. DCT32 & mad_synth_frame Software Flow Diagram



Using the Nios Embedded Processor, Programmable Logic, IP & SOPC Builder Tools to Construct Custom Microcontrollers, continued from page 9

`f_mul` was the most efficient custom instruction, reducing the number of cycles needed by 77% with an increase in system size of 3%. This small increase was due to removing the dedicated hardware multiplier in favor of the `f_mul` custom instruction.

The `DCT32` instruction runs in parallel mode and reduces the number of cycles needed by 21% compared to `f_mul`, using 18.9% of LE resources from the `f_mul` design.

For a reduction of over 80% in the number of cycles needed to perform `mad_synth_frame`, the system size only increased by 22.3%. This example executes on a Nios development board at 33 MHz, and all performance gains are achieved without increasing clock frequency. If higher performance is required, the designer still has other options available, such as increasing clock frequency, using faster memory, or adding instruction or data cache.

Conclusion

The use of FPGA microcontrollers extends the set of tools that a designer has available to improve system performance. As with all tools, it is the skilled application of these tools that determine the speed with which performance targets can be met. The beauty of using FPGAs for microcontrollers is experimenting with new designs in an iterative approach, further blurring the lines between software and hardware development.

References

1 *The Beginner's Guide to Making a Hardware MP3 Player Version 2.0*
2 *Celoxica, Ltd., 20 Park Gate, Milton Park, Abingdon Oxfordshire, OX14 4SH United Kingdom*
3 *AN 188: Custom Instructions for the Nios Embedded Processor*

Nios in the News

Altera's Trojan Horse
Exerpted from Electronic News, 2/17/03

> The Nios® part has excelled beyond the company's expectations, with more than 10,000 licenses sold to date. Cary Snyder, senior analyst with Forward Concepts, estimates the number of embedded applications using the soft-core processor is much greater. "I don't think that Altera even knows how much people are using it. In other words, how many times in a given chip it might be used. In some cases it is simple enough to use it in multiple substantiations in a chip. If you want flexibility in your design—which is why people would go to FPGAs in general—they can get it by popping in a Nios core."

Test Drive the Nios Processor for Free!

Altera's low cost-solution is now available on CD-ROM. Take the Nios processor out for a spin at absolutely no cost to you and see what over 10,000 developers are raving about. The Low-Cost Solution CD contains the Nios embedded processor (evaluation version), a complete Nios development kit, Quartus® II Web Edition, SOPC Builder, and accompanying documentation. Order Altera's Low-Cost Solution CD now at **www.altera.com/niostestdrive**.

Stratix Devices Enable EoS for MAN Applications (with up to a 10-Gbps Data Rate)

by Bamdad Afra
Senior Engineer/GEOS Chief Architect
Nuvation Engineering

There is an increasing demand for Ethernet traffic over metropolitan area networks (MANs). Since their infrastructures are not geared towards packet-switched traffic (e.g., Ethernet), carriers are now struggling to provide this service capability. In recent years, these carriers have invested a large amount of capital in creating the time-domain multiplexing (TDM) infrastructure (e.g., circuit-switched oriented SONET) to provide voice and private-line connections.

The most cost-effective solution for providing Ethernet services is to transport it over the existing infrastructure to make use of the capital already invested—transport Ethernet traffic (packet-switched) over SONET (circuit-switched) equipment.

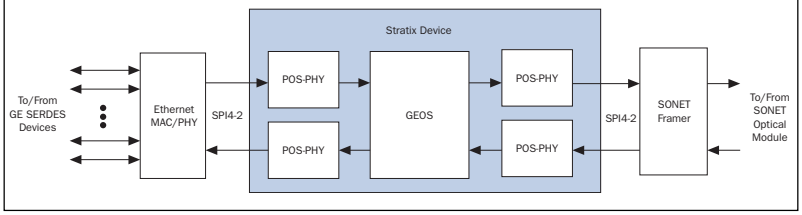
For instance, consider a special case of Ethernet-over-SONET (EoS) equipment. In this case, the EoS equipment is required to transport up to 10 ports of Gigabit Ethernet traffic by connecting to a SONET ring. An optimal solution is to aggregate the traffic from all gigabit Ethernet ports into a single 10-gigabit per second (Gbps) SONET pipe (e.g., OC-192). The traffic aggregation requires all EoS equipment to adopt a standard protocol, such as generic framing procedure (GFP), to de-multiplex the traffic at the destination.

To design such equipment, one would have to choose a number of system components. The major system components are listed below:

- Serializer/deserializer (SERDES) devices for gigabit Ethernet ports
- MAC/PHY devices for handling Ethernet traffic
- A device for aggregation and GFP protocol implementation
- SONET framer
- SONET optical module

SERDES, MAC/PHY, SONET framer, and SONET optical modules are available from a number of well-known companies such as Intel and PMC Sierra. Designers can implement a GFP protocol in an FPGA (a GFP protocol is required to interface the MAC and SONET framer). Altera® Stratix™ FPGAs handle traffic aggregation and GFP protocol implementation, as shown in Figure 1.

Figure 1. Stratix Implementation Block Diagram



The Stratix device interfaces to the MAC/PHY and SONET framer devices using the SPI4.2 interface specification from the Optical Internetworking Forum (OIF). This interface uses a 16-bit double data rate (DDR) with a clock rate of up to 400 MHz, making it capable of handling over 10-Gbps data rates.

The internal components of the Stratix device are readily accessible through easy-to-use Altera megafunctions. You can implement Stratix devices using two types of intellectual property (IP) cores: POS-PHY Level 4 and GEOS. The POS-PHY Level 4 IP core facilitates interfacing to the SPI4.2 bus for application-specific implementations in the Stratix device. The GEOS IP core implements the GFP protocol in addition to traffic aggregation. Additionally, GEOS implements features such as full-duplex pause flow control and Ethernet jumbo frame transport over SONET.

The POS-PHY Level 4 IP core is available through Altera, and the GEOS IP core is available through Nuvation.

For more information on Nuvation, go to **www.nuvation.com**.

Company:
Nuvation Engineering

Industry:
Electronic Design Services

End Product:
FPGA Design Firmware

Altera Product:
Stratix Devices

The Dini Group Announces Stratix FPGA-Based Logic Emulation Product Ideal for Memory-Intensive or DSP-Focused Applications

by Mike Dini
President
The Dini Group

Company:
The Dini Group

Industry:
Consulting Design Services

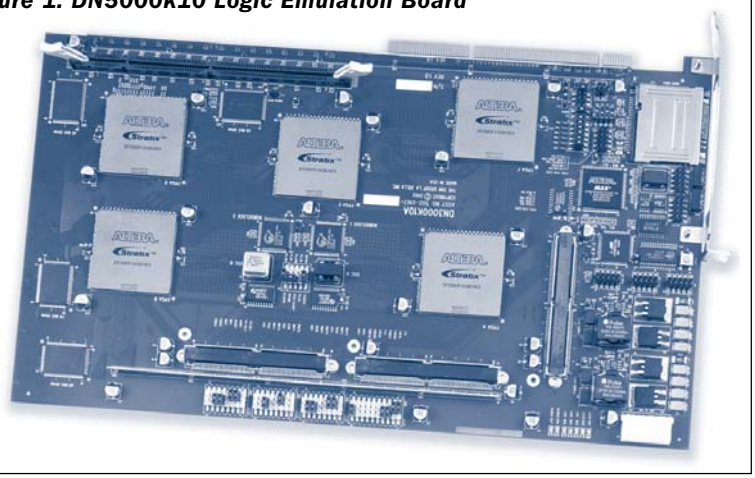
End Product:
Logic Emulation
Algorithm Acceleration
Reconfigurable Computing

Altera Products:
Stratix Devices
APEX II Devices

With ASIC mask costs nearing and sometimes exceeding $1 million, designers need to pay more attention than ever to the verification of logic design. Prototyping the logic in an FPGA before the masks are cut is a good way to assure first-time success. Prototyping a design can also help to catch oversights and errors in a simulation test fixture. Additionally, since hardware prototypes can be clocked at frequencies in the MHz range, billions (even trillions) of test vectors are possible. With these issues in mind, The Dini Group has developed a line of off-the-shelf products based on Stratix™ FPGAs that can be used for logic emulation, algorithm acceleration, and reconfigurable computing.

The DN5000k10 emulation board can be equipped with two to five Stratix EP1S80 FPGAs (see Figure 1). The block diagram is shown in Figure 2. The EP1S80 device is one of the largest FPGAs available today, providing 79,040 flipflops, 7.4 Mbits of embedded RAM, and 22 digital signal processing (DSP) blocks. The embedded Stratix DSP blocks allow designers to implement multiplier-based logic such as finite impulse response (FIR) filters, modulators, correlators, and coder/encoders.

Figure 1. DN5000k10 Logic Emulation Board



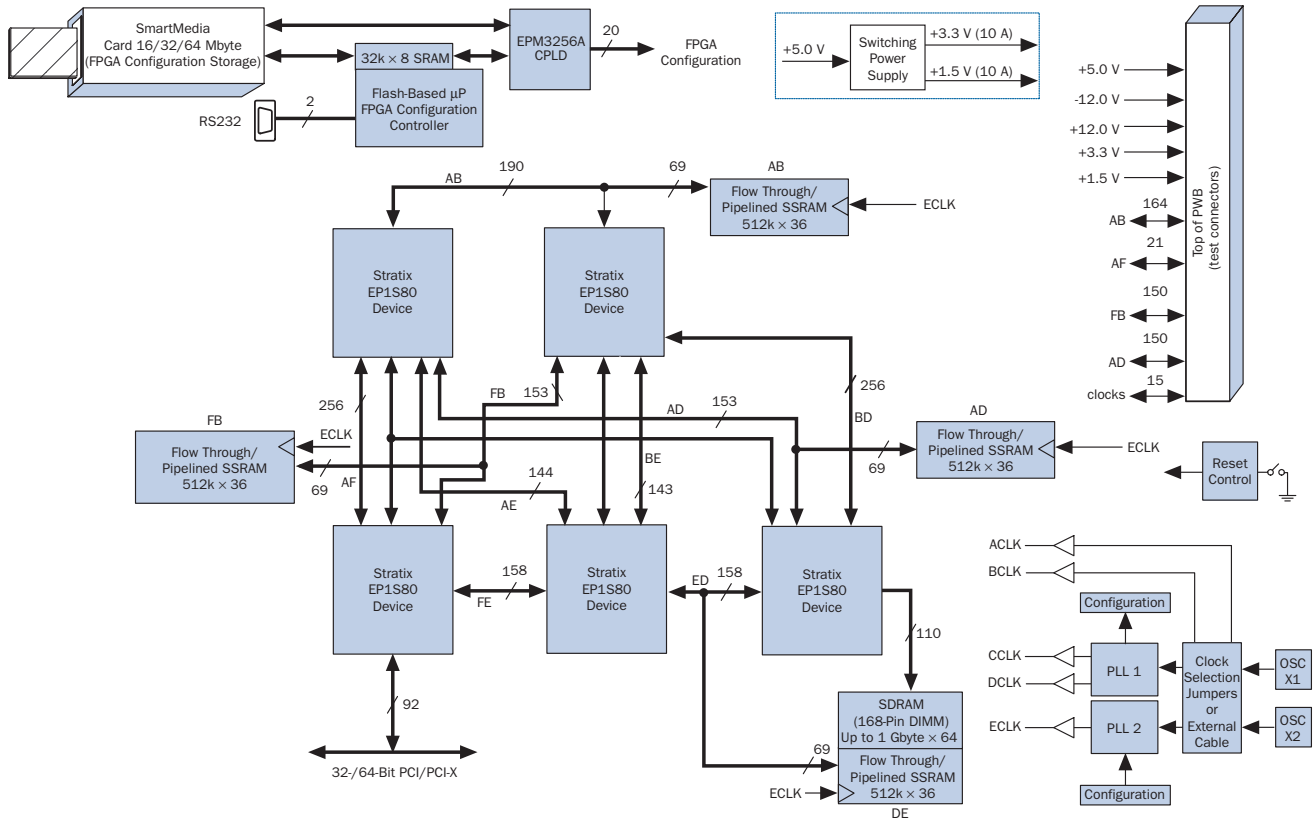
Four external 512k × 36 pipelined/flowthrough/zero bus turnaround (ZBT) SSRAM devices and a 128 Mbytes × 72 SDRAM device are available to bolster the large amount of embedded memory already available in each Stratix device. The board uses high I/O count, 1,508-pin FineLine BGA® packages to support a rich, fixed interconnect scheme between the FPGAs. A flexible clocking scheme, based on two external phase-locked loop (PLL) devices, works in concert with the 12 PLLs available in each Stratix FPGA to enable a wide variety of board clocking options.

The DN5000k10 board can be hosted in a 32-/64-bit PCI/PCI-X slot, or can be used as a stand-alone board. The board includes a 32-bit target PCI interface (in Verilog HDL and VHDL). It also includes drivers for a number of operating systems at no additional cost, as well as source code for the PCI target and the drivers.

Because it is necessary to interface logic emulation boards to custom circuitry, the DN5000k10 board has three high-speed 200-pin connectors on the top of the circuit board. A total of 488 signals are available to handle the complex interfaces to custom circuitry.

FPGA configuration is performed using a SmartMedia card. The user copies configuration files for the FPGAs to the SmartMedia card via a FlashPath floppy adapter, and a microprocessor on the DN5000k10 board controls the configuration process. It configures in parallel at 48 MHz. The microprocessor performs sanity checks on the configuration files in an attempt to take as much mystery as possible out of an occasionally difficult process. An RS232 port is available to determine the status of the configuration process, and to manually select the configuration files. A single SmartMedia card can store several configuration files. It takes less than five seconds to configure a fully equipped DN5000k10 board with five EP1S80 devices.

Figure 2. DN5000k10 Block Diagram



The DN5000k10 board is built to order, and can typically be assembled, tested, and shipped in about one week. A version of the DN5000k10 board with a single Stratix EP1S80 device is also available. The Dini Group also has a series of emulation products based on Altera's APEX™ II devices.

About The Dini Group

The Dini Group is headquartered in La Jolla, California. In addition to its logic emulation products, The Dini Group is a hardware and software consulting firm specializing in high-performance digital circuit design using ASICs and FPGAs. More information is available at **www.dinigroup.com**.

Mike Dini has been in the industry for 20 years and is a regular contributor to various conferences on the subject of FPGAs and their applications. He has been using FPGAs since 1984 and has done hundreds of designs.

Stratix FPGAs Enable Real-Time Microprocessor Development

by Nick Klein
Logic Product Development

With the availability of contract silicon manufacturing from companies such as UMC, TSMC, and a wide variety of licensed peripheral intellectual property (IP), microprocessor manufacturers are now offering their cores as part of a customizable system-on-a-chip (SOC) solution.

Company:
Logic Product Development

Industry:
Embedded Systems

End Product:
SuperH (SH4-202) Processor Development Platform

Altera Products:
Stratix Devices
Configuration Devices
MAX 3000A Devices

One of the issues facing SOC developers is the ability to prototype their SOC solution and provide a software development platform prior to silicon availability. Logic Product Development works with SuperH, Inc. (a leading supplier of multimedia RISC CPU cores) to produce a modular development and prototyping platform. The solution is a stackable three-board configuration, including a CPU board, a system board, and an FPGA board. Both the CPU board and FPGA board are equipped with Stratix™ FPGAs.

System Board

The system board is located at the bottom of the three-board configuration. It has an array of peripherals and interfaces that would be found on a typical PC motherboard:

- 3.3-V peripheral component interconnect (PCI) slot
- Three 5.0-V PCI slots
- PC card connection
- Super I/O controller that provides 1× parallel, 2× PS2, 2× serial, and 2× IDE ports
- On-board video controller
- Ethernet pass-through from CPU board
- Micro ATX form factor that uses standard ATX power supply
- Two universal serial bus (USB) 1.1 ports (host side)

Logic Product Development used a MAX® 3000A (EPM3256A) CPLD to handle PCI arbitration and to manage access to the SRAM buffer that is shared between the microprocessor and the PCI bridge. Another MAX 3000A CPLD provides I^2S to microprocessor local bus conversion (operating as a transceiver), allowing a connection to a low-cost I^2S stereo coder/decoder.

CPU Board

The first CPU board developed contains the SH4-202 evaluation device from SuperH, a serial port, Ethernet, SDRAM, flash memory, a Stratix EP1S10 FPGA, and an EPC4 configuration device (used to configure the EP1S10 device). These peripherals enable the board to be operated as a stand-alone evaluation board. A designer can also connect the CPU board to the system board allowing additional peripheral availability. The SH4-202 is a 32-bit RISC CPU core with a 128b-vector floating point unit, and 16K I and 32K D caches running at speeds of up to 266 MHz. This core is implemented in a device produced through UMC's 0.13-µm CMOS technology. This device includes the SuperHyway Bus on-chip interconnect that provides a high-bandwidth, low-latency bus to connect the CPU core to the peripherals.

The Stratix EP1S10 FPGA on the CPU board ties the entire system together. It handles multiple selectable address maps for the entire system, provides a programmable interrupt controller for 32 interrupt sources, and an interface for programming the FPGA board from the SH4-202, and connects to the SuperHyway via an off-chip port and FlashEMI SH4-202 interface. "This allows complete flexibility for interfacing the rest of the system with the SuperH evaluation device," says Jason Sheard, Program Manager at Logic Product Development.

FPGA Board

The FPGA board is designed for customer IP development of SOC custom peripherals. A designer can stack up to eight FPGA boards onto the CPU board for additional logic and I/O resources. This number is limited only by the power supply and the connector's current capability. These boards connect to the CPU board for power and access to the SuperHyway Bus off-chip SH4-202 interface.

The FPGA board contains a Stratix EP1S40 FPGA, the core and I/O power supplies, an EPC16 configuration device, and a number of I/O connectors. The I/O connectors on the board support both differential and single-ended signals to accommodate a wide variety of I/O standards at selectable voltage levels. The Stratix FPGA can be programmed using the EPC16 configuration device, Joint Test Action Group (JTAG), or passive serial from the CPU board. A designer can select bank I/O voltage and programming options by using jumpers on each FPGA board.

Stratix Devices

EP1S10 and EP1S40 devices provide the large number of logic elements (LEs), I/O pins, speed, and advanced logic capabilities that are required for this design. "SuperH and SuperH core users need the IP Emulation FPGAs to run complex logic at speeds of up to 150 MHz and Stratix devices offer the best solution available today for meeting this need. As an Altera® Certified Design Center (CDC), Logic has the tools and experience to implement this design," says Matt Tilstra, FPGA Design Engineer at Logic Product Development.

While the FPGA board currently uses a Stratix EP1S40 device, the board is compatible with any member of the Stratix family in a 1,020-pin ball-grid array (BGA) package. This range includes Stratix EP1S25 to EP1S60 devices, providing an additional level of flexibility in offering different cost and FPGA resource options.

About Logic Product Development

Logic Product Development is the largest fully integrated product development consulting firm in the American midwest, and has helped transform product concepts to market success for over 40 years. By balancing goals and end-user requirements, Logic's comprehensive array of capabilities propels the development process, allowing a product to move rapidly from concept to full production. Logic's integrated approach enables multiple disciplines to work concurrently on the development of a product, greatly reducing development time and accelerating market launch.

For more information, visit **www.logicpd.com** or call (612) 672-9495.

While the FPGA board currently uses a Stratix EP1S40 device, the board is compatible with any member of the Stratix family in a 1,020-pin ball-grid array (BGA) package.

Plexus Develops a DSP Development & Evaluation Platform Using Altera Excalibur Devices

by Michael Tendick & Tim Murphy
Plexus

Company:
Plexus

Industry:
Electronic Manufacturing Services

End Product:
Product Realization Services

Altera Product:
Excalibur Devices

In the highly competitive digital signal processing (DSP) market, time to market is critical. Plexus was given 6 months to develop a platform that was designed for end customers to verify their DSP applications. Given the wide variety of DSP interfaces, the system must be flexible enough to handle different communications protocols and interfaces such as UTOPIA, HDLC, and peripheral component interconnect (PCI). With all these system requirements, the selection of a system architecture would be the key to the project's success. The risk of "show-stopping" problems had to be minimized while the speed of implementation must be maximized. After looking at potential architectures for their development and operational platform, Plexus chose Altera® Excalibur™ devices.

The combination of programmable logic, an ARM® processor, memory controllers, and on-board SRAM resulted in reduced printed circuit board (PCB) space and development time. The dual-port RAM was an ideal interface between the processor and programmable logic sections. The tools accelerated development by allowing parallel hardware and software design.

Custom Kernel Design

The Excalibur ARM922™ processor was used to adjust the platform's operating conditions and provide an interface between a PC and the cores embedded in the Excalibur device's programmable logic array. Plexus created a custom kernel to run on the ARM processor which was set up in a tiered command structure, allowing the designer to add new commands, or groups of commands, at any time without affecting the existing commands.

The first group of commands adjusts operating conditions, including several on-board clock speeds and voltages, and monitors on-board temperatures. The second group of commands provide an abstract interface to the FPGA communication cores. These commands allow load transmit buffers to be loaded with data, to transmit that data over any desired interface, to receive data over any interface, to place that data in receive buffers, and to output the data to a PC. The PC interface to the development platform is a standard RS232 interface. This arrangement allows any standard PC to interface with the development platform using standard software such as HyperTerminal. With this well-defined command structure, Plexus created a graphical user interface (GUI) that could be installed on a PC. The GUI allows users unfamiliar with the command structure to control the platform.

The development platform contains flash memory dedicated to holding scripts and DSP bootcode, allowing the DSP technology to be verified without user intervention. This automated testing is made possible by kernel commands that compare transmit and receive signals.

Communication Subsystem Design

The rest of the Excalibur system consists of several communication blocks used to test the various communications interfaces. These interface blocks include UTOPIA Level 2, multi-channel buffered serial port (McBSP), universal host port interface (UHPI), HDLC, and PCI. The UTOPIA, HDLC, and PCI blocks are third-party purchased cores. Plexus developed the UHPI and McBSP cores. The ARM processor controls the data flowing through the cores through both the AMBA™ bus and the dual-port RAM. AMBA, the ARM system-level processor bus, allows peripheral cores designed for the AMBA bus to be quickly and easily connected to the system. The dual-port RAM acts as a mailbox between the ARM core and the FPGA's logic. The ARM processor has access to one side of the dual-port RAM and the FPGA design has access to the other side.

Unfortunately, the cores did not have AMBA interfaces, so the main task for Plexus was to customize the cores' back-end interface to allow them to talk to the ARM processor. The register block was designed to be AMBA-compliant, which allowed access to each core's configuration registers. The dual-port RAM was used to pass data between the ARM processor and the cores. The ARM processor uses the register block to set up accesses and the dual-port RAM to send and receive data. Direct memory access (DMA) engines were designed on the FPGA side to control the flow of data without additional ARM overhead.

At one time, there were five digital design engineers working on the design in two locations. To enable the design engineers to work as autonomously as possible, the Quartus® II software's LogicLock™ feature was used. LogicLock regions allow multiple blocks to be independently implemented and then merged.

Simulation

Multiple engineers on the team were responsible for block-level simulations, while system-level simulations were performed by a dedicated verification engineer. The verification engineer caught specification misinterpretations made by the design engineers, whereas the design engineers tested implementation-specific corner cases not apparent by reading the specification. Using the Excalibur device required cooperation between the HDL and software design teams throughout the project. This tight working relationship was beneficial as it allowed for cross-functional design. The full ARM model was used for system-level simulations. Kernel software was written, compiled, and used in simulation months before the hardware was complete. This method worked well in that actual application code could be run and debugged before hardware was available. With simulation proving basic functionality of the kernel and the HDL, the entire engineering team was able to focus on hardware, saving valuable time in the six-month development schedule.

To enable the design engineers to work as autonomously as possible, the Quartus II software's LogicLock feature was used.

Conclusion

The development and evaluation platform allows designers to see "signs of life" from the silicon in only five minutes. Within a month, the customer began requesting additional prototypes to allow their customers to accelerate the time to market of their silicon-based applications. This successful project helped to create a close partnership between Plexus and their customer. Additional IP cores and kernel functionality are being added continuously to allow more rigorous and thorough testing of the new silicon.

Cyclone

Cyclone: The Lowest-Cost FGPAs Ever are Shipping in Volume Today

Altera is now shipping production devices of the first two family members from its low-cost Cyclone™ FPGA family. Based on an industry-leading 1.5-V, 0.13-µm, all-layer-copper process, EP1C20 FPGAs in the 324- and 400-pin FineLine BGA® packages and EP1C6 FPGAs in the 144-pin thin quad flat pack (TQFP), 240-pin plastic quad flat pack (PQFP), and 256-pin FineLine BGA packages are now available.

At less than $1.50 per 1,000 logic elements (LEs) for volume applications, engineers can begin designing for Cyclone devices using the Altera® Quartus® II design software, the Nios® embedded processor, and Altera's intellectual property (IP) cores.

Only 15 months from conception to shipment, Altera developed the Cyclone FPGA family faster than any other device family in company history. Altera rolled out Cyclone devices in record time, having shipped multiple device densities since December 2002. For a true low-cost solution for high-volume applications, designers can have immediate access to Cyclone devices through Altera's distributors. The Quartus II design software supports all Cyclone FPGAs.

Table 1 shows Cyclone device availability.

Table 1. Cyclone Device Availability

Device	Production Availability
EP1C3	April 2003
EP1C4	September 2003
EP1C6	Now
EP1C12	March 2003
EP1C20	Now

Cyclone FPGA Features

Cyclone FPGAs provide:

- Up to 20,060 LEs
- Up to 294,912 bits of embedded RAM
- Dedicated external memory interface circuitry for integration with double data rate (DDR) SDRAM and FCRAM devices as well as single data rate (SDR) SDRAM memory devices
- Up to two phase-locked loops (PLLs) for on- and off-chip system timing management
- LVDS support of up to 129 channels capable of 311 megabits per second (Mbps)
- Nios embedded processor support
- Free software support with the Quartus II Web Edition software

What Customers are Saying about Cyclone FPGAs

"Our company had not used programmable logic before, but the Cyclone FPGA family convinced us that we could achieve a high degree of design flexibility at the lowest possible cost. Even though it is a new product family, Altera's successful track record of shipping Stratix™ devices demonstrated to us that they could deliver Cyclone devices in a short amount of time, and the fact that we now have them in-hand proves that we made the right decision."

Gary Pace
Principal Engineer
Oilfield Electric Marine

Stratix

All Stratix Devices Now Shipping in Production

All Stratix devices are now shipping in production volume. EP1S10, EP1S20, EP1S25, EP1S30, EP1S40, EP1S60, and EP1S80 production devices are now shipping. See Table 2.

Table 2. Stratix Device Availability *Note (1)*

Device	Availability
EP1S10	Now
EP1S20	Now
EP1S25	Now
EP1S30	Now
EP1S40	Now
EP1S60	Now
EP1S80	Now

Note to Table 2:

(1) Since production devices are available, engineering samples will no longer be offered for these devices.

Stratix Devices Offered in Two New Packages

Stratix devices are now available in two new packages. The EP1S40 device will be offered in the 780-pin Fineline BGA package, and the EP1S80 device will be available in the 1,020-pin Fineline BGA package. The 780-pin FineLine BGA package supports vertical migration between the EP1S10 device up to and including the EP1S40 device. The 1,020-pin FineLine BGA package also supports vertical migration between the EP1S30 device up to and including the EP1S80 device.

The EP1S40 device in the 780-pin FineLine BGA package and the EP1S80 device in the 1,020-pin FineLine BGA package will be available in Q2 2003. These packages are supported in the Quartus II software version 2.2 and higher.

Stratix GX

Stratix GX: The High-Speed System Solution

Altera is now shipping Stratix GX EP1SGX25C, EP1SGX25D, and EP1SGX25F devices; these devices were released in both a 672-pin and 1,020-pin ball-grid array (BGA) package. The first EP1SGX25 devices have been released to validation partners, but will not generally be available to customers until June 2003. This schedule allows time for the completion of characterization, and will ensure that a full design pack is available. See Table 3 for Stratix GX device availability.

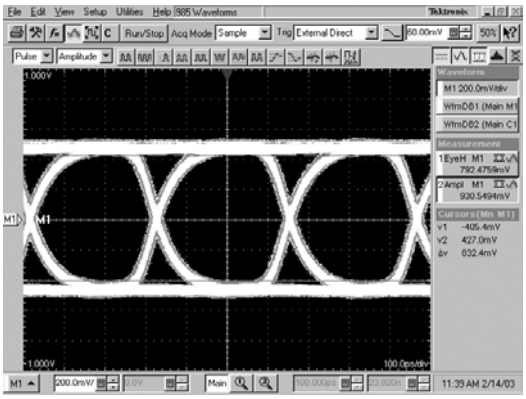
Table 3. Stratix GX Device Availability

Device	General ES Availability
EP1SGX10C	Q3 2003
EP1SGX10D	Q3 2003
EP1SGX25C	Q2 2003
EP1SGX25D	Q2 2003
EP1SGX25F	Q2 2003
EP1SGX40D	Q3 2003
EP1SGX40G	Q3 2003

Characterization

The characterization process is proceeding to schedule. Initial results have been extremely encouraging, with better than expected performance. Figure 1 shows an eye diagram measurement taken from the transmitter Stratix GX high-speed transceiver.

Figure 1. Transceiver Eye Diagram (3.125 Gbps)



Stratix GX has been characterized to operate successfully at 3.125 gigabits per second (Gbps) across 40 inches of FR-4 fabric. Characterization has also been ongoing on the source-synchronous dynamic phase alignment (DPA) circuitry. Source-synchronous operation has been shown to be successful above 1 Gbps.

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Excalibur

Implementing SA-1110-Like Designs in Excalibur Devices

Many embedded processor solutions are available on the market today. In many cases, they target application-specific or application-oriented devices. Although they have generic appeal, peripheral availability may not be optimal for particular applications.

One example of such a device is the Intel® SA-1110 StrongARM® processor. Based on a core compliant with the ARM V4 instruction set, this device targets higher-end personal digital assistant (PDA) and consumer device applications. If a designer is using an Intel SA-1110 device in an application space other than the consumer market, it may not be the best solution. The design may not require all three on-board UARTs, the LCD controller, or the infrared data association (IrDA) peripheral, or you might want a similar peripheral, or another complete functional block in its place.

Altera's solution is to implement StrongARM-like designs in Excalibur™ devices using SOPC Builder. Because it uses an Excalibur device, the instruction set architecture (ISA) remains consistent between the two devices and the custom peripheral set of the Intel SA-1110 device can be mapped into the Excalibur device.

A designer can use an Excalibur EPXA1 device to integrate the Intel SA-1110 functionality as a stand-alone processor. In many cases, an Intel SA-1110 device will be used in conjunction with an FPGA to provide a PCI interface. A design that uses an Excalibur EPXA4 device can implement both of these functions.

EPXA10D Development Kit

Using an Excalibur EPXA10 device, the EPXA10D Development Kit is an ideal platform for developing system-on-a-programmable-chip (SOPC) designs for a wide variety of applications requiring high-density logic with a high-performance processor (e.g., wireless base stations and network switches).

The board provides an Ethernet physical interface (PHY), magnetics, and a connector, which are supported by an OpenCore® Plus version of an Ethernet media access control (MAC) interface provided as part of the kit. The board also includes two UART port connectors, one connected directly to the UART pins on the embedded processor subsystem, and one to the general-purpose I/O pins in the programmable logic. A UART OpenCore Plus IP core is also provided.

The EPXA10D development board features include:

- Excalibur EPXA10 device in a 1,020-pin Fineline BGA package
- 10/100 Ethernet PHY, supporting full and half duplex modes
- Two off RS232 UART connectors
- 16-Mbyte flash memory (boot from flash supported)
- 64-Mbyte double data rate (DDR) SDRAM on board
- Five on-/off-board clock sources for system design
- ByteBlasterMV™ download cable
- IEEE Std. 1149.1 Joint Test Action Group (JTAG) connector
- Multi-ICE® connector for ARM® debug tools
- Two Altera expansion headers for daughter cards (one standard and one long)
- One user-definable 8-bit dual in-line parallel (DIP) switch block
- Four user-defined, push-button switches

The EPXA10D Development Kit includes:

- Excalibur EPXA10 development board
- Power supply
- Documentation
- Software, drivers, and application examples on CD-ROM
- Connection cables
- Quartus II software with one-year time limited license
- SOPC Builder and GNUPro tools

The ordering code for the development kit is EPXA-DEVKIT-XA10D, and the retail price is $7,995.

Nios Processor

Nios Embedded Processor Version 3.0 Now Shipping

The Nios embedded processor version 3.0 further enhances the industry's most popular configurable embedded processor. Version 3.0 builds on the successful version 2.*x* CPU architecture, and gives designers the following enhancements:

- *JTAG-Based Software Debugger Interface*: The Nios on-chip instrumentation debugging module supports processor run control, hardware breakpoints, and real-time trace via a standard JTAG connection.
- *Instruction and Data Cache*: The cache memory improves CPU performance when accessing off-chip memory devices.
- *Enhanced SDRAM Controller*: Offers higher f_{MAX} performance with low-cost SDRAM devices, and achieves approximately one memory access per clock cycle in conjunction with the new cache memory feature.

The Nios embedded processor version 3.0 ships with SOPC Builder version 2.8, offering the same easy-to-use graphical interface for defining and integrating Nios processor systems.

Nios Development Kit, Stratix Edition Now Shipping

The Nios Development Kit, Stratix Edition provides all the hardware and software development tools required for a designer to begin developing custom embedded systems based on the Nios processor. The kit includes the Nios processor version 3.0 and a development board featuring a Stratix EP1S10 device, in addition to 8-Mbyte flash memory, 1-Mbyte SRAM, 16-Mbyte SDRAM, a CompactFlash connector, 10/100 Ethernet MAC/PHY device, and switches, LEDs and prototype connectors. The Nios Development Kit, Stratix Edition is priced at $995, and is available today.

For the most recent news on the Nios processor version 3.0 and the Nios Development Kit, Stratix Edition, visit **www.altera.com/nios** or see "Nios Processor Version 3.0 Delivers the Features Customers Want Most" on page 4.

APEX II

APEX II Device Availability

All members of the APEX™ II device family are shipping. APEX II devices range in density from 16,640 to 67,200 LEs and are memory-rich; they offer 4 Kbits of memory per embedded system block (ESB), with total device memory ranging from 416 Kbits to 1.1 Mbits. The APEX II device family supports high-speed data transfers through a wide range of high-speed I/O standards such as LVDS, PCML, LVPECL, HSTL, SSTL, and HyperTransport™ technology. With True-LVDS™ circuitry, APEX II devices can achieve data transfer rates of up to 1 Gbps per channel. Designers can take advantage of these I/O features by using APEX devices in the following applications:

- PHY-link layer interface applications (POS-PHY, Flexbus, and UTOPIA)
- Host-processor interface applications (HyperTransport technology, PCI, and PCI-X)
- Switch fabric interfaces (CSIX and LCS)
- External memory interfaces (DDR, zero bus turnaround (ZBT), and quad data rate (QDR) memory devices)

For new designs requiring high performance, use Stratix and Stratix GX FPGAs. These FPGAs deliver top performance and are feature rich.

See Table 4 for APEX II device availability.

Table 4. APEX II Device Availability

Device	Package	Availability
EP2A15	672-pin FineLine BGA 724-pin BGA	Now
EP2A25	672-pin FineLine BGA 724-pin BGA	Now
EP2A40	672-pin FineLine BGA 724-pin BGA 1,020-pin FineLine BGA	Now
EP2A70	724-pin BGA 1,508-pin FineLine BGA	Now

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APEX II Industrial Offerings

All the industrial-grade devices for the APEX II device family are now available. Industrial-grade production versions of the device offerings are available in a -8 speed grade. Table 5 shows the availability for industrial-grade offerings.

Table 5. APEX II Industrial Device Offering

Device	Package	Availability
EP2A15	672-pin FineLine BGA	Now
EP2A25	672-pin FineLine BGA	Now
	724-pin BGA	Now
EP2A40	724-pin BGA	Now
	1,020-pin FineLine BGA	Now

Mercury

Mercury Devices Available in Production Mode

All devices and all speed grades of the Mercury™ device family are shipping in production mode, including industrial-grade offerings in both product lines (see Table 6). High-speed 1.25-Gbps serial links featuring clock data recovery (CDR) circuitry and an embedded serializer/deserializer (SERDES) make these devices ideal for serial backplane applications.

Table 6. Mercury Device Availability

Device	Package	Temperature Grade	Availability
EP1M120	484-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now
EP1M350	780-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now

APEX

APEX 20KC Devices Available in Production Mode

All APEX 20KC devices and packages are available. Table 7 shows the availability of APEX 20KC devices.

For new designs requiring high performance, use Stratix and Stratix GX FPGAs. These FPGAs deliver top performance and are feature rich.

Table 7. APEX 20KC Device Availability

Device	Package	Availability
EP20K200C	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K400C	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000C	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now

Industrial-Grade APEX Device Offerings

Industrial-grade APEX devices are now available in a wide variety of package offerings. Refer to Tables 8, 9, and 10.

Table 8. APEX 20KC Device Industrial Offering

Device	Package	Speed Grade
EP20K200C	484-pin FineLine BGA	-8
EP20K400C	672-pin FineLine BGA	-8
EP20K600C	652-pin BGA 672-pin FineLine BGA	-8
EP20K1000C	1,020-pin FineLine BGA	-8

Table 9. APEX 20KE Device Industrial Offering

Device	Package	Speed Grade
EP20K30E	144-pin FineLine BGA	-2X *(1)*
EP20K60E	144-pin FineLine BGA 208-pin PQFP 324-pin FineLine BGA	-2X *(1)*
EP20K100E	144-pin FineLine BGA 240-pin PQFP 324-pin FineLine BGA 356-pin BGA	-2X *(1)*
EP20K160E	484-pin FineLine BGA	-2X *(1)*
EP20K200E	240-pin PQFP 356-pin BGA 484-pin FineLine BGA 672-pin FineLine BGA	-2X *(1)*
EP20K300E	240-pin PQFP 652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K400E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K600E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K1000E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*

Note to Table 9:

(1) The "X" denotes phase-locked loop (PLL) and LVDS support.

Table 10. APEX 20K Device Industrial Offering

Device	Package	Speed Grade
EP20K100	208-pin PQFP 240-pin PQFP 324-pin FineLine BGA	-2V *(1)* -2V *(1)* -2XV *(1)*
EP20K200	240-pin PQFP 484-pin FineLine BGA	-2V *(1)*
EP20K400	652-pin BGA 672-pin FineLine BGA	-2V *(1)*

Note to Table 10:

(1) The "V" denotes 5.0-V tolerant I/O interfaces. The "X" denotes PLL support.

ACEX

ACEX 1K Device Availability

ACEX® 1K devices are available in quad flat pack (QFP) and FineLine BGA packages in 576-, 1,728-, 2,880-, and 4,992-LE densities. These cost-optimized devices are specially suited for low-cost, high-volume applications. For mid- and high-density designs, see Altera's newest and lowest-cost Cyclone FPGA family on page 18.

Free software support for all ACEX 1K devices is available in the Quartus II Web Edition software version 2.2, which is available for download at **www.altera.com**.

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MAX

MAX Power Calculator

The MAX® Power Calculator spreadsheet is now available for download on the Altera® web site on the MAX Design Utilities page. This spreadsheet allows for easy and seamless power estimation for MAX 3000 and all MAX 7000 device families. It automatically calculates the power according to the equations and constants within each MAX device family data sheet. Choose the family and target device, and enter the number of macrocells used (with turbo on or off) with frequency of operation and toggle rate. The number of macrocells used and number of macrocells with turbo are in the MAX+PLUS® II or Quartus II software report (**.rpt**) files.

If you enter the ambient temperature and the device package, the spreadsheet can combine data with the power result to verify that the design meets thermal requirements. The spreadsheet also automatically lists available packages according to the device family and density selected, providing a simple and complete power analysis tool for any MAX design.

Free ByteBlasterMV Cable

Altera values customer feedback to better understand how our products are used and what we can do to improve them in future. To gather input from the broadest range of customers, the new MAX web pages include an on-line survey. The survey is accessible from the promotion button at the right side of the page and the first 50 survey responses will receive a free ByteBlasterMV™ cable.

Configuration

New Serial Configuration Devices

Altera's new serial configuration devices are the lowest-cost configuration devices in the industry and provide the ideal complement to Cyclone FPGAs in addressing high-volume, price-sensitive applications. Engineered for maximum efficiency, serial configuration devices deliver features such as in-system programmability (ISP) and re-programming capabilities at a cost even lower than one-time programmable (OTP) solutions.

Enhanced Configuration Devices

Enhanced configuration devices provide a complete single-device solution for a wide range of density requirements. Vertical migration capability allows designers to easily migrate from the EPC4 to the EPC8 to the EPC16 device in the same package without having to change the board layout. Commercial and industrial grade EPC4, EPC8, and EPC16 devices are all now available.

Enhanced configuration devices offer ISP through a built-in IEEE standard for boundary-scan-based, in-system configuration standard of programmable devices (IEEE 1532). The inclusion of ISP and re-programmability provides a significant advantage over OTP solutions by introducing flexibility and reusability to the configuration process.

Design Software

Quartus II Software Version 2.2 Service Pack 1 Adds Full Support for Cyclone Devices

Service pack 1 for the Quartus II software version 2.2 is now available from the Altera web site. This release adds programming file generation for the first Cyclone devices, adds pin-out support for Cyclone EP1C6 and EP1C12 devices in the 256-pin FineLine BGA package, and adds advanced support for two new Stratix packages.

New Device Support

Service pack 1 for the Quartus II software version 2.2 adds support for the devices listed in Table 11.

Table 11. New Quartus II Software Device Support

Family	Device	Package
Cyclone	EP1C6	144-pin TQFP 240-pin QFP
	EP1C20	324-pin FineLine BGA 400-pin FineLine BGA
Stratix	EP1S40	780-pin FineLine BGA *(1)* 956-pin BGA 1,020-pin FineLine BGA 1,508-pin FineLine BGA
	EP1S80	1,020-pin FineLine BGA *(1)*

Note to Table 11:
(1) Advanced compilation and simulation only.

Customer Release Notes

Information regarding all of the major enhancements in Quartus II software releases is contained in the *Quartus II Software Release Notes* document. This document is available from the Literature section of the Altera web site at **www.altera.com** within one week of each release.

Quartus II Web Edition Software Adds Full Support for Cyclone Devices

The Quartus II Web Edition software is an entry-level version of the Quartus II design software supporting all devices in the new Cyclone family—the lowest cost FPGAs ever. The Quartus II Web Edition software version 2.2 service pack 1 is now available on the Altera web site including programming file generation for the first available members of the new Cyclone family listed in Table 11. The Quartus II Web Edition software also supports selected Stratix, APEX II, APEX 20KE, Excalibur, MAX 7000, MAX 3000, FLEX® 10KE, ACEX 1K, and FLEX 6000 devices.

New Design Software Starter Suite CD is Now Available

The Altera Design Software Starter Suite CD-ROM includes all of the software necessary to start designing with Altera devices. The CD-ROM includes a complete environment for system-level design, FPGA and CPLD design, and embedded software development, including the following software:

- Quartus II Web Edition FPGA and CPLD design software
- SOPC Builder automated system development software
- GNUPro toolkit embedded processor development software
- Nios OpenCore Plus hardware evaluation
- DSP Builder interface to The MathWorks Simulink and MATLAB software evaluation
- MAX+PLUS II BASELINE CPLD design software

This CD-ROM can be requested as an option from the Quartus II Web Edition download page or by emailing **lit_req@altera.com**.

ByteBlaster II Cable Now Shipping

The ByteBlaster™ II programming cable is a direct replacement for the ByteBlasterMV™ programming cable. The ByteBlaster II cable supports all the same features as the ByteBlasterMV cable and adds the following new features:

- Support for active serial configuration mode to support the new low-cost EPCS1 and EPCS4 configuration devices
- Support for 1.8-V programming and configuration

The ByteBlaster II is now shipping and is supported in the Quartus II software version 2.2 and higher. An updated ByteBlaster II software driver is included in the Quartus II software version 2.2 service pack 1 to support the new EPCS1 and EPCS4 configuration devices.

The Development of an Altera-Based 10 Gigabit Ethernet Tester

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The growing presence of the Internet protocol (IP) at the heart of telecom networks puts pressure on service providers and vendors to optimize management of user traffic. One change that has resulted from this is extending long-established local area network (LAN)-based Ethernet protocols into network cores. This change spawned the creation of Gigabit Ethernet and, more recently, 10 Gigabit Ethernet as defined by the IEEE in its 802.3ae specification. Vendors and service providers now seek independent sources to verify their 10 Gigabit Ethernet products. The main challenge for test equipment manufacturers consists of determining which specific feature set meets the needs of the 10 Gigabit Ethernet user. The starting point is to understand how 10 Gigabit Ethernet is used.

Innocor's 10 Gigabit test products use Altera's programmable logic exclusively. The high-speed SFI-4, PL4/SPI-4.2, and 8b10b I/O capabilities combined with the high logic element (LE) density and embedded RAM of the Stratix™ and APEX™ II devices make them ideal for such demanding broadband applications.

Test feature needs vary largely between 10 Gigabit Ethernet applications. Three main areas of testing are transport with a focus on framing and error conditions; routing/switching/storage where latency, loss, and upper layers are of high interest; and the component level that concentrates on the physical layer. Test equipment that can provide testing for 10 Gigabit Ethernet LAN and wide area network (WAN) on the same hardware provides savings to the user and protects the product investment. Requirements for core routing, switching, and even storage are very different. 10 Gigabit Ethernet is a new PHY interface that supports test needs related to POS and lower speed Ethernet. In this environment, test applications focus more on upper layer applications and network simulations when compared to transport-based users.

The 802.3ae standard is the starting point to determine the specific elements of 10 Gigabit Ethernet that require testing. Target users and applications must then be identified to refine the requirements and derive the test equipment's overall architecture. Innocor designed its Testpoint SM-9953EX 10 Gigabit Ethernet offering in collaboration with customers involved in providing and developing transport technology. As a result, Innocor initially focused on defining strong Layer 2 features to test aspects that impact framing devices. Additional features were provided to test the system level and flow control. The following were found to be the key elements to ensure flexibility and investment protection for the user:

- Support for 10 Gigabit Ethernet WAN (9.953 Gbps) and 10 Gigabit Ethernet LAN (10.3 Gbps) on a single hardware platform.
- Simple field upgrades to support incremental features via programmable logic technology.
- Support for multiple laser types at different wavelengths and power level via multi-source agreement (MSA) technology.
- Ability to support long-haul applications using forward error correction (FEC) with ITU-T G.709 for 10 Gigabit Ethernet WAN (10.7 gigabits per second (Gbps)) and 10 Gigabit Ethernet LAN (11.1 Gbps).

Key feature areas were identified to test 10 Gigabit Ethernet interfaces on transport equipment:

- *Frame Sizes*: Support to inject and identify short, in-range, and long frames. The test equipment must also test MAC frame length mismatches. Virtual local area network (VLAN) support is also required.
- *Payload Test Patterns*: Data test equipment sometimes validates payload via proprietary cyclic redundancy code (CRC) schemes. Transport equipment testing requires the more robust pseudo-random bit sequence (PRBS) approach to test down to the bit level. Tests based on PRBS31 is supported at the media access control (MAC) and physical coding sub-layers (PCSs).

- *Bandwidth Control*: Refers to varying the inter-frame gap length including invalid condition tests where the inter-frame gaps is less than the smallest allowable value.
- *Flow Control Features*: Ensures matching traffic rates between the LAN (10.3 Gbps) and WAN (9.953 Gbps) interfaces via either MAC pause frames or ifsStretch capabilities to regulate the inter-frame gap size.
- *PCS Layer*: PCS encodes the information from the MAC layer. The test equipment must detect and inject discrete errors and block rates. In addition, tests must be provided to detect remote and local faults.
- *MAC Layer Errors*: Capabilities to provide CRC error injection in the form of packet error rates.
- *Disruption Time Measurement*: The response of the transport equipment to protection switching should be measured for 10 Gigabit Ethernet WAN or LAN.
- *Synchronization*: Options to provide clocking, including internal clock, loop timing, and clock rate variations.

To meet the requirements listed above, the tester's hardware architecture must include flexible framing technology and field-upgradable programmable logic. Bidirectional line rate technology is important to push the limits of systems under test up to the 10 Gigabit Ethernet LAN rate of 10.3 Gbps. A different set of requirements is driven by the applications supported by routing, switching, and storage devices that demand more at the upper layers. These additional needs result in either higher costs to address all requirements or a more tailored hardware architecture. The best approach for any test equipment manufacturer is to use programmable logic within the confines of logic element usage and input-output architectures. An example of design choice for IP testing is how to perform Internet traffic simulations that integrate multiple complex protocols and traffic flows. This requirement, especially in the case of 10-Gbps rates, can imply a large number of dedicated hardware resources raising equipment cost. Alternatively, traffic patterns can be constructed via software and played from high-speed memory devices resulting in repeatable traffic sequences. 10 Gigabit Ethernet testers must consider the following high-level requirements:

- Provisions for multiple protocol support including 802.2 LLC/SNAP, IPv4, IPv6, TCP, and UDP. Header field edition must be provided.
- Generation and analysis of multiple traffic streams. Simulation of a multitude of MAC, IP addresses to emulate traffic from multiple sources, and destinations. Each stream must have its own bandwidth, packet length, and protocol definitions.
- Testing for quality of service parameters including the evaluation of delays and latency through a system under test and identifying out-of-sequence, lost, and discarded packets.
- Packet filtering for statistics and to enable buffer captures along with protocol decodes.
- Routing protocol conformance and performance testing, which is similar to simulating a network on the control plane for protocols such as MPLS, OSPF, and BGP-4.

On the 10 Gigabit Ethernet component testing front, dedicated hardware is required in a test set. The requirements for that market segment include:

- Evaluation of optical signal to noise ratio (OSNR)
- Stressed-eye testing
- Jitter tolerance generation and measurements
- Receiver sensitivity
- XAUI interface testing

In many cases, these requirements overlap, which poses not only technical but also cost-control challenges. The development of 10 Gigabit Ethernet test equipment therefore depends on the target market and applications. The key is to provide a balance and give the user the most flexibility for the price.

Innocor has developed its SM-9953EX to address the needs of manufacturing and research and development facilities for the emerging transport market based on 10 Gigabit Ethernet. In addition, a set of complementary features such as IP streaming, time-stamping, packet sequencing, and filtering addresses the requirements of routing, switching, and storage device testing for manufacturing. Besides testing 10 Gigabit Ethernet LAN and WAN, Innocor's SM-9953EX can also test SONET, SDH, ATM, and POS at rates of 10 Gbps.

For more information about Innocor's test solutions, visit the Innocor web site at **www.innocor.com** or email **info@innocor.com**.

Altera is Listening

Customers who have recently contacted Altera® Applications were asked to evaluate their technical support experience through Altera's continuing customer applications survey program.

Nearly 1,000 customers in 2002 were asked how they felt about Altera Technical Support. Respondents were asked questions such as the quality of our answers, and the timeliness of our reply. They were also asked to indicate the types of services they might like to see from us in the future. From increased employee training to enhanced web site organization, these surveys helped us plan a number of improvements in the way we do business.

To thank those who took the time to give feedback, Altera has rewarded some survey takers with **Amazon.com** gift certificates or Palm handhelds. Pictured in Figure 1 is Ray Schouten, Altera Field Applications Engineer congratulating Scott Gygi of L3 Communications on winning a new Palm m515 handheld.

Figure 1. Palm m515 Winner

Altera Presents Good Design Practices at Third-Party Conferences

Design practices have an enormous impact on a design's timing performance, logic utilization, and system reliability. Using good design practices allows successful design migration between ASIC and FPGA implementations for prototyping and production. Poor design practices can lead to low performance, high logic or resource utilization, and unstable or unreliable designs associated with increased verification time.

Altera Contributes to Third-Party Conferences

To help you with good design practices, Altera will be presenting at the Synopsys Users Group (SNUG) Conference (March 17 to 19) and the International Mentor Users Group (MUG) Conference (April 28 to 30). Altera speakers will discuss how designers can obtain optimal results for FPGA designs by:

- Understanding the impact of synchronous design practices
- Following recommended design techniques
- Targeting the advanced FPGA architectural features

For more details, go to **www.snug-universal.org** or **www.mentorug.org**.

Discontinued Devices Update

Altera will be obsoleting select devices from product-term and FPGA families (see Table 1). Most of the devices will have longer-than-usual last-time buy (18 months) and last-time ship dates (an additional 6 months) to allow customers to gradually transition to using alternative ordering codes.

Select ordering codes from mature families such as MAX® 7000S are being obsoleted to increase the operational efficiency in the manufacturing flow. On mainstream product families such as the MAX 7000A, FLEX® 10KE, APEX™ 20K and newer product families, such as the MAX 7000B, ACEX® 1K, and APEX 20KE, ordering codes have been consolidated to offer a limited set of codes that will cover the various package and speed grade options.

Continued support for devices beyond the phase-out period may be available through Rochester Electronics, an extended after-market supplier. For more information, contact Rochester Electronics at (508) 462-9332 or your local Altera sales office.

Continued support for devices beyond the phase out period may be available through Rochester Electronics, an extended after-market supplier.

Product Family	Device	Last Order Date	Last Shipment Date	Reference
MAX 7000S	Selected devices with fixed-pulse width programming option	10/31/03	04/30/04	PDN 0203
MAX 7000A	Selected devices in micro ball-grid array (BGA), FineLine BGA™, and TQFP packages	10/31/03	04/30/04	PDN 0203
MAX 7000B	Selected devices	10/31/03	04/30/04	PDN 0203
FLEX 8000	Selected FLEX 8000 pin-grid array (PGA) packages	02/28/02	08/31/02	PDN 0107
	Selected devices	02/28/03	08/31/03	PDN 0107
FLEX 10K	Selected FLEX 10K PGA packages	02/28/02	08/31/02	PDN 0107
	Selected FLEX 10K PGA & BGA packages	02/28/03	08/31/03	PDN 0107
FLEX 10KA	Selected PGA packages	02/28/03	08/31/03	PDN 0107
FLEX 10KE	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	Selected devices	10/31/03	04/30/04	PDN 0204
APEX 20K	Selected PGA packages	02/28/03	08/31/03	PDN 0107
	Selected devices	10/31/03	04/30/04	PDN 0204
APEX 20KE	Selected devices	10/31/03	04/30/04	PDN 0204
ACEX 1K	Selected devices	10/31/03	04/30/04	PDN 0204

How to Contact Altera

It is now easier than ever to get information and services from Altera. The table below lists some of the ways you can reach Altera.

Information Type	U.S. & Canada	All Other Locations
Product Literature	**http://www.altera.com**	**http://www.altera.com**
Altera Literature Services *(1)*	**lit_req@altera.com**	**lit_req@altera.com**
News & Views Information	**http://www.altera.com/literature/nview.html** **n_v@altera.com**	**http://www.altera.com/literature/nview.html** **n_v@altera.com**
Non-Technical Customer Service	(800) 767-3753	(408) 544-7000
Technical Support	**http://www.altera.com/mysupport**	**http://www.altera.com/mysupport**
	(408) 544-6401	(408) 544-6401 *(2)*
FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	(408) 544-7104	(408) 544-7104 *(2)*
	http://www.altera.com	**http://www.altera.com**

Notes:

(1) The ***Quartus Installation and Licensing*** and ***MAX+PLUS II Getting Started*** manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.

(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for the latest listing.