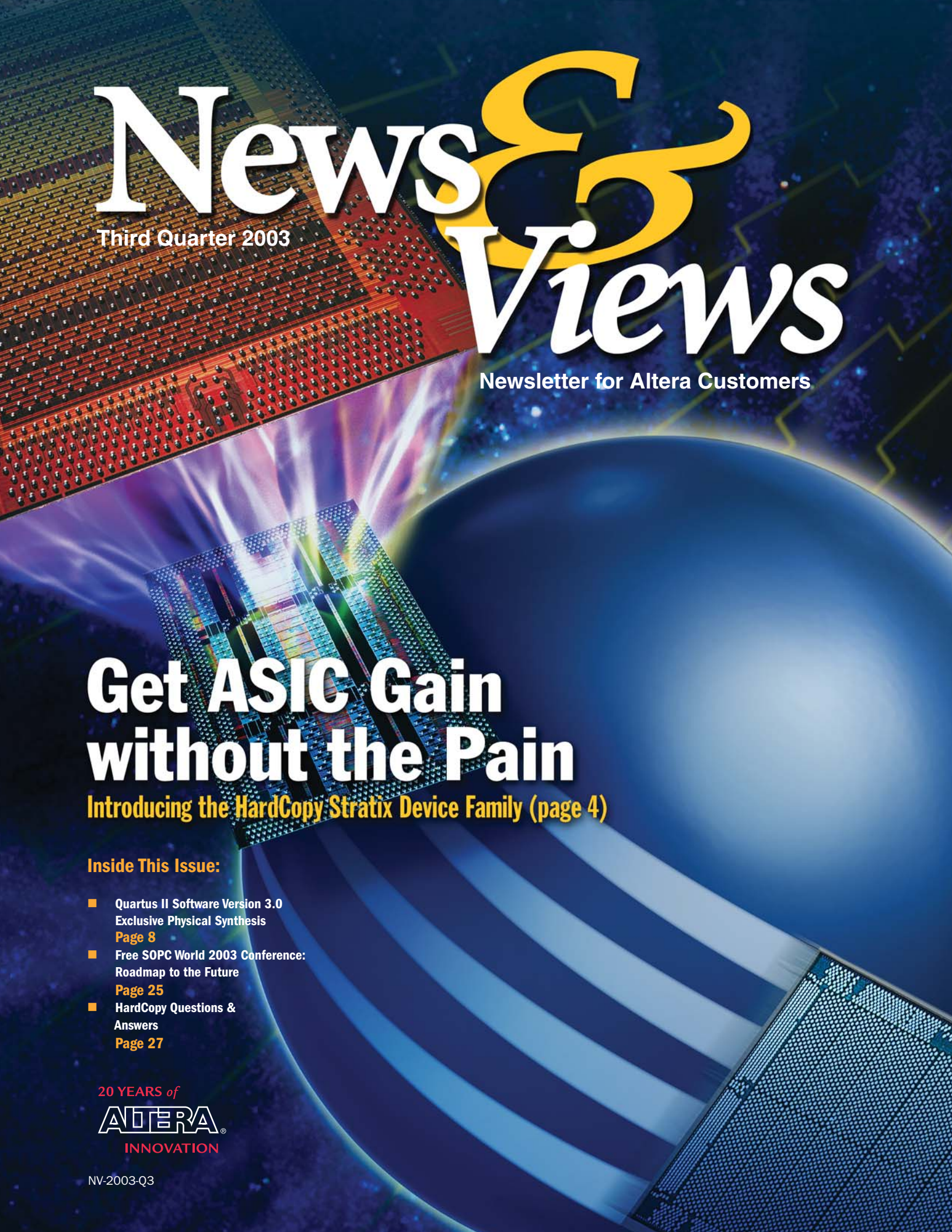
News & Views

Third Quarter 2003

Newsletter for Altera Customers



Get ASIC Gain without the Pain

Introducing the HardCopy Stratix Device Family (page 4)

Inside This Issue:

- Quartus II Software Version 3.0 Exclusive Physical Synthesis
  Page 8
- Free SOPC World 2003 Conference: Roadmap to the Future
  Page 25
- HardCopy Questions & Answers
  Page 27

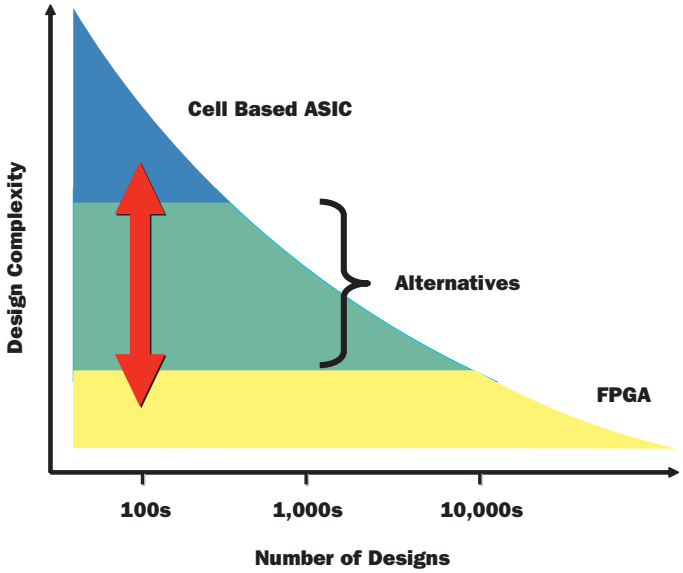
20 YEARS of ALTERA® INNOVATION

NV-2003-Q3

HardCopy Stratix – A Class All Its Own

It's no secret that the rising cost of ASIC development is concern throughout the industry. With development costs steadily increasing with each new process geometry, most system designers are hard pressed to justify this escalating investment. These risks are in fact a big issue for ASIC manufacturers themselves. ASICs certainly have their place—remaining a viable solution for a certain class of high-volume, very-high-density and high-performance applications. But, the number of these high-volume applications continues to dwindle. With up-front development expenses in the millions of dollars, ASICs are a decreasingly viable option for applications with volume ranges from tens of thousands to hundreds of thousands, such as routers, modems, set-top boxes, enterprise storage systems, printers, HDTVs, and the like. These and similar applications need a new cost-effective solution, which has opened a "gap" in the chip industry—that application space where volumes are too low to justify the expense of an ASIC, and FPGAs don't meet the overall system needs. (see chart).

Sensing this opportunity early on, Altera introduced the first HardCopy™ devices back in October of 2001. This FPGA-based ASIC alternative not only lowered the overall silicon cost by as much as 70%, but significantly decreased the typical ASIC development cycle from 15 months to 8 months, concept to production.

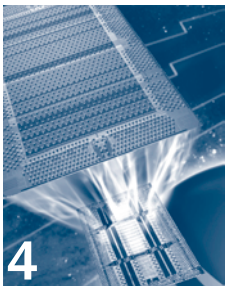


This year, solidifying its leadership position, Altera has taken a giant leap forward with the introduction of HardCopy Stratix™ devices. Unique in its design methodology, this new edition of the HardCopy series is supported by the new Quartus® II software version 3.0. ASIC and FPGA designers alike can now target HardCopy devices right from start. The Quartus II design software has all of the timing and power estimation tools a designer needs to take advantage of the many benefits of HardCopy Stratix devices, such as the option to boost performance an average of 50% or reduce power consumption by 40% on average over the equivalent Stratix™ device. Altera's intellectual property cores—in particular the popular Nios® embedded processor—migrate seamlessly and royalty free to HardCopy Stratix devices.

FPGAs for smaller volume—HardCopy devices for high volume—FPGAs for prototyping to HardCopy implementations—Change your mind mid-stream—All of these risk-free options are available at your fingertips via the Quartus II tools for only $2000! Finally, system designers have all of the flexibility they need for rapid and cost-effective system development.

Gain more insight on the HardCopy Stratix and Quartus II software version 3.0 story in this issue of News & Views. They're a unique and compelling combination that brings complete design control to every designer.

Tim Colleran,
Vice President of Product Marketing



Get ASIC Gain without the Pain

Quartus II Software Version 3.0

SOPC World

Features

Get ASIC Gain without the Pain: Introducing the HardCopy Stratix Device Family 4
Quartus II Software Version 3.0 Exclusive Physical Synthesis 8

Devices & Tools

HardCopy: The Comprehensive ASIC-Alternative 10
All Cyclone Devices Now Shipping in Production 10
All Stratix Devices Now Shipping in Production 11
Meeting the Challenges of High-Speed Systems 12
Software Development Pack Now Part of Quartus II 3.0 12
Nios Development Kit, Stratix Professional Edition Now Shipping 13
MAX 3000A Supports Industrial & Extended Temperatures 15
Quartus II Software Version 3.0 Shortens Design Cycles by 40% 16

Contributed Article

Implementing High-Performance DSP Designs with Precision RTL Synthesis 19

Technical Article

Straightforward DDR SDRAM Connection to FPGAs Using IP 21

Altera News

Altera University Program 23
Introducing Altera Handbooks—One-Click Access to Product Documentation 24
Free SOPC World 2003 Conference: Your Roadmap to the Future 25
Altera Training 26

Questions & Answers

Altera Questions & Answers 27

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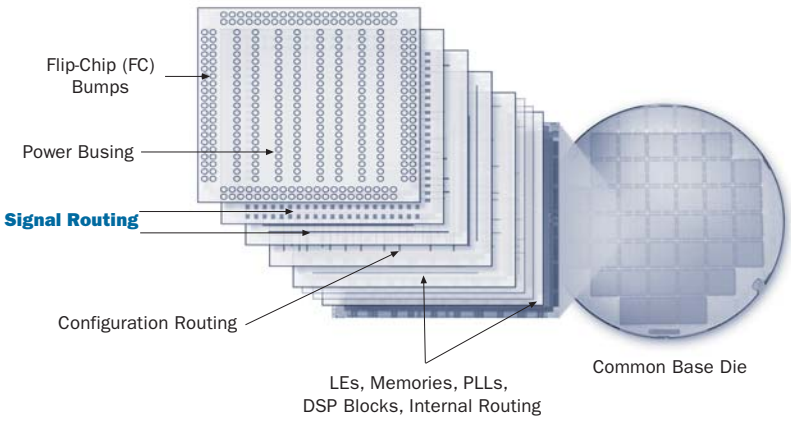
Get ASIC Gain Without the Pain: Introducing the HardCopy Stratix Device Family

A comprehensive alternative to ASICs, Altera HardCopy Stratix™ devices are the industry's only complete prototype-to-volume-production solution for high-density designs. As process geometries continue to shrink, mask and wafer costs have increased significantly. For example, today's mask costs range from $600,000 for a 0.13-µm design to $1.5 million for a 90 nm design ("Sticker Shock for Photomasks", Electronic Business, May 1, 2003). ASIC design demands large up-front investments through expensive tools, long product development cycles, and considerable engineering resources to develop multi-million gate devices. Furthermore, uncertain market conditions and lost market opportunities due to time consumed by performing multiple re-spins have amplified the risks of using ASICs.

These technical and economic challenges are driving a fundamental change in ASIC design and development. It has become apparent that an alternative to ASICs—a solution that is capable of providing a guaranteed path to first-time success in the quickest possible time and with minimal development cost—is necessary.



HardCopy Stratix Silicon Technology

ASIC Gain without the Pain

Altera's HardCopy Stratix devices address the same concerns—huge development costs, uncertain market conditions, long design and development cycles, and the risk of non-functional silicon—described earlier. Together with the Quartus® II software and a large intellectual property (IP) portfolio, HardCopy Stratix devices provide a comprehensive alternative to ASICs without the risks and exorbitant development costs.

HardCopy devices are low-cost, mask-programmed devices that preserve the architecture and features of their FPGA equivalents without the programmability, resulting in considerable die-size reduction. You can design with FPGAs for the usual benefits of flexibility, rapid design changes with the same silicon, and in-system verification of the design for proper functionality before seamlessly migrating to a mask-programmed device with minimal risk, lowest cost, and quickest time-to-market. This capability, not available in any competing solution, enables you to implement powerful device features and differentiate your solutions from your competition.

HardCopy Stratix Devices

The second-generation HardCopy devices from Altera, HardCopy Stratix devices, are built on the architecture and features of the industry-leading Stratix™ FPGAs and provide an equivalent ASIC gate density range of 300,000 to 1.5 million standard cell gates (including digital signal processing (DSP) blocks). They are manufactured using a set of base arrays common to multiple designs for a particular resource density with few top-level metal layers for customization. See Table 1.

By retaining the characteristics of their Stratix FPGA counterparts, HardCopy Stratix devices benefit from a perfected process technology (Alera has been shipping Stratix FPGAs for over a year), proven architecture, and valuable features used in a variety of applications. At the same time, HardCopy Stratix devices provide 60 to 70% die-size reduction over the equivalent FPGA. The resulting price benefits enable customers to position their products competitively and move them rapidly in their market segments.

Additionally, HardCopy Stratix devices are on average 50% faster and consume up to 40% less power than their Stratix FPGA counterparts. See the "Single Tool Delivers Unified Design Methodology" section for a description of how HardCopy Stratix devices can be designed for higher performance.

HardCopy Stratix devices contain powerful custom-designed features like high-speed phase-locked loops (PLLs) and high-speed I/O pins supporting differential signaling and DSP blocks that can be used to implement efficient and fast arithmetic functions. With these features, you can obtain superior performance and maximize your throughput. While these complex design blocks are available as IP cores from several vendors to be stitched with other logic in an ASIC, you must deal with integration and verification issues, with the associated performance and functionality risks.

Table 1. HardCopy Stratix Device Family						
Device	**LEs**	**Total RAM Bits**	**DSP Blocks**	**PLLS**	**Max. User I/O Pins**	**Package**
HC1S25	25,660	1,944,576	10	6	473	672 FineLine BGA®
HC1S30	32,470	2,137,536 *(1)*	12	6	597	780 FineLine BGA
HC1S40	41,250	2,244,096 *(1)*	14	6	615	780 FineLine BGA
HC1S60	57,120	5,215,104	18	12	773	1,020 FineLine BGA
HC1S80	79,040	5,658,048 *(1)*	22	12	773	1,020 FineLine BGA

Note to Table 1:
(1) The number of M-RAM blocks in HardCopy Stratix devices is less than their FPGA counterparts.

Guaranteed First-Silicon Success Means Fastest Time-to-Market

A set of base arrays manufactured ahead of time up to design interconnects and packaging provide significant cost and time-to-market benefits. However, the objective of lowering development costs and providing production devices in the quickest time will be missed if the risk of non-functional silicon is not eliminated. In other words, guaranteed first-silicon success is a must.

While HardCopy Stratix devices use the same base-array approach described earlier to provide high-volume devices in the shortest time, they also benefit from the ability to migrate a design proven in an FPGA. The proven netlist reduces the verification time considerably while minimizing the risks, since the netlist is preserved.

Secondly, the base arrays are manufactured in the same established process technology as their FPGA counterparts. You do not need to re-target your designs to new design libraries, which entails synthesis and verification, so you can enjoy considerable savings in design cycle time.

Finally, the base arrays maintain the various features of the FPGA counterpart to eliminate re-design or verification of high-performance FPGA features. During attempts to convert FPGA designs to ASICs, it is possible to replicate these features, but at the risk of considerable design time, effort, and introducing functional and performance inconsistencies. It is no surprise that several of these ASIC alternative solutions mandate that these structures not be used in the designs.

HardCopy Stratix devices not only offer the manufacturing process cost and time benefits similar to competing solutions, they are the only solution to provide the fastest time-to-market with guaranteed first-silicon success. To date, Altera has provided customers 100% first-silicon success with their HardCopy devices. Competing solutions cannot offer such a powerful alternative to ASICs.

HardCopy Stratix devices not only offer the manufacturing process cost and time benefits similar to competing solutions, they are the only solution to provide the fastest time-to-market with guaranteed first-silicon success.

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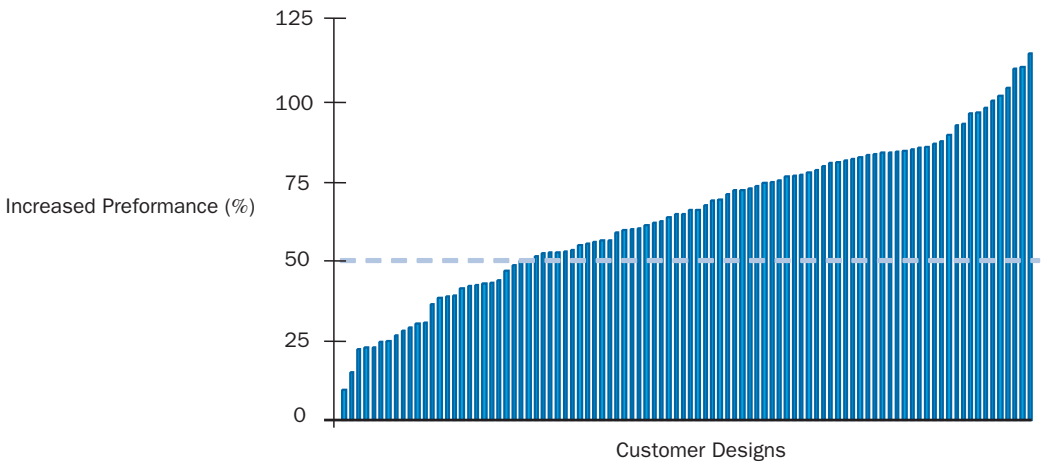
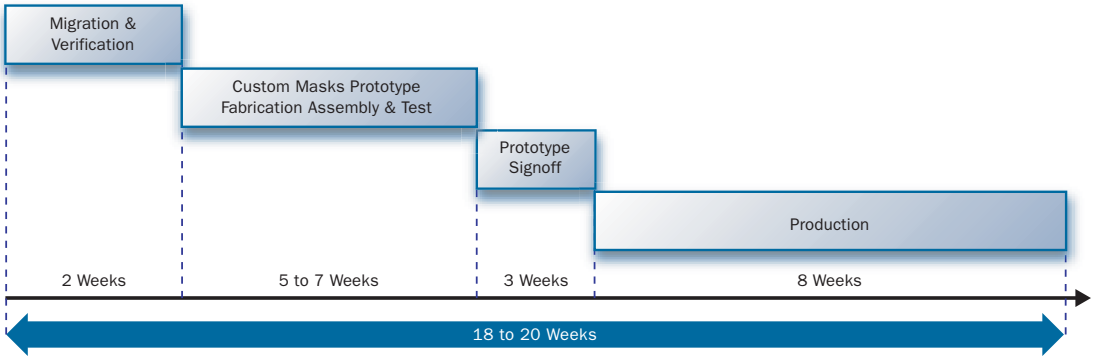


HardCopy Stratix Device Performance

HardCopy Device Time-to-Market



Single Tool Delivers Unified Design Methodology

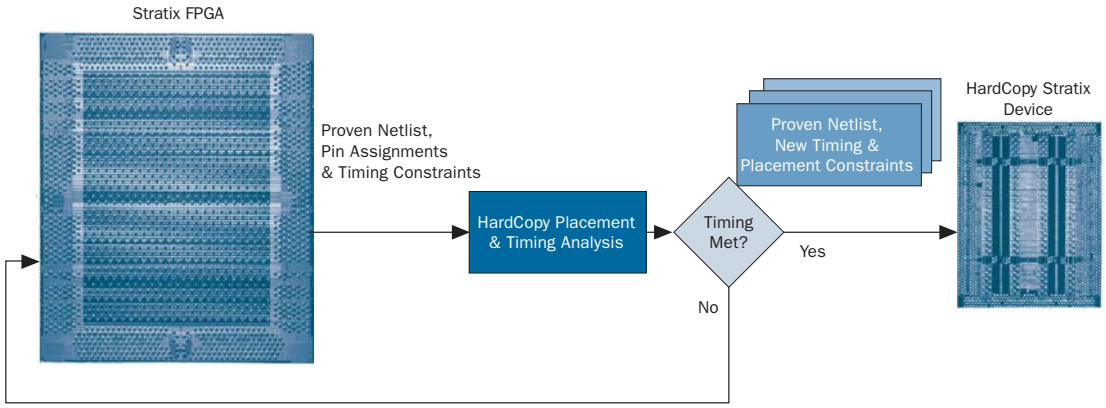
ASIC design and development tools typically cost several hundreds of thousands of dollars. Shrinking process geometries have also made it necessary to address physical design issues like cross-talk, the floorplan of power-hungry design blocks, and proper layout of supply rings. These issues have mandated that various tools be part of the development suite, adding to the tools budget.

HardCopy Stratix devices can be designed with the state-of-the-art Quartus II design software.

HardCopy Stratix devices can be designed with the state-of-the-art Quartus II design software. While the issues listed above are just as relevant to HardCopy Stratix devices as ASICs, the base arrays are already designed to meet these technical specifications. Benefiting from the preserved and tested FPGA architecture, the Quartus II tool contains all the technical details of the HardCopy Stratix device, eliminating the need for any additional tools.

The Quartus II design software version 3.0 or later allows you to design a HardCopy Stratix device directly or through a Stratix FPGA before seamlessly migrating to the HardCopy Stratix device. The former allows targeting a "virtual" Stratix FPGA within the Quartus II software. You can design to prove functionality and timing through simulation (just as with the regular ASIC design flow) before migrating to a fixed-function device by transferring the design database to Altera. The latter allows prototyping the FPGA design to prove in-system functionality prior to migration.

You can choose to retain the design's performance in the Stratix FPGA or obtain performance improvements over what can be achieved using a Stratix FPGA. You can optimize your design before migration, using the HardCopy Timing Optimization Wizard and obtain on average a 50% performance gain and approximately a 40% reduction in power consumption (compared to the implementation of the design in a Stratix FPGA) and maximize system throughput by leveraging the optimization results. The HardCopy Timing Optimization Wizard removes the guesswork on system performance and provides unparalleled design advantages.



HardCopy Device Performance Optimization

Migration, Not Conversion, Minimizes Risk

ASICs designed from scratch or through conversion of an FPGA design carry significant risks with the possibility of failed silicon. In either case, the benefits from the prototyping phase are discarded and a new design is created with a new netlist. The possibility of a re-spin entails additional development costs and lost market opportunities. These challenges have only been exacerbated as physical design issues, due to shrinking process geometries, have taken more prominence in the device design.

The ability to prove the design in an FPGA and migrate the successful netlist to a custom device provides a distinct advantage to HardCopy Stratix users. This path guarantees first-silicon success not available with any other ASIC-alternative design flows offered today. The successful seamless migration process (see flow at right) preserves the FPGA design verified in-system and includes standard ASIC back-end design activities like timing closure and design testability.

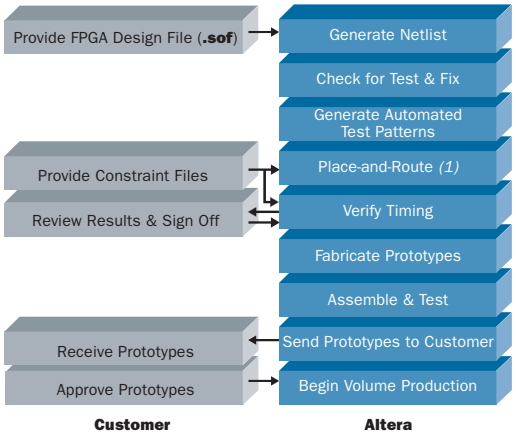
A significant benefit with this process is that you can use the same board—designed, verified, and qualified in the field with the FPGA—and replace the FPGA with the pin-to-pin compatible HardCopy Stratix device. This easy replacement eliminates the need to redo the verification, field qualification, and validation, which would be needed with any other solution.

Single Vendor Advantage

With a single vendor, you can have the ease of procurement and the guaranteed success in an integrated environment. Altera provides all the elements you need to migrate from an ASIC to a HardCopy Stratix device:

- Stratix FPGAs
- HardCopy devices
- Quartus II software tools
- IP

While there are several ASIC-alternatives available today in the market, Altera's HardCopy Stratix devices are the only complete solution that offers the lowest cost and quickest time-to-market with minimal risk and guaranteed success of future silicon.

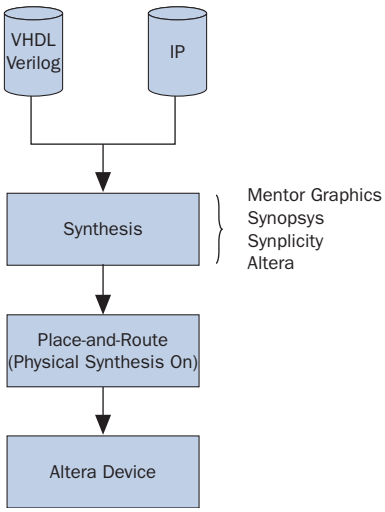


HardCopy Device Migration Process

Note:
(1) If placement constraints are provided, Altera will place as per these constraints and only route the design.

Quartus II Software Version 3.0 Exclusive Physical Synthesis

You can use the Quartus® II software version 3.0 physical synthesis compiler settings to increase design performance an average of 12% just by enabling a few checkbox compiler settings options. Quartus II physical synthesis options are applied during the fitting stage of the compilation process and can therefore be applied regardless of the synthesis tool used. The Quartus II software is the only design software available from an FPGA vendor that includes a suite of physical synthesis options to increase push-button design performance. A new design space explorer script is also available to automatically apply different combinations of physical synthesis and other Quartus II settings to seek out the optimum settings and performance for a particular design.



Quartus II Physical Synthesis Flow

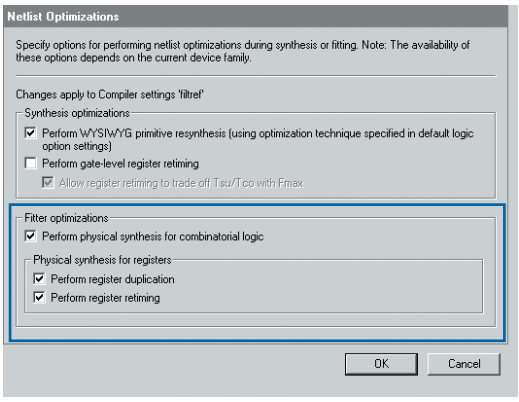
Physical Synthesis Optimizations

Physical synthesis optimizations tightly couple the synthesis and fitting processes and apply silicon- and design-specific timing information during the fitting/place-and-route process to perform additional synthesis optimizations, improving design performance. Physical synthesis optimizations in the Quartus II software are push-button features used to increase design performance without consuming any designer resources or requiring any advanced training. Full details about Quartus II physical synthesis optimizations are available in *AN 198: Timing Closure in the Quartus II Software* from the Altera web site.

In a standard compilation flow, the synthesis step optimizes the logical structure of a circuit for area, speed, or both, and maps the circuit to device-specific primitives such as logic elements (LEs), memory, and digital signal processing (DSP) block primitives. You can perform the synthesis step with third-party synthesis tools or the Quartus II software's integrated synthesis feature. The fitter step, also known as the place-and-route step, places and routes the device primitives specified by the synthesis tool to ensure that critical portions of the logic are close together and connected by the fastest possible routing resources. This standard flow produces excellent push-button results while delivering very fast compilation times. Physical synthesis optimizations use the Quartus II fitter's knowledge of post place-and-route delays in a design and perform additional synthesis optimizations to intelligently restructure a circuit to compensate for these delays. Changes to the circuit structure are applied incrementally by the fitter to critical "hot spots" in the design to improve design performance.

Enabling Physical Synthesis Options to Increase Design Performance

Physical synthesis options are turned off by default. To turn them on, use the **Netlist Optimization** page of the **Settings** dialog box (Assignments menu). It is important to note that you are in control of how these optimizations are performed. You can perform physical synthesis on an entire design or on a specific LogicLock™ module that will be imported into a top-level design. You can also specify nodes and entities that must not be touched by physical synthesis optimizations.



Quartus II Netlist Optimizations Dialog Box

The Quartus II software now includes three physical synthesis fitter optimization selections:

- Physical Synthesis for Combinatorial Logic
- Physical Synthesis for Registers – Register Duplication
- Physical Synthesis for Registers – Register Retiming

Turning on the **Perform WYSIWYG primitive resynthesis** option and all three physical synthesis fitter optimizations will increase design performance (f_{MAX}) an average of 12%.

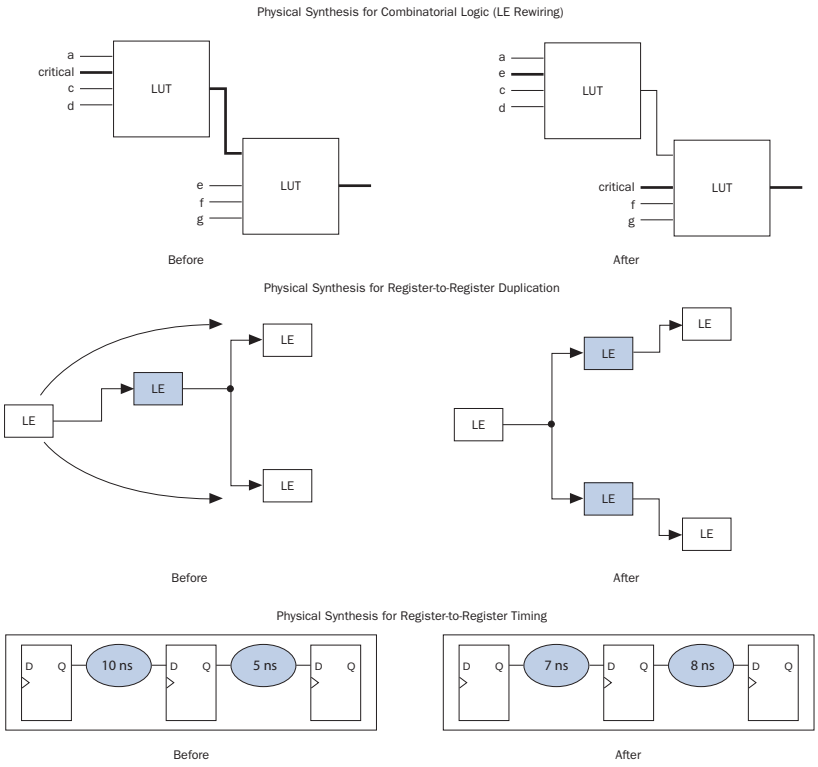
The figure to the right shows examples of some of the types of optimizations performed by each selection. The **Physical Synthesis for Combinatorial Logic** option can re-wire LE connections so the critical path has fewer layers through which to travel. The **Physical Synthesis for Registers – Register Duplication** option can duplicate a register that fans out to multiple locations, reducing the delay of one path without degrading the delay of another path. The **Physical Synthesis for Registers – Register Retiming** option allows the Quartus II fitter to move registers across combinatorial logic, balancing timing delays and improving overall circuit performance.

Design Space Explorer Increases Average Design Performance 20%

Each design has its own unique characteristics. Particular physical synthesis algorithms and compiler settings performance improvements over standard compilation flows will vary from design to design. The Quartus II software version 3.0 now includes a new Design Space Explorer script that you can use to automatically apply many combinations of physical synthesis options and other compiler settings, seeking out the optimum settings for a given design. Design Space Explorer is fully configurable to maximize design performance or area and can be set to run for a few hours or a few days depending on your needs. The new settings reported by the Design Space Explorer can then be used for subsequent compilations to get the same optimum performance with much shorter compilation times.

Learn How to Get the Most from Quartus II Physical Synthesis Features

For complete details on Quartus II Physical Synthesis options and how to reach timing closure faster, download *AN 198: Timing Closure in the Quartus II Software* from the Altera web site.



Optimization Examples

Altera Devices & Tools

HardCopy

HardCopy: The Comprehensive ASIC-Alternative

HardCopy Stratix™ devices, the second-generation HardCopy devices, provide a complete solution from prototype to high-volume production. The Quartus® II software now supports HardCopy Stratix devices enabling you to design the HardCopy device directly to a mask-programmed device, with the ability to prototype the design in an equivalent FPGA before migrating to a HardCopy device. For more information on HardCopy devices, see "Get ASIC Gain without the Pain: Introducing the HardCopy Stratix Device Family" on page 4.

HardCopy devices are now available in logic element (LE) densities ranging from 16,000 to 80,000, or an equivalent of 200,000 to 1.5 million (includes 2,000 LEs per DSP block, calculated at 12 gates per LE) standard cell gates.

Table 1 shows the HardCopy Stratix availability.

Table 1. HardCopy Stratix Availability

Device	Package	Device Availability
HC1S25	672-Pin FineLine BGA®	Q1 2004
HC1S30	780-Pin FineLine BGA	Q2 2004
HC1S40	780-Pin FineLine BGA	Q2 2004
HC1S60	1,020-Pin FineLine BGA	October 2003
HC1S80	1,020-Pin FineLine BGA	October 2003

Altera has been shipping HardCopy APEX 20KC™ and HardCopy APEX 20KE™ devices in volume since 2001. See Table 2.

Table 2. HardCopy APEX 20KC & HardCopy APEX 20KE Availability

Device	Package	Device Availability
HC20K400	652-Pin ball-grid array (BGA) 672-Pin FineLine BGA	Now
HC20K600	652-Pin BGA 672-Pin FineLine BGA	Now
HC20K1000	652-Pin BGA 672-Pin FineLine BGA 1,020-Pin FineLine BGA	Now
HC20K1500	652-Pin BGA 672-Pin FineLine BGA 1,020-Pin FineLine BGA	Now

Cyclone

All Cyclone Devices Now Shipping in Production

All members of the Cyclone™ FPGA family are now production qualified and readily available from Altera distributors. Customers now have access to the lowest-cost, highest-volume FPGA solutions currently available in the market. With over 1,400 unique customers worldwide—having received devices since its introduction—Cyclone FPGAs are the fastest ramping products in Altera's history. See Table 3.

Table 3. Cyclone Device Availability

Device	Production Availability
EP1C3	Now
EP1C4	Now
EP1C6	Now
EP1C12	Now
EP1C20	Now

All Cyclone devices are now shipping in production volume. For less than $1.50 per 1,000 LEs for volume applications, you can begin designing for all Cyclone FPGAs using the free Quartus II Web Edition design software, Nios® embedded processors, and intellectual property (IP) cores.

Cyclone Advantages over Other Low-Cost FPGAs

Cyclone devices offer advantages over other low-cost FPGAs, including:

- *Production Availability*: Only production-qualified 0.13-micron low-cost FPGA family shipping today in high volume
- *Lowest Price*: Less than $1.50 per 1,000 LEs for high-volume applications
- *Highest Performance*: 60% faster than competing low-cost FPGAs
- *Differential Signaling*: LVDS signaling support at up to 640 Mbps
- *Hot-Socketing Support*: Insertion of an un-powered board into a powered system
- *Full 3.3-V I/O Support*: Full support for many 3.3-V single-ended I/O standards
- *3.3-V PCI Compliant*: Fully compliant with the 3.3-V PCI specification
- *Free Software Support*: Only low-cost FPGA family entirely supported in a free programmable logic design software tool
- *Free Evaluation of IP Cores*: Free test drive of IP functions that can be parameterized, compiled, and simulated using Altera's development tools

New & Enhanced I/O Standard

Cyclone FPGAs have raised the bar once again by supporting higher data transfer rates via the LVDS I/O standard as well as supporting the RSDS I/O standard. Cyclone FPGAs now support LVDS signaling at data transfer rates up to 640 Mbps per channel and RSDS signaling at up to 311 Mbps per channel.

What Customers are Saying about Cyclone FPGAs

"The price/performance ratio of Cyclone FPGAs allows us to keep PLD flexibility for the cost of an ASIC. Our adoption of Cyclone FPGAs has enabled us to implement unparalleled product programmability while still meeting our cost goals."

Tom Freeburg
Corporate Vice President and Director
Motorola Broadband Wireless Technology

Stratix

All Stratix Devices Now Shipping in Production

All Stratix™ devices have been qualified for production and are now shipping in volume quantities. EP1S10, EP1S20, EP1S25, EP1S30, EP1S40, EP1S60, and EP1S80 production devices are now shipping in all package and pin combinations. See Table 4.

Table 4. Stratix Device Availability

Device	Availability
EP1S10	Now
EP1S20	Now
EP1S25	Now
EP1S30	Now
EP1S40	Now
EP1S60	Now
EP1S80	Now

Industrial Grade Stratix Devices Now Shipping in Production

Industrial-grade Stratix devices are now available for volume production. Table 5 summarizes the different industrial codes available today.

Table 5. Stratix Industrial Ordering Codes & Availability

Industrial Device Ordering Code	Availability
EP1S10F484I6	Now
EP1S10F672I7	Now
EP1S10F780I6	Now
EP1S20F484I6	Now
EP1S20F672I7	Now
EP1S20F780I6	Now
EP1S25F672I7	Now
EP1S25F780I6	Now
EP1S25F1020I6	Now
EP1S30F1020I6	Now
EP1S40F1020I6	Now
EP1S60F1020I6	Now

continued on page 12

Stratix GX

Meeting the Challenges of High-Speed Systems

Faster ports and higher port densities on line cards has created a bottleneck in the backplane. Designers are faced with the task of redesigning backplanes or line cards to meet the high bandwidth demands of the system.

Altera can help. The Stratix GX device integrates high-speed transceivers and source synchronous I/O pins to reduce power, board real estate, time-to-market, and risk. Stratix GX devices feature the perfect combination of pre-emphasis and equalization creating robust transceivers for driving lossy backplane channels. Stratix GX devices have been proven to drive up to 3.1875 Gbps across 40 inches of FR-4 material and longer when both pre-emphasis and equalization are enabled.

Altera is now shipping all devices in the Stratix GX family. See Table 6 for Stratix GX device availability.

Table 6. Stratix GX Device Availability

Device	General ES Availability
EP1SGX10C	Now
EP1SGX10D	Now
EP1SGX25C	Now
EP1SGX25D	Now
EP1SGX25F	Now
EP1SGX40D	Now
EP1SGX40G	Now

Altera also offers the High-Speed Development Kit, Stratix GX Edition that includes a development board, layout files, schematics, design examples, and high-speed board layout guidelines to help you be successful.

Excalibur

Software Development Pack Now Part of Quartus II 3.0

The Quartus II software version 3.0 now ships with a supplemental CD-ROM specifically to support Excalibur™ devices. These include the SOPC Builder component for the ARM® processor and peripherals, the GNU software development tools, and reference designs and examples. This CD will install automatically during a Quartus II software version 3.0 standard installation, providing you with all of the resources to design with Excalibur devices. The CD will also install on PCs without the Quartus II software to allow deployment of the development tools to software engineers who do not need to access the hardware development tools.

Linux Provides Operating System Solution for Excalibur Devices

Altera has a partnership with MontaVista to provide a port of Linux to the Excalibur devices, including a Linux Support Package (LSP) based on the available peripherals on the Excalibur EPXA1 Development Kit. This system also includes a full TCP/IP protocol stack for the external 10/100 Ethernet MAC and the on-chip peripherals. This port is available as a preview kit to allow free evaluation of embedded Linux running on Excalibur devices prior to a purchase of MontaVista Linux Professional edition.

The preview kit and MontaVista Linux Professional Edition are available directly from MontaVista at **www.mvista.com**.

American Arium Ships Linux Kernel Debug Tools

American Arium has launched a new version of the SourcePoint debugger software SC-1000 Joint Test Action Group (JTAG) emulator that allows Excalibur device-based systems to be debugged via a single JTAG port. Also included in this release is support for debug of a Linux kernel without network connectivity or serial ports. All I/O requirements for the Linux kernel are supported via JTAG, removing the requirement to have an Ethernet solution or serial port on a production board, while still having the ability to debug a design in the development phase. Excalibur devices are supported by the KIT-XA4 development kit comprising a proprietary EPXA4 device-based development board, the Quartus II software, the ARM RealView® Development suite, and embedded Linux operating system support.

SourcePoint, SC-1000 JTAG emulator, and KIT-XA4 are available directly from American Arium at **www.arium.com**.

Nios Processor

Nios Development Kit, Stratix Professional Edition Now Shipping

The Nios Development Kit, Stratix Professional Edition provides all of the software and hardware tools necessary to create complete system-on-a-programmable-chip (SOPC) solutions. This kit includes the popular Nios processor version 3.1 and a development board featuring a Stratix EP1S40 device, 1-Mbyte SRAM, 16-Mbytes SDRAM, a CompactFlash connector, 10/100 Ethernet MAC/PHY device, switches, LEDs, and prototype connectors. The kit also ships with the powerful Quartus II design software version 3.0, including a one-year license and the GNUPro Toolkit—for all your embedded software development needs.

Also included in this high-end development kit is an advanced set of software debug features by First Silicon Solutions (FS2). The configurable Nios CPU features an option to use FS2's on-chip instrumentation (OCI) extensions. The Nios OCI debug module provides an in-circuit emulator feature set including run-control, hardware break points, watch points, on-chip trace, off-chip trace, and more. See "Nios Partner News" for more information regarding advanced debug add-ons available from FS2.

The Nios Development Kit, Stratix Professional Edition is priced at $2,495 and is available today.

For more information regarding this development kit, visit **www.altera.com/nios**.

Nios Partner News

In addition to the baseline OCI debug module included in all Nios development kits, FS2 offers several debug feature upgrade packages. These upgrade packages extend the capabilities of the ByteBlaster™ II download cable or add an ISA-NIOS BlackBox for a faster debug connection and a large off-chip trace buffer. These add-on features can be purchased online from FS2. For more information, go to **www.fs2.com/isa-nios**.

Accelerated Technology, the Embedded Systems Division of Mentor Graphics, has introduced their latest version of the code|lab Developer Suite. This suite includes the code|lab EDE tool (a full-featured integrated development environment for embedded systems development) and the code|lab debug tool. The code|lab Debug tool supports software debug of the Nios processor using FS2's system analyzer debug extensions. For more information regarding the code|lab Developer Suite, go to **www.acceleratedtechnology.com**.

Microtronix Datacom Ltd. is now supporting the Nios development kits with the µC/OS-II real-time operating system. The Microtronix µC/OS-II RTOS Development Kit provides:

- A stable and tested port of the kernel for the Nios embedded processor
- TCP/IP network stack library, and device drivers for several development boards
- MicroC/OS-II Second Edition, by Jean Labrosse
- Operating system component for the Altera SOPC Builder system development tool

The µC/OS-II real-time operating system is royalty-free. For more details, go to **www.microtronix.com**.

Convert your graphical state machine design into Nios processor–ready C/C++ code with the push of a button, using IAR Systems' visualSTATE for Altera Nios embedded processor tool. Find out more information at **www.iar.com**.

APEX II

APEX II Device Availability

All members of the APEX™ II device family are shipping. APEX II devices range in density from 16,640 to 67,200 LEs and are memory rich; they offer 4 Kbits of memory per embedded system block (ESB), with total device memory ranging from 416 Kbits to 1.1 Mbits. The APEX II device family supports high-speed data transfers through a wide range of high-speed I/O standards such as LVDS, PCML, LVPECL, HSTL, SSTL, and HyperTransport™ technology. With True-LVDS™ circuitry, APEX II devices can achieve data transfer rates of up to 1 Gbps per channel. Designers can take advantage of these I/O features by using APEX devices in the following applications:

- PHY-link layer interface applications (POS-PHY, Flexbus, and UTOPIA)
- Host-processor interface applications (HyperTransport technology, PCI, and PCI-X)
- Switch fabric interfaces (CSIX and LCS)
- External memory interfaces (DDR, zero-bus turnaround (ZBT), and quad data rate (QDR) memory devices)

continued on page 14

See Table 7 for APEX II device availability.

Table 7. APEX II Device Availability

Device	Package	Availability
EP2A15	672-pin FineLine BGA 724-pin BGA	Now
EP2A25	672-pin FineLine BGA 724-pin BGA	Now
EP2A40	672-pin FineLine BGA 724-pin BGA 1,020-pin FineLine BGA	Now
EP2A70	724-pin BGA 1,508-pin FineLine BGA	Now

APEX II Industrial Offerings

All the industrial-grade devices for the APEX II device family are now available. Industrial-grade production versions of the device offerings are available in a -8 speed grade. Table 8 shows the availability for industrial-grade offerings.

Table 8. APEX II Industrial Device Offerings

Device	Package	Availability
EP2A15	672-pin FineLine BGA	Now
EP2A25	672-pin FineLine BGA 724-pin BGA	Now Now
EP2A40	724-pin BGA 1,020-pin FineLine BGA	Now Now

Mercury

Mercury Devices Available in Production Mode

All devices and all speed grades of the Mercury™ device family are shipping in production mode, including industrial-grade offerings in both product lines (see Table 9). High-speed 1.25-Gbps serial links featuring clock data recovery (CDR) circuitry and an embedded serializer/deserializer (SERDES) make these devices ideal for serial backplane applications.

Table 9. Mercury Device Availability

Device	Package	Temperature Grade	Availability
EP1M120	484-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now
EP1M350	780-pin FineLine BGA	Commercial in -5, -6, -7 speed grade	Now
		Industrial in -6 speed grade	Now

APEX

All APEX Devices Available in Production Mode

All APEX 20KC, APEX 20KE, and APEX 20K devices and packages are now available. APEX devices offer complete system-level integration on a single device, providing tremendous breadth in density, I/O capability, and package options.

For new designs requiring high performance, use Stratix and Stratix GX FPGAs. These feature-rich FPGAs deliver top performance.

Industrial Grade APEX Device Offerings

Industrial-grade APEX devices are now available in a wide variety of package offerings. Refer to Tables 10, 11, and 12.

Table 10. APEX 20KC Device Industrial Offerings

Device	Package	Speed Grade
EP20K200C	484-pin FineLine BGA	-8
EP20K400C	672-pin FineLine BGA	-8
EP20K600C	652-pin BGA 672-pin FineLine BGA	-8
EP20K1000C	1,020-pin FineLine BGA	-8

Table 11. APEX 20KE Device Industrial Offerings		
Device	**Package**	**Speed Grade**
EP20K30E	144-pin FineLine BGA	-2X *(1)*
EP20K60E	144-pin FineLine BGA 208-pin PQFP 324-pin FineLine BGA	-2X *(1)*
EP20K100E	144-pin FineLine BGA 240-pin PQFP 324-pin FineLine BGA 356-pin BGA	-2X *(1)*
EP20K160E	484-pin FineLine BGA	-2X *(1)*
EP20K200E	240-pin PQFP 356-pin BGA 484-pin FineLine BGA 672-pin FineLine BGA	-2X *(1)*
EP20K300E	240-pin PQFP 652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K400E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K600E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*
EP20K1000E	652-pin BGA 672-pin FineLine BGA	-2X *(1)*

Note to Table 11:
(1) The "X" denotes phase-locked loop (PLL) and LVDS support.

Table 12. APEX 20K Device Industrial Offerings		
Device	**Package**	**Speed Grade**
EP20K100	208-pin PQFP 240-pin PQFP 324-pin FineLine BGA	-2V *(1)* -2V *(1)* -2XV *(1)*
EP20K200	240-pin PQFP 484-pin FineLine BGA	-2V *(1)*
EP20K400	652-pin BGA 672-pin FineLine BGA	-2V *(1)*

Note to Table 12:
(1) The "V" denotes 5.0-V tolerant I/O interfaces. The "X" denotes PLL support.

ACEX 1K

ACEX 1K Device Availability

ACEX® 1K devices are available in quad flat pack (QFP) and FineLine BGA packages in 576-, 1,728-, 2,880-, and 4,992-LE densities. These cost-optimized devices are specially suited for low-cost, high-volume applications. For mid- and high-density designs, see Altera's newest and lowest-cost Cyclone FPGA family on page 10.

Free software support for all ACEX 1K devices is available in the Quartus II Web Edition software version 3.0, which is available for download at **www.altera.com**.

MAX

MAX 3000A Supports Industrial & Extended Temperatures

Because they feature ease-of-use and flexibility, any designer can make use of the MAX® CPLD advantages. Altera's MAX CPLD family is the best selling CPLD in the industry for eight years straight. Altera continues to build on that leadership by extending CPLD benefits into new markets.

One example is the need for a lower cost industrial temperature CPLD family. Industrial temperature devices are no longer a solution only for the industrial market. Many communication and instrumentation customers benefit from the expanded operating temperature range of industrial devices. Industrial devices are also ideal for outdoor products with minimal protection from the elements. To satisfy this demand, Altera has expanded the MAX 3000A low-cost, high-volume family to include industrial devices rated at -40° to +105° C junction temperature. These devices are available now, as shown in Table 13.

Table 13. MAX 3000A Device Industrial Offerings	
Device	**Package**
EPM3032A	44-pin PLCC *(1)* 44-pin TQFP
EPM3064A	44-pin PLCC 44-pin TQFP 100-pin TQFP
EPM3128A	100-pin TQFP 144-pin TQFP 256-pin FineLine BGA
EPM3256A	144-pin TQFP 208-pin PQFP 256-pin FineLine BGA
EPM3512A	208-pin PQFP 256-pin FineLine BGA

Note to Table 13:
(1) PLCC: plastic J-lead chip carrier.

continued on page 16

As the automotive market becomes increasingly competitive, programmable logic provides product differentiation across models. To provide support for this growing market, Altera now provides its 3.3-V MAX 7000AE family with 5.0-V I/O support, qualified to extended temperature, from -40° to +130° C junction temperature (see Table 14). For details, see **www.altera.com/products/devices/temperature/tem-extended.html**.

Table 14. MAX 7000AE Device Extended Offerings

Device	Package
EPM7032AE	44-pin TQFP
EPM7064AE	44-pin TQFP 100-pin TQFP
EPM7128AE	100-pin TQFP 144-pin TQFP
EPM7256AE	144-pin TQFP 256-pin FineLine BGA

With these new additions to Altera's CPLD portfolio, Altera can offer the advantages of CPLDs with the additional flexibility of a wide range of temperature options from commercial to extended.

Configuration

Serial Configuration Devices

Altera's new serial configuration devices are the lowest-cost configuration devices in the industry, and provide the ideal complement to Cyclone FPGAs in addressing high-volume, price-sensitive applications. Engineered for maximum efficiency, serial configuration devices deliver features such as in-system programmability (ISP) and reprogramming capabilities at a cost even lower than one-time programmable (OTP) solutions.

Enhanced Configuration Devices

Enhanced configuration devices provide a complete single-device solution for a wide range of density requirements. Vertical migration capability allows you to easily migrate from the EPC4 to the EPC8 to the EPC16 device in the same package without having to change the board layout. Commercial and industrial grade EPC4, EPC8, and EPC16 devices are all now available.

Enhanced configuration devices offer ISP through a built-in IEEE standard for boundary-scan-based, in-system configuration standard of programmable devices (IEEE 1532). The inclusion of ISP and re-programmability provides a significant advantage over one-time programmable solutions by introducing flexibility and reusability to the configuration process.

Altera's enhanced configuration devices also introduce numerous features for specialized configuration needs. These features include an external flash interface that allows unused portions of the flash memory to be used as general-purpose memory, parallel configuration capability to accelerate configuration times, a new page mode that allows you to store multiple configurations, block protection for partial reprogramming support, and full clocking flexibility through the programmable clock and external clock features. This advanced feature set enhances the overall PLD design experience.

Quartus II

Quartus II Software Version 3.0 Shortens Design Cycles by 40%

A suite of new features in the Quartus II software version 3.0 shortens all phases of the design cycle, whether the software targets CPLDs, FPGAs, or HardCopy devices. This release includes a new HardCopy Stratix design flow that gives designers the industry's first and only design tool with a unified design flow for developing both FPGAs and mask-programmed devices from the beginning of a design cycle.

The Quartus II software version 3.0 shortens all phases of the design cycle with a suite of new features and enhancements, including:

- New Physical Synthesis and Design Space Explorer script provide automated features to increase the average design performance by 20%
- Up-front I/O assignment and validation
- Chip Editor feature to easily make incremental design changes
- Incremental fitting feature for small design changes reduces compilation times an average of 40% while maintaining design performance
- Updated Assignment Editor supports all device families and offers improved usability
- Enhanced LogicLock™ methodology so routing can be locked down in addition to logic placement
- Faster behavioral and timing simulation with ModelSim®-Altera version 5.7c

Experience the New HardCopy Stratix Design Flow: ASIC Gain Without the Pain

Using the Quartus II software version 3.0 designers can for the first time take the low-cost, easy-to-use tools, methodologies, and intellectual property (IP) they use for Altera's cutting-edge FPGAs and target the extremely high-performance mask-programmed HardCopy Stratix devices from the start of the design cycle.

Take Your Pick: GUI or Command-Line Operation

All major Quartus II software version 3.0 design flow functions can now be run independently from either the graphical user interface (GUI) or command line. In addition to Synopsys design constraint (SDC) script support, the Quartus II software supports a new tool command language (Tcl) application programming interface with simplified syntax to script custom design flows.

New Quartus II Software Literature

New or updated Quartus II software version 3.0 technical documents are now available on the Quartus II Literature page on the Altera web site, including:

- *Introduction to Quartus II*
- *Quartus II Support for HardCopy Devices Chapter of the HardCopy Device Handbook*
- *Engineering Change Order Support In Programmable Logic Design White Paper*
- *Pin Assignment & I/O Analysis Using the Quartus II Software White Paper*
- *Using the Assignment Editor in the Quartus II Software White Paper*
- *AN 310: Using the Quartus II Chip Editor*
- *AN 309: Command-Line Scripting in the Quartus II Software*
- *AN 307: Altera Design Flow for Xilinx Users*
- *AN 297: Optimizing FPGA Performance Using the Quartus II Software*
- *AN 280: Design Verification Using the SignalTap II Embedded Logic Analyzer*
- *AN 238: Using Quartus II Verilog HDL & VHDL Integrated Synthesis*
- *AN 198: Timing Closure Using the Quartus II Software*
- *AN 161: Using the LogicLock Methodology in the Quartus II Design Software*
- *Single & Dual-Clock FIFO Megafunctions User Guide*
- *Altera Double Data Rate Megafunctions User Guide*

New Device Support

The Quartus II software version 3.0 adds support for HardCopy Stratix, FLEX® 10K, FLEX 10KA, MAX 7000S, MAX 3000A industrial ordering codes, and two new MAX 3000A device packages. See Table 15.

Table 15. Quartus II Software Version 3.0 Additional Device Support

Support	Family	Device	Packages
Full support (includes Programmer Object File (**.pof**) generation)	HardCopy Stratix *(1)*	HC1S25	672-pin FineLine BGA
		HC1S30	780-pin FineLine BGA
		HC1S40	780-pin FineLine BGA
		HC1S30	1,020-pin FineLine BGA
		HC1S60	1,020-pin FineLine BGA
	Stratix GX	EP1SGX25	1,020-pin FineLine BGA
		EP1SGX25	672-pin FineLine BGA
		EP1SGX40	1,020-pin FineLine BGA
	FLEX 10K	All	All
	FLEX 10KA	All	All
	MAX 7000S	All	All
	MAX 3000A	EPM3128A	256-pin FineLine BGA
		EPM3256A	256-pin FineLine BGA

Note to Table 15:

(1) POF generation is only available for HardCopy Stratix prototype FPGAs. You can compile for the HardCopy Stratix devices to obtain a floorplan view and performance estimates of the final silicon implementation.

Quartus II Software Release Notes

To find out all of the major enhancements in Quartus II software releases, refer to the Quartus II Software Release Notes document. This document is available from the Literature section of the Altera web site at **www.altera.com/literature/rn/rn_qts.pdf** within one week after each release.

continued on page 18

Quartus II Web Edition Device & Feature Support Expanded

The free download of the Quartus II Web Edition software version 3.0 includes entry-level device support for all Cyclone and selected MAX devices and support for at least one device from every general-purpose FPGA and CPLD family, including the Stratix EP1S10 device. Version 3.0 adds support for MAX 7000S, FLEX 10K, and FLEX 10KA device families and additional MAX 3000A devices. See Table 16.

Table 16. Quartus II Web Edition Device Support

Device Family	Devices
Cyclone	Complete Device Support
Stratix	EP1S10
APEX II	EP2A15
ARM-Excalibur	EPXA1
APEX 20KE	EP20K30E EP20K60E EP20K100E EP20K160E
ACEX 1K	Complete Device Support
FLEX 10KE	EPF10K30E EPF10K50S EPF10K100E EPF10K130E EPF10K200S
FLEX 10K	Complete Device Support
FLEX 10KA	Complete Device Support
FLEX 6000	Complete Device Support
MAX 7000S	Complete Device Support
MAX 7000AE	Complete Device Support
MAX7000B	Complete Device Support
MAX 3000A	Complete Device Support

The following features are now included with versions of Quartus II Web Edition version 3.0:

- Enable/disable messages
- IBIS model generation
- Test bench generation from the Vector Waveform File (**.vwf**)
- PowerGauge™ power estimation
- Project archive feature
- STAMP model generation

New Quartus II Software Starter Suite CD is Now Available

The Quartus II Software Starter Suite CD-ROM includes all of the software necessary to start designing with Altera devices. Included on this CD-ROM are:

- Quartus II Web Edition FPGA and CPLD Design Software
- SOPC Builder Automated System Development Software
- Quartus II and HardCopy flash movie

You can request this CD-ROM as an option from the Quartus II Web Edition download page or by emailing **lit_req@altera.com**.

Programming Cables Now Available for USB & Parallel Port PC Connections

The new USB-Blaster programming cable supports all of the same features as the recently announced ByteBlaster™ II cable except that it connects to a PC via a universal serial bus (USB) connection instead of a parallel port connection. You can use both of these cables as a replacement for the ByteBlasterMV™ programming cable. The USB-Blaster and ByteBlaster II cable support all of the same programming features as the ByteBlasterMV cable and add the following new programming features:

- Support for active serial configuration mode to support the new EPCS1 and EPCS4 configuration devices
- Support for 1.8-V programming and configuration

The USB-Blaster and ByteBlaster II programming cables are both supported in the Quartus II software version 3.0. You can also download a stand-alone version of the Quartus II programmer feature from the Altera web site download center.

Implementing High-Performance DSP Designs With Precision RTL Synthesis

by Rakesh Jain
Mentor Graphics

Digital signal processing (DSP) is a rapidly growing technology with its applications spanning a wide variety of segments such as 3G wireless, software-defined radio (SDR), and video/image processing for the consumer electronics, entertainment, and medical systems markets. These applications cover a broad range of complexity, performance, cost, and time-to-market requirements. The challenge is to find a solution that meets these requirements.

A solution for implementation of DSP applications may be found in DSP processors or cores, ASICs, or FPGAs. DSP processors offer some flexibility, but lack the performance requirements of today's DSP applications. ASICs offer high performance, but are expensive to manufacture, require long lead times, and high-volume production. Therefore, an increasing number of DSP designers are turning to FPGAs for the flexibility of their architecture, high performance, lower costs, and faster time-to-market.

Among the various programmable devices that are available in the market today, Altera's Stratix™ devices offer many powerful features—dedicated DSP blocks, abundant memory resources, phase-locked loop (PLL) blocks, and high-speed I/O pins, making Stratix devices an ideal choice for DSP applications. However, efficient implementation of DSP applications using programmable logic devices requires utilization of all the specialized resources in FPGAs.

In an HDL-based design flow, you can choose to instantiate these special resources in the HDL code or rely on the synthesis tool to infer them. An ideal solution is for the synthesis tool to automatically infer DSP blocks, memory resources, and shift registers from generic HDL code. The synthesis tool must also understand and provide advanced capabilities to handle the complex timing requirements of high-performance DSP designs. The Mentor Graphics® Precision™ RTL Synthesis tool offers an ideal solution to meet your design's performance goals.

DSP Block Support

The most commonly used functions in DSP design are finite impulse response (FIR) filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT), direct cosine transform (DCT), encoder/decoder and error correction/detection. All of these blocks perform intensive arithmetic operations such as add, subtract, multiply, multiply-add, and multiply-accumulate. Stratix devices have dedicated DSP blocks that are optimized for implementing such arithmetic operations faster than purely logic-cell-based implementations.

Precision RTL Synthesis automatically infers the appropriate Altera® megafunctions: `altmult_accum`, `altmult_add`, or `lpm_mult` from the HDL code for implementation in the dedicated DSP resources. The following HDL code shows the inference of these megafunctions.

Among the various programmable devices that are available in the market today, Altera's Stratix devices offer many powerful features dedicated DSP blocks, abundant memory resources, phase-locked loop (PLL) blocks, and high-speed I/O pins, making Stratix devices an ideal choice for DSP applications.

VHDL code describing multiply-accumulate function

```
prod_result <= a * b;

process (clk)
  begin
    if (clk'event and clk = '1') then
      result <= result + prod_result;
    end if;
end process;
```

Verilog code describing multiply-add/subtract function

```
wire [17:0] mult1 = data_a * data_b;
wire [17:0] mult2 = data_c * data_d;
reg [17:0] data_out;

always @(posedge clk) begin
  if (add_mode)
    data_out <= mult1 + mult2;
  else
    data_out <= mult1 - mult2;
  end
```

TriMatrix Memory Support

Memory is another resource that is commonly used in DSP applications. Stratix devices provide abundant memory resources for memory-intensive applications. The largest Stratix device has over 7.5 Mbits of embedded memory, thus eliminating the need for external memory devices for many DSP applications. Its TriMatrix™ memory structure consists of three different sizes of embedded RAM blocks: 512-bit M512 blocks, 4-Kbit M4K blocks, and 512-Kbit M-RAM blocks. The memory blocks

continued on page 20

can implement true dual-port, simple dual-port, and single-port RAM, ROM, and first-in first-out (FIFO) blocks. Both M512 and M4K blocks can also be configured as shift registers. This option provides a more efficient implementation of shift registers than using standard registers, saving general logic and routing resources, resulting in higher performance for DSP applications.

Precision RTL Synthesis infers RAM, ROM, and first-in first-out (FIFO) blocks from generic HDL description and implements them in the appropriate Stratix memory blocks (M512, M4K, or M-RAM). It also infers shift registers and automatically implements them in the M512 or M4K memory blocks. The following example HDL code infers a dual-port RAM block and shift register and implements them using the `altsyncram` and `altshift_taps` megafunctions.

Together, Altera's Stratix devices and Precision RTL Synthesis provide a unique solution that meets the needs of today's high-performance and complex DSP designs.

VHDL code describing dual-port RAM

```
type mem_type is array (32 downto 0)
  of UNSIGNED(3 downto 0);
signal mem : mem_type;

begin
I0: process (clk_in)
  begin
    if (clk_in'event and clk_in = '1')
     then
      if (write_enable = '1') then
        mem(conv_integer(address_in))
              <= data_in;
      end if;
    end if;
end process I0;

I1: process (clk_out)
  begin
    if (clk_out'event and clk_out =
      '1') then
      data_out <= mem(conv_
              integer(address_out));
    end if;
end process I1;
```

Verilog code describing shift register

```
assign shiftout = D;

always @(posedge clock)
begin
    A <= shiftin;
    B <= A;
    C <= B;
    D <= C;
end
```

Stratix PLL Support

Stratix devices offer highly versatile PLL blocks. These high-performance clock management blocks offer many features that were previously found only in high-end discrete PLL devices. The most common uses of the PLL are for clock multiplication and clock division. In an HDL-based design flow, the PLL megafunction component is instantiated in the HDL code and its properties are defined by the parameters.

Precision RTL Synthesis is unique in the industry, because it detects the clock and automatically calculates its intended output value based on the parameters passed along with the instantiated PLL component. Automatic propagation of a clock through the PLL results in better synthesis results, due to the availability of valid constraints, and also increases the accuracy of timing analysis.

Advanced I/O Support

Today's complex DSP applications need high-speed I/O standards to achieve high data transfer rates. To handle this requirement, Stratix devices support a variety of single-ended and differential I/O standards such as LVDS, LVPECL, PCML, PCI, and the RapidIO™ standard. It also provides interfaces to microprocessors, peripherals, gate arrays, and external memory devices such as double data rate (DDR) SDRAM, DDR fast-cylce RAM (FCRAM), and zero-bus turnaround (ZBT) SRAM.

Precision RTL Synthesis offers a convenient method to choose and set a desired I/O standard, drive strength, and slew rate on the ports of your choice using the graphical user interface (GUI) or attributes. Precision RTL also has the capability to automatically use the Stratix I/O registers, based on the timing requirements of your design. Therefore, it gives you the best overall performance for your design.

Conclusion

Mentor Graphics' Precision RTL Synthesis has a detailed understanding of the Stratix architecture. It offers an optimal solution for implementation of DSP applications in FPGAs. Together, Altera's Stratix devices and Precision RTL Synthesis provide a unique solution that meets the needs of today's high-performance and complex DSP designs.

Straightforward DDR SDRAM Connection to FPGAs Using IP

Double data rate (DDR) SDRAM is now the most popular memory type for designers of embedded applications needing large amounts of low-cost, high-performance memory. It provides a performance boost over single data rate (SDR) SDRAM using extra interface logic that doubles the raw bandwidth of the data path by clocking data on both edges. Due to widespread adoption by the PC industry, and improved long-term availability over SDR SDRAM, it also makes good commercial sense for use in today's applications.

Today's system-on-chip (SOC) designs with large external RAM requirements need to support a DDR SDRAM interface. System-on-a-programmable-chip (SOPC) designs utilizing FPGA technology are no different (apart from being accessible to all designers without non-recurring engineering (NRE) barriers).

The requirements for connecting to DDR SDRAM can be broken down into two categories: electrical and timing. Electrically, SSTL-II single-ended I/O must be supported at 2.5 V for data and control signals, and a 2.5-V differential clock signal must also be supported. FPGAs can easily support these requirements; however, timing presents more of a challenge, especially with data being transferred on both edges of the clock. This extra challenge means that I/O cells must be capable of running at twice the frequency of the clock. You can do this by doubling the number of registers such that the I/O cell is able to latch data on both clock edges. The alternative is to run the I/O cell at double the clock rate, and use general-purpose logic to separate the data on the rising and falling edges of the clock. The Stratix™ device family includes six registers and supports up to 200 MHz (400 megabits per second (Mbps)) DDR SDRAM connection. Cyclone™ devices include three registers per I/O cell but still support up to 133 MHz (266 Mbps) DDR SDRAM operation.

Perhaps the most challenging timing requirement of connecting DDR SDRAM is presented by the DQS pin. The DQS pin is a bidirectional strobe used for clocking the data on the DQ lines. The problem is that, depending on whether the SDRAM is being read from or written to, both the strobe direction and timing are different. When reading from DDR SDRAM, the phase of the DQS signal should be shifted 90° to make sure the data is being captured from the center of the window. It is possible to insert external fixed delays to help this, such as using an extended printed circuit board (PCB) track relative to the DQ lines, but this method has several problems. First, because the DQS pin is bidirectional, any delay included to ensure correct read operation will then need removing from the write phase. This means the write data clock may then also need shifting, requiring an extra clock phase. Depending on the flexibility of the on-chip clock managers, it may not be possible to provide this without an extra clock source, which uses further on-chip resources.

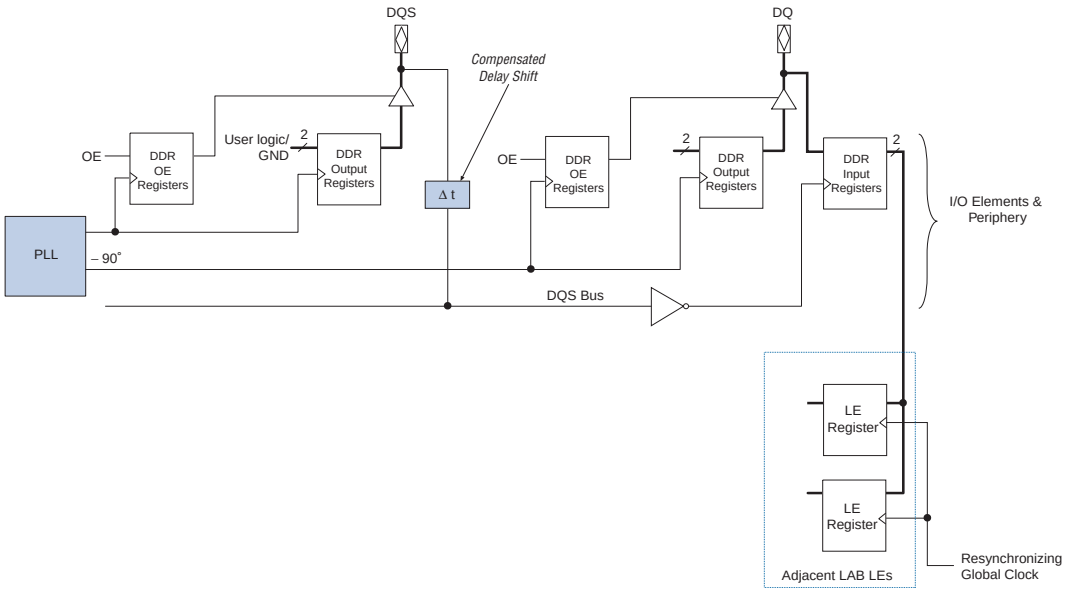
Using extended PCB traces can also cause problems when PCB routing is limited, and in extreme cases, it can force the use of extra PCB layers. The amount of extra trace needed to be added to the DQS line will depend on frequency; signals propagate at around 166 ps per inch on a FR-4 PCB. For DDR SDRAM running at 100 or 200 MHz, an additional 7 to 15 inches of track length per DQS may be required. Also, it is often necessary to develop a system that can work at reduced clock frequencies, particularly during development. Fixed delay elements will only provide the correct phase shift at a single frequency, making de-rating or prototyping at lower frequencies challenging.

To address this problem, Altera's Stratix™ and Cyclone devices have built-in dedicated support for delayed DQS read samplings. This support not only makes it easy to meet timing over process, voltage, and temperature variations, but also minimizes general-purpose resource usage in the FPGA such as logic elements (LEs) and phase-locked loops (PLLs). The key is that the delayed DQS input signal directly clocks the input registers of the DQ pins. Inclusion of this simple feature solves a huge headache for designers connecting not only DDR SDRAM, but many other high-speed memory types.

Several clock sources are needed for a DDR SDRAM controller and the memory devices. These include the differential SDRAM clock, core system clock, write data clock, and possibly a read capture clock depending on round-trip timing. Using simple delay-locked loops (DLLs) with limited outputs can mean instantiating up to three such blocks to meet the required timing. In most cases, a single Stratix or Cyclone PLL provides all of these due to the large number of individually configurable outputs.

Once it is established that the FPGA supports the correct functionality to connect to DDR SDRAM, it is necessary to prove that the memory controller and all external signals pass the timing analysis. Today's high-performance FPGAs can support 200-MHz system speeds, and synchronous I/O speeds approaching 1 gigabit per second (Gbps). However, ensuring your DDR memory controller meets the specification still requires the appropriate placement within the FPGA and I/O banks, as well as PCB layout and timing analysis.

continued on page 22



Dedicated Stratix DQS Delay Circuitry

You must consider four categories of timing analysis: write data timing, address, command timing, and read capture using DQS and the resynchronization of captured read data to the system clock domain. By using a known working reference design based around an IP core, and by following the accompanying documentation, meeting timing requirements is straightforward.

In addition to the high-speed data path, the DDR SDRAM state machine must be correctly implemented, and care must be taken for proper initialization and refresh of the DRAM cells. Since DDR SDRAM is defined by a JEDEC standard, the memory controller must also be compliant with the JEDEC standard. If you want the flexibility of specifying different DDR SDRAM configurations and sources, further testing must be done.

When using an application-specific standard product (ASSP) with DDR SDRAM support, once the memory has been correctly initialized, the application can simply treat the DDR SDRAM as a block of memory in the memory map. In an SOC or SOPC application with a well-designed DDR SDRAM controller, this will also be the case, except you must also consider how to internally connect the memory controller to internal buses. The most straightforward way of doing this is by using an SRAM-type interface (address, data, and strobes) with arbitration signals. The Altera DDR SDRAM controller IP core provides this, and solves all of the problems that have been discussed previously by providing an off-the-shelf, fully tested solution.

Each designer of a system including DDR SDRAM may have slightly differing requirements. One designer may wish to use a single low-cost, 16-bit wide discrete DDR SDRAM device, while another might favor a full 64-bit DIMM interface to support off-the-shelf DIMM modules and future upgrades. Depending on the memory device(s) selected, it can be necessary to support multiple chip selects and varying numbers of address lines. Other variables include column address strobe (CAS) latency and refresh periods; hence, any memory controller IP used must be fully parameterizable. The Altera DDR SDRAM IP core is shipped as a graphically parameterizable software package that generates VHDL source and reference designs for project inclusion.

The logic usage for a 32-bit DDR SDRAM interface in Cyclone devices is around 1,000 logic elements (LEs) and 800 LEs in Stratix devices. Using Stratix devices, even a full 64-bit interface, consumes only 1,000 LEs. Therefore, the overall system cost is kept extremely low.

Conclusion

The use of DDR SDRAM controller IP in conjunction with FPGAs designed with DDR SDRAM support features enable the designer to concentrate on the rest of the system, saving time and maximizing the possibility of success the first time.

You can use a free OpenCore® evaluation of the DDR SDRAM controller at by downloading it from the Altera® web site at **www.altera.com**. The OpenCore evaluation allows you to perform a functional simulation of the IP, place-and-route, and static timing analysis.

Altera University Program

Altera's commitment to education goes far beyond that of most companies our size. The programmable nature of Altera's devices make them ideal for educational uses. To promote education, the Altera® University Program has been working with schools worldwide for most of the company's 20 years. Five years ago, the program stepped it up a notch with the introduction of the UP1 development board, specifically targeted to undergraduate education. The first UP1 boards featured the MAX® EPM7128 CPLD and the FLEX® EPF10K20 FPGA and were programmed with the MAX+PLUS® II software. This original board has appeared in countless class projects and in dozens of textbooks worldwide.

Two years ago, the very successful UP1 became the UP2 (Altera just celebrated its 20,000th unit delivered this month), including the FLEX EPF10K70 FPGA and the addition of a power supply, cables, and a textbook written by two professors at Georgia State University. In July 2003, Altera upgraded the package again with the transition to the Quartus® II Web Edition software, giving students (and educators) experience with world-class Altera tools that they will be using well after graduation.

University Program Growth

The Altera University Program has grown dramatically in the past two years with the adoption of three basic principles:

First, Altera offers educational institutions the exact development kits, devices, and tools that are currently selling to commercial customers. In the case of development kits, Altera drastically reduced the price so all schools worldwide could have access to cutting-edge hardware, software, and intellectual property (IP). Devices are the backbone of hundreds of university undergraduate and graduate programs. Altera offers the best devices (Stratix™ and Cyclone™ FPGAs) to schools at little or no charge. Altera also sets up all schools in the program with the full version of the Quartus II software.

Second, Altera provides graduate- and post-graduate level research in the form of development kits and device grants. Altera's engagement at this level in the past two years has grown to include over two dozen universities in almost as many countries.

Third, Altera maintains active communication with schools to provide us with a basis for recruiting top students. Approximately six times a year, Altera hosts groups of graduate students at the San Jose facility. These students have traveled to Altera from China, Italy, Germany, and Canada, in addition to several schools in the United States.

The Altera University Program is on a steady growth curve and is expanding with additional resources focusing on growth in the Asia Pacific Region. In the fall of 2003, the program will increase its visibility with an exclusive focus on the Quartus II software as the primary teaching tool. Also, several design contests will be held to challenge students at all levels using Altera's popular Nios® Development Kit, Cyclone Edition.

Conclusion

While the numbers of universities, professors, and students in the program is Altera confidential, it is possible to say that the program has grown by a factor of three in all categories. Engaging with educators at the same high standard that we use with commercial customers has made this program very successful.

Introducing Altera Handbooks–One-Click Access to Product Documentation

To improve access to technical documentation, Altera has introduced product handbooks. Organized by function and feature rather than document type, you can download comprehensive product handbooks from the Altera® literature web site (**www.altera.com/literature**) with a single click, or get just the specific handbook sections you need.

Commencing with the Stratix™, Cyclone™, HardCopy™, and Configuration Device Handbooks, Altera will offer product handbooks for its flagship device families, development tools, and embedded processor solutions, as well as application-based volumes on a variety of subjects. See Table 1.

In addition, printed handbooks are available at **www.ShopAltera.com**, a new e-commerce service developed to provide overnight access to always up-to-date printed technical product documentation. Taking advantage of print-on-demand technology, Altera product handbooks are printed, bound, and shipped as quickly as 24 hours from order placement.

"Altera's new print-on-demand service delivers the substantial usability advantages of printed technical documentation without the traditional downside risk of buying out-of-date information," said Tim Southgate, VP of Corporate Marketing at Altera. "Customers can be confident that the handbooks they order contain the latest technical product information."

Table 1. Stratix, Cyclone & HardCopy Handbooks

Device Family Handbooks	Description
Stratix	*Volume 1*: Stratix FPGA Family Data Sheet, including feature definitions, configurations and testing information, DC operating conditions, AC timing specifications, power consumption, and ordering information.
	Volume 2: Detailed information on how to use Stratix features, IP functions, and supported configurations modes.
	Volume 3: Device pin tables, PCB layout guidelines, and package specifications.
Cyclone	*Volume 1*: The Cyclone FPGA Family Data Sheet and detailed information on how to use Cyclone features, IP functions and supported configurations modes.
	Volume 2: Device Pin tables, PCB layout guidelines, and package specifications.
HardCopy	Comprised of the HardCopy Stratix and HardCopy APEX 20K Data Sheets, Hardware Design Considerations, and Software Support.
Configuration	*Volume 1:* Configuring Stratix and Stratix GX Devices, Configuring Cyclone FPGAs, Configuring APEX II Devices, Configuring APEX 20KE and APEX 20KC Devices, Configuring Mercury, APEX 20K (2.5 V), ACEX 1K and FLEX 10K Devices.
	Volume 2: Enhanced Configuration Devices (EPC4, EPC8 & EPC16) Data Sheet, Using Altera Enhanced Configuration Devices, Serial Configuration Devices (EPCS1 & EPCS4) Data Sheet, Configuration Devices for SRAM-Based LUT Devices Data Sheet, Device Configuration Options, Configuration File Formats, Configuring Mixed Altera FPGA Chains, Combining Different Configuration Schemes, Using Flash Memory to Configure FPGAs, and Debugging Configuration Problems.

Free SOPC World 2003 Conference: Your Roadmap to the Future

Dramatic cost reductions, unprecedented performance, and design simplicity have made programmable logic a compelling alternative to traditional system design techniques, especially in embedded design, digital signal processing (DSP), signal interfacing/bridging, and designs with high-speed signaling. For an instructive and intriguing look at how you can benefit from the industry's most advanced programmable solutions, attend Altera's free SOPC World 2003.

PLD WORLD 2003

Altera's SOPC World 2003 will be held from September to November 2003 in over 20 cities worldwide, including Altera Japan's PLD World in Tokyo on October 17. This year's lineup will offer free detailed technical sessions analyzing several key system design challenges and solutions, including:

- Developing custom peripherals and instructions for embedded programmable processing
- Solutions for high-speed systems
- Simplifying system design and integration using the powerful SOPC Builder tool
- FPGA co-processors for DSP
- Plus an advance look at Altera's three new product families coming in 2004

Demo Village

SOPC World 2003 will also have many hands-on demonstrations exhibiting effective solutions from Altera and its partners, such as communicating with 200-MHz double data rate (DDR) memories, boosting DSP performance of system processors, and transferring data at speeds as high as 3.125 Gbps.

Come see how Altera can help you break through boundaries, propel innovation, and quickly drive your vision to reality. See Table 1 for SOPC World 2003 dates and locations. To find out more and to register for SOPC World 2003, go to **www.altera.com/sopcworld**.

Altera to announce three significant new product families during SOPC World 2003

Table 1. SOPC World 2003 World-Wide Dates & Locations

North America		Europe		Asia	
Dates	**Locations**	**Dates**	**Locations**	**Dates**	**Locations**
September 30, 2003	Richardson, TX (Dallas)	October 30, 2003	Milan, Italy	October 15, 2003	Shanghai, China
October 1, 2003	Irvine, CA	November 4, 2003	Munich, Germany	October 20, 2003	Beijing, China
October 2, 2003	Manhattan Beach, CA (Los Angeles)	November 6, 2003	Stuttgart, Germany	October 28, 2003	Hsinchu, Taiwan
October 6, 2003	Toronto, ON Canada	November 11, 2003	Kista, Sweden	October 30, 2003	Seoul, South Korea
October 7, 2003	Chelmsford, MA (Boston)	November 13, 2003	Espoo, Finland	November 5, 2003	Bangalore, India
October 8, 2003	Edison, NJ	November 18, 2003	Paris, France		
October 9, 2003	Cary, NC (Raleigh)	November 20, 2003	Bedfordshire, UK		
October 10, 2003	Bethesda, MD				
October 21, 2003	Broomfield, CO (Denver)				
October 28, 2003	Oakbrook Terrace, IL (Chicago)				
November 6, 2003	Santa Clara, CA				

Altera Training

Altera® Technical Training empowers you to design the most efficient system-on-a-programmable-chip (SOPC) solutions by ensuring your skills are up-to-date with the latest tools and technology. Altera courses show you how to take advantage of the newest features in Altera's Quartus® II software version 3.0 and related EDA tools to achieve the highest performance and smallest footprint designs—resulting in cost savings and faster time-to-market. Digital signal processing (DSP) applications, embedded processor systems, and high-speed designs are a few areas of focus within Altera's course catalog, demonstrating Altera's commitment to provide courses that meet specific customer needs.

Hands-On Experience

Hands-on experience is the best way to learn a new skill; therefore, laboratory exercises are a key part of every training class. Many classes enable you to test what you learn in hardware on an Altera development board. When you attend the DSP Series Part I or DSP Series Part II technical training class, you can receive a 20% discount on any DSP development kit to continue your development. Similarly, you will receive a 20% discount on any Nios® Development Kit by attending a Nios or SOPC technical training class. See Table 1 for some of Altera's most popular classes.

If you are considering purchasing a Nios or DSP development kit before attending a class, you will find a coupon included in the kit for a 20% discount on any one instructor-led Altera Technical Training course in North America. Altera is committed to making it as easy as possible for you to achieve your design goals.

Visit **www.altera.com/training** and register for a class today.

Table 1. Popular Altera Courses

Course Name	Duration	Course Type	Suggested Resale Price Per Student
DSP Design Series Part I: Implementing DSP Designs in FPGAs	8 Hours	Instructor-Led	$495
DSP Design Series Part II: Using FPGAs to Architect and Optimize a DSP System	8 Hours	Instructor-Led	$495
Designing with Nios & SOPC Builder	8 Hours	Instructor-Led	$195
Designing a System on a Programmable Chip	8 Hours	Instructor-Led	$495
Designing with Quartus II	8 Hours	Instructor-Led	$195
Designing with Synplicity Synplify Pro & Altera Quartus II Software	8 Hours	Instructor-Led	$195
Analyzing Designs Using Model Technology's ModelSim & Altera's Quartus II Software	8 Hours	Instructor-Led	$195
Designing with Cyclone Devices	8 Hours	Instructor-Led	$195
Fundamental Design Techniques for Stratix Devices	8 Hours	Instructor-Led	$195
Advanced Design Techniques for Stratix Devices	8 Hours	Instructor-Led	$195
Using Intellectual Property & Optimizing Stratix Designs	8 Hours	Instructor-Led	$495
Introduction to VHDL	8 Hours	Instructor-Led	$195
Advanced VHDL Design Techniques	8 Hours	Instructor-Led	$495
Introduction to Verilog HDL	8 Hours	Instructor-Led	$195
Advanced Verilog Design Techniques	8 Hours	Instructor-Led	$495

HardCopy Questions & Answers

Q *How is Altera's HardCopy™ device family different than similar offerings from other vendors?*

A Altera's HardCopy device family is the only product that provides a complete path from prototype to production. Unlike competing solutions that require multiple vendors, Altera provides the FPGA, the development tools, the intellectual property (IP) cores, and the seamless migration path from the function-verified prototype device to a high-volume production device with minimal risk and rapid time-to-market benefits. The designer uses the same easy-to-use, low-cost design tools from FPGA to production. There is no need to re-synthesize designs during migration unlike other offerings in the marketplace. This minimizes the risk of creating a new design and guarantees first-time success.

Q *Does Altera guarantee that the timing of a HardCopy device is the same as an FPGA?*

A Yes, Altera guarantees that HardCopy timing parameters are within the worst-case FPGA parameters.

This means that individual HardCopy timing paths will be equal to or faster than the corresponding timing path on the FPGA. However, all timing paths do not necessarily speed up by the same percentages, so you should avoid significant asynchronous designing.

Q *What kind of performance improvements can I expect to achieve with a HardCopy device?*

A By migrating to a HardCopy device, design performance can increase on average 50% over the performance in an equivalent FPGA. The HardCopy device performance improvement is design-dependent. Altera guarantees that the HardCopy design performance will either be equal to or greater than the performance in the equivalent FPGA. You can use the HardCopy Timing Optimization Wizard in the latest version of the Quartus II design software to estimate design performance in a HardCopy Stratix device.

Q *Can the HardCopy Timing Optimization Wizard be used to estimate and optimize the performance of HardCopy APEX 20KC™ and HardCopy APEX 20KE™ devices?*

A The HardCopy Timing Optimization Wizard can only be used to estimate and optimize performance of a HardCopy Stratix™ device. However, a designer can contact the Altera® HardCopy Design Center to receive a performance estimate for a HardCopy APEX 20KC and HardCopy APEX 20KE device. This information is available one week after the design is submitted for migration.

Q *Do HardCopy devices consume less power than equivalent FPGAs? If so, what is the power consumption rate?*

A Yes, HardCopy devices typically consume on average 40% less power than their equivalent FPGAs. The reduction is dependent upon the design parameters. You can use the HardCopy APEX power calculator and the HardCopy Stratix™ power calculator to determine a design's power consumption before generating the design deliverables for migration.

Q *Is I/O electrical performance the same in HardCopy devices as in the equivalent FPGA?*

A Yes, the HardCopy device I/O electrical performance is the same as its equivalent FPGA. This enables you to retain the system board used for FPGA design and guarantees the same board performance when the FPGA is replaced with a HardCopy device.

Q *How is testability addressed in HardCopy devices?*

A HardCopy base arrays are embedded with testability circuits. Boundary insertion scan test (BIST) circuits for memories and phase-locked loop (PLL), and boundary scan logic for the design are available in all HardCopy devices. Altera's HardCopy devices do not require any functional vectors from customers. Using automatic test pattern generation (ATPG) vectors, HardCopy devices are tested on the structural design resulting in very high fault coverage of ~99%.

continued on page 28

Q *How is the FPGA configuration feature handled in the HardCopy device?*

A The FPGA configuration circuitry does not interfere with the HardCopy device. HardCopy devices can either power-up instantly like an ASIC or can emulate the configuration process of the FPGA. This enables you to retain the system board used with the FPGA with no need to make costly design changes or modify the configuration device software.

Q *Is it possible to combine multiple FPGAs into one HardCopy device?*

A While there is no direct conversion available for this, you may convert multiple smaller FPGAs into a single, larger device. Once you have verified functionality and timing in your new device, you may migrate to a HardCopy device.

Q *What tools do I need to design for Altera's HardCopy devices?*

A You can use the Quartus® II software version 3.0, the same easy-to-use software used to design FPGAs, to design for Altera's HardCopy devices. No additional tools are required.

Q *What is the HardCopy Files Wizard in the Quartus II software?*

A The HardCopy Files Wizard, a push-button feature in the Quartus II design software, generates the entire design database to be transferred to HardCopy devices. This feature also asks for user input about the design, which is used during the migration process.

Q *What is the Design Assistant in the Quartus II software? Why is it important to check the design database with Design Assistant?*

A The Design Assistant, a feature in the Quartus II design software, verifies that a design meets industry-standard design rules. Any violations will be reported to the designer before the database is transferred to the Altera HardCopy Design Center for migration. The designer has to fix any violations before the design is migrated. This process guarantees first-time success.

Q *What deliverables should be provided to Altera for migration to HardCopy devices?*

A You must submit FPGA design files (**.sof**), timing constraints, and pin assignment files from the Quartus II software. These deliverables can be generated using the HardCopy Files Wizard feature. The Altera HardCopy Design Center handles the migration process.

Q *What happens to the unused I/O pins in a HardCopy device during boundary scan?*

A In Altera FPGAs, the unused I/O pins are always connected to the Joint Test Action Group (JTAG) chain. However, the boundary scan order is not the same. Therefore, specific boundary-scan description language (BSDL) files are necessary for HardCopy devices.

Q *Can Altera provide me with a gate-level HardCopy netlist for functional verification?*

A Yes, Altera can provide you with a final HardCopy device netlist and standard delay file (**.sdf**) for verification. However, this is not required to guarantee migration.

Q *Can IP cores be migrated to HardCopy devices?*

A Yes, both Altera's in-house designed MegaCore® and third-party-developed Altera Megafunction Partner Program (AMPP^{SM}) IP cores used in the FPGA design can be migrated seamlessly to a HardCopy device. With AMPP cores, however, there may be an additional license fee.

Q *Can the Nios® embedded processor be migrated to HardCopy devices?*

A Yes, Altera's popular Nios embedded processor can be migrated to HardCopy devices. No royalties or additional license fees are required.

Q *By migrating an FPGA design to a HardCopy device, is the die size reduced?*

A Yes, since the programmability is removed, the die size is reduced by as much as 70% in a HardCopy device compared to its FPGA counterpart. This results in significant performance gains and power reduction.

Discontinued Devices

Altera will obsolete select devices from product-term and FPGA families (see Table 1). Most devices will have a 12 month last time buy period and an additionasl 6 month last time ship period to allow customers to transition to using new components and ordering codes.

Table 1. Discontinued Device Update

Product Family	Device	Last Order Date	Last Shipment Date
MAX® 7000	Selected Devices	10/31/04	04/30/05
MAX 7000A	Selected Devices	10/31/04	04/30/05
MAX 7000B	Selected Devices	10/31/04	04/30/05
MAX 7000S	Selected Devices	10/31/04	04/30/05
FLEX® 10KA	Selected Devices	10/31/04	04/30/05
FLEX 10KE	Selected Devices	10/31/04	04/30/05
FLEX 6000	Selected Devices	10/31/04	04/30/05
FLEX 8000	Selected Devices	10/31/04	04/30/05
APEX™ 20K	Selected Devices	10/31/04	04/30/05
APEX 20KE	Selected Devices	10/31/04	04/30/05
ACEX® 1K	Selected Devices	10/31/04	04/30/05
Configuration Devices	Selected devices from the following device families: EPC1064, EPC1064V, EPC1213, and EPC1441	10/31/04	04/30/05

Contact Information

It is now easier than ever to get information and services from Altera. The table below lists some of the ways you can reach Altera.

Information Type	U.S. & Canada	All Other Locations
Product Literature	**www.altera.com**	**www.altera.com**
Altera Literature Services *(1)*	**lit_req@altera.com**	**lit_req@altera.com**
News & Views Information	**www.altera.com/literature/nview.html** **n_v@altera.com**	**www.altera.com/literature/nview.html** **n_v@altera.com**
Non-Technical Customer Service	(800) 767-3753	(408) 544-7000
Technical Support	**www.altera.com/mysupport**	**www.altera.com/mysupport**
	(408) 544-6401	(408) 544-6401 *(2)*
FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	(408) 544-7104	(408) 544-7104 *(2)*
	www.altera.com	**www.altera.com**

Notes:

(1) The ***Quartus II Installation and Licensing***, ***Introduction to Quartus II***, and ***MAX+PLUS II Getting Started*** manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.

(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for the latest listing.