News & Views

First Quarter 2004

Newsletter for Altera Customers

Innovation to the Power of *II*

ALTERA

NV-2004-Q1

Altera's Legacy of Innovation Lives On

Innovation has been the cornerstone of the semiconductor industry. Constantly challenged by Moore's law, Metcalf's Law, Gilder's Law, and other phenomena, we thrive when faced with seemingly daunting and insurmountable challenges. Time and time again, through pure genius and just plain entrepreneurial drive, we as an industry have overcome dire predictions and consistently raised the technology bar. At Altera, this passion and burning desire to break barriers and set new standards is in our blood.

As we conclude our twentieth anniversary, we ring in our twenty-first year with the introduction of new architectures that represent significant breakthroughs in programmable logic technology. Just as we've reached new heights in performance, density, and cost over the past two years, we are now launching two new families: Stratix™ II and MAX® II devices—the industry's largest and fastest FPGAs and the lowest-cost CPLDs—once again pushing the envelope of product leadership.

With the intent of expanding FPGA penetration beyond traditional PLD applications within a system, our engineers took a fresh look at the nearly fifteen-year-old 4-input look-up table (LUT) structure and developed the Stratix II family. Based on an innovative new logic structure, Stratix II devices deliver much greater levels of integration and performance that now give you even more compelling reasons to exploit the flexibility and time-to-market capabilities of FPGAs. For example, Stratix II devices have significant memory and performance bandwidth that makes them ideal for data processing on high-performance line cards in a broad range of routers and edge switchers. Or, for wireless base station applications, we've made significant improvement to performance features that make Stratix II devices ideal for VoIP gateways. Many other applications that were once exclusively ASIC territory are now addressable by Stratix II devices. Our intent is to make Altera a larger part of your bill of materials. Significant savings are realized in overall system and supply chain costs, while risk is also substantially reduced.

Altera maintains the CPLD market leadership it has held for more than ten years, led by the MAX 7000 architecture, introduced in 1991. Purchased annually by over 10,000 customers around the globe, MAX devices populate a multitude of systems, performing functions anywhere from glue logic to bus bridging, power-up sequencing, device configuration, and I/O expansion. With the introduction of MAX II devices, we've redefined the CPLD architecture to deliver much greater densities at unheard of prices. Ultimately, MAX II devices will not only address traditional CPLD applications, but will also find their way into applications that small ASSPs and standard logic devices used to address.

This quarter, we treat you to a special issue of *News & Views* to give you an in depth look at the Stratix II and MAX II families. As we pave our path towards the next twenty years, our mission remains clear—to deliver high-value programmable solutions to our customers. To that end, our focus and commitment to continuous innovation only gets stronger. We're not done innovating at Altera—not by a long shot.

Erik Cleage,
Senior Vice President of Marketing

MAX II CPLDs

Stratix II FPGAs

Quartus II Version 4.0

Features

Devices & Tools

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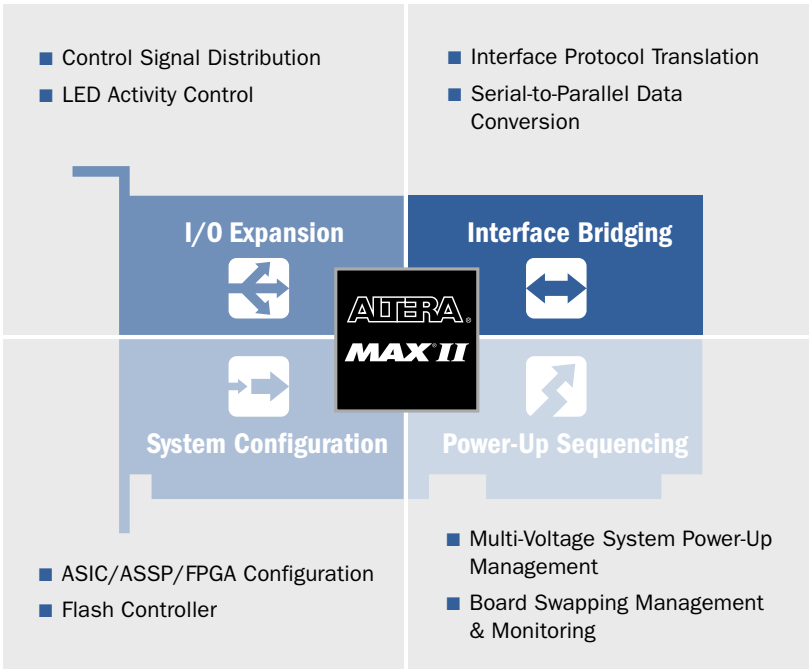
MAX II—The Lowest-Cost CPLD Ever

Building on more than a decade of CPLD leadership and innovation, Altera introduces the MAX® II device family, the lowest-cost CPLDs ever. MAX II devices are based on a groundbreaking new CPLD architecture that delivers the lowest cost and the lowest power consumption of any CPLD family. At less than half the price of other CPLDs, this instant-on, non-volatile device family targets general-purpose, low-density logic applications. In addition, MAX II devices extend cost and power improvements to higher densities, enabling designers to use MAX II devices in place of higher-cost or higher-power ASSPs, ASICs, and standard logic devices.

CPLDs are commonly used for control path applications (see Figure 1) in a wide range of electronic systems. These applications require more performance and density than macrocell-based CPLDs can cost-effectively deliver. As a result, engineers building complex systems often use ASICs and ASSPs. However, these alternatives complicate design because they lack the flexibility, ease-of-use, and low cost that are critical to these applications.

Figure 1. CPLD Application Areas



Because ASICs and ASSPs offer a poor solution for control path applications, there was a growing need in the industry for a new CPLD architecture to deliver cost-effective, instant-on, non-volatile devices at higher densities. Altera meets this need with its new MAX II family, which offers unprecedented levels of CPLD density (see Table 1). Based on a 0.18-µm flash process, the MAX II family is optimized for the lowest possible cost per I/O pin. It delivers the higher densities required for system control in a non-volatile, instant-on device at half the cost and one-tenth the power consumption of prior MAX CPLD generations.

Groundbreaking New CPLD Architecture

Based on a groundbreaking new CPLD architecture, MAX II devices redefine the value proposition for CPLDs. Historically, CPLDs differ from FPGAs because of their macrocell-based architecture. Unlike FPGAs, traditional CPLDs are designed around a base unit called the product-term, and have a global routing structure. However, the macrocell-based architecture is not efficiently scalable beyond approximately 1,000 macrocells because its routing area increases quadratically with density. At higher densities, the look-up table (LUT) architecture with row-and-column routing is more die-size efficient (see Figure 2), providing a significant cost advantage as well as delivering faster performance, smaller die size, and lower power consumption per gate.

MAX II devices are classified as CPLDs because they target the non-data path applications in which CPLDs are used. Classifying these devices based on intended application, rather than architecture emphasizes the benefits of technology, rather than the technology itself.

The MAX II architecture was developed to reduce the cost of general-purpose programmable logic designs by delivering the lowest cost per I/O pin in the smallest possible die size. Altera employed the following design techniques to develop this new architecture.

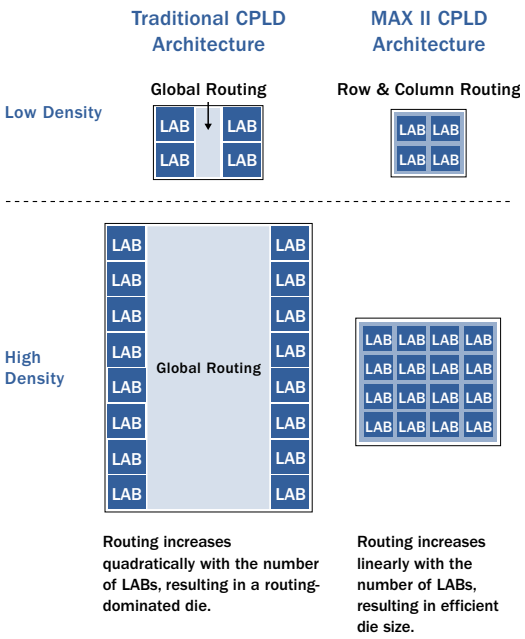
Table 1. MAX II Family Overview					
Device	**Logic Elements**	**Equivalent Macrocells**	**Maximum User I/O Pins**	**User Flash Memory (Kbits)**	**Available Packages** *(1)*
EPM240	240	192	80	8,192	100-pin TQFP (2)
EPM570	570	440	160	8,192	100-pin TQFP 144-pin TQFP 256-pin FineLine BGA® *(3)*
EPM1270	1,270	980	212	8,192	144-pin TQFP 256-pin FineLine BGA
EPM2210	2,210	1,700	272	8,192	256-pin FineLine BGA 324-pin FineLine BGA

Notes to Table 1:
(1) All packages support vertical migration across all densities.
(2) TQFP: thin quad flat pack.
(3) FineLine BGA package (1.0-mm pitch)

First, the MAX II I/O cells were optimized for size and placed in a staggered ring to minimize die size. Then, the devices were targeted to a set of popular, low-cost TQFP and FineLine BGA packages. Because of the focus on low cost per I/O pin, MAX II devices are pad-limited. In other words, device die size is defined by the number and size of I/O cells. It is critical to define the smallest I/O cell dimension possible because they, in turn, define the device's absolute die area and directly impact device cost.

Second, Altera selected a low-cost, low-power process technology on which to manufacture the MAX II family. TSMC's 0.18-µm flash process technology was selected to meet customers' instant-on and non-volatility requirements, while offering a dramatic reduction in device cost and power consumption.

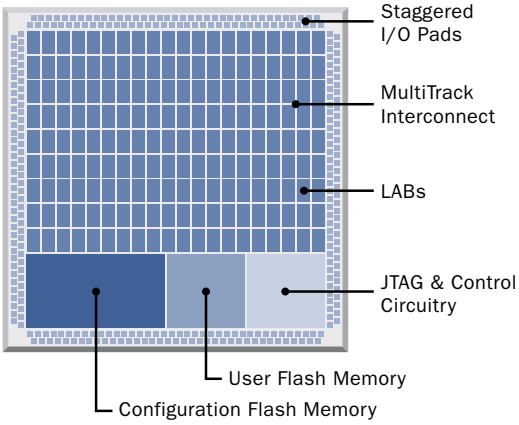
Figure 2. Low-Cost MAX II Architecture Delivers Smaller Die Size



Finally, a new logic architecture was applied to deliver the highest density and performance within the available silicon area. The result is the MAX II device, the industry's lowest-cost CPLD ever.

Figure 3 shows the groundbreaking MAX II CPLD architecture, consisting of an array of LUT-based logic array blocks (LABs), a bank of non-volatile flash memory, a staggered ring of area-optimized I/O cells, and Joint Test Action Group (JTAG) control circuitry. The MultiTrack™ interconnect is designed to maximize performance and minimize power by using the most efficient direct connection from input to logic to output.

Figure 3. MAX II Device Floorplan



Board-Management Features

In addition to reducing the cost of the CPLD itself, the MAX II architecture includes a number of board-management features that help reduce costs and board space, while improving reliability at the board level.

continued on page 6

User Flash Memory—An Industry First

The user flash memory is a non-volatile 8-Kbit memory block embedded within the MAX II device. It reduces cost and board space by delivering on-board electrically erasable programmable read-only memory (EEPROM) functionality that would otherwise require a separate device. MAX II devices are the first CPLDs to offer this feature. Typical applications for the user flash memory include storage of common board "housekeeping" information, such as manufacturing IDs, board revision or software revision information or power management diagnostic statistics.

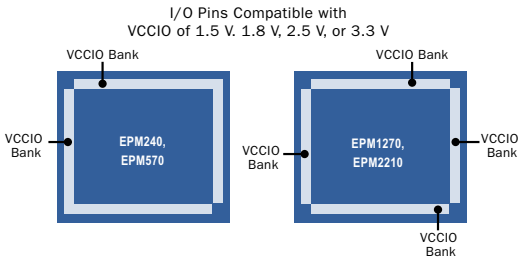
MultiVolt Core

The MultiVolt™ core—another industry first—allows users to power MAX II devices with any of three different supply voltages. It leverages the performance, cost, and power benefits of the 0.18-µm manufacturing process while supporting 3.3-V, 2.5-V, and 1.8-V power rails. An internal voltage regulator regulates the incoming voltage down to 1.8 V, enabling the user to choose whichever power rail is most convenient for a particular board-level design.

I/O Features

The new CPLD architecture also improves I/O usability. There are two I/O banks in EPM240 and EPM570 devices and four I/O banks in the EPM1270 and EPM2210 devices. Each I/O bank has its own VCCIO pin and can be configured independently to support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces. Each can also independently support a different I/O standard. Figure 4 highlights the I/O bank configurations, and Table 2 shows the I/O features available in MAX II devices.

Figure 4. MAX II I/O Bank Configurations



Real-Time ISP

Real-time in-system programmability (ISP) provides a flexible field upgrade solution designed to reduce the cost of remote field updates. MAX II devices include the capability to update the configuration flash memory block while the logic is running, with the new programming file taking effect without requiring the system to be turned off and initiate reconfiguration. This feature permits board management function updates without expensive system downtime or the cost of sending engineers to remote sites.

Ease-of-Use

In addition to having new board management features, the MAX II architecture is optimized for ease of use with features such as improved second-time fitting. The MultiTrack™ interconnect decouples the LABs from the I/O pins, allowing a pin-locked design to have a very high success rate for second-time fitting. This accommodates last-minute design changes.

Table 2. MAX II I/O Features

Feature	Description	Benefit
MultiVolt I/O Banks	Each bank of I/O contains a unique set of VCCIO pins for setting the voltage of that bank to either 3.3 V, 2.5 V, 1.8 V, or 1.5 V.	Supports multiple voltage standards on one device.
3.3-V/2.5-V/1.8-V/1.5-V LVTTL/LVCMOS	Support for LVTTL/LVCMOS standards down to 1.5 V with multiple I/O banks.	Enables broad application support and compatibility with LVTTL standards.
PCI Support	The EPM1270 and EPM2210 devices support PCI I/O capability.	Enables support for 32-bit, 33-MHz PCI and use of MAX II devices as a PCI slave and arbiter.
Schmitt Triggers	Programmable hysteresis on any input pin.	Enables noise tolerance on inputs with up to 300 mV on 3.3-V inputs and 160 mV on 2.5-V inputs.
Programmable Drive Strength and Slew Rate	High and low drive strength settings not available in prior MAX families. Slew rate control has more dramatic effect than in previous MAX families.	Enables user control to improve signal integrity.
Unique OE (tri-state control) per Pin	No limit to the number of OE signals in the design except I/O count.	Improvement over deficiency in prior MAX architectures.
Programmable Bus-Hold, Pull-Up Resistor, and Open-Drain	Programmable I/O features that are also available in MAX 7000B.	More user control of on-chip I/O behavior saving the user from using external components.

Free Design Software

MAX II devices are supported by Altera's Quartus® II software, the easiest-to-use design software available for CPLD design. Now featuring a built-in MAX+PLUS® II look-and-feel option, MAX+PLUS II users can benefit from the Quartus II software without having to learn a new user interface. The Quartus II software also integrates seamlessly with all of the leading third-party synthesis and simulation tools.

A free version of the software, Quartus II Web Edition, can be downloaded from the Altera web site at **www.altera.com** and is also available on the Quartus II Software Starter Suite CD-ROM.

Conclusion

Today's system designers continue to be challenged to deliver smaller and less costly electronics systems. While CPLDs have traditionally been the device of choice for control path functions, limits in density and performance have driven designers of advanced systems to consider more costly alternatives such as ASICs and ASSPs. Altera's new MAX II family of CPLDs leverages a LUT-based architecture that delivers significant new benefits for designers low-cost, low-power logic needs. To learn more about MAX II CPLDs, visit **www.altera.com/max2**.

Stratix II—The Latest High-Performance, High-Density FPGAs

FPGA performance and density reaches new heights with the Stratix™ II device family, the latest FPGA product from Altera. Built on a new and innovative logic structure, Stratix II devices deliver on average 50% faster performance and offer more than twice the logic capacity of first-generation Stratix FPGAs. Stratix II devices extend the possibilities of FPGA design, allowing designers to meet the high-performance requirements of today's advanced systems and avoid developing with costly, time-consuming ASICs. Based on the award-winning Stratix device family architecture, Stratix II devices cost 40% less than first-generation Stratix devices and are outfitted with a powerful set of system-level features and incorporate many significant enhancements and new capabilities.

Stratix II FPGAs are manufactured on 300-mm wafers using TSMC's 90-nm, low-k dielectric process technology. Featuring numerous technological innovations and industry firsts, Stratix II FPGAs contain a new FPGA logic structure that increases device performance and densities to unprecedented levels. The innovative logic structure is built with adaptive logic modules (ALMs), which use logic resources more efficiently than traditional 4-input look-up table (LUT)-based logic elements (LEs). As a result, Stratix II FPGAs require fewer resources and reduce the levels of logic for a given function, yielding higher performance at a lower system cost. Performance advantages include support for 500-MHz clock rates and 250-MHz system clock frequencies. Stratix II device densities approach 180K equivalent LEs and 9 Mbits of RAM, a more than two-fold increase over its predecessor (see Table 1).

The Challenge of Today's Digital Systems

Consumers are demanding real-time access to up-to-date data, pushing end-user and infrastructure equipment to their performance limits. Enterprise servers, video switcher systems, and digital subscriber line multiplexers all require logic devices that support faster performance. To meet the needs of today's digital systems, Altera went back to the drawing board and developed a completely new logic structure for achieving or exceeding these challenging performance and cost requirements.

Why FPGA Performance Matters

An important but often overlooked point is that using an FPGA with support for higher clock frequencies can be more cost-effective than using one with lower performance, even though faster speed grade FPGAs often have an associated cost premium. This is because the faster performance can be used to reduce the size of a design by dividing the bus structure in half and operating at twice the frequency, allowing the user to fit the design into a smaller device density.

To illustrate this, consider a SPI-4.2 interface, typically found in backplane applications, that can be implemented in both Stratix and Stratix II FPGAs. A 16-channel configuration of this design consumes approximately 16,000 LEs in a Stratix FPGA and requires the fastest speed grade to function correctly. Because Stratix II devices support much higher core logic and I/O speeds, this same design running at twice the speed with the bus divided into half consumes less than half the number of logic resources

Table 1. Stratix II Device Family Overview

Device	ALMs	Equivalent LEs	M512 RAM Blocks	M4K RAM Blocks	M-RAM	Total Memory Bits	18- x 18-Bit Multipliers *(1)*	PLLs *(2)*	Availability
EP2S15	6,240	15,600	104	78	419,328	0	48	6	Q4 2004
EP2S30	13,552	33,880	202	144	1,369,728	1	64	6	Q4 2004
EP2S60	24,176	60,440	329	255	2,544,192	2	144	12	July 2004
EP2S90	36,384	90,960	488	408	4,520,448	4	192	12	Q4 2004
EP2S130	53,016	132,540	699	609	6,747,840	6	252	12	October 2004
EP2S180	71,760	179,400	930	768	9,383,040	9	384	12	Q4 2004

Notes to Table 1:

(1) Does not include soft multipliers implemented in memory blocks.

(2) Includes enhanced and fast PLLs.

than the Stratix implementation. This translates to a reduction in cost by approximately 75% with the Stratix II device. Further reductions in logic usage are also gained as a result of the more efficient packing capabilities of the Stratix II ALM, as discussed later in this issue of *News & Views*.

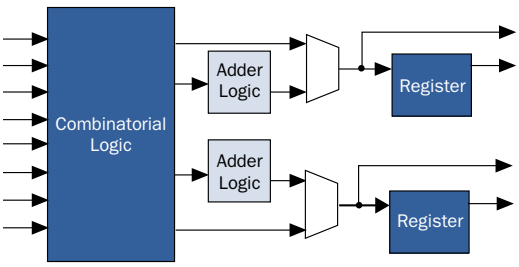
Developing and manufacturing semiconductors at deep submicron nodes with support for faster performance and larger densities is no longer academic. At the same time, porting an older FPGA architecture to a new process technology node does not necessarily result in faster performance as in the past. Rather, careful design considerations such as area-performance-power trade-offs and new architectural innovations are critical and must be made to reach the FPGA performance-price requirements of next-generation systems.

Breaking from Tradition to Address Submicron Challenges

Issues associated with designing semiconductors at the submicron level have drawn significant attention over the past few years. This is not without good reason—nanometer effects, whether from leakage current, inductive coupling, or supply drop—result in formidable challenges for FPGAs in the areas of performance and power management.

As a result, Altera has made significant changes in the logic array, developing an innovative, new logic structure, far ahead, in terms of performance and efficiency, of the 4-input LUT architectures that have been the basis of FPGAs for the last two decades. As shown in Figure 1, the logic structure of the Stratix II device family is built using ALMs that are composed of combinational, arithmetic, and register logic.

Figure 1. The New Stratix II Adaptive Logic Module



The Stratix II ALM is much more than two conjoined LEs with shared resources. What sets the ALM apart from all other FPGA architectures is its ability to adapt. The ALM can support either a single function that ranges in input width from 1 to 7, or it can support multiple, independent functions of different (or the same) widths. For example, a design may be synthesized into multiple functions of varying widths, say 5- and 3-input functions. Rather than having to build these functions across multiple levels (for the 5-input functions) or to waste resources (for the 3-input functions) when implemented in a fixed 4-input based architecture, both the 3- and 5-input functions can be placed within a single Stratix II ALM. Inputs and combinational LUT logic can be shared across the functions, saving even more resources. This is the case whether the design is synthesized as a combination of 7-, 5-, and 2-input functions, or any other combination of functions with up to 8 inputs. The end result is an average performance increase of 50% and a drastic increase in logic usage efficiency, reaching a 4-to-1 ratio in some cases.

Enhancing a Proven Feature Set

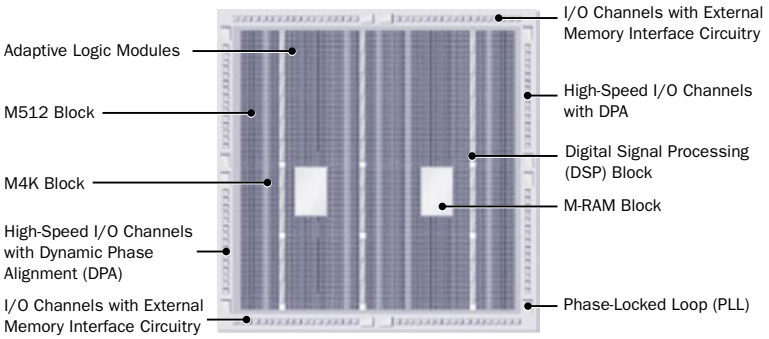
In addition to a new logic structure, the Stratix II device family is optimized for the 90-nm process and offers many performance enhancements to the award-winning features of the original Stratix FPGA family (see Figure 2 on page 10). These enhancements include:

- TriMatrix™ Memory: More than 9 Mbits per device, up to 370-MHz performance with new capabilities for more efficient resource usage
- Digital Signal Processing Blocks: Up to 4× more bandwidth, support for rounding and saturation, and mixed-modes
- External Memory Interfaces: Support for the latest memory devices, including DDR2, SDRAM, QDR SRAM, and RLDRAM II (see Table 2 on page 10)
- Phase-Locked Loops: Enhanced jitter performance and on-the-fly reconfiguration capabilities
- High-Speed I/O Pins: Up to 1-Gbps performance on over 150 receive and 150 transmit channels with dynamic phase alignment (DPA)

continued on page 10

Table 2. Stratix II External Memory Interface Support	
Memory Technology	**Maximum Clock Rate (MHz)**
SDR SDRAM	166
DDR SDRAM	200
DDR2 SDRAM	266
RLDRAM II	300
QDRII SDRAM	250

Figure 2. EP2S260 Device Floorplan



High-Speed Signal Integrity

A true all-purpose FPGA, the Stratix II device family includes support for high-speed interfaces with dedicated DPA circuitry. DPA was first introduced to the FPGA market by Altera in the Stratix GX device family, Altera's transceiver-based family of FPGAs. As maximum system performance specifications rise and as backplane interfaces become chip-to-chip interfaces, there is an increasing need for a flexible, robust FPGA solution for high-speed signal alignment.

High-speed interfaces with source-synchronous clocking schemes are rapidly approaching one gigabit per second (Gbps) transfer rates. Due to these high speeds, digital designs require highly accurate data and clock synchronization and must meet very tight clock-to-channel and channel-to-channel skew specifications. To stay within the permitted skew, designers must use precise printed circuit board (PCB) design techniques because the slightest mismatch in trace lengths could result in erroneous data transfer. Other effects such as jitter, temperature, and voltage variations compound the problem, making simpler, static phase alignment techniques ineffective. Recognizing the challenges that engineers face when designing systems that transfer high-speed data, Altera developed the DPA feature to dramatically simplify PCB design, eliminating the signal alignment problems that result from skew-inducing effects.

Ensuring Design Security

In today's highly competitive commercial and military environments, design security is becoming an important consideration for digital designers. As FPGAs continue to play more critical functions in these systems, companies and governments will have increasing concerns about their intellectual property (IP) contained within FPGAs. Altera's Stratix II devices are the industry's first FPGAs to support configuration bitstream encryption using 128-bit Advanced Encryption Standard (AES). The new AES algorithm was developed by the U.S. National Security Association (NSA) as a successor to the older Data Encryption Standard (DES) and triple-DES algorithms. Starting with a user-defined 128-bit key, a user can generate an encrypted programming file in the Quartus® II software that is used to configure a Stratix II FPGA. That same key is securely stored in a non-volatile location in the FPGA and is used to decrypt the incoming programming file from the memory or configuration device.

High-Volume Production Support: Altera's HardCopy Device Family

For high-volume designs, Stratix II devices are supported by Altera's HardCopy™ structured ASIC family. HardCopy devices for Stratix II FPGAs deliver additional increases in performance and reduced power consumption, at a significant risk reduction and cost savings. The HardCopy design methodology provides volume-driven customers with a unique prototype-to-production solution not offered by any other semiconductor company.

Conclusion

The new Stratix II device family—with an average 50% faster performance, 2× more density, an all-new logic structure, DPA circuitry, and design security features—is just the beginning of what you will see from Altera in 2004. Much more is on the way, including HardCopy for Stratix II devices and a host of new development kits and IP. Get your next high-performance design on its way—install the new Quartus II software version 4.0 to start designing with Stratix II devices.

For more detailed information on Stratix II devices, see "Secure Your Design with Stratix II FPGAs" on page 31 and "New & Innovative Stratix II Logic Structure Brings Unprecedented Performance & Logic Efficiency" on page 33.

Make the Move from the MAX+PLUS II to Quartus II Software

The Quartus® II software is now the best and easiest-to-use software for designing with CPLDs, FPGAs, and structured ASICs. MAX+PLUS® II software users will be amazed at how familiar the Quartus II software version 4.0 looks and feels while delivering better performance, more features, and access to exciting new CPLD and FPGA device families.

Quartus II Software Benefits

Version 4.0 of the Quartus II software offers MAX+PLUS II users faster push-button performance, superior integrated synthesis support, a familiar MAX+PLUS II look-and-feel, and enhancements to better support converting MAX+PLUS II projects to Quartus II projects. Along with support for your favorite MAX® and FLEX® 10K devices, the Quartus II software version 4.0 adds support for the MAX II CPLD family and supports all of Altera's latest FPGA and structured ASIC devices.

Table 1 summarizes the Quartus II software's advantages for MAX+PLUS II software customers.

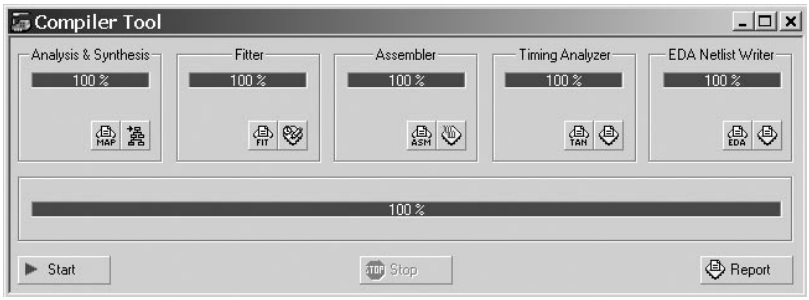
Quartus II Software's New MAX+PLUS II Look-&-Feel Optional Setting

With the built-in MAX+PLUS II look-and-feel option, users can get the full benefit of the Quartus II software without learning a new user interface. This option provides Quartus II users the same basic menu structure and toolbar as seen in the MAX+PLUS II software (see Figure 1).

Figure 1. MAX+PLUS II Look & Feel Toolbar in the Quartus II Software

The new Quartus II compiler tool is similar to the MAX+PLUS II compiler tool and offers the same one-click compilation capability (see Figure 2).

Figure 2. Quartus II Compiler Window



New in version 4.0 of the Quartus II software are timing analyzer and simulator tools with similar interfaces to those in the MAX+PLUS II software. The Quartus II simulator tool (see Figure 3 on page 12) has been enhanced to emulate MAX+PLUS II simulator functionality by allowing users to overwrite simulation input files with simulation results. Users can generate functional simulation netlists separately from the compilation process to accelerate compilation and simulation run times.

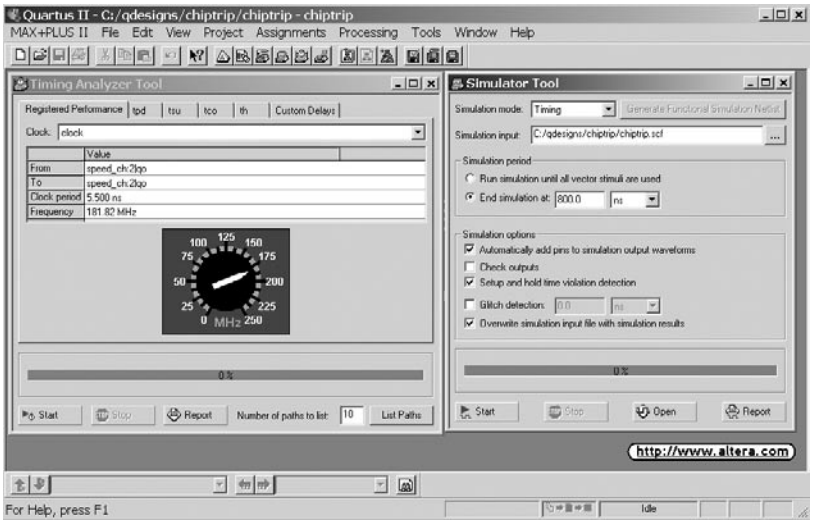
continued on page 12

MAX+PLUS II Users

Table 1. Quartus II Advantages over the MAX+PLUS II Software

Design Method	Supported Features
Device Support	■ Supports the new MAX II family in addition to MAX 3000A, 7000S, MAX 7000AE, and MAX 7000B families ■ Supports the latest FPGA devices such as Stratix II, Cyclone™, and Stratix™ families, in addition to FLEX 10KE, FLEX 10K, FLEX 10KA, ACEX® 1K, and FLEX 6000 families
Performance	■ Twice the design performance of the CPLD push-button design using MAX II devices o The Quartus II design space explorer script can raise performance an average of an additional 35% ■ Offers better average performance than MAX+PLUS II software version 10.2 for MAX 3000A, MAX 7000AE, MAX 7000S, MAX 7000B, FLEX 10K, and ACEX 1K designs o 15% faster average design performance than MAX designs originally compiled with the MAX+PLUS II software version 10.2 o Requires an average of 5% fewer device resources for any given MAX design
Synthesis	■ Integrates RTL synthesis support for the latest VHDL and Verilog HDL standards in addition to AHDL support ■ RTL viewer provides a graphical representation of VHDL or Verilog HDL designs before synthesis and design implementation (Quartus II software only) ■ Supports all leading third-party synthesis flows

Figure 3. New Quartus II Timing Analyzer & Simulator Tools



Experience the Power of the Quartus II Software Now

Many designers are already enjoying the benefits of the Quartus II software:

- "The Quartus II software is more reliable and user-friendly than MAX+PLUS II…" Hussein Moradi, President, Quintessence Technologies Corporation
- "…I found it very easy to switch from the MAX+PLUS II software to the Quartus II software, which I now use for all of my new Altera designs..." Bill Swanson, Principal Engineer, Vytek Corporation
- "I am very impressed with the ease-of-use, speed, and exceptional quality of results yielded by the Quartus II software…" Alfredo Mendez, Principal Consultant, Intrinsix Corporation

You can download the free Quartus II Web Edition software from the Altera® web site download center or request the Quartus II Software Starter Suite CD-ROM from the literature section of the Altera web site.

Also available is a new online demonstrations that shows how easy it is to convert a MAX+PLUS II project into a Quartus II project. For more detailed information you can also refer to the *Quartus II Design Flow for MAX+PLUS II Users* chapter of the new *Quartus II Development Software Handbook*.

The Quartus II software is now recommended for all new CPLD, FPGA, and structured ASIC designs. MAX+PLUS II users who try the Quartus II software will realize performance and productivity gains and get access to advanced features and exciting new device families. Making the move to the Quartus II software is risk-free—the free Quartus II Web Edition version 4.0, including the MAX+PLUS II look-and-feel-option and MAX II device support is now available on the Altera web site.

Quartus II Version 4.0—Design Software Technology Leadership

Version 4.0 of the Quartus® II software extends Altera's software technology leadership for high-density FPGA design and continues Altera's tradition of CPLD design tool leadership.

Design for Stratix II FPGAs Today

Stratix™ II devices are 50% faster than previous FPGA families and can reach even higher performance levels by taking advantage of the Quartus II software's advanced physical synthesis and timing closure methodologies. The Quartus II software technology leadership and the Stratix II device family delivers the highest performance and efficiency for high-density FPGA designs.

Design for MAX II CPLDs Today

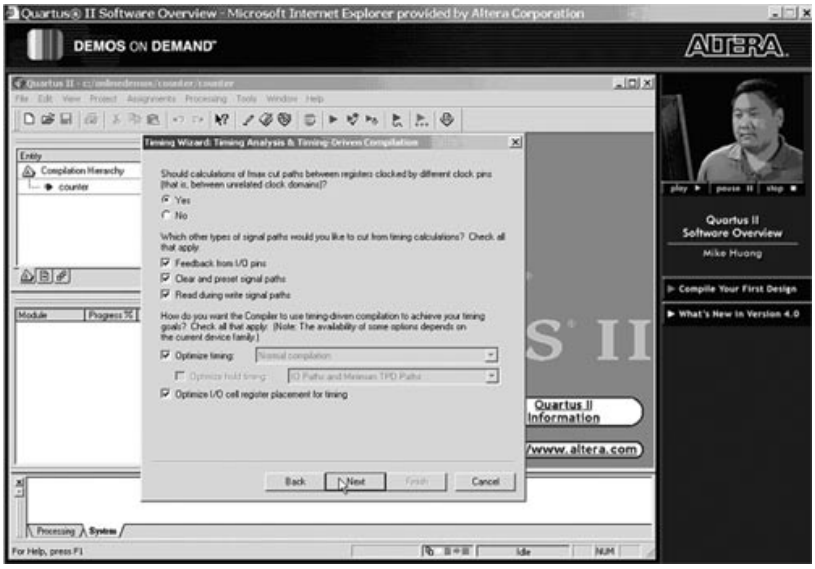
The Quartus II software continues Altera's tradition of CPLD design tool leadership with an easy-to-use and complete design environment for CPLD design entry, synthesis, place-and-route, and verification. In addition to supporting the new MAX® II CPLD family, the Quartus II software now includes a MAX+PLUS® II look-and-feel option, so thousands of MAX+PLUS II designers can make the move to the Quartus II software without having to learn a new software interface. See the "Make the Move from MAX+PLUS II to Quartus II Software" on page 11 for more information.

Quartus II On-line Demos & Software Handbook Now Available

There are now over 20 short video demonstrations of Quartus II software features and design methodologies available from the Altera web site at **www.altera.com/quartusdemos**. This is the easiest way to see the latest Quartus II software features in action and learn where to get more information. See Figure 1.

The new *Quartus II Development Software Handbook* includes detailed applications information on design and synthesis, design implementation and optimization, and verification. The Quartus II software handbook is now available from the Altera® web site.

Figure 1. Quartus II On-Line Demonstrations



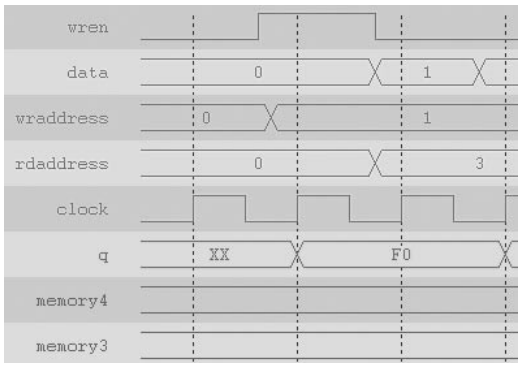
New Features Extending Software Technology Leadership

The Quartus II software version 4.0 includes new technology to simplify and accelerate high-density FPGA designs.

Memory Compiler Waveform Generation

The Quartus II software memory compiler can now produce waveform displays of RAM and first-in first-out (FIFO) memory operation based on memory parameterization and configuration selections. This feature makes it easier to understand the effects of different memory configuration settings. See Figure 2.

Figure 2. Memory Compiler Waveform Generation

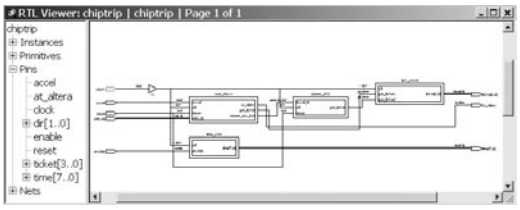


continued on page 14

RTL Viewer

The new register transfer level (RTL) viewer feature provides a schematic representation of designs that can be used to analyze a design's structure before further behavioral simulation, synthesis, and place-and-route steps are performed (see Figure 3). The RTL viewer allows designers to navigate a design's hierarchy and easily locate particular items of interest easily to aid in debugging and optimization. Selected items in the RTL viewer can be directly traced back to source design files.

Figure 3. RTL Viewer



Revisions

The Quartus II software now allows designers to easily experiment using different compilation settings and assignments for a given design. A group of settings, assignments, and compilation results can be stored and processed separately as an individual design revision.

Physical Synthesis Enhancements

Version 4.0 of the Quartus II software adds physical synthesis optimization support for the Stratix II FPGA family in addition to the support included previously for Stratix, Stratix GX, and Cyclone™ device families.

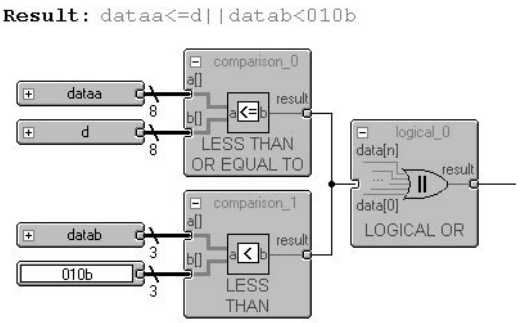
Design Space Explorer Distributed Computing Support

The Quartus II software design space explorer script provides an automated option to increase average design performance by 20% by applying combinations of compilation settings and physical synthesis settings. The Quartus II software version 4.0 enhances the design space explorer feature to support distributed environments where multiple computers can run simultaneous compilations using different optimization settings to dramatically reduce design space explorer run times.

SignalTap II Advanced Triggering Feature

SignalTap® II logic analysis facilitates the verification process by integrating the functionality of a logic analyzer within the software. Version 4.0 of the Quartus II software adds a new graphical environment to implement complex user-defined trigger logic to compare bus states with individual signals to initiate SignalTap II embedded logic analyzer data capture. This feature gives FPGA designers unprecedented flexibility to isolate system design problems in-system and at system speeds. See Figure 4.

Figure 4. SignalTap II Advanced Triggering Example



Faster Compile Times on Linux Platforms

New software optimizations improves compile times by an average of 40% when using the Quartus II software for Red Hat Linux 7.3 or 8.0.

Experience Quartus II Software Version 4.0 Today

The Quartus II software version 4.0 delivers unmatched performance, efficiency, and ease-of-use for CPLD, FPGA, and structured ASIC designs. The Quartus II software version 4.0 is now shipping to all customers with active software subscriptions. The Quartus II Web Edition software is available for downloading from the Altera web site or as part of the Quartus II Software Starter Suite CD-ROM.

Altera Devices

Tables 1 through 14 list the logic element (LE), macrocell and gate counts, pin/package options, I/O pin counts, supply voltage, RAM bits, and other device-specific features of Altera® CPLDs, FPGAs, HardCopy™ devices, and configuration devices.

Table 1. MAX II Devices

Device	LEs	Typical Equivalent Macrocells	Pin/Package Options (1)	Maximum User I/O Pins	Supply Voltage	User Flash Memory Bits
EPM240	240	192	100-Pin TQFP	80	3.3 V, 2.5 V, 1.8 V	8,192
EPM570	570	440	100-Pin TQFP, 144-Pin TQFP, 256-Pin BGA	76, 116, 160	3.3 V, 2.5 V, 1.8 V	8,192
EPM1270	1,270	980	144-Pin TQFP, 256-Pin BGA	116, 212	3.3 V, 2.5 V, 1.8 V	8,192
EPM2210	2,210	1,700	256-Pin BGA, 324-Pin BGA	204, 272	3.3 V, 2.5 V, 1.8 V	8,192

Note to Table 1:

(1) All BGA packages are 1.0-mm FineLine BGA® packages.

Table 2. Stratix II Devices

Device	Adaptive Logic Modules (ALMs) (1)	Equivalent LEs (1)	M512 RAM Blocks	M4K RAM Blocks	M-RAM Blocks	Total RAM Bits	Pin/Package Options	Maximum User I/O Pins	DSP Blocks	Embedded Multipliers (2)	Supply Voltage	PLLs (3)
EP2S15	6,240	15,600	104	78	0	419,328	484-Pin BGA, 672-Pin BGA	341 365	12	48	1.2 V	6
EP2S30	13,552	33,880	202	144	1	1,369,728	484-Pin BGA, 672-Pin BGA	341 499	16	64	1.2 V	6
EP2S60	24,176	60,440	329	255	2	2,544,192	484-Pin BGA, 672-Pin BGA, 1,020-Pin BGA	341 499 717	36	144	1.2 V	12
EP2S90	36,384	90,960	488	408	4	4,520,448	1,020-Pin BGA, 1,508-Pin BGA	757 901	48	192	1.2 V	12
EP2S130	53,016	132,540	699	609	6	6,747,840	1,020-Pin BGA 1,508-Pin BGA	741 1,109	63	252	1.2 V	12
EP2S180	71,760	179,400	930	768	9	9,383,040	1,020-Pin BGA 1,508-Pin BGA	741 1,173	96	484	1.2 V	12

Notes to Table 2:

(1) Each Stratix™ II ALM is equivalent to 2.5, 4-input look-up table (LUT)-based LEs.
(2) Each DSP block supports four 18-bit × 18-bit multipliers.
(3) Includes enhanced and fast PLLs.

Table 3. Stratix Devices Note (1)

Device	LEs	Pin/Package Options	I/O Pins	Supply Voltage	Total RAM Bits	DSP Blocks
EP1S10	10,570	484-Pin BGA *(2)*, 672-Pin BGA, 672-Pin BGA *(2)*, 780-Pin BGA *(2)*	335, 345, 345, 426	1.5 V	920,448	6
EP1S20	18,460	484-Pin BGA *(2)*, 672-Pin BGA, 672-Pin BGA *(2)*, 780-Pin BGA *(2)*	361, 426, 426, 586	1.5 V	1,669,248	10
EP1S25	25,660	672-Pin BGA, 672-Pin BGA *(2)*, 780-Pin BGA *(2)*, 1,020-Pin BGA *(2)*	473, 473, 597, 706	1.5 V	1,944,576	10
EP1S30	32,470	780-Pin BGA *(2)*, 956-Pin BGA, 1,020-Pin BGA *(2)*	589, 683, 726	1.5 V	3,317,184	12
EP1S40	41,250	780-Pin BGA *(2)*, 956-Pin BGA, 1,020-Pin BGA *(2)*, 1,508-Pin BGA *(2)*	615, 683, 773, 822	1.5 V	3,423,744	14
EP1S60	57,120	956-Pin BGA, 1,020-Pin BGA *(2)*, 1,508-Pin BGA *(2)*	683, 773, 1,022	1.5 V	5,215,104	18
EP1S80	79,040	956-Pin BGA, 1,020-Pin BGA *(2)*, 1,508-Pin BGA *(2)*	683, 773, 1,203	1.5 V	7,427,520	22

Notes to Table 3:

(1) The ordering code for Stratix devices is based on the number of LEs; therefore, gate count numbers are not included.
(2) Space-saving FineLine BGA package.

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Table 4. APEX 20K Devices

Device	Gates	Pin/Package Options	I/O Pins	Supply Voltage	LEs	RAM Bits
EP20K30E	30,000	144-Pin TQFP, 144-Pin BGA *(1)*, 208-Pin PQFP	92, 93, 125	1.8 V	1,200	24,576
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA *(1)*, 208-Pin PQFP, 324-Pin BGA *(1)*, 356-Pin BGA	92, 93, 148, 196, 196	1.8 V	2,560	32,768
EP20K100 EP20K100E	100,000 100,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA *(1)*, 356-Pin BGA 144-Pin TQFP, 144-Pin BGA *(1)*, 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA *(1)*, 356-Pin BGA	101, 159, 189, 252, 252 92, 93, 151, 183, 246, 246	2.5 V 1.8 V	4,160 4,160	53,248 53,248
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA *(1)*	88, 143, 175, 271, 316	1.8 V	6,400	81,920
EP20K200 EP20K200E EP20K200C	200,000 200,000 200,000	208-Pin PQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA *(1)* 208-Pin PQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA *(1)*, 652-Pin BGA, 672-Pin BGA *(1)* 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA *(1)*	144, 174, 277, 382 136, 168, 271, 376, 376, 376 136, 168, 271, 376	2.5 V 1.8 V 1.8 V	8,320 8,320 8,320	106,496 106,496 106,496
EP20K300E	300,000	240-Pin PQFP, 652-Pin BGA, 672-Pin BGA *(1)*	152, 408, 408	1.8 V	11,520	147,456
EP20K400 EP20K400E EP20K400C	400,000 400,000 400,000	652-Pin BGA, 672-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)*	502, 502 488, 488 488, 488	2.5 V 1.8 V 1.8 V	16,640 16,640 16,640	212,992 212,992 212,992
EP20K600E EP20K600C	600,000 600,000	652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	488, 508, 588 488, 508, 588	1.8 V 1.8 V	24,320 24,320	311,296 311,296
EP20K1000E EP20K1000C	1,000,000 1,000,000	652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	488, 508, 708 488, 508, 708	1.8 V 1.8 V	38,400 38,400	327,680 327,680
EP20K1500E	1,500,000	652-Pin BGA, 1,020-Pin BGA *(1)*	488, 808	1.8 V	51,840	442,368

Note to Table 4:
(1) Space-saving FineLine BGA package.

HARDCOPY™

HardCopy Structured ASICs: ASIC Gain without the Pain

HardCopy structured ASICs provide a comprehensive alternative to standard cell ASICs. Engineers can directly design HardCopy structured ASICs using the advanced features of the Quartus® II design software with the added capability to prototype and verify functionality in-system. The in-system verification feature not only facilitates changes to the design while testing the design in-silicon, but also helps develop the total system including software thus offering true time-to-market benefits. Further, the seamless migration of this proven design to the HardCopy structured ASIC guarantees first-silicon functionality.

HardCopy devices are now available in LE densities ranging from 16K to 79M, or an equivalent of 200K to 1 million standard cell gates. Fully tested first samples of HardCopy devices are available in as little as 8 weeks after the design is accepted by Altera.

HardCopy Stratix™ HC1S25, HC1S60, and HC1S80 devices are shipping in volume. HC1S30 and HC1S40 devices will begin shipping in volume by Q3 2004.

With numerous design wins in the first generation HardCopy devices, Altera has been shipping HardCopy APEX 20KC™ and HardCopy APEX 20KE™ devices in volume since 2001.

For more information on HardCopy devices, refer to **www.altera.com/hardcopy**.

What Customers are Saying about HardCopy Structured ASICs

"Altera HardCopy Stratix devices provide a low-risk, cost-optimized, high-volume solution for our next-generation 3G base station, eliminating the need for us to use an ASIC or standard product. By offering industry-leading density and a seamless migration path from Stratix FPGAs to HardCopy devices, Altera improves our time-to-market and lowers our costs, enabling us to penetrate new markets."

Bong-Bin Park
Senior Vice President of CDMA System Research Lab
LG Electronics

Table 5. HardCopy Devices						
Device	**Pin/Package Options**	**I/O Pins**	**Supply Voltage**	**Estimated Logic Gates (K)** *(1)*	**LEs**	**RAM Bits**
HC1S25	672-Pin BGA *(2)*	473	1.5 V	325	25,660	1,944,576
HC1S30	780-Pin BGA *(2)*	597	1.5 V	400	32,470	2,137,536
HC1S40	780-Pin BGA *(2)*	615	1.5 V	500	41,250	2,244,096
HC1S60	1,020-Pin BGA *(2)*	773	1.5 V	700	57,120	5,215,104
HC1S80	1,020-Pin BGA *(2)*	773	1.5 V	1,000	79,040	5,658,048
HC20K400	652-Pin BGA, 672-Pin BGA *(2)*	488, 488	1.8 V	200	16,640	212,992
HC20K600	652-Pin BGA, 672-Pin BGA *(2)*	488, 508	1.8 V	300	24,320	311,296
HC20K1000	652-Pin BGA, 672-Pin BGA1, 1,020-Pin BGA *(2)*	488, 508, 708	1.8 V	460	38,400	327,680
HC20K1500	652-Pin BGA, 1,020-Pin BGA *(2)*	488, 808	1.8 V	625	51,840	442,368

Notes to Table 5:
(1) Does not include digital signal processing (DSP) blocks or memories.
(2) Space-saving FineLine BGA package.

Table 6. Cyclone Devices					
Device	**LEs**	**Pin/Package Options**	**I/O Pins**	**Supply Voltage**	**RAM Bits**
EP1C3	2,910	100-Pin TQFP, 144-Pin TQFP *(1)*	65, 104	1.5 V	59,904
EP1C4	4,000	324-Pin BGA *(1)*, 400-Pin BGA *(1)*	249, 301	1.5 V	78,336
EP1C6	5,980	144-Pin TQFP, 240-Pin PQFP, 256-Pin BGA *(1)*	98, 185, 185	1.5 V	92,160
EP1C12	12,060	240-Pin PQFP, 256-Pin BGA *(1)*, 324-Pin BGA *(1)*	173, 185, 249	1.5 V	239,616
EP1C20	20,060	324-Pin BGA *(1)*, 400-Pin BGA *(1)*	233, 301	1.5 V	294,912

Note to Table 6:
(1) Space-saving FineLine BGA package.

Table 7. ACEX Devices						
Device	**Gates**	**Pin/Package Options**	**I/O Pins**	**Supply Voltage**	**LEs**	**RAM Bits**
EP1K10	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*	66, 92, 120, 136	2.5 V	576	12,288
EP1K30	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*	102, 147, 171	2.5 V	1,728	24,576
EP1K50	50,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*, 484-Pin BGA *(1)*	102, 147, 186, 249	2.5 V	2,880	40,960
EP1K100	100,000	208-Pin PQFP, 256-Pin BGA *(1)*, 484-Pin BGA *(1)*	147, 186, 333	2.5 V	4,992	49,152

Note to Table 7:
(1) Space-saving FineLine BGA package.

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Stratix GX Devices Shipping in Production

All Stratix GX devices have been qualified for production and are now shipping in volume quantities (see Table 8). In addition, the High-Speed Development Kit, Stratix GX Edition is now shipping. The kit includes a development board, layout files, schematics, design examples, and high-speed board layout guidelines.

Since the inception of Stratix GX devices, Altera has committed to providing customers with a complete solution for high-speed I/O designs. With the availability of detailed characterization reports, user guides, board layout guidelines, and development boards, Altera strives to ease the design process associated with high-speed I/O devices. To extend this effort further, Altera and Innocor have announced support for the SerialLite protocol on Stratix GX devices. The SerialLite protocol is designed as a lightweight, point-to-point protocol aimed at reducing footprint, latency, and overhead compared to other serial protocols. Because SerialLite focuses on providing essential functionality through scalability, this new, no-cost protocol serves as a complement to other serial protocols.

Table 8. Stratix GX Devices

Device	LEs	Transceiver Channels	Pin/Package Options	I/O Pins	Supply Voltage	RAM Bits	Source-Synchronous Channels
EP1SGX10C	10,570	4	672-Pin BGA *(1)*	330	1.5 V	920,488	22
EP1SGX10D	10,570	8	672-Pin BGA *(1)*	330	1.5 V	920,488	22
EP1SGX25C	25,660	4	672-Pin BGA *(1)*	426	1.5 V	1,944,576	39
EP1SGX25D	25,660	8	672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	426, 542	1.5 V	1,944,576	39
EP1SGX25F	25,660	16	1,020-Pin BGA *(1)*	542	1.5 V	1,944,576	39
EP1SGX40D	41,250	8	1,020-Pin BGA *(1)*	548	1.5 V	3,423,744	45
EP1SGX40G	41,250	20	1,020-Pin BGA *(1)*	548	1.5 V	3,423,744	45

Note to Table 8:
(1) Space-saving FineLine BGA package.

Table 9. Mercury Devices

Device	Gates	Pin/Package Options	I/O Pins	Supply Voltage	CDR Channels	Logic Elements	RAM Bits
EP1M120	120,000	484-Pin BGA *(1)*	303	1.8 V	8	4,800	49,152
EP1M350	350,000	780-Pin BGA *(1)*	486	1.8 V	18	14,400	114,688

Note to Table 9:
(1) Space-saving FineLine BGA package.

Table 10. Excalibur Devices

Device	Gates	Pin/Package Options	I/O Pins	Supply Voltage	Logic Elements	RAM Bits	Embedded Processor
EPXA1	100,000	484-Pin BGA *(1)*, 672-Pin BGA *(1)*	186, 246	1.8 V	4,160	53,248	32-Bit ARM922T™
EPXA4	400,000	672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	426, 488	1.8 V	16,640	212,992	32-Bit ARM922T
EPXA10	1,000,000	1,020-Pin BGA *(1)*	711	1.8 V	38,400	327,680	32-Bit ARM922T

Note to Table 10:
(1) Space-saving FineLine BGA package.

Table 11. Serial Configuration Devices for Cyclone FPGAs

Device	Pin/Package Options	Supply Voltage	Description
EPCS1	8-Pin SOIC *(1)*	3.3 V	In-system programmable 1-Mbit serial configuration device designed to configure Cyclone devices
EPCS4	8-Pin SOIC	3.3 V	In-system programmable 4-Mbit serial configuration device designed to configure Cyclone devices

Note to Table 11:
(1) SOIC: Small outline integrated circuit.

Table 12. Configuration Devices for Stratix, Stratix GX, Cyclone, APEX II, APEX, Excalibur, FLEX, Mercury & ACEX FPGAs			
Device	**Pin/Package Options**	**Supply Voltage**	**Description**
EPC1441	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 or 5.0 V	441-Kbit configuration device designed to configure all FLEX® and ACEX® devices
EPC1	8-Pin PDIP, 20-Pin PLCC	3.3 or 5.0 V	1-Mbit configuration device designed to configure APEX™, FLEX, and ACEX devices
EPC2	20-Pin PLCC, 32-Pin TQFP	3.3 or 5.0 V	In-system programmable 1.6-Mbit configuration device designed to configure Stratix, Stratix GX, Cyclone™, APEX II, APEX, FLEX, Mercury™, ACEX, and Excalibur™ devices
EPC4	100-Pin PQFP	3.3 V	In-system programmable 4-Mbit configuration device designed to configure Stratix, Stratix GX, Cyclone, APEX II, APEX, FLEX, Mercury, ACEX, and Excalibur devices
EPC8	100-Pin PQFP	3.3 V	In-system programmable 8-Mbit configuration device designed to configure Stratix, Stratix, Stratix GX, Cyclone, APEX II, APEX, FLEX, Mercury, ACEX, and Excalibur devices
EPC16	88-Pin BGA *(1)*, 100-Pin PQFP	3.3 V	In-system programmable 16-Mbit configuration device designed to configure Stratix, Stratix GX, Cyclone, APEX II, APEX, FLEX, Mercury, ACEX, and Excalibur devices

Note to Table 12:
(1) Ultra FineLine BGA package.

Table 13. MAX 3000 Devices					
Device	**Macrocells**	**Pin/Package Options**	**I/O Pins**	**Supply Voltage**	**Speed Grade**
EPM3032A	32	44-Pin PLCC/TQFP	34	3.3 V	-4, -7, -10
EPM3064A	64	44-Pin PLCC/TQFP, 100-Pin TQFP	34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-Pin TQFP, 144-Pin TQFP, 256-Pin BGA *(1)*	80, 96, 98	3.3 V	-5, -7, -10
EPM3256A	256	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*	116, 158, 161	3.3 V	-7, -10
EPM3512A	512	208-Pin PQFP, 256-Pin BGA *(1)*	172, 208	3.3 V	-7, -10

Note to Table 13:
(1) 1.0-mm pitch FineLine BGA package.

Table 14. MAX 7000 Devices					
Device	**Macrocells**	**Pin/Package Options**	**I/O Pins**	**Supply Voltage**	**Speed Grade**
EPM7032S EPM7032AE EPM7032B	32 32 32	44-Pin PLCC/TQFP 44-Pin PLCC/TQFP 44-Pin PLCC/TQFP, 49-Pin BGA *(2)*	36 36 36, 36	5.0 V 3.3 V 2.5 V	-5, -6, -7, -10 -4, -7, -10 -3, -5, -7
EPM7064S EPM7064AE EPM7064B	64 64 64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP 44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin BGA *(1)* 44-Pin TQFP, 49-Pin BGA *(2)*, 100-Pin TQFP, 100-Pin BGA *(1)*	36, 68, 68 36, 68, 68 36, 41, 68, 68	5.0 V 3.3 V 2.5 V	-5, -6, -7, -10 -4, -7, -10 -3, -5, -7
EPM7128S EPM7128AE EPM7128B	128 128 128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP 84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA *(1)*, 144-Pin TQFP, 256-Pin BGA *(1)* 100-Pin TQFP, 100-Pin BGA *(1)*, 144-Pin TQFP, 256-Pin BGA *(1)*	68, 84, 100 68, 84, 84, 100, 100 84, 84, 100, 100	5.0 V 3.3 V 2.5 V	-6, -7, -10, -15 -5, -7, -10 -4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-6, -7, -10
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S EPM7256AE EPM7256B	256 256 256	208-Pin PQFP/RQFP 100-Pin TQFP, 100-Pin BGA *(1)*, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)* 100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA *(2)*, 208-Pin PQFP, 256-Pin BGA *(1)*	164 84, 84, 120, 164, 164 84, 120, 141, 164, 164	5.0 V 3.3 V 2.5 V	-7, -10, -15 -5, -7, -10 -5, -7, -10
EPM7512AE EPM7512B	512 512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*, 256-Pin BGA 144-Pin TQFP, 169-Pin BGA *(2)*, 208-Pin PQFP, 256-Pin BGA *(1)*, 256-Pin BGA	120, 176, 212, 212 120, 141, 176, 212, 212	3.3 V 2.5 V	-7, -10, -12 -5, -7, -10

Notes to Table 14:
(1) 1.0-mm pitch FineLine BGA package.
(2) 0.8-mm pitch Ultra FineLine BGA package.

Altera Tools

Quartus II Software Version 4.0—Software Technology Leadership

Version 4.0 of the Quartus® II software is now shipping to all customers with an active Altera® software subscription. This release extends Altera's software technology leadership and supports the new MAX® II CPLD and Stratix™ II FPGA families. For more information on version 4.0 of the Quartus II software, see the "Quartus II Software Version 4.0—Design Software Technology Leadership" feature article on page 13.

MAX+PLUS II Users: Make the Move to the Quartus II Software

The Quartus II software is now recommended for all new CPLD, FPGA, and structured ASIC designs. In addition to supporting the new MAX II CPLD device family, the Quartus II software now includes a MAX+PLUS® II look-and-feel option, so MAX+PLUS II designers can make the move to the Quartus II software without having to learn a new software interface. For more information, see the "Make the Move from MAX+PLUS II to Quartus II Software" feature article on page 11.

Quartus II On-line Demonstrations

There are now over 20 short video demonstrations of Quartus II software features and design methodologies available from the Altera® web site. This is the easiest way to see the latest Quartus II software features in action and learn where to get more information. View the demonstrations at **www.altera.com/quartusdemos**.

New Quartus II Software Handbook Now Available

The new *Quartus II Development Software Handbook* provides detailed applications information on design and synthesis, design implementation & optimization, and verification. The *Quartus II Development Software Handbook* is now available from the Altera web site.

Nios Processor Version 3.2 Now Shipping

Altera is now shipping the Nios® processor version 3.2. This release of the Nios processor introduces support for the new 90-nm Stratix™ II device family.

The Nios processor once again rides the performance curve enabled by the world's latest and most advanced FPGA technology.

Active Nios subscribers will receive this update automatically. For more information regarding the Nios embedded processor, go to **www.altera.com/nios**.

Nios Processor Chosen among EDN Hot 100

EDN magazine has named the Nios embedded processor version 3.0 as one of its Hot 100 Products of 2003. With more than 12,000 Nios development kits shipped to date, thousands of designers have selected the Nios embedded processor for its ease-of-use and flexibility, making it one of the most popular embedded processors in the industry.

Nios Partner News—New Microtronix All-in-One Kit

Microtronix Datacom Ltd. is now supporting development with the Nios embedded processor by providing a cost-effective development kit bundle. Customers choose from Microtronix's available Nios-compatible development boards (featuring Cyclone™ or Stratix devices), select either Embedded Linux or the MicroC/OS-II operating systems, and receive the Nios embedded processor for a low price.

For more information, go to **www.altera.com** or contact Microtronix directly at **www.microtronix.com**.

Tips for Improving Synplify Pro Performance for Stratix II Devices

by Steve Pereira
Technical Marketing Manager
Synplicity

The recent announcement of the Stratix™ II device family has ushered in a new era of FPGA technology. To allow designers to take advantage of these engineering advances, Synplicity collaborated closely with Altera for nearly a year before the product was announced. The working partnership between the two companies has resulted in a design methodology for Stratix II devices that addresses maximum performance and minimum area. The Synplify Pro® tool is a culmination of the joint effort between Altera and Synplicity to provide customers with the ideal software and hardware implementation for their complex designs. This article describes four preferred methods to set up a design and to fine-tune synthesis to leverage the Stratix II capabilities. These methods can be used together or independently.

Design Set-Up to Improve Timing or Area

Setting up a design correctly can result in huge performance increases or area reductions. The following four methods describe the best practices to use when setting up a design.

Include Any Clear Box VQMs or Timing Models for Black Boxes

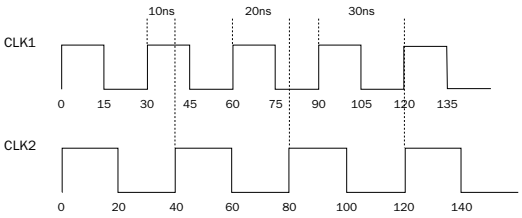
If the clear box files or timing models are provided, the Synplify Pro tool knows the path timing and can alter the logic surrounding the boxes based on the timing constraints. If the critical path starts or ends in a black box, adding the Verilog Quartus Mapped file (**.vqm**) usually results in better performance.

Provide Accurate Clock Constraints

Under-constraining or over-constraining results reduces performance. The user should not over-constrain by more than 20%. For maximum performance, ensure that there is 10% negative slack on the critical clock. This ensures that critical paths are squeezed (the Route Constraint section has more information). The f_{MAX} field on the front panel is fine for a quick run, but it should not be used if the user needs maximum performance. Put unrelated clocks in separate clock groups in the Synplify Pro Synopsys Design Constraint file (**.sdc**). If your clocks are in the same group, the Synplify Pro tool works out the worst-case set-up time for the clock-to-clock paths.

Example: Figure 1 shows a timing diagram for two clocks that are in the same clock group. Synplify rolls the clocks forward until they match up again. The tool then calculates the minimum set-up time between the clocks (in this case, 10 ns).

Figure 1. Timing Diagram for Two Clocks in the Same Group



Warning: If the clocks are unrelated, it may require several hundred clock periods before the clocks match up again. This may result in the worst-case set-up time being very small (e.g., 100 ps). Designers can check the set-up time in the Clock Relationships Table in the log file. If the set-up time is too short, it is best to re-constrain the clocks so that they are more related.

Specify Timing Exceptions

Provide all timing exceptions, such as false and multi-cycle paths, to the Synplify Pro tool. With this information, the tool can ignore these paths and concentrate on the real critical paths.

Example: In the Synplify Pro 7.5 tool, timing-driven tri-state to multiplexer conversion is enabled. If a tri-state path is critical, the Synplify Pro software automatically converts the logic to multiplexers, thus speeding up the path. Usually data on buses is not critical and can survive a few clock cycles, as the bus master has to wait.

Constrain I/O Pins

If the design has I/O timing constraints, it is likely that the critical path is through the IOE. The Synplify Pro software sees these paths as the most critical and tries to optimize them. Usually, I/O paths cannot be optimized physically any further, and, as they are the most critical, the Synplify Pro software stops optimizing the rest of the design. A new "Use clock period for unconstrained IO switch" has been added to the Synplify Pro 7.3 release. When enabled, the tool does not include any unconstrained I/O paths in timing optimizations.

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Fine-Tuning Designs to Improve Timing or Area

Once a design is set up using the methods described above and is synthesized, there are additional options to improve design performance or area.

Standard Optimization Techniques

The following four optimization techniques are design dependent. Not all designs benefit from enabling these features. The best method is to analyze the design and see if the following optimizations improve performance.

- *Retiming & Pipelining*: These options can improve performance by as much as 50%.
- *Resource Sharing*: As a rule, this option should be turned on for area and turned off for speed.
- *FSM Compiler*: The FSM Compiler is based upon the number of states.
- *FSM Explorer*: The FSM Explorer allows timing-driven state encoding.

Resource Allocation

The use of dedicated macro blocks in Altera® devices usually provides the best solution, but this is not always the case. A well-pipelined multiplier in logic can often provide a faster (but larger) solution. The user can configure macro blocks within the Synplify Pro tool based on the design requirements. You can force the tool to use a specific resource implementation by adding any of the following attributes (default values are underlined):

- Multiplier syn_multstyle {logic | lpm_mult}
- RAM syn_ramstyle {registers | block_ram | no_rw_check}
- Block_ram generates ALTSYNCRAM
- ROM syn_romstyle {logic | block_rom | lpm_rom}
- Shift Registers syn_srlstyle {registers | altshift_tap}

Optimization Controls

The Synplify Pro tool provides directives and attributes to shape and control logic according to the user's design requirements. The following attributes and directives are the most commonly used:

- syn_keep (in source code): Preserves an RTL net throughout synthesis and prevents look-up table (LUT) packing and replication. It is also useful for timing exceptions, because the user can apply a –thru constraint to it.
- syn_preserve: Disables sequential optimizations on registers, preventing removal, merging, inverter push-through, and FSM extraction.
- syn_replicate (in constraint file): Prevents replication of registers.
- syn_maxfan (in constraint file): Controls the maximum fan-out limit, triggering register replication and buffering. This control is a hard limit on modules and instances but a soft limit when it is set globally.
- syn_direct_enable (in constraint file): Forces a connection to the enable pin of the register; additional logic is moved to the D-input path.

More information on attributes and directives is available in the Synplify Pro on-line help and Reference Manual.

Route Constraint

The –route constraint is probably the most important but least known timing constraint. It can provide a +10% performance improvement with minimal effort. It can also drastically reduce area.

The –route constraint adds the specified delay to Synplify Pro tool's routing estimates. A positive value adds to the routing delay estimate and increases criticality; a negative value reduces the routing delay estimate and decreases criticality.

If the Synplify Pro timing estimate is different from the value of the PowerFit™ fitter, the difference will prevent the Synplify Pro tool from optimizing the real critical paths. The -route switch allows the user to align synthesis estimates with the place-and-route delays. Aligning the routing delays almost always results in far better results.

The –route constraint can make synthesis see the same critical path as the fitter, and to estimate the same slack as the fitter. If many clocks fail fitter timing, the user can apply –route to the clock. If there are only a few paths failing fitter timing, the user can apply –route to just these paths.

Summary: Suggested Settings

By setting up your design correctly and using features and constraints described in this document, you can meet and often surpass performance. The author found that on 50% of the designs, using the following settings increased f_{MAX} by over 25%: add Clear Box VQM, apply –route constraint to paths or clocks, set Resource Sharing to Off, set Pipelining/Retiming to On, and set "use clock period for unconstrained IO" to Off.

Using the Mentor Graphics Precision RTL Synthesis Tool for Advanced Stratix II Designs

by Rakesh Jain, Mentor Graphics

Altera® Stratix™ II devices are targeted to the highest-performance and highest-density designs. Stratix II FPGAs have a revolutionary logic structure, called the adaptive logic module (ALM) that enables arithmetic and data processing functions to be implemented more efficiently. Precision® RTL Synthesis has a detailed understanding of the Stratix II family's unique architectural features. It supports all of these features to create an optimal implementation of your design.

Stratix II Design Flow

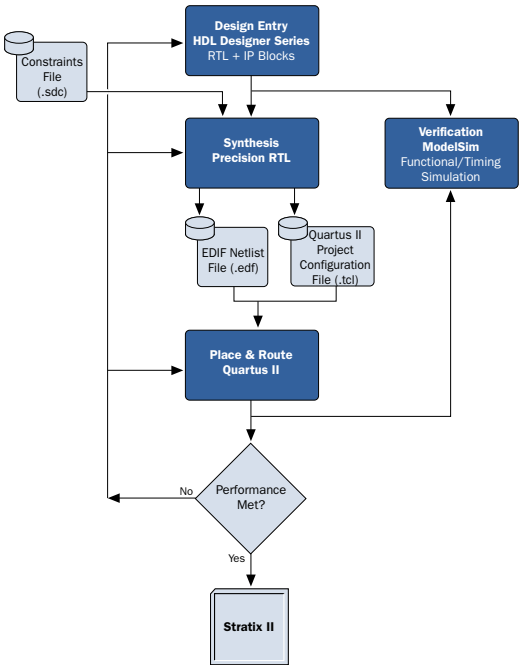
The design methodology (see Figure 1) from design entry to programming your device is the same for Stratix II and Stratix devices. Use the Mentor Graphics® HDL Designer™ Series or Precision Synthesis (both of which are part of the FPGA Advantage® product, that also includes ModelSim®) to create the register transfer level (RTL) description of your design. Then, select the desired target technology, enter design constraints in the industry-standard Synopsys Design Constraint (SDC) format, and synthesize the design using Precision Synthesis. Two files are generated after synthesis: a tool command language (Tcl) file that forwards the constraints specified during synthesis to the Quartus® II software, and an EDIF netlist file that is optimized for the target architecture. Place and route the design using the Quartus® II software. Use the ModelSim simulator to perform functional and timing simulations to verify the design at various stages of the design flow.

ALM Support

Altera introduces the ALM, a unique logic structure in the Stratix II family. The ALM has eight inputs, allowing it to efficiently support various configurations such as 6- or 7-input look-up tables (LUTs) or two independent 4-input LUTs. Each ALM also contains two embedded full adders to decrease the number of logic levels for arithmetic operations, enabling the addition of two 4-input functions or the addition of three numbers using one carry chain in the shared arithmetic mode. For more information about the Stratix II ALM, refer to "New & Innovative Stratix II Logic Structure Brings Unprecedented Performance & Logic Efficiency" on page 33.

The flexibility offered by the Stratix II ALM structure provides many implementation possibilities. Precision RTL Synthesis balances the distribution of various LUT sizes by selecting the best configuration

Figure 1. Stratix II Design Flow



for each ALM, based on the design functionality and timing constraints.

For a simple 8-to-1 multiplexer design described below, Precison uses two LUT5s and one LUT7 for Stratix II devices, while it takes six LUT4s for Stratix devices. The number of logic levels in the critical path for this design has decreased from three LUTs to two LUTs in Stratix II devices, as shown in Figure 2. The unique Stratix II ALM architecture results in smaller area and faster performance for your designs.

```
architecture RTL of MUX81_ALL is
begin
 main:process (SEL,A,B,C,D,E,F,G,H)
  begin
          case SEL is
              when "000" => Y <= A;
              when "001" => Y <= B;
              when "010" => Y <= C;
              when "011" => Y <= D;
              when "100" => Y <= E;
              when "101" => Y <= F;
              when "110" => Y <= G;
              when "111" => Y <= H;
              when others => Y <= H;
          end case;
 end process main;
end RTL;
```

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Similarly, Precision Synthesis uses other features of the ALM, such as the built-in adders, to maximize performance and decrease logic resource usage for your designs.

DSP Block Support

Stratix II devices have dedicated digital signal processing (DSP) blocks that are optimized for implementing intensive arithmetic operations such as add, subtract, multiply, multiply-add, or multiply-accumulate. These operations are common in most DSP designs using finite impulse response (FIR) filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT), direct cosine transform (DCT), encoder/decoder functions, and error correction/detection functions.

Precision RTL Synthesis automatically infers the appropriate megafunctions (`altmult_accum`, `altmult_add` or `lpm_mult`) from the HDL code for implementation in the dedicated DSP resources.

TriMatrix Memory Support

The TriMatrix™ memory structure consists of three different sizes of embedded RAM blocks (512-bit M512 blocks, 4-Kbit M4K blocks, and 512-Kbit M-RAM blocks). The memory blocks can implement true dual-port, simple dual-port, single-port RAM, ROM, and first-in first-out (FIFO) blocks. Both M512 and M4K blocks can also be configured as shift registers. In Stratix II devices, the memory blocks now support the use of an address stall feature and provide additional clock enable functionality.

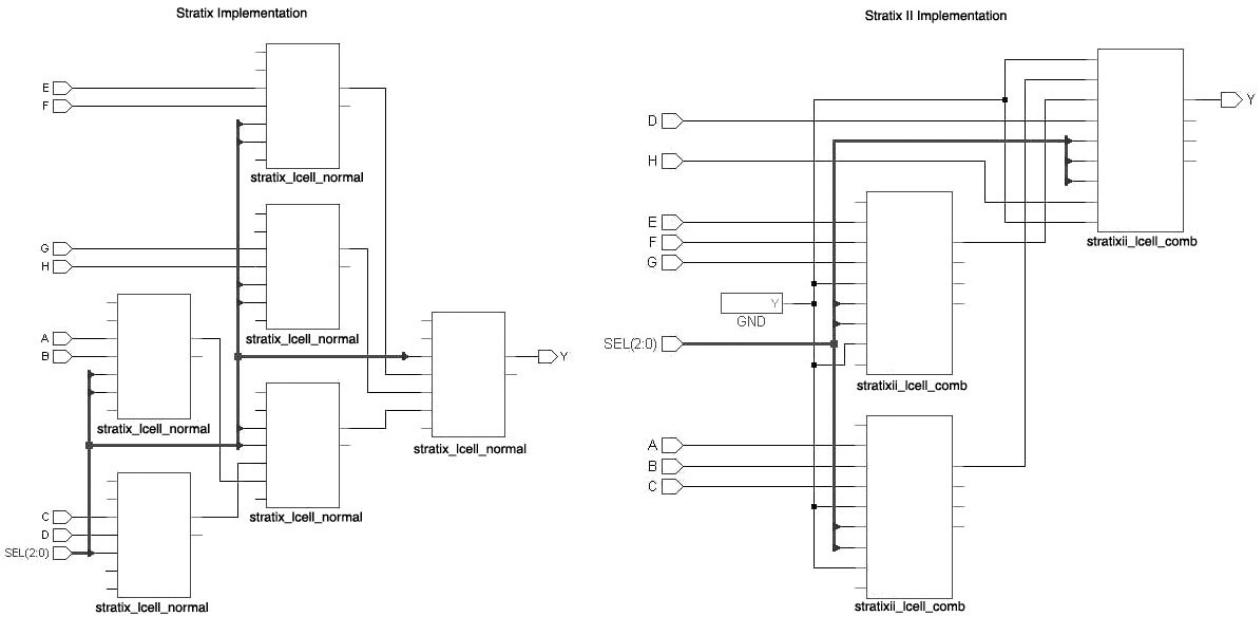
Precision RTL Synthesis infers memories and shift registers from generic HDL description and implements them in the appropriate Stratix II memory blocks using the `altsyncram` and `altshift_taps` megafunctions. For example, Precision infers an `altsyncram` megafunction from the following HDL code that describes a RAM with an address stall option.

```
always @ (posedge clk)
begin
  if (!addr_stall)
    real_addr = addr;
  if (wren)
    mem[real_addr] = din;
  dout = mem[real_addr];
end
```

Conclusion

The unique architecture of Stratix II devices with the ALM structure, DSP blocks, and memory resources, offers tremendous flexibility for many different design applications. This flexibility makes the role of a synthesis tool even more important in obtaining the best results for your design. Precision RTL Synthesis uses its advanced optimization algorithms to find an optimal implementation for a design utilizing the new Stratix II ALM, DSP blocks, and memory block resources.

Figure 2. Implementation of an 8-to-1 Multiplexer in the Stratix II Device versus a Stratix Device



System Design with Multi-GHz Serial Links: Clearing the Hurdle

by Brad Griffin
Product Marketing Director
Cadence Design Systems, Inc.

If you want to build competitive systems featuring Stratix™ GX high-speed serial interface (HSSI) links or Stratix II 1-Gbps high-speed interface links, you need to use multi-gigahertz (MGH) serial data links. However, there are three issues with these MGH serial data links that have created a hurdle for systems designers to overcome to keep their projects on schedule and on budget. These issues are as follows:

- I/O buffer information specification (IBIS) models don't support MGH serial data links
- Encrypted SPICE models have compatibility and convergence issues
- High-frequency signals put performance demands on simulation tools because of the need to simulate large quantities of random bit sequences to understand the effects of signal loss

IBIS Models

Simulating MGH serial links requires the ability to model advanced driver and receiver behaviors, such as active and/or passive driver pre-emphasis and receiver equalization. Receivers are expected to progressively get more complex, and may include both passive and active analog equalizers as well as digital decision feedback equalizers (DFE). Because these behaviors are not well supported by industry-standard IBIS specifications, users have had to turn to transistor-level SPICE simulators to perform analysis.

SPICE Models

Since MGH serial links are typically proprietary, SPICE models of the I/O buffers are normally only distributed in an encrypted format. Encrypting a model provides the model distributor with a level of security, but the consumer of that model now has to use the simulator that supports the encryption. This creates an issue if any of the other devices in the circuit under simulation are not compatible with the simulator that supports the encryption.

Performance

Most importantly, there is the performance issue. If you have ever simulated a few dozen bits with a circuit simulator using transistor-level SPICE models, then you know you must wait all day for the results from just one simulation run.

Solution for Stratix GX

To overcome the hurdle that these MGH issues create, Altera and Cadence Design Systems have jointly developed a solution for the Stratix GX FPGA. This solution—the Stratix GX design-in kit for the Allegro platform—is a silicon design-in kit featuring Device Modeling Language (DML) MacroModels for MGH applications, as well as sample topologies and electronic constraints that are native to the Cadence printed circuit board (PCB) design environment.

The Allegro system interconnect design platform is well known for supplying an ideal integrated simulation and design environment featuring integrated constraint management. However, with the migration away from IBIS to transistor-level I/O buffer models, systems designers may not understand that the Allegro simulation environment supports behavioral modeling constructs beyond what can be represented in a standard IBIS model.

Silicon Design-In Kits

Electrical and physical design-in is often delayed by the need to interpret the documentation from the semiconductor company. Interpreting these documents and performing analysis to validate the device meets performance requirements can take weeks for each of the complex devices that are considered for the system. Systems designers benefit from the availability of silicon design-in kits to accelerate their design-in time. Starting with the kits instead of mere documentation jump-starts the design-in process and reduces a design cycle by months.

Silicon design-in kits provide examples that illustrate a circuit's behavior in electrical topologies that capture the topology limits as boundary constraint templates. Systems designers can modify the sample topologies based on their own system requirements and quickly learn what modifications are necessary to ensure that the Altera® HSSI transceivers are satisfactorily driving the interconnect required to meet their system's specifications.

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The kits also include an electronic reference PCB design with physical examples of an interconnect adhering to the boundary constraint templates. Working with these physically-implemented constraints gives designers an option to re-use working constructs or to easily explore the performance impact of modifications.

Device Modeling Language (DML) MacroModels

DML MacroModels are behavioral driver or receiver IOCell models described in SPICE syntax, using the circuit elements supported by the Allegro PCB SI time domain simulator.

MacroModels provide a powerful behavioral device modeling capability. They combine table-based IBIS data with the flexibility of node-based SPICE circuit descriptions, then add SPICE circuit elements (such as resistors, capacitors, inductors), and a wide variety of voltage and current sources. Using these techniques, Allegro or Allegro PCB SI can be easily used to model advanced MGH behavior such as:

- Active or passive driver pre-emphasis
- Active or passive receiver equalization
- Receiver amplification

Carefully constructed MacroModels are capable of matching transistor-level device model accuracy while simulating at several hundred times the speed. For example, detailed MGH simulations of 100-bit streams taking over five hours with transistor-level models can be simulated in about one minute with MacroModels. These models can be used directly in the Allegro PCB SI, providing systems designers with productivity gains and a familiar use model with their well-integrated design flow.

Stratix II Design Issues & Solutions

Altera and Cadence are also addressing high-speed system design issues associated with Stratix II devices. As mentioned earlier, systems utilizing Stratix II devices that support data transfer rates up to 1-Gbps will be subject to many of the same signal integrity issues that MGH applications encounter. Stratix II systems featuring high-speed interfaces such as SPI-4.2, RapidIO™, and NPSI will benefit from the design-in aids that Cadence and Altera provide.

Access to Design-In Kits & Models

The challenge for users is obtaining the silicon design-in kits and models. Cadence is working with Altera and other semiconductor companies to provide an array of design-in aids. The easiest way to develop MacroModels for the Allegro PCB SI is to start with a well-documented working model, as it is easier to edit an existing working model than create one from scratch. Examples of MGH drivers and receivers are accessible through **www.allegrosi.com**, and can be copied and used as the basis for new models, allowing users to tweak parameters, substitute VI curves, and make other modifications. With good examples, it is expected that experienced Allegro PCB SI users will be able to quickly model complex drivers and receivers for use in simulating MGH serial data links.

More Information

For more information, visit **www.altera.com** or **www.allegrosi.com** or contact an Altera sales representative.

MAX II CPLDs: Addressing the Increasing Requirements of Control Path Applications

A New Architecture to Meet Needs

Electronic systems have been increasing in complexity for a number of years. Simultaneously, competitive and economic pressures—especially for consumer, automotive, and computing applications—limit the prices manufacturers can charge for these systems, despite increased capabilities. In addition, as electronic systems become more mobile and battery-dependent, system power consumption is becoming an increasing concern in a wide range of applications. As a result, there is a growing need for a family of CPLDs with high densities, faster performance, and reduced power requirements at a low price.

Control path applications such as power-up sequencing, I/O expansion, system configuration and initialization, and interface bridging are commonly implemented in CPLDs. CPLDs are ideal for these applications because they meet the instant-on, non-volatile requirements while offering robust, low-cost I/O pins. The MAX® II device family, with its low cost, high density and high I/O pin counts, is optimized for such functions.

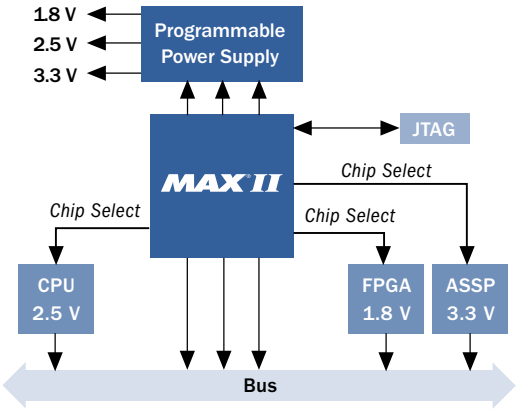
Power-Up Sequencing

With their low cost per I/O pin and higher densities, MAX II devices are ideal for power-up sequencing. Power-up sequencing is the process of bringing a board to full operating status without any device failures or glitches on the I/O pin. This task becomes more challenging as the number of board voltage planes and board complexity increase.

In this application, the CPLD ensures that the printed circuit board (PCB) powers up according to the requirements of all its devices. The power-up sequence is usually managed by a state machine in the CPLD that controls the timing at either predefined interval or on receipt of ready signals from other devices on the same board. The CPLD controls all device resets and is, therefore, also the logical choice for controlling individual chip selects. In multi-voltage systems, the power-up function requires a CPLD that can be instantly on and ready to manage the power-up sequence for other power planes on the PCB.

Figure 1 illustrates a typical MAX II device power-up sequencing application. In this example, multiple power rails support devices at different voltage levels; control logic is used to manage each device's power-up sequence. As the number of voltage levels increases, power-up control logic grows in complexity, demanding an instant-on device with increased logic capacity. MAX II devices can also be used to control critical bus signals until the power up is completed, ensuring these signals are not driven during the power-up process.

Figure 1. Multi-Voltage System Power-Up Management



Interfacing with other devices involved in the power-up sequence requires a large number of I/O pins. This requirement increases as the number of signals required to complete a system's power-up sequence grows. As a result, new systems will use higher-density CPLDs to implement the control logic.

System Configuration & Initialization

Once powered up, many volatile devices must be configured or initialized to be operational. This device configuration application is most cost-effectively implemented by MAX II CPLDs.

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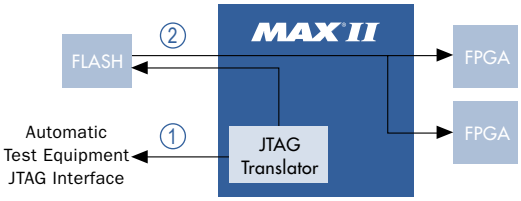
A MAX II device can be used, for example, to implement a state machine that configures an FPGA. Typically, a memory controller is used to manage the bitstream download to the FPGA at the same time. Using a MAX II CPLD allows the designer to use a low-cost, general-purpose flash device on the system board for configuration. Alternative solutions such as a vendor-specific serial configuration device or a microcontroller are less cost-effective than using MAX II CPLDs.

As shown in Figure 2, MAX II devices can interface to general-purpose flash memory to configure multiple FPGAs. This cost-effective, flexible solution can be implemented using any shared, low-cost flash memory device on the system board. High-density MAX II CPLDs can be used to implement complex configuration systems—including multiple pages in the flash memory devices—and can be used to reconfigure the FPGA as needed.

Figure 2. FPGA Configuration Management & Flash Controller



Step 1: Program Flash via JTAG Translator on MAX II Device
Step 2: Configure FPGAs

MAX II devices contain 8 Kbits of user-accessible flash memory that can store the initialization data required by ASSPs. It reduces board component count and costs by replacing small serial flash memories that would be used to store this data. MAX II CPLDs are the first and only PLDs that offer this feature.

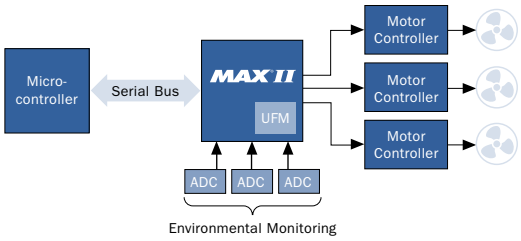
Like other CPLDs, MAX II devices can load bitstreams from discrete non-volatile devices to FPGAs or to program such memories during manufacturing. Shown in Figure 2, the MAX II device's JTAG translator feature can configure the flash storage device via the MAX II device pins, making MAX II JTAG circuitry available to non-JTAG enabled devices, thereby reducing manufacturing complexity and cost.

I/O Expansion

Insufficient I/O resources is a common board-level problem for digital designers. As semiconductor process geometries shrink, the size of the I/O pad ring becomes a significant portion of the die size, dictating semiconductor unit cost. As a result, many semiconductor manufacturers reduce the number of general-purpose I/O pins per device to minimize die size. At the same time, many board systems are becoming more complex with growing I/O signal distribution requirements. To support the need for additional I/O pin, both FPGAs and CPLDs are commonly used for I/O expansion functions.

I/O expansion mainly involves address-decoding functions in the CPLD that control signal distribution to multiple chips or to control LEDs and switches. Such functions require a large number of I/O pins. Figure 3, for example, shows a microcontroller with limited I/O capability controlling multiple devices in a system using only a two-wire serial bus. In this example, a MAX II device distributes the control data to manage multiple fan motor controllers. MAX II devices can also convert data from parallel to serial for functions that involve receiving information in parallel from analog-to-digital converters (ADC) and communicating it to microcontrollers via two-wire serial buses. Also, the MAX II device can use its 8 Kbits of on-chip user flash memory to store information, such as motor frequency or duty cycles.

Figure 3. Control Signal Distribution



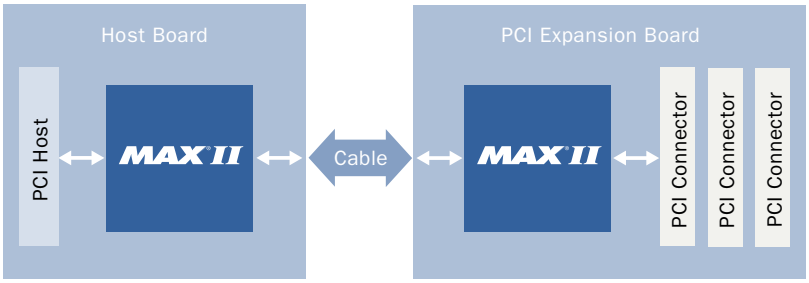
Interface Bridging

Facilitating communication between components on a PCB is a significant challenge. These applications are categorized as interface bridging, and include serial-to-parallel conversions, converting non-compatible bus standards and voltage leveling. While some of these conversions may be industry-standard, others are unique to a particular design, requiring the use of PLDs. While it is possible to use either an FPGA or a CPLD for such applications, the requirement often is for high I/O pin counts. MAX II CPLDs offer the lowest cost method to implement this function in those cases where the needed device density is determined by the I/O pin requirement. In addition, using the higher-density MAX II devices enables the support of complex bus systems. For example, MAX II devices support a 32-bit, 33-MHz, PCI-compatible, IP core.

MAX II devices can implement address decoding on the wide-input functions, often required in this application, without losing resources due to the lack of useable outputs from the logic block. Performance and fitting requirements can be met without extensive use of input sharing, which improves second-time fitting. Software is also used to optimize the wide-input functions for the LUT-based architecture, providing fast and efficient logic implementation.

Figure 4 shows two MAX II devices forming a PCI bridge between two boards to enable the integration of an optional add-on board to the PCI bus sub-system. The large MAX II devices can be added to a PCI bus as a 32-bit PCI target operating at 33 MHz. They can be physically separated via a cable or as part of a backplane configuration. MAX II devices can also act as repeaters for other bus systems. This type of configuration increases the drive strength of the bus, and the number of devices that can be supported on the bus.

Figure 4. PCI Bus Bridge



Integrating Multiple Functions into a Single Device

Many end-use electronic system applications are both cost- and size-sensitive. Integrating two or more of the key control path applications into a single device can deliver significant cost and board real estate savings that make the end-product more competitive. MAX II devices, with up to 2,210 logic elements, 272 I/O pins, and 8 Kbits of user flash memory, provide an ideal platform on which to integrate these applications.

Conclusion

Control path functions are increasing in complexity, and traditional CPLD architectures cannot cost-effectively support the increased functionality required. Leveraging Altera's new low-cost MAX II CPLD family, with its groundbreaking new CPLD architecture and unique features, designers can introduce new, smaller, and more powerful systems at a lower cost.

Effective FPGA Performance Benchmarking—Comparisons Between Leading FPGA Architectures

FPGA performance is a critical factor in enabling designers to maximize system processing speed at the lowest cost. It also allows designers to manage risk by increasing the system-performance margin. The increase in FPGA architecture complexity and rapid advancements in development tools make comparing FPGA performance challenging.

During the early stage of the design process, vendor-supplied performance comparison results are often used as a guideline for choosing which FPGA to use. The lack of an industry-standardized benchmarking methodology forces FPGA vendors to adhere to their own benchmarking methodologies, which can lead to flawed or severely skewed results.

Altera recognizes that meaningful benchmark results can be obtained only through a fair and objective benchmarking methodology. Altera invests significant resources to ensure the accuracy of benchmarking results. Tables 1, 2, and 3 show a relative f_{MAX} performance comparison between Altera® and Xilinx programmable logic families.

On April 8, 2004, Altera will host a net seminar on how to conduct effective FPGA performance benchmarking of leading FPGA architectures. To register for this net seminar, visit the Altera web site at **www.altera.com**. Detailed benchmark results and architecture comparisons between Altera and Xilinx FPGA families can be found on the Altera® web site.

Related Material

- *Stratix vs. Virtex-II Pro FPGA Performance Analysis* white paper
- *Cyclone vs. Spartan-3 FPGA Performance Analysis* white paper
- *FPGA Performance Benchmarking Methodology* white paper

Table 1. Altera & Xilinx High-Performance FGPA Relative f_{MAX} Performance Comparison

Comparison Category	Altera		Xilinx	
	FPGA Family	Relative f_{MAX} Performance	FPGA Family	Relative f_{MAX} Performance
130-nm FPGA	Stratix	1.0	Virtex-II Pro	1.0
90-nm FPGA	Stratix II	1.5 (1)	Next-Generation Family	1.0 to 1.2 (2)

Notes to Table 1:

(1) Stratix™ II relative comparison is comparing against the Stratix family.

(2) The anticipated performance of the next-generation Xilinx family based on 90-nm transistors in a 130-nm process of the current Virtex-II Pro family.

Table 2. Altera & Xilinx Low-Cost FPGA Relative Performance Comparison

Cyclone Relative f_{MAX} Performance	Spartan-3 Relative f_{MAX} Performance
>1.5	1.0

Table 3. Altera & Xilinx CPLD Relative Performance Comparison

MAX II Relative f_{MAX} Performance	CoolRunner II Relative f_{MAX} Performance
~1.4	1.0

Secure Your Design with Stratix II FPGAs

As the commercial and military environments become more competitive and more products are manufactured and shipped globally, designers have increasing concerns of protecting their intellectual property (IP) and sensitive system data. SRAM-based FPGAs are traditionally used in places where design security is not a concern. This all changes with Stratix™ II FPGAs, as designers can now leverage the benefits and flexibility of a high-density FPGA, with the peace of mind that their designs are secure. Stratix II devices are the industry's first FPGAs to provide configuration bitstream encryption using the advanced encryption standard (AES) algorithm with a 128-bit, non-volatile key.

Design Security

Design security is becoming more important as FPGAs move from glue logic to core logic in the system, and more customer-developed IP is delivered to market via FPGAs. For example, the military is deploying a growing number of increasingly complex electronic systems, the commercial electronics environment is becoming more competitive, and more products are manufactured and shipped globally. As a result, designers are faced with an increasing need to protect sensitive system information and proprietary IP.

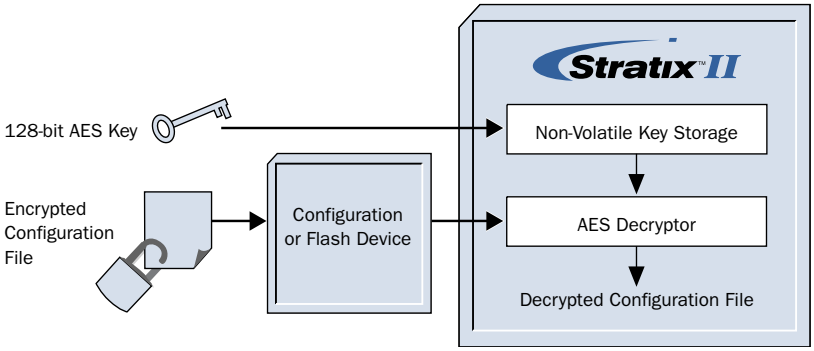
The level of security required by a particular product depends on a variety of factors including the system's function, application and physical location. In addition, usually only those components performing critical system functions actually require protection. In the past, such functions were most often implemented in inflexible ASICs, or in other non-volatile devices with much lower density. SRAM-based FPGAs are the only programmable devices that provided both flexibility and density. However, they were traditionally not used where design security was a concern, because they are volatile and required external memory to store configuration data. At power up, the configuration data is sent from the external memory to the FPGA. This scenario could result in the interception of the bitstream during transmission. With configuration bitstream encryption, Stratix II devices provide the flexibility and density of SRAM-based FPGAs and also provide design security.

Stratix II FPGAs Enable Design Security

Stratix II design security is enabled by encrypting the configuration file. Stratix II devices have a built-in AES decryptor and a 128-bit non-volatile key storage. Figure 1 shows a secure configuration flow, which is implemented in three steps:

1. The 128-bit AES key is programmed into the non-volatile key storage in the Stratix II device.
2. The Quartus® II software uses the same AES key to generate an encrypted configuration file, which is then stored in a configuration device or flash memory.
3. At power-up, the configuration or flash memory device(s) sends the encrypted configuration file to the Stratix II device, which then uses the stored AES key to decrypt the file and configure itself.

Figure 1. Stratix II Secure Configuration Flow



AES is a new encryption standard that was developed by the U.S. National Institute of Standards and Technology (NIST) to replace the Data Encryption Standard (DES). AES has been approved by the Federal Information Processing Standard (FIPS) for use by U.S. Government organizations to protect sensitive, unclassified information (see FIPS-197). The standard is expected to be adopted internationally.

continued on page 32

AES uses the same key which comes in various sizes for encryption and decryption. Altera has selected the 128-bit key for optimal security and efficiency. Studies have shown that if one could build a machine that could crack a DES key in seconds, it would take that same machine approximately 149 trillion years to crack a 128-bit AES key (source: NIST).

With AES encryption, the encrypted configuration file exists only in the system. Without the key, the configuration file cannot be decrypted, analyzed, or used to configure another FPGA, preventing IP theft. The Stratix II FPGA's non-volatile memory eliminates the need for an external back-up battery when the system is powered down.

US Export Controls

The US export controls for the Stratix II family are generally governed by the US Export Control Classification Numbers (ECCN) 3A001 or 3A991. Despite the Stratix II family's encryption/decryption capabilities, the export control classifications are not impacted because its decryption capability is only used to protect the configuration bitstream. Contact **opexp_imp@altera.com** with any export-related questions.

Conclusion

As FPGAs continue to displace ASICs and ASSPs, there is a growing need to protect the IP they contain. Altera's Stratix II FPGAs are the first high-density FPGAs in the industry to provide IP protection using 128-bit AES and a non-volatile key.

With this new design security feature, designers can now leverage the flexibility of FPGAs while also protecting their designs.

New & Innovative Stratix II Logic Structure Brings Unprecedented Performance & Logic Efficiency

The 90-nm node has proven to be a challenging stop on the march through submicron process geometries. Submicron effects have forced semiconductor companies to make decisions that tradeoff performance, power, and area. Faster performance and higher densities no longer come automatically for FPGAs as they have in the past. With current generation, 4-input look-up table (LUT)-based architectures reaching their performance limits, Altera decided to address this in the most effective manner: the development of a completely new logic structure.

Continuing its strong tradition of innovation, Altera designed a new logic structure for the 90-nm-based Stratix™ II family with LUT resources that can adapt to custom logic functions, depending on each function's input width. With this new and innovative logic structure, the Stratix II family offers an average 50% boost in performance while minimizing the power consumption. The adaptive nature of Stratix II logic structure dramatically reduces the logic resource requirements (by an average of 25%) for a given design.

Of the 80 benchmarked designs, the Stratix II family shows great advantages in both performance and logic efficiency over the Stratix family. Figure 1 shows the results of the entire benchmark design set, where each data point represents the comparison ratio for a design. R_p and R_l represent the performance and logic efficiency comparison ratios of a design.

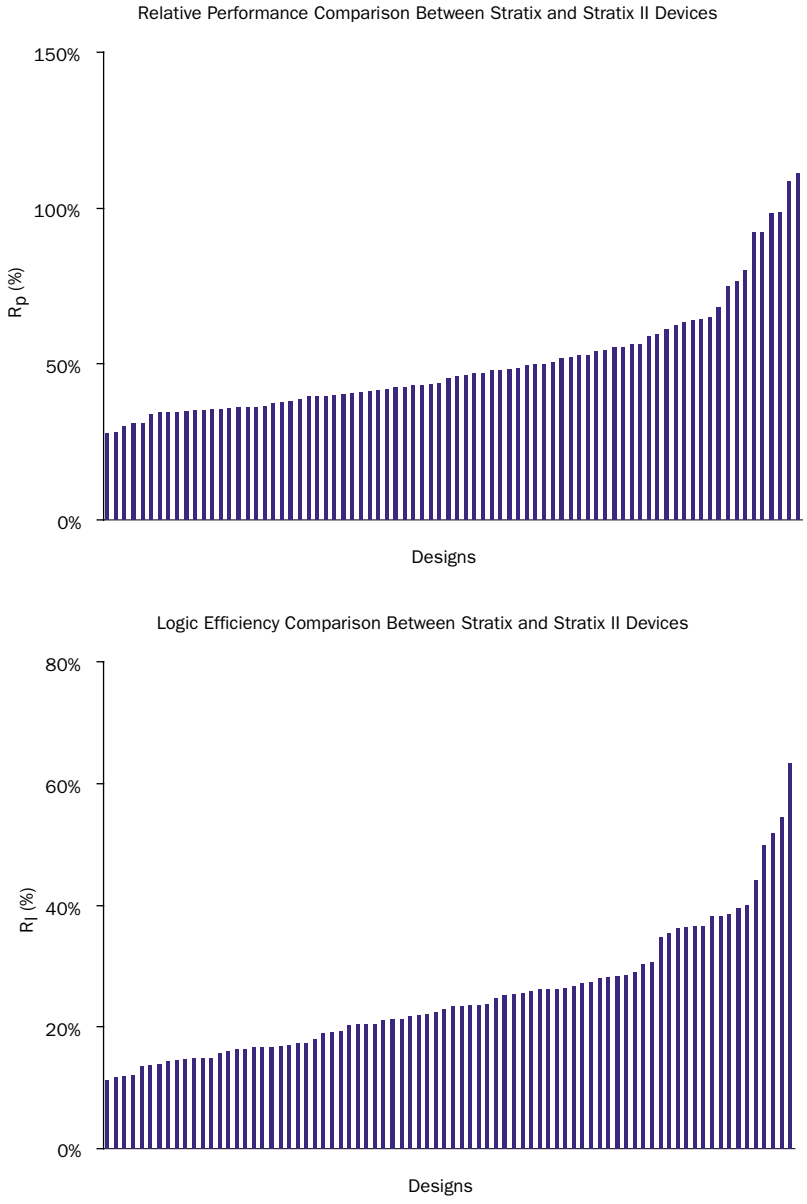
Stratix II Adaptive Logic Module

The Stratix II devices' logic structure is based on a matrix of logic array blocks (LABs) for implementing custom logic functions. Each LAB contains eight adaptive logic modules (ALMs)—the basic building block of logic for Stratix II devices. Each ALM can be configured to perform combinational logic functions of the same or different input widths or logic-and-arithmetic operations. Table 1 on page 34 shows a summary of various supported configurations in an ALM.

Stratix II Performance & Logic Efficiency Advantages

Research has shown that FPGA logic fabric with wider LUTs is more optimal for the performance versus fabrics with narrower LUTs. Narrower LUTs are more optimal for area efficiency and hence cost as shown in Figure 2 on page 35. To achieve the optimal cost-performance cross point, the development of FPGA logic structure has been primarily based on the fixed-size 4-input LUTs over the past decade.

Figure 1. Customer Design Benchmark Relative Performance & Logic Efficiency Comparison Note (1)

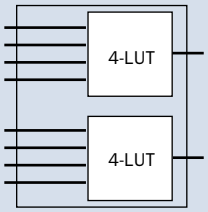
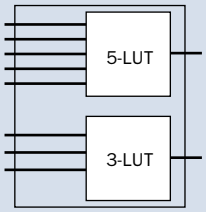
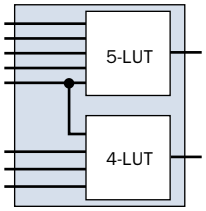
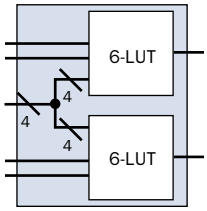
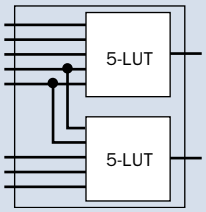
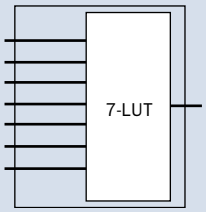
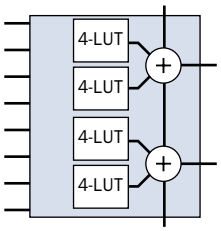
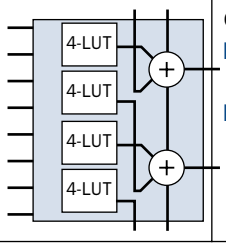


Note to Figure 1:

(1) The performance and logic utilization of a design depends on the design details, optimization techniques, CAD software algorithms, and device capabilities. The benchmark data shows typical results. Individual results may vary.

continued on page 34

Table 1. ALM Adaptive Combinational Logic & Arithmetic Configurations *Note (1)*

Configuration	Description	Configuration	Description
	**Two independent 4-input (or smaller) LUTs** ■ Backward compatible to 4-input LUT FPGAs ■ Allow easy migration to the Stratix II family		**One 5-input LUT and one 3-input LUT** ■ The two LUTs are independent ■ 5LUT-2LUT configuration is also allowed
	**One 5-input LUT and one 4-input LUT** ■ One input is shared between the two LUTs ■ 5-LUT has up to 4 independent inputs ■ 4-LUT has up to 3 independent inputs ■ The Quartus® II software automatically seeks to find this construct		**6-input LUT support** ■ One ALM can implement any 6-input function ■ Two 6-input functions with four shared inputs have the same logic operation and can fit in one ALM. Example: 4 × 2 crossbar switch and 6-input AND gate
	**Two 5-input LUTs** ■ Two of the inputs between the LUTs are common ■ Three independent inputs are available for each 5-input LUT		**7-input LUT support** ■ One ALM in the extended mode can implement a subset of a 7-variable function ■ The Quartus II software automatically recognizes the applicable 7-input function and fits it into an ALM
	**Logic-arithmetic combined operation** ■ Two full adders are embedded in an ALM ■ Four 4-input LUTs can be used for pre-arithmetic logic ■ Example: data selection before summation		**Complex arithmetic operation** ■ Dedicated routing for complex arithmetic operations ■ Example: 3-input adder structure

Note to Table 1:
(1) Refer to the *Stratix II Device Handbook* for detailed architecture descriptions.

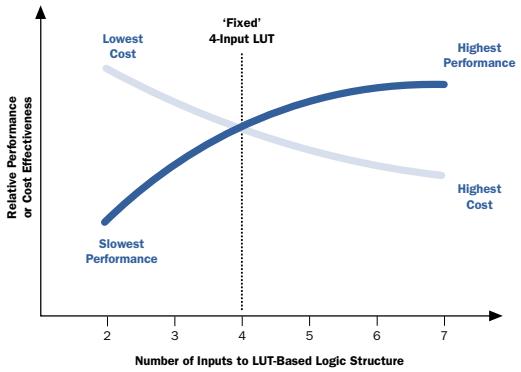
Altera's Stratix II FPGAs break the barrier of the fixed 4-input LUT FPGA cost-performance cross point and provide the architecture you need to raise the performance and reduce the cost of your systems. By supporting LUTs with input widths of up to 7 inputs, Stratix II devices offer high performance, comparable to a wide-input-LUT-based FPGA. In addition, the versatility of the Stratix II ALM enables the logic efficiency better than that of a 4-input, LUT-based FPGA.

Empirical data shows that Stratix II family delivers an average 50% performance advantage over first-generation Stratix devices.

Inputs supporting logic functions with more than four inputs per ALM. The Stratix II logic structure increases the performance of your design by:

- Reducing the number of logic levels required for the overall combinational logic
- Reducing the extra programmable routing needed in fixed-4-input LUT implementations
- Reducing the stress on the demand for general routing resources

Figure 2. Conceptual View of Relative Performance, Cost Effectiveness & LUT Input Size Comparison



A fixed-size, 4-input-LUT FPGA architecture is less efficient when implementing logic functions that do not have exactly 4 inputs. The adaptive nature of Stratix II ALMs can minimize the logic resource inefficiency caused by partially utilized LUTs in a fixed-size LUT FPGA architecture through:

- Packing functions with larger input counts with functions with smaller input counts (see Figure 3)
- Reducing the need for logic duplication by sharing logic resources for different combinational logic with common inputs
- Implementing complex arithmetic functions and combining logic and arithmetic operations (e.g., data selection before summation and subtraction)
- Implementing high-input-count arithmetic functions such as an adder tree

The Stratix II family provides an ideal design platform to efficiently implement high-performance systems.

Case Study 1 – Crossbar Switch

In many telecommunication designs, FPGAs are often used in the data path to handle the ingress and egress data, for example, a crossbar switch. Figure 4 compares Stratix and Stratix II implementation of a 4 × 2 crossbar switch. This switch has four data input ports (*A* to *D*), two sets of select input ports (*SelectA* and *SelectB*) and two data output ports. The two sets of select signals (2 bits per set) are used to switch the data from input ports to the output ports.

To implement this crossbar switch in Stratix devices, four logic elements (LEs) are consumed. For each input to be switched to the output, two LEs are cascaded; each LE represents one logic level. The speed of the system is limited by the two logic levels and the programmable routing delay of the data path.

When implementing this same circuit in Stratix II devices, each bit of the 4 × 2 switch can be thought of as two 6-variable functions. Each function, based on different select lines, selects the same input data (*A* to D) to appear at the outputs. Since an ALM can implement two 6-input functions that have four common inputs and perform the same logic function, each bit of the 4 × 2 crossbar switch can be absorbed into just one ALM. This improves the performance by eliminating one logic level and the programmable routing while reducing the logic resource utilization by half. See Table 2 on page 36.

Figure 3. Stratix II ALM Logic Efficiency Example

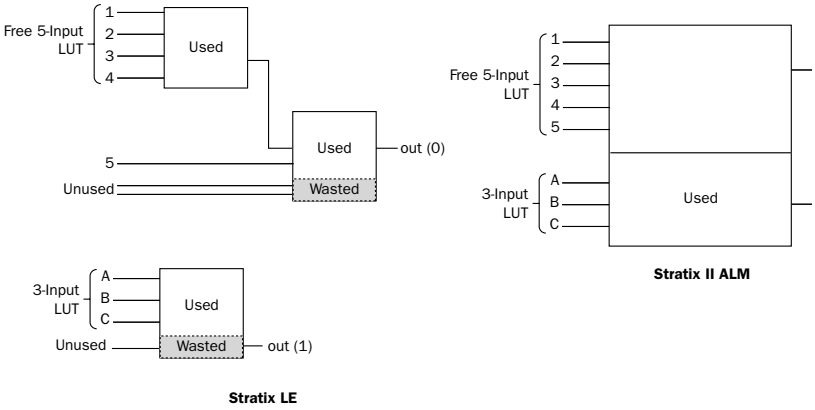
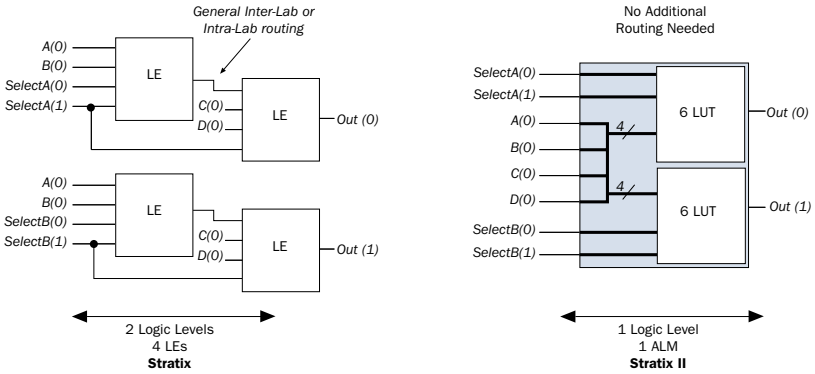


Figure 4. Stratix II vs. Stratix II 4 × 2 Crossbar Switch Implementation



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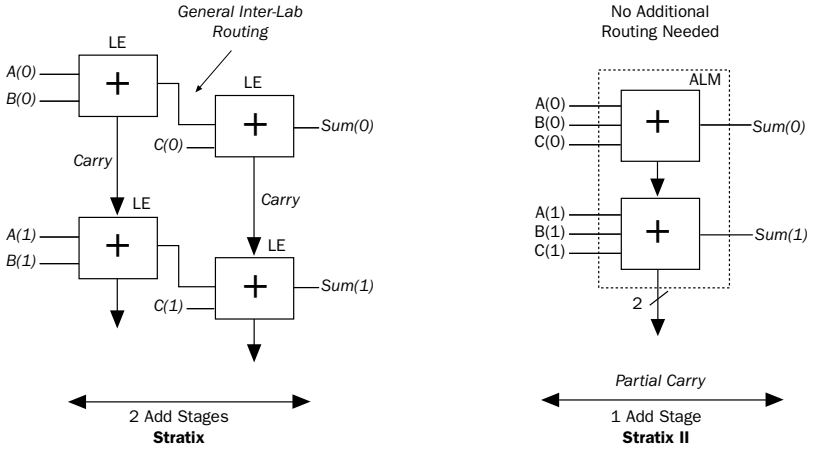
Case Study 2 – Adder Tree

In digital signal processing (DSP) applications, it is common to find the use of an adder tree to sum a large set of processed samples (numbers). For example, the correlators in the 3G wireless base station channel cards contain large adder trees to recover the data that is transmitted through spread-spectrum signals. Stratix II ALMs offer a great performance and logic efficiency advantage in adder tree implementation by supporting the summation of three numbers in one step. Figure 5 shows the Stratix and Stratix II implementations of a simple 3-input adder.

Figure 5. Stratix II ALM 3-Input Adder Advantage



When adding three numbers in a FPGA logic structure that only supports 2-input arithmetic operation, the sum is generated by repeatedly adding two numbers. The performance of this binary-tree style summation is limited by the delay of each add stage and by the delay of the programmable routing between each add stage.

The Stratix II ALMs support the ternary arithmetic operations (in shared arithmetic mode) that collapse the two add stages in to one and hence improve the performance by eliminating one add stage and the extra programmable routing. The performance improvement is even more obvious when the number of inputs to the adder tree increases. For fully pipelined implementation of an adder tree, Stratix II devices reduce the latency by reducing the add stages.

In addition to the performance gain that Stratix II devices offer, the logic resource requirement for an adder tree is greatly reduced. Instead of consuming 4 LEs in the binary-adder implementation as shown in Figure 5, the Stratix II devices can absorb the entire adder into one ALM.

Table 2 shows the benchmark comparison of adder trees between Stratix and Stratix II devices.

Conclusion

The Stratix II logic structure innovation has delivered unprecedented performance and logic efficiency over first generation of Stratix devices. On average, performance is 50% faster for a given design in Stratix II FPGAs and 25% more efficient. The Stratix II FPGA family provides a superior solution for you to cost effectively implement high-performance systems.

Table 2. Benchmark Comparison between Stratix II & Stratix Devices

	Performance (MHz) *(1)*		Logic Utilization	
	Stratix II	**Stratix**	**Stratix II (ALUT)**	**Stratix (LE)**
8-bit, 4 × 2 crossbar switch	696.86 *(2)*	472.81 *(2)*	16	32
128-number Adder Tree (Pipeline)	339.31	313.58	1,489	2,279
128-number Adder Tree (Non-Pipeline) *(3)*	108.92	64.41	1,209	2,279

Notes to Table 2:

(1) The performance and logic utilization of a design depends on the design details, optimization techniques, CAD software algorithms, and device capabilities. The benchmark data shows typical results. Individual results may vary with each design.
(2) The performance in MHz is derived from the propagation delay of the critical path.
(3) Pipeline registers are inserted between each add stage.

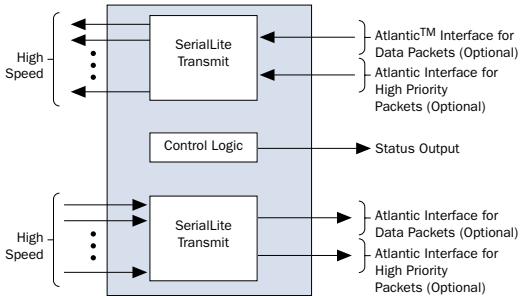
SerialLite Protocol Overview

This article provides an overview of the SerialLite protocol, describing its relationship to other serial standards and its basic functionality. SerialLite is a lightweight, point-to-point serial protocol suitable for both packet and streaming data applications. See Figrure 1.

The SerialLite protocol is designed to be:

- High-performance, supporting I/O speeds up to 3.125 Gbps
- Lightweight, utilizing under 700 logic elements (LEs) in an Altera® Stratix™ GX FPGA
- Simple and ready-to-use with easy-to-understand documentation on a stable platform
- Efficient and flexible, allowing the designer to utilize the features of SeriaLite that are most useful and eliminate the unwanted features
- Open source and accessibile for all platforms

Figure 1. High-Level SerialLite Block Diagram



Comparison to Other Serial Protocols

As a high-speed serial communication protocol, it is useful to compare SerialLite with other serial protocols, the highest profile of which are Serial RapidIO™ and PCI Express. These protocols and others like them address applications that are different from those targeted by SerialLite. They are intended to be heavyweight protocols for supporting large-scale networks or meshes of inter-operating systems, where the choice of systems that may inter-operate may be made by an end user. These requirements result in the following characteristics:

- Features are defined at a high level, and require either a very rich set of features, or an elaborate scheme for managing options to allow seamless inter-operation.
- Because of the existence of switches in the network, and the fact that data is intended to cross those switches to its intended destination, the protocols must include addressing information in the headers, leading to relatively complex framing and encapsulation.

Getting Data from Point A to Point B

Unlike heavyweight protocols, the SerialLite protocol is intended to solve the simple problem of getting data from one place to another. The system designer is responsible for ensuring interoperability of optional features. No addressing of the data is required since the protocol does not route data. This means that the protocol can be streamlined significantly, and that many features can be made optional. The existence of IP cores implementing the SerialLite protocol relieves the designer from the significant details involved in designing a serial scheme by hand. These characteristics make the SerialLite protocol particularly well suited to implementation in FPGAs, where the designer has complete control over options and can remove any unneeded logic at design time. Table 1 compares several serial protocols.

Table 1. Serial Protocol Comparison ***Note (1)***

Feature	SerialLite	Serial RapidIO	PCI Express	10G Ethernet (XAUI)	InfiniBand	CSIX over PICMG
Layers above Data Link Layer required		▲	▲	▲	▲	▲
Switching support required		▲	▲	▲	▲	▲
Arbitrary number of lanes	▲					
Arbitrary frequency	▲					
Lane polarity reversal	●				▲	
Lane order reversal	●		▲		▲	
Packet data	●	▲	▲	▲	▲	▲
Streaming data	●					
Synchronous operation	●					
Asynchronous operation	●			▲	▲	
Priority data	●	▲			▲	▲
No data error detection	●					
CRC-16	●	▲	▲		▲	
CRC-32	●			▲	▲	
Channel multiplexing (2)	●	▲	▲	▲	▲	▲
Flow control	●	▲	▲	▲	▲	▲
Retry On Error	●	▲	▲		▲	

Notes to Table 1:

(1) ▲ = Required Behavior ● = Optional Behavior.

(2) Because destination addressing can be thought of as a more elaborate form of channel multiplexing, all protocols supporting switching addresses can theoretically support channel multiplexing if the feature is so utilized.

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Functional Description

SerialLite defines packet encapsulation at the link layer and data encoding at the physical layer. Table 2 details SerialLite function relative to each layer.

Table 2. Physical Layer & Link Layer Functions

Physical Layer	
Transmit	**Receive**
Parallel to Serial Conversion 8B/10B Encoding IDLE Character Conversion Insert Clock Compensation Characters	Serial to Parallel Conversion 8B/10B Decoding Lane Alignment Character Alignment using Comma Control Symbol Check for Running Disparity Error and Invalid Character Error Clock Tolerance Compensation
Link Layer	
Transmit	**Receive**
Packet Encapsulation Packet Nesting IDLE Character Generation Link Initialization Flow Control (Optional) CRC Generation (Optional) Lane Striping for Multi-Lane Link	Remove Packet Encapsulation Link Initialization Separate Nested Packets IDLE Character Deletion FCS Verification (Optional) Generate Flow Control Commands Error handling Faulty Packet Retransmit Request Commands (Optional)

Link Configuration

A serial link can be composed of one or more lanes. Each lane is a full-duplex connection between a pair of transceivers. The collection of transceivers on one side of the link is jointly referred to as a port.

Data Encoding

SerialLite encodes physical lanes using the industry-standard 8B/10B encoding scheme as specified in Clause 36 of the IEEE 802.3-2002 Specification. This ensures that a clock signal can be successfully transmitted with the data, and that the clock can be recovered reliably at the receiver.

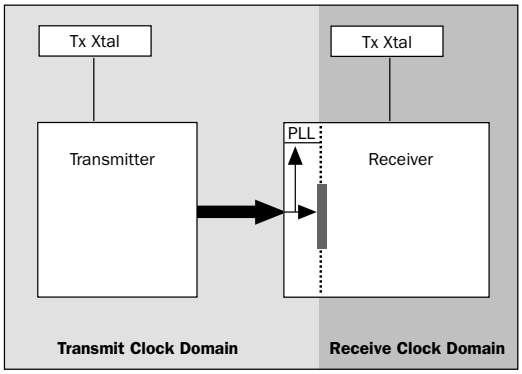
Synchronous & Asynchronous Operation

If the transceivers at both ends of a lane are clocked by signals derived from the same crystals, then data can be moved from transmitter to receiver with no loss of synchronization. This is referred to as a "synchronous" or "single-crystal" configuration.

In other cases, the transmitter is driven by a reference frequency with a given tolerance. The main logic of the receiver is driven by a different crystal of the same frequency and tolerance. This is referred to as an "asynchronous" or "multi-crystal" configuration. While the nominal frequencies of the transmitter and receiver are the same, the actual frequencies will differ by some amount because of the allowed tolerances. The worst case frequency difference occurs when one is at the fast end of its range and the other is at the slow end.

The transmitter embeds its clock signal into the transmitted data stream. The receiver, using a phase-locked loop (PLL), will recover the transmit clock from the incoming data stream. There are therefore actually two frequencies present in the receiver: the transmit clock frequency, as recovered from the data stream, and the receiver reference clock, as driven by the receiver's crystal (Figure 2). This slight mismatch in frequencies within the receiver means that either the data arrives slightly faster than the receiver can process it (which can cause data to be lost if not handled properly), or slightly slower (which may not be a problem).

Figure 2. Asynchronous (Multi-Crystal) Configuration



To compensate for this mismatch in frequencies, an "elastic buffer" is placed in the receive path. Data is written into the elastic buffer using the recovered transmit clock. Data is read out of the elastic buffer using the receive reference clock. The elastic buffer compensates for the differences between the transmit and receive clock domains by dropping or inserting clock compensation ordered sets.

The management of clock compensation sequences is transparently handled by the SerialLite protocol to any logic outside the SerialLite logic. This means that there is some slight bandwidth lost to the clock compensation sequence.

Uniquely among serial protocols, SerialLite allows operation in asynchronous mode, with automatic compensation, or in synchronous mode, where there is no compensation and the overhead and logic

required for compensation can be eliminated. This is a choice that is made at design time.

Link Initialization & Training

Link initialization and training is the process of synchronizing data within a lane and lanes within a link. This process occurs in three stages; lane initialization, link de-skew, and link up. Initialization is automatically handled by a SerialLite-compliant core. For maximal logic savings, the user can elect not to reverse lane polarity and/or lane order. The stages are described as follows:

- *Lane Initialization*: Each individual lane goes through this procedure to establish code group synchronization and determine correct lane polarity.
- *Link De-skew*: This process applies to multi-lane links only. It performs lane-to-lane de-skew within a link and determines correct lane order.
- *Link Up*: This stage waits for the remote port to complete its initialization and then declare link initialization complete.

User Packet Types

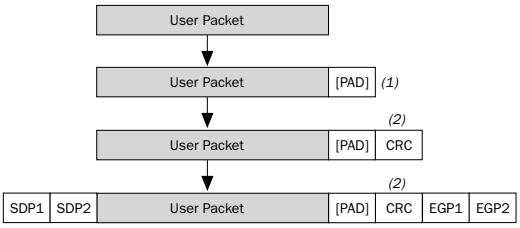
The SerialLite protocol supports two different user packet types; data packets and priority packets. These two types of packets are transferred through the two Atlantic interfaces shown in Figure 1.

- *Data Packets*: A "cut-through" data flow is used for data packets. This means that the transmitter starts transmitting the packet as soon as enough data has been received to place across all lanes. For large packets, it means that the receiver will have passed early portions of the packet on to the higher-level logic even before the transmitter has received the end of the packet.
- *Priority Packets*: A "store-and-forward" data flow is used for priority packets. This means that the transmitter will not begin transmitting a packet until it has received the entire packet. This is required to support the packet retransmission option.

User Packet Encapsulation

SerialLite encapsulates data and priority packets by wrapping start and end of packet symbols around them. The PAD symbol is conditionally inserted to maintain a word boundary. Optionally, a cyclic redundancy code (CRC) can also be generated and appended to the end of the user packet to protect against errors. Figure 3 shows how user packets are encapsulated.

Figure 3. User Packet Encapsulation



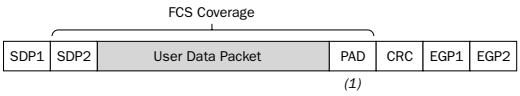
Notes to Figure 3:

(1) A PAD is required if the user packet has an odd number of characters.
(2) Optional.

Error Protection

SerialLite optionally provides CRC error-checking coverage to data and/or priority packets to protect against errors. Two types of CRC polynomials are supported; CRC-16 and CRC-32. The CRC covers all bytes from the second symbol of the start-of-packet sequence to the optionally inserted PAD symbol, as shown in Figure 4. The second start-of-packet symbol is protected because it contains the packet number, which is used if the retry-on-error feature is implemented.

Figure 4. CRC Coverage



Note to Figure 4:

(1) Optional.

Lane Striping

Lane striping is the process of distributing packet byte streams to multiple lanes within a link. SerialLite distributes a word (two bytes) of data at a time to each lane. Therefore, all transmitted data is word-aligned.

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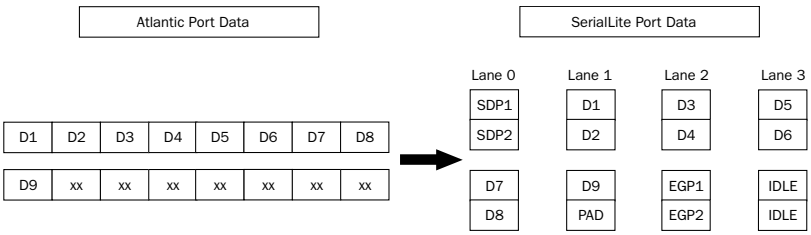
An example of striping of a nine-byte packet across a four-lane link is shown in Figure 5.

Figure 5. Lane Striping Example



Flow Control (Optional)

Flow control is an optional feature that can be implemented to ensure that data is not transmitted faster than the receiving system can consume it. A typical setup consists of a near transmitter sending data to a far receiver. Flow control allows the far receiver to exert "back pressure" on the data it is receiving. This gives the receiver a chance to catch up before the incoming data overflows the receiver buffer. The flow control is not required to compensate for transmit and receive clock frequency tolerance discrepancy. That is handled automatically by the clock compensation feature. Flow control would only be required for systems in which the designer expected that the logic outside of SerialLite might not consume the data quickly enough. If the outside logic isn't accepting the data fast enough, the internal storage will fill up. Flow control, if implemented, automatically causes data transmission to pause when the storage becomes too full.

SerialLite utilizes a "pause" flow control scheme. When the far receiver is not able to receive more data, the far transmitter sends a flow control packet (pause packet) to the near receiver to instruct the near transmitter to stop transmitting data for a user-defined period of time. The designer decides how far ahead of "full" to pause transmission. That consideration must take into account the amount of time it will take the pause command to reach the receiver, and how much data will already be "in flight" by the time the pause command is enacted.

Retry-on-Error (Optional)

Retry-on-error is an optional feature that provides a mechanism for ensuring the reliability of priority data transmission. A typical set up consists of a near transmitter sending data to a far receiver. Retry-on-error allows the far end to request re-transmission of priority packets that were received with errors. This requires the far transmitter to acknowledge every priority packet received. Re-transmission is only possible for priority packets, not for regular data packets. There are two types of acknowledgement:

- *ACK*: packet received is good and error free
- *NACK*: packet received with an error

SerialLite keeps track of packet numbers so that out-of-order packets can be trapped, and re-transmission restarted to recapture any lost data, and to discard any packets sent more than once. There is also a timeout mechanism so that any lost acknowledgment packets can be accommodated.

If the retry-on-error option is not implemented, then all packets are transmitted without any acknowledgements from the receiver.

Conclusion

The SerialLite protocol provides robust data transport for getting information from one point to another. Because it focuses only on the physical and data link layers, it is a simple, lightweight protocol. It is the only serial protocol to provide both an extremely small minimal configuration with the option of adding numerous capabilities only as required by the application.

SerialLite is targeted for designers that don't need higher OSI Reference Model layers, blind interoperability, or data routing supported by heavier-weight protocols. It also encompasses all of the key requirements for a wide variety of data transfer applications, so that designers making the transition from an older scheme to a serial scheme do not need to be burdened with the complex details involved in serial communication. By focusing on the higher-level requirements of the application and allowing a SerialLite-compliant core to implement the details, the designer saves many weeks of work, and is able to focus on high-level aspects of the application.

Resources

The following SerialLite resources are available on **www.seriallite.org**:

- Preliminary SerialLite Reference Design
- SerialLite Protocol Overview White paper version 1.0
- SerialLite Protocol Specification version 1.0

The full reference design and Altera® MegaCore® function will be available in May 2004.

Discontinued Devices

Altera will obsolete select devices from its FPGA families (see Table 1). Most devices will have a 12-month last-time buy period and an additional 6-month last-time shipping period to allow customers to transition to new components and ordering codes.

Table 1. Discontinued Device Update

Product Family	Device	Ordering Codes	Last Order Date	Last Shipment Date	Product Change Notice
FLEX® 10KA	Selected Devices	EPF10K10AQI208-3	12/15/04	06/15/05	PDN0314
FLEX 10KE	Selected Devices	EPF10K50SFI484-2	12/15/04	06/15/05	PDN0314
FLEX 6000	Selected Devices	EPF6016AQI208-2 EPF6016AQI208-3 EPF6016ATI144-2 EPF6024ABI256-2 EPF6024AQI208-3	12/15/04	06/15/05	PDN0314
FLEX 8000	Selected Devices	EPF81188AQI208-3 EPF8282ALI84-4 EPF8452AQI160-3 EPF8636AGC192-3 EPF8636ARC208-3 EPF8636ARC208-4 EPF8820ARI208-4	12/15/04	06/15/05	PDN0314
APEX™ 20K	Selected Devices	EP20K100BC356-1V EP20K100FC324-1V EP20K100FC324-2V EP20K100FC324-3V EP20K100QC208-3V EP20K100QI208-2V EP20K100QC240-3V EP20K100QI240-2V EP20K100TC144-1V EP20K100TC144-3V EP20K200BC356-1XV EP20K200FC484-1XV EP20K200FC484-3V EP20K200RI240-2V EP20K400BC652-1V EP20K400BC652-2V EP20K400BC652-2XV EP20K400BC652-3V EP20K400FC672-1V EP20K400FC672-1XV EP20K400FC672-2V EP20K400FC672-3V	07/22/05	01/22/06	PDN0401
APEX 20KE	Selected Devices	EP20K200EBI356-2X EP20K200EFI672-2X EP20K200EQI240-2X EP20K30EQC208-1 EP20K30EQC208-1X EP20K30EQC208-2 EP20K30EQC208-2X EP20K30EQC208-3 EP20K60EFI324-2 EP20K60EQI208-2X	06/15/05	12/15/05	PDN0316
Configuration Devices	Selected devices from the following device families: EPC1064, EPC1064V, EPC1213, and EPC1441 EPC16	EPC1064TC32 EPC1064VLC20 EPC1064VPC8 EPC16UC88AA	12/15/04 12/15/04	06/15/05 06/15/05	PDN0314 PDN0315

Contact Information

It is now easier than ever to get information and services from Altera. The table below lists some of the ways you can reach Altera.

Information Type	U.S. & Canada	All Other Locations
Product Literature	**www.altera.com**	**www.altera.com**
Altera Literature Services *(1)*	**lit_req@altera.com**	**lit_req@altera.com**
News & Views Information	**www.altera.com/literature/nview.html** **n_v@altera.com**	**www.altera.com/literature/nview.html** **n_v@altera.com**
Non-Technical Customer Service	(800) 767-3753	(408) 544-7000
Technical Support	**www.altera.com/mysupport**	**www.altera.com/mysupport**
	(408) 544-6401	(408) 544-6401 *(2)*
FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	(408) 544-7104	(408) 544-7104 *(2)*
	www.altera.com	**www.altera.com**

Notes:

(1) The Quartus II Installation and Licensing, Introduction to Quartus II, and MAX+PLUS II Getting Started manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.

(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for the latest listing.