News & Views

Second Quarter 2004

Newsletter for Altera Customers

Altera's Summer Blockbusters

Featuring Quartus II Version 4.1

ALTERA®

NV-2004-Q2

Sequels that Improve on the Originals—The Power of *II*

In his keynote address to the 2003 SIA Annual Forecast and Awards dinner, Altera CEO John Daane predicted that 2004 would be a "vintage year," one that would be highlighted by strong growth and considerable change in the semiconductor industry. Here we are half way into the year, and sure enough, the chip industry is experiencing a strong rebound. There is one significant change, however. While past up cycles were largely driven by communications or PC industry growth, today's expansion is driven by digital consumer applications. This is the era of the consumer, and, subsequently, it's also a period of fierce competition.

Because of our concerted effort to get closer to our customers and involve them in our product-definition process, we have gained deep and valuable insight into their end markets. What we saw early on, particularly in the consumer market, was the collision between radically shortened end-product lifecycles and the expensive and lengthy ASIC design cycle. Shortened product lifecycles and the resulting need to quickly innovate is a natural fit for FPGAs. It was with this in mind that Altera developed the first-generation low-cost Cyclone™ devices in 2002—specifically to address the needs of high-volume manufacturers who wanted to stay ahead in the race to the store shelves. As of this writing, over 3,000 customers are designing with Cyclone devices and we've shipped over three million Cyclone units around the world—setting a new Altera record for the fastest ramping product in company history.

Likewise, we developed the Nios® soft core processor to address processor obsolescence issues our customers were facing with hard embedded processors. By the time their design was finalized, the hard embedded core in the design was obsolete. The obsolescence-proof Nios processor can grow with design requirements—from one processor to as many as needed for higher processing power. The Nios processor has grown to over 12,000 licenses and counting. It is undoubtedly a smashing success!

This summer, Altera is proud to bring you sequels to those blockbusters—Cyclone II FPGAs and the Nios II embedded processor family. We've taken these two highly successful products and made them even better. This next generation of the Cyclone series maintains its low-cost leadership and offers even higher densities. The Nios II processor family delivers high-performance (200 DMIPS) and low-cost options with a new integrated development environment.

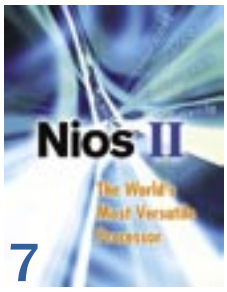
By combining the Nios II processor with Cyclone II FPGAs, you can build your own powerful 32-bit microprocessor for as little as $0.35 cents of logic—possibly the lowest-cost microprocessor in the market. And there's more: the free Web Edition of the Quartus® II software version 4.1 has full support for the entire Cyclone II family!

Also in this issue, our customers share their experiences using Cyclone FPGAs and the Nios processor to gain a competitive edge. In fact, Altera's drive for continuous innovation—three new silicon architectures, a new 90-nm process geometry, and a new family of embedded processor cores this year alone—is the result of a single objective: to give our customers the blockbuster solutions they need to win in this highly competitive marketplace.

Happy summer to all,

Jordan Plofsky,
Senior Vice President, Applications Business Groups

Cyclone II FPGAs



Nios II Processor

Quartus II Version 4.1

CycloneBot

Features

Devices & Tools

Customer Applications

Contributed Articles

Altera News

Questions & Answers

Publisher
John Panattoni

Technical Editor
Justin Bennett

Cover Layout
Paula Cruz

101 Innovation Drive
San Jose, CA 95134
Tel: (408) 544-7000
Fax: (408) 544-7809
n_v@altera.com
www.altera.com

Cyclone II: The Lowest-Cost FPGAs Ever

Furthering its low-cost FPGA leadership, Altera introduces the Cyclone™ II family, the latest in the Cyclone series of low-cost FPGAs. Altera forever changed the FPGA industry with the introduction of the Cyclone device family in 2002—bringing to market the first and only FPGA family designed from the ground up for the lowest cost. The Cyclone II FPGA family offers the same benefits as its predecessor—a customer-defined feature set, industry-leading performance, and low power consumption—but with more density and features—at dramatically lower costs. Cyclone II devices extend the low-cost FPGA density range up to 68,416 logic elements (LEs) and up to 1.1 Mbits of embedded memory.

Cyclone II devices are manufactured on 300-mm wafers using TSMC's 90-nm low-k dielectric process, the same proven process used with Altera's Stratix® II devices. To ensure rapid availability and low cost, by minimizing silicon area, Cyclone II devices can support complex digital systems on a single chip at a cost that rivals that of ASICs.

The Ideal ASIC Alternative

The evolution of the programmable logic industry has fundamentally changed the value proposition of FPGAs to include high-volume, low-cost applications. A few years ago, the closest an FPGA could get to low-cost applications was as an ASIC prototyping tool. With the increasing development and production cost of ASICs, FPGAs today are becoming the de facto standard for system design in the consumer, industrial, data communications, telecommunications, wireless, medical, and automotive markets. At prices comparable to ASICs, Altera's new Cyclone II device family delivers a low-risk, low-cost, and fast time-to-market solution.

The Cyclone II family was developed with the objective of building the lowest-cost FPGA and making it easy to adopt in high-volume, traditionally ASIC applications. The Cyclone II product-development process was based on extensive interaction with customers in markets that traditionally rely on ASICs. These customers identified the threshold price points, key features, and performance required to make FPGAs a viable solution in high-volume systems. Cyclone II devices are offered in low-cost packages with a wide range of user I/O pins.

For applications that currently use low- to mid-density ASICs, Cyclone II FPGAs provide a flexible, risk-free option without up-front non-recurring engineering (NRE) charges or minimum order quantities. With a feature set unmatched by any other low-cost FPGA—such as embedded 18 × 18 multipliers for high-performance digital signal processing (DSP) applications and support for DDR2 and QDRII memory interfaces at up to 668 Mbps—Cyclone II devices are well equipped to integrate complex, system-level functions.

Key Cyclone II Features

Cyclone II FPGAs offer several system-level features to meet the needs of the low-cost, high-volume marketplace. See Table 1.

- *Logic Density*: Cyclone II devices continue the success of the first-generation Cyclone device family and extend the reach of FPGAs further into cost-sensitive, high-volume applications by offering up to 68,416 LEs—three times more logic density than Cyclone devices.

Table 1. Cyclone II Family Overview

Feature	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
Logic Elements	4,608	8,256	18,752	33,216	50,528	68,416
M4K RAM Blocks	26	36	52	105	129	250
Total RAM Bits	119,808	165,888	239,616	483,840	594,432	1,152,000
Embedded 18 × 18 Multipliers	13	18	26	35	86	150
Phase-Locked Loops	2	2	4	4	4	4
Maximum User I/O Pins	142	182	315	475	450	622
Package Offerings	144-pin TQFP 208-pin PQFP 256-pin FBGA	144-pin TQFP 208-pin PQFP 256-pin FBGA	208-pin PQFP 256-pin FBGA 484-pin FBGA	484-pin FBGA 672-pin FBGA	484-pin FBGA 672-pin FBGA	672-pin FBGA 896-pin FBGA

- *Embedded Memory*: Typical systems require on-chip memory capabilities for system cache, data buffering, clock domain translation, and first-in first-out (FIFO) applications. Cyclone II devices contain M4K embedded memory blocks consisting of 4,608 bits per block (4,096 bits plus 512 parity bits). With up to 1.1 Mbits of on-chip memory, Cyclone II embedded memory blocks support multiple configurations, including true dual-port and single-port RAM, ROM, and FIFO buffers.
- *External Memory Interface*: Cyclone II devices provide ample on-chip memory for many low-cost applications. However, many other applications also require external memory devices for additional storage resources. As storage requirements exceed the abundant on-chip memory resources, devices must be able to interface to external memory devices. Altera worked with leading memory vendors to ensure that users can connect the very latest memory devices to Cyclone II FPGAs. Cyclone II devices have been designed for high-speed data transfer to and from external memory devices. Cyclone II devices are designed to communicate with double data rate (DDR and DDR2), single data rate (SDR) SDRAM devices and quad data rate (QDRII) SRAM devices through a dedicated interface that ensures fast, reliable data transfer at up to 668 Mbps.
- *Embedded Multipliers*: A convergence of data, audio, and video in DSP applications has led to increased performance requirements to support emerging protocols such as JPEG 2000, MPEG-4, 802.11×, CDMA2000, 1× EV DV, HSDPA, and W-CDMA. Cyclone II devices feature up to 150 embedded 18 × 18 multipliers that are ideal for low-cost DSP applications such as consumer, wireless, and image processing. Cyclone II embedded 18 × 18 multipliers are capable of implementing common DSP functions such as finite impulse response (FIR) filters, fast Fourier Transfers (FFTs), correlators, and encoders/decoders. Capable of running at 250 MHz, the embedded multipliers in Cyclone II devices eliminate the performance bottleneck in complex arithmetic calculations and increase overall DSP system throughput by orders of magnitude. Cyclone II devices can be used as "FPGA co-processors" for DSP applications that offload complex arithmetic computations from the digital signal processor and boost overall system performance for lower system costs.
- *I/O Standards*: Cyclone II devices support a variety of single-ended and differential I/O standards commonly used for interfacing with other devices on the board. This capability gives designers flexibility in designing their high-performance systems. New to Cyclone II devices is support for the mini-LVDS and LVPECL differential I/O standards, and PCI-X and HSTL single-ended I/O standards. Single-ended I/O standards are critical when working with advanced memory devices such as double-data rate (DDR/DDR2) SDRAM and QDRII SRAM. Additional Cyclone II supported single-ended and differential I/O standards include LVTTL, LVCMOS, PCI, SSTL, LVDS, and RSDS.

Table 2. Cyclone Series Target Applications

Consumer	Wireline & Wireless Communications	Automotive	Computers & Storage Devices	Military, Industrial & Medical
■ Cameras ■ A/V Conference Equipment ■ Plasma Displays ■ HDTVs ■ DVD Players ■ Camcorders ■ Set-Top Boxes	■ Modems ■ DSLAM Systems ■ Low-End Routers & Switches ■ High-Speed Wireless CPEs ■ Wireless LAN Access Points ■ Wireless Basestations	■ Navigation Systems ■ Satellite Radio Receivers ■ Hybrid TV Receivers ■ Telematics ■ Entertainment	■ Printers ■ Copiers ■ SAN Subsystems ■ Storage Servers ■ Storage Switches	■ Factory Automation ■ Process Control ■ MRIs ■ X-Rays ■ Radar ■ SDR ■ Network Test Equipment

continued on page 6

New Applications for FPGAs

With its higher densities, enhanced features, and lower price points, Cyclone II devices extend the use of FPGAs in cost-sensitive, high-volume applications that previously required an ASIC. Over 3,000 customers have used the first-generation Cyclone devices since its introduction, and Cyclone II devices will extend this success in the consumer, computer and storage, wireless, wireline, industrial, medical, and automotive markets. Table 2 provides examples of applications that benefit from using the Cyclone series.

Low-Cost Processor Solution: Cyclone II Devices & Nios II Processor

Cyclone II devices support the Nios® II family of embedded processors, a widely adopted (and obsolescence free) user-configurable, general-purpose RISC embedded processor. The Nios II processor family extends Altera's soft embedded processor leadership with better performance, lower cost, and the most complete set of software development tools available anywhere. Cyclone II dedicated multipliers help improve Nios II processor performance and efficiency. The Cyclone II family can incorporate multiple processors in one device, providing savings in cost, footprint, and power efficiency. Cyclone II devices provide designers with maximum flexibility, and balance performance needs and device resource usage by supporting all three Nios II processor cores, each optimized for a particular price and performance range. All three cores support a single instruction set architecture, making them 100% code compatible:

- Nios II /f (fast) – Highest performance, moderate FPGA utilization (~ 1,800 LEs)
- Nios II /s (standard) – High performance, low FPGA utilization (~ 1,200 LEs)
- Nios II /e (economy) – Lower performance, smallest FPGA utilization (~ 600 LEs)

Low-Cost Configuration Devices

To offer the lowest total solution cost, Altera created a low-cost serial configuration device family for the Cyclone series. Serial configuration devices are priced for volume applications as low as 10% of the price of the corresponding Cyclone series device. Four serial configuration devices (1 Mbit, 4 Mbits, 16 Mbits, and 64 Mbits) are offered in a space-saving 8-pin and 16-pin small-outline integrated circuit (SOIC) package, as shown in Table 3. To add even more value, any unused memory in these devices can be used for general-purpose storage, such as storing the software code for Nios II embedded processors.

Free Design Software

All Cyclone II devices are fully supported in the free Web Edition of the Quartus® II version 4.1 development software. Additionally, subscribers to the Altera Subscription Program will receive full Cyclone II support in the subscription edition of the Quartus II software version 4.1. The Quartus II software is the industry's most advanced development tool for FPGAs, providing a comprehensive suite of synthesis, optimization, and verification tools in a single, unified design environment. The Quartus II software technology advantage enables designers to select, integrate, and evaluate intellectual property (IP) in Cyclone II designs in a matter of minutes. Quartus II advanced technology reduces development costs and helps bring products to market faster. The Quartus II software also integrates seamlessly with all leading third-party synthesis and simulation tools. The free Quartus II Web Edition can be downloaded at no cost from **www.altera.com/q2webedition**.

Learn more about the advantages of the Cyclone II family by visiting the Altera web site today at **www.altera.com/cyclone2**.

Table 3. Serial Configuration Devices

Configuration Device	Capacity	Package	Cyclone Devices Supported	Cyclone II Devices Supported
EPCS1	1 Mbit	8-pin SOIC	EP1C3, EP1C4, EP1C6	EP2C5
EPCS4	4 Mbit	8-pin SOIC	All	EP2C5, EP2C8, EP2C20
EPCS16	16 Mbit	16-pin SOIC	All	All
EPCS64	64 Mbit	16-pin SOPC	N/A	All

Nios II: The World's Most Versatile Processor

With widespread customer adoption, the 16-bit Nios® processor has set the standard for soft-core processors in programmable logic, and Altera sold over 13,000 development kits in under three years. The 32-bit Nios II family of embedded processors builds upon this success, delivering higher performance and lower cost with a robust set of software development tools.

Family of Embedded Processors

The Nios II family consists of three members—fast, standard, and economy—each optimized for a specific price and performance range. All three cores use a common 32-bit instruction set architecture (ISA) and are 100% binary code compatible. See Table 1.

- *Nios II /f Fast CPU*: Optimized for maximum performance, the Nios II /f processor delivers 220 DMIPs performance in the Stratix® II family of high-performance FPGAs, placing it squarely in the ARM® 9 class of processor. Four times faster than the original Nios CPU, it is 40% smaller as well.
- *Nios II /s Standard CPU*: The Nios II /s core strikes a balance between processing performance and logic element (LE) usage. It is 60% faster than the fastest Nios CPU, and smaller than the smallest Nios CPU, achieving over 120 DMIPS and consuming only 930 equivalent LEs in Stratix II devices.
- *Nios II /e Economy CPU*: Optimized for lowest cost, the Nios II /e core achieves a smaller FPGA footprint (less than 600 LEs), consuming as little as $0.35 worth of logic in a Cyclone™ II device. The Nios II /e core is half the size of the smallest Nios core and four times the performance.

Nios® II

Getting the Perfect Fit Processor

Designers of embedded systems often think of processor performance in terms of clock frequency, or benchmarks (e.g., Dhrystones, EEMBC, etc.). The true performance of an embedded system has less to do with its clock frequency or DMIPS alone, and more with the system that surrounds it. With the Nios II processor, designers can create in minutes a system with the exact mix of processors, peripherals, and interfaces required using the SOPC Builder design tool. Over 60 peripherals are available from Altera and third-party partners that integrate seamlessly with the Nios II family of processors, including a wide range communications, memory, signal processing, and interface cores. Developers can also incorporate their own logic with the "Interface to User Logic" wizard, providing the ultimate in versatility.

continued on page 8

Table 1. Nios II Architectural Overview

Feature		Core		
		Nios II /f	Nios II /s	Nios II /e
Objective		Performance	Performance/ Size Balance	Minimal Size
Performance *(1)*	Max DMIPS *(2)*	220	128	31
	Max f_{MAX}	188	170	201
Address and Data Bus		32 bit	32 bit	32 bit
Pipeline		6 Stages	5 Stages	None
External Address Space		32 Gigabytes	32 Gigabytes	32 Gigabytes
Cache (Configurable)	Instruction	512 bytes- 64 Kbytes	512 bytes - 64 Kbytes	None
	Data	512 bytes- 64 Kbytes	None	None
Area	Cyclone, Cyclone II, Stratix	× < 1,800 LEs	× < 1400 LEs	× < 700 LEs
	Stratix II	× < 1,050 LEs	× < 950 LEs	× < 500 LEs

Notes to Table 1:

(1) Performance varies based on the target device architecture. Numbers shown above are for Stratix II devices.

(2) DMIPS: Dhrystone MIPS (Utilizing Dhrystone 2.1 Benchmark)

Flexible Performance & Cost

Nios II system performance can scale to fit the application. Designers can choose any combination of CPU cores, and place as many as needed, in an Altera® FPGA. For example, a single Nios II /f core in a Stratix II device achieves 220 DMIPS performance in approximately 1,800 equivalent LEs. For low cost systems, the Nios II /e core consumes less than $0.35 of logic in a Cyclone II device, leaving plenty of logic for implementing functions previously handled by external devices, which reduces board cost, complexity, and power consumption. See Table 2.

Accelerating System Performance

Developers of embedded systems must pick a processor that delivers the system performance they need. Conventional benchmarks have limited value since the final measure is a system running the user's application code. Designers often select a processor with higher performance (and higher cost) than they need to gain a margin of safety. Performance of Nios II systems can scale to fit the application using custom instructions, high bandwidth switch fabric, and hardware accelerators.

The Nios II family of processors supports up to 256 custom instructions to accelerate logic or mathematically complex algorithms normally handled in software. For example, a block of logic that performs a cyclic redundancy code (CRC) calculation on a 64-Kb buffer operated 27 times faster as a custom instruction than when performed by software. Nios II processors support fixed and variable cycle operations, include a wizard for importing user logic as a custom instruction, and automatically create software macros for use in developers' code. See Figure 1.

Traditional processors share a single system bus with DMA channels and other "master" functions limiting bus access to one master at a time. Nios II systems benefit from the Avalon™ switch fabric, which provides a dedicated data path to each master, allowing all masters to transfer data simultaneously. Only when two (or more) masters try to access the same slave peripheral at the same time is one master forced to wait for access. Simultaneous transactions provide orders-of-magnitude greater system performance than bus-based embedded processors. See Figure 2.

Large blocks of data can be processed concurrently with CPU operation by adding application-specific hardware accelerators. The Avalon switch fabric provides a flexible interconnect path that allows multiple cores (e.g., CPU and accelerator) to perform simultaneous reads and writes using dedicated data paths, dramatically boosting system throughput. Hardware accelerators act as a custom co-processor within the FPGA, typically by having the processor initiate the operation (i.e., instruct the DMA to feed the accelerator from one buffer, empty it into another buffer and notify the CPU when it is complete). The previously mentioned CRC example runs over 530 times faster using the hardware accelerator. See Figure 3.

Figure 1. Nios II Custom Instruction Implementation

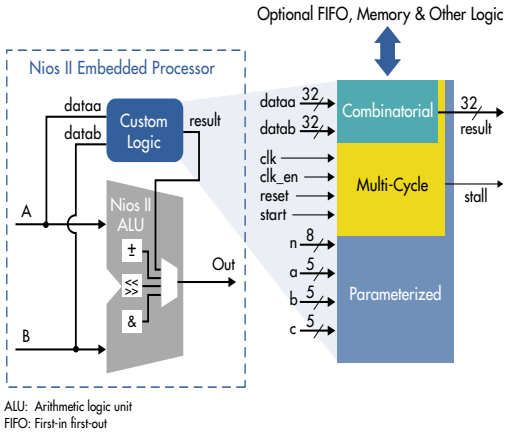
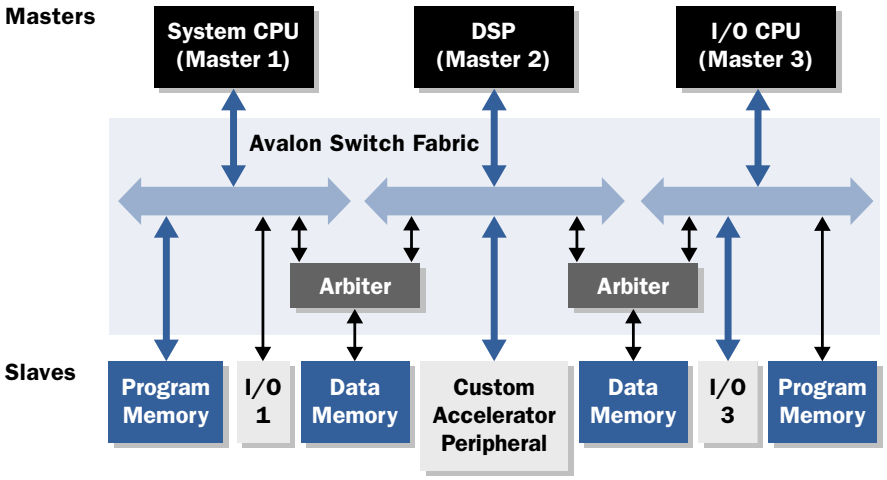


Table 2. Nios II Performance & Size

Family	Nios II /f (fast)			Nios II /s (standard)			Nios II /e (economy)		
	f_{MAX}	DMIPS	LEs	f_{MAX}	DMIPS	LEs	f_{MAX}	DMIPS	LEs
Stratix II *(1)*	188	220	1,012	170	128	930	201	31	527
Stratix	141	165	1,849	130	97	1,313	144	22	571
Cyclone	125	92	1,732	124	54	1,207	140	17	583
Cyclone II (1)	125	105	1,732	124	60	1,207	140	22	583
HardCopy	143	167	1836	138	103	1368	152	24	568

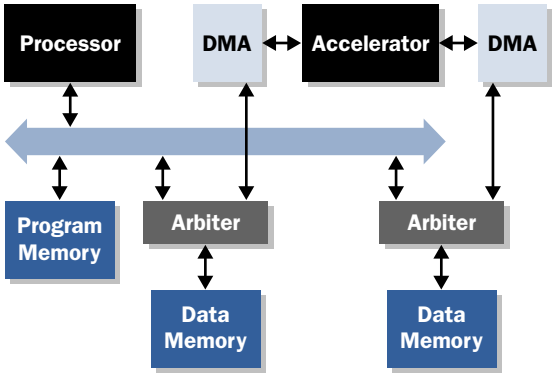
Note to Table 2:
(1) Estimated performance.

Figure 2. Avalon Switch Fabric Operation



DSP: Digital signal processing

Figure 3. Hardware Accelerator in Avalon Switch Fabric



DMA: Direct memory access

Nios II Integrated Development Environment

The Nios II Integrated Development Environment (IDE) provides a complete software development environment, including automatic library generation, editing, compiling, debugging, and flash programming facilities (see Figure 4). The Nios II IDE features include:

- *Library Generation*: The Nios II IDE automatically generates a custom software library based on the hardware configuration (i.e., peripheral driver support).
- *Project Templates*: The Nios II IDE provides a set of example projects that provide a starting point for application development. Project templates include a web server, a board diagnostic program, and a custom instruction example. Users can add their own templates to facilitate design reuse.
- *Editor*: The Nios II IDE includes a C/C++ aware editor with code completion and advance search capabilities.
- *Compiler*: The Nios II IDE provides seamless integration with the GNU compiler, assembler, and linker.

Figure 4. Nios II IDE

continued on page 10

- *Multi-Target Support*:
  - Hardware Debugging: Debugging connection to physical target through any Altera JTAG cable. High-speed USB Blaster included in Nios II kit.
  - Instruction set simulator: The Nios II IDE enables a virtual software debug session on the user's workstation, requiring no physical hardware.
  - ModelSim® simulator: Run software on an RTL model of the Nios II processor and system (Verilog or VHDL).
- *Debugger*:
  - Debugging controls: Set breakpoints, run, stop, and step through program execution.
  - Two hardware breakpoints: The Nios II IDE allows the debugging of code in non-volatile memory regions.
  - Two data triggers: Locate troublesome software bugs by triggering on any address, data, and bus cycle (load/store) combination. Diagnose complex system problems by combining two data triggers into a "Super Trigger" for triggering on address ranges and data patterns with mask.
- *Flash Programmer*: The Nios II IDE enables users to program FPGA configurations (SRAM Object File (**.sof**)), system firmware, and arbitrary data into any common flash interface (CFI).
  - On-chip trace: Analyze a program's execution by capturing up to 16 frames of instruction trace into on-chip memory, and viewing in source, assembly, or mixed display.
  - Advanced debugging solutions (add-on packages): Developers can expand their debug capabilities to include two additional hardware breakpoints, two additional data triggers, and boost on-chip trace capture to 128 frames through a software upgrade package for $695. Users seeking complete debugging coverage can get all the features mentioned above, plus 128,000 frames of external trace capture via the ISA-NIOS/T system probe for $4,995. Both packages are available for purchase from the First Silicon Solutions (FS2) Corporation.

Table 3. Third-Party Support

Product	Description	Provider
Nios II IDE *(1)*	IDE/Debugger	Altera (**www.altera.com**)
Code|lab *(2)*	IDE/Debugger	Mentor/Accelerated Technology (**www.acceleratedtechnology.com**)
MicroC/OS-II *(2)*	RTOS	Micrium (**www.micrium.com**)
Nucleus Plus *(2)*	RTOS	Mentor/ Accelerated Technology (**www.acceleratedtechnology.com**)
uCLinux	OS	Open Source (www.niosforum.com)
KROS	RTOS	KROS Technologies (**www.krostech.com**)
NORTi	RTOS	MiSPO (**www.mispo.co.jp**)
PrKERNELv4	RTOS	eSOL (**www.esol.co.jp**)
Lightweight IP *(1)*	TCP / IP Stack	Altera (**www.altera.com**)
ISA-Nios/T	JTAG Trace Probe	First Silicon Solutions (FS2) (**www.fs2.com**)

Notes to Table 3:
(1) The full version is included in the Nios II development kits from Altera.
(2) The evaluation version is included in the Nios II development kits from Altera.

RTOS & Middleware Included

Nios II development kits ship with a complete, portable, ROMable, pre-emptive real-time kernel from Micrium (MicroC/OS-II) that includes full source code, printed reference documentation, and a license to develop applications using Altera development boards. Once developers migrate their designs to their own board, they must purchase a license from Micrium. The Nios II processors also include Lightweight IP, a sockets based, open source TCP/IP stack that can be used in MicroC/OS-II applications.. The software is shipped as source code with documentation, reference designs, and technical support from Altera. See Table 3.

The Nios II development kits also ship with an evaluation version of Accelerated Technology's Nucleus Plus RTOS and code|lab debugger, providing developers with an opportunity to evaluate these powerful software packages.

Availability

The Nios II processor family is available in complete development kits from Altera for the Stratix, Stratix II, Cyclone, and Cyclone II FPGA device families. These kits include the Nios II development tools, the Quartus® II design software (development kit edition), a development board, and the USB Blaster download cable.

An evaluation version of the Nios II processor family and tool chain will be provided to all active Quartus II subscribers through their Altera Software Subscription, and is available for download at **www.altera.com/testdriveniosii**. Additionally, customers can go to **www.niosforum.com** to exchange ideas, designs, and exchange information with other Nios II processor users.

Introducing Nios II.

The world's most versatile processor!

Nios® II The ultimate in design flexibility.

The world's most popular soft-core processor just got better! Altera introduces the Nios® II family of embedded processors, featuring three CPU cores offering unprecedented performance and cost options. With Nios II processors, designers can define the exact features, performance, and cost they need in Altera's high-performance Stratix® series, low-cost Cyclone™ series, and HardCopy® device families.

The Nios II development kits provide a complete, easy to use tool set including the new Nios II integrated development environment to accelerate software design. Try the Nios II processor today and experience the ultimate in design flexibility.

Supported by QUARTUS® II

- Over 200 DMIPs performance
- Consumes as little as $0.35 of logic
- Supports multi-processor systems
- Library of over 60 programmable peripherals
- Industry's most complete development kits
- Royalty-free & obsolescence-proof

ALTERA®

The Programmable Solutions Company®

www.altera.com/nios2

Leading through innovation.

Quartus II Software Version 4.1 Adds Support for Cyclone II Devices & Extends Software Technology Leadership

Version 4.1 of the Quartus® II design software extends Altera's software technology leadership by adding support for the Cyclone™ II FPGA family—the lowest cost FPGAs ever—and lowering development costs with new verification, optimization, and ease-of-use features.

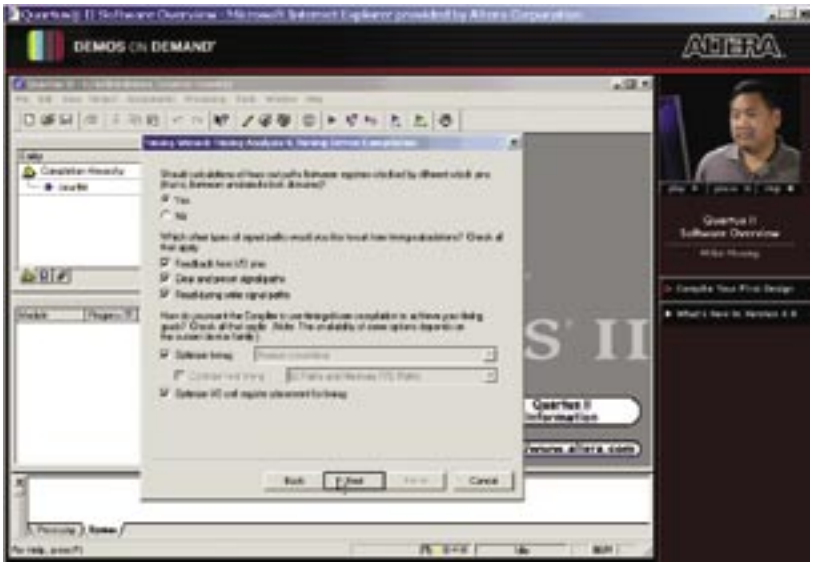
Design for Cyclone II Devices Today

Cyclone™ II devices are low-cost, general-purpose FPGAs that are based on TSMC's 90-nm, 1.2-V, 9-layer-metal low-k dielectric process technology and built on 300-mm wafers. Cyclone II devices, the second generation in the Cyclone series, are designed with the same approach as their first-generation predecessors, meaning they built to specifically minimize silicon area, while being armed with a full set of robust, system-enabling features. For more information on Cyclone II devices, refer to "Cyclone II: The Lowest-Cost FPGAs Ever" on page 4.

Quartus II On-Line Demos & Software Handbook Updated

Quartus II on-line demonstrations (see Figure 1) available on the Altera® web site are the easiest way to see the latest Quartus II software features in action and learn where to get more information.

Figure 1. Quartus II On-Line Demonstrations



Existing videos have been updated with the latest Quartus II software version 4.1 enhancements and the following new video demonstrations:

- Scripting
- Interfacing to External Memory
- Optimization Assistant
- Using the RTL Viewer and Tech Map Viewer
- Updating RAM/ROM via JTAG

The Quartus II Software Handbook has been updated with the latest Quartus II software version 4.1 enhancements and the following new chapters:

- Synopsys DC FPGA Support
- Analyzing Designs with the Quartus II RTL Viewer and Technology Map Viewer
- Effective Use of Revisions
- In-System Updating of Memory and Constants

The Quartus II Handbook is available from the Altera web site.

Quartus II Subscriptions Now Include Altera MegaCore IP Library CD-ROM

Quartus II software subscriptions now include the Altera MegaCore® IP Library CD-ROM, including OpenCore® Plus evaluation versions of all Altera MegaCore functions, and the Nios® II embedded processor evaluation edition. The MegaCore IP Library CD-ROM includes off-the-shelf MegaCore intellectual property (IP) functions optimized for Altera devices. Only the Quartus II software offers OpenCore Plus infrastructure technology to support IP evaluation in third-party simulation environments and in hardware before making any IP purchases.

New Features—Extending Software Technology Leadership

The Quartus II software version 4.1 includes new technology that lowers development costs and further simplifies and accelerates high-density FPGA design.

Stratix II Physical Synthesis Optimization

Physical synthesis optimizations now provide an average of 9% faster performance for Stratix® II designs. This gain is on top of the 50% performance gain delivered over Stratix designs without using physical synthesis.

Synthesis Multiplexer Optimizations Reduce Area Up to 30%

Designers using the Quartus II integrated synthesis feature can now reduce device area usage up to 30% to fit into a smaller device and save cost. Area reductions come from a new Quartus II integrated synthesis optimization option optimizes multiplexer usage to take advantage of Altera FPGA architectural features. Results will vary depending on the amount of multiplexers included in your design.

New Tools Simplify Design Optimization

New timing and resource optimization advisor tools are included in Quartus II software version 4.1 to provide specific advice on optimizing design timing performance and/or resource utilization based on the current design project settings and assignments. Detailed instructions and links to recommended software features to implement the proposed suggestions are included. Figure 2 shows an example of the timing optimization advisor interface. Figure 3 shows a legend for the symbols displayed in the optimization advisors.

Figure 2. Timing Optimization Advisor Example

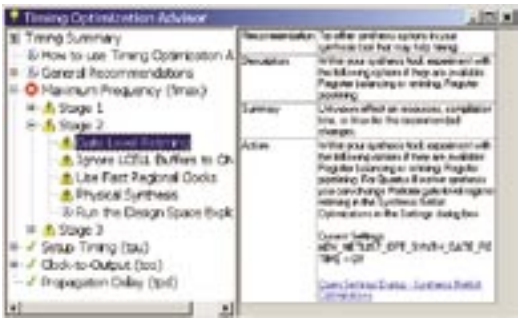


Figure 3. How to Use the Timing Optimization Advisor

Recommendation	Use the recommendations in the Timing Optimization advisor to optimize the timing in your design.
Description	For each problem area, there are a set of recommendations. It is recommended to follow the order of the recommendations to make your changes.
Legend	-- means there are some violations in the specified area. -- means the settings in your design don't match what are recommended in Optimization Advisor. -- means the settings in your design match what are recommended in Optimization Advisor. -- means you need to check it and do as recommended, but Optimization Advisor has no way to detect if the recommended changes are made or not.
Action	Follow the recommendations to make your changes.

Time Groups Simplify Timing Constraint Entry

The new time group feature allows users to organize nodes into a group so that timing assignments can be made to the group instead of to each individual node. The time group feature is available through the graphical user interface and can be set through tool-command language (Tcl) commands.

Incrementally Update RAM & Constants In-System

Using the new in-system memory content editor feature, engineers can now easily perform "what if" type experiments in-system in just seconds. The Quartus II software enables FPGA memory contents and design constants to be updated in-system without recompiling a design or reconfiguring the rest of the FPGA.

Technology Map Viewer

The new technology map viewer feature included in the Quartus II software version 4.1 can be used after the synthesis step to debug designs at a detailed level by viewing a logical representation of the design implementations mapped into Altera device primitives. Once the fitting and timing analysis steps have been performed, critical timing paths and timing information can be highlighted and cross-probed to the technology map viewer display. From the technology map viewer display, users can cross-probe to design source files, the assignment editor, the Timing Closure Floorplan Editor, or the Quartus II Chip Editor for design optimization. See Figure 4 on page 14.

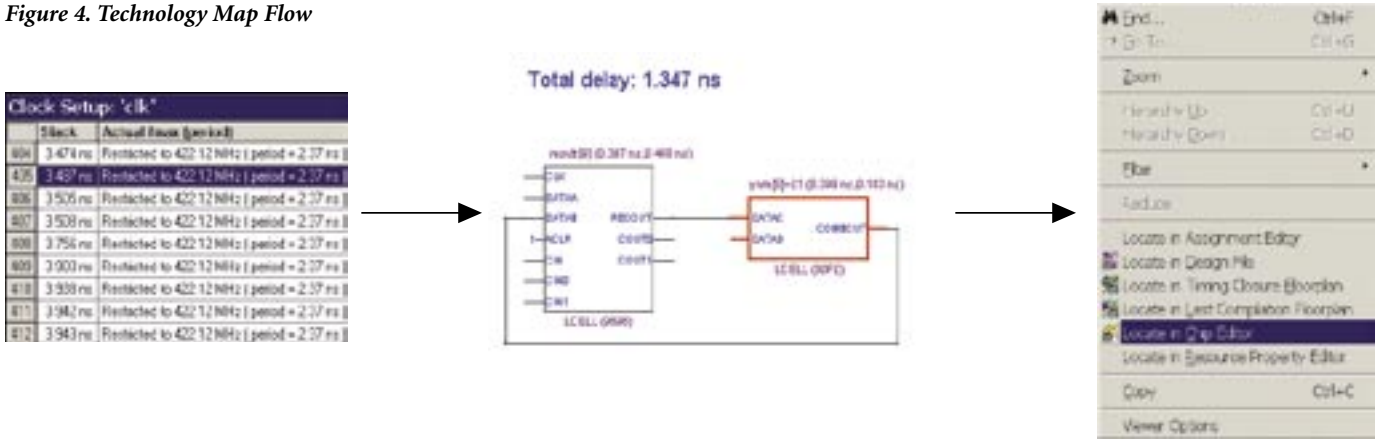
More information is available in the new *Analyzing Designs with the Quartus II RTL Viewer and Technology Map Viewer* chapter of the Quartus II handbook.

Import/Export Assignments in CSV Format

Engineers can now easily transfer assignments between the Quartus II software and Excel spreadsheets using the comma-separated value (CSV) format. This capability can aid in transferring pin-out information to printed circuit board design software packages that support interfaces with Excel spreadsheets.

continued on page 14

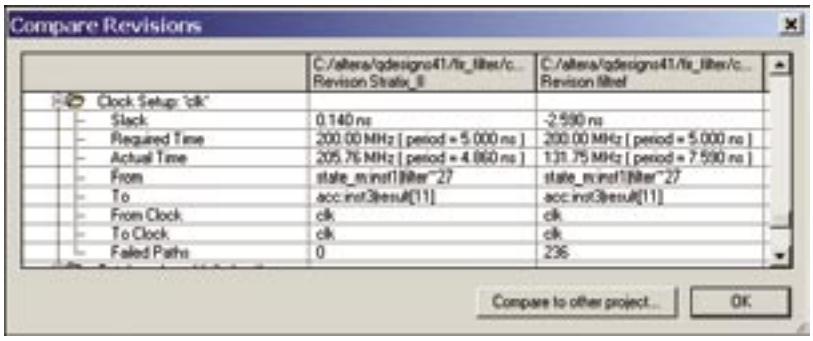
Figure 4. Technology Map Flow



SignalTap II Embedded Logic Analyzer Enhancements

The free Quartus II programmer software now includes device configuration and the SignalTap® II embedded logic analyzer viewer, allowing easy deployment of in-system logic analysis capabilities to multiple lab locations or field service personnel. The Quartus II programmer software is a no-cost, stand-alone version of the Quartus II device programming and configuration functions available from the download center of the Altera web site. The SignalTap II embedded logic analyzer advanced trigger feature has also been updated with an event counter trigger condition function. This feature provides the ability not just to trigger on an event, but also to trigger after an event is satisfied a specified number of times. To improve usability, users now have the choice to configure SignalTap II embedded logic analyzers using the MegaWizard® Plug-In Manager and to instantiate them directly in HDL source code, in addition to the graphical user interface instantiation method.

Figure 5. Compare Revisions Feature



Version Support & Compare Revisions Feature

Version support gives designers the ability to easily experiment with different versions of design source files and settings. This feature complements the previously introduced revisions feature, which has been updated to allow users to easily compare the results of two more project revisions side by side in a spreadsheet display format (see Figure 5). Users can also compare results of a revision settings to the results obtained in other projects.

Version Compatible Database

Designers can now analyze designs in future versions of the Quartus II software without recompiling the design, thus preserving design results and saving time. The Quartus II software can generate a version-compatible database that allows designers to export a design database from a project and import the database into a future version of the Quartus II software for analysis.

Experience Quartus II Software Version 4.1 Today

The Quartus II software version 4.1 delivers unmatched performance, efficiency, and ease of use for CPLD, FPGA, and structured ASIC designs. Quartus II software version 4.1 is now shipping to all customers with active software subscriptions. The Quartus II version 4.1 Web Edition software is available for downloading from the Altera web site or as part of the Quartus II Web Edition Software Suite CD-ROM.

Altera Devices

Tables 1 through 16 list the logic element (LE), macrocell and gate counts, pin/package options, I/O pin counts, supply voltages, RAM bits, and other device-specific features of Altera® CPLDs, FPGAs, HardCopy® structured ASICs, and configuration devices.

Table 1. Cyclone II Devices

Device	Logic Elements (LEs)	M4K RAM Blocks *(1)*	Total RAM Bits	Embedded Multipliers *(2)*	PLLs	Supply Voltage	Pin/Package Options *(3)*	Maximum User I/O Pins
EP2C5	4,608	26	119,808	13	2	1.2 V	144-Pin TQFP *(4)*, 208-Pin PQFP, 256-Pin FineLine BGA® *(5)*	89, 142
EP2C8	8,256	36	165,888	18	2	1.2 V	144-Pin TQFP, 208-Pin PQFP, 256-Pin FineLine BGA	85, 138, 182
EP2C20	18,752	52	239,616	26	4	1.2 V	208-Pin PQFP *(5)* *(6)*, 256-Pin FineLine BGA, 484-Pin FineLine BGA	152, 315
EP2C35	33,216	105	483,840	35	4	1.2 V	484-Pin FineLine BGA, 672-Pin FineLine BGA	322, 475
EP2C50	50,528	129	594,432	86	4	1.2 V	484-Pin FineLine BGA, 672-Pin FineLine BGA	294, 450
EP2C70	68,416	250	1,152,000	150	4	1.2 V	672-Pin FineLine BGA, 896-pin FineLine BGA	422, 622

Notes to Table 1:

(1) Each RAM block has 4 Kbits and 512 parity bits.
(2) Total number of 18-bit × 18-bit multipliers. For the total number of 9-bit × 9-bit multipliers per device, multiply the total number of 18-bit × 18-bit multipliers by 2.
(3) Cyclone II devices support vertical migration within the same package.
(4) TQFP: thin quad flat pack.
(5) Contact your local Altera sales representative for more information.
(6) PQFP: plastic quad flat pack.

Table 2. Cyclone Devices

Device	LEs	M4K RAM Blocks *(1)*	Total RAM Bits	PLLs	Supply Voltage	Pin/Package Options *(2)*	Maximum User I/O Pins
EP1C3	2,910	13	59,904	1	1.5 V	100-Pin TQFP, 144-Pin TQFP	65, 104
EP1C4	4,000	17	78,336	2	1.5 V	324-Pin FineLine BGA, 400-Pin FineLine BGA	249, 301
EP1C6	5,980	20	92,160	2	1.5 V	144-Pin TQFP, 240-Pin PQFP, 256-Pin FineLine BGA	98, 185, 185
EP1C12	12,060	52	239,616	2	1.5 V	240-Pin PQFP, 256-Pin FineLine BGA, 324-Pin FineLine BGA	173, 185, 249
EP1C20	20,060	64	294,912	2	1.5 V	324-Pin FineLine BGA, 400-Pin FineLine BGA	233, 301

Notes to Table 2:

(1) Each RAM block has 4 Kbits and 512 parity bits.
(2) Cyclone devices support vertical migration within the same package.

Table 3. Stratix II Devices

Device	Adaptive Logic Modules (ALMs) *(1)*	Equivalent LEs *(1)*	M512 RAM Blocks	M4K RAM Blocks	M-RAM Blocks	Total RAM Bits	DSP Blocks	Embedded Multipliers *(2)*	PLLs *(3)*	Supply Voltage	Pin/Package Options *(4)*	Maximum User I/O Pins
EP2S15	6,240	15,600	104	78	0	419,328	12	48	6	1.2 V	484-Pin FBGA *(5)* 672-Pin FBGA *(5)*	341 365
EP2S30	13,552	33,880	202	144	1	1,369,728	16	64	6	1.2 V	484-Pin FBGA *(5)* 672-Pin FBGA *(5)*	341 499
EP2S60	24,176	60,440	329	255	2	2,544,192	36	144	12	1.2 V	484-Pin FBGA *(5)* 672-Pin FBGA *(5)* 1,020-Pin FBGA *(5)*	341 499 717
EP2S90	36,384	90,960	488	408	4	4,520,448	48	192	12	1.2 V	1,020-Pin FBGA *(5)* 1,508-Pin FBGA *(5)*	757 901
EP2S130	53,016	132,540	699	609	6	6,747,840	63	252	12	1.2 V	1,020-Pin FBGA *(5)* 1,508-Pin FBGA *(5)*	741 1,109
EP2S180	71,760	179,400	930	768	9	9,383,040	96	484	12	1.2 V	1,020-Pin FBGA *(5)* 1,508-Pin FBGA *(5)*	741 1,173

Notes to Table 3:

(1) Each Stratix® II ALM is equivalent to 2.5, 4-input look-up table (LUT)-based LEs.
(2) Each DSP block supports four 18-bit × 18-bit multipliers.
(3) Includes enhanced and fast PLLs.
(4) Stratix II devices support vertical migration within the same package.
(5) FBGA: FineLine BGA.

continued on page 16

Table 4. Stratix Devices Note (1)						
Device	**LEs**	**Pin/Package Options**	**I/O Pins**	**Supply Voltage**	**Total RAM Bits**	**DSP Blocks**
EP1S10	10,570	484-Pin BGA *(2)*, 672-Pin BGA, 672-Pin BGA *(2)*, 780-Pin BGA *(2)*	335, 345, 345, 426	1.5 V	920,448	6
EP1S20	18,460	484-Pin BGA *(2)*, 672-Pin BGA, 672-Pin BGA *(2)*, 780-Pin BGA *(2)*	361, 426, 426, 586	1.5 V	1,669,248	10
EP1S25	25,660	672-Pin BGA, 672-Pin BGA *(2)*, 780-Pin BGA *(2)*, 1,020-Pin BGA *(2)*	473, 473, 597, 706	1.5 V	1,944,576	10
EP1S30	32,470	780-Pin BGA *(2)*, 956-Pin BGA, 1,020-Pin BGA *(2)*	589, 683, 726	1.5 V	3,317,184	12
EP1S40	41,250	780-Pin BGA *(2)*, 956-Pin BGA, 1,020-Pin BGA *(2)*, 1,508-Pin BGA *(2)*	615, 683, 773, 822	1.5 V	3,423,744	14
EP1S60	57,120	956-Pin BGA, 1,020-Pin BGA *(2)*, 1,508-Pin BGA *(2)*	683, 773, 1,022	1.5 V	5,215,104	18
EP1S80	79,040	956-Pin BGA, 1,020-Pin BGA *(2)*, 1,508-Pin BGA *(2)*	683, 773, 1,203	1.5 V	7,427,520	22

Notes to Table 4:
(1) The ordering code for Stratix devices is based on the number of LEs; therefore, gate count numbers are not included.
(2) Space-saving FineLine BGA package.

Table 5. Stratix GX Devices							
Device	**LEs**	**Transceiver Channels**	**Pin/Package Options**	**I/O Pins**	**Supply Voltage**	**RAM Bits**	**Source-Synchronous Channels**
EP1SGX10C	10,570	4	672-Pin BGA *(1)*	330	1.5 V	920,488	22
EP1SGX10D	10,570	8	672-Pin BGA *(1)*	330	1.5 V	920,488	22
EP1SGX25C	25,660	4	672-Pin BGA *(1)*	426	1.5 V	1,944,576	39
EP1SGX25D	25,660	8	672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	426, 542	1.5 V	1,944,576	39
EP1SGX25F	25,660	16	1,020-Pin BGA *(1)*	542	1.5 V	1,944,576	39
EP1SGX40D	41,250	8	1,020-Pin BGA *(1)*	548	1.5 V	3,423,744	45
EP1SGX40G	41,250	20	1,020-Pin BGA *(1)*	548	1.5 V	3,423,744	45

Note to Table 5:
(1) Space-saving FineLine BGA package.

MAX II Devices & PCI Compiler 3.2.0 Deliver Complete PCI Solutions

Altera's PCI Compiler has been used in over 1,000 FPGA-based PCI designs, and now it provides 32-bit, 33-MHz PCI IP support for the MAX® II CPLD device family. PCI Compiler version 3.2.0 IP cores support both bus mastering and target-only MAX II PCI control path applications in very compact implementations, providing designers with ample logic and I/O resources for their value-add design components. The PCI/T32 target-only core is supported in both EPM1270 and EPM2210 devices; the PCI/MT32 master/target core is supported in EPM2210 devices. For a limited time, the PCI/T32 core is available to MAX II designers for the special price of $1,995, a $3,000 discount from the list price. The PCI/MT32 core is available for $8,995. See your Altera sales representative for details.

Table 6. MAX II CPLDs						
Device	**LEs**	**Typical Equivalent Macrocells**	**Pin/Package Options *(1)***	**Maximum User I/O Pins**	**Supply Voltage**	**User Flash Memory Bits**
EPM240	240	192	100-Pin TQFP	80	3.3 V, 2.5 V, 1.8 V	8,192
EPM570	570	440	100-Pin TQFP, 144-Pin TQFP, 256-Pin BGA	76, 116, 160	3.3 V, 2.5 V, 1.8 V	8,192
EPM1270	1,270	980	144-Pin TQFP, 256-Pin BGA	116, 212	3.3 V, 2.5 V, 1.8 V	8,192
EPM2210	2,210	1,700	256-Pin BGA, 324-Pin BGA	204, 272	3.3 V, 2.5 V, 1.8 V	8,192

Note to Table 6:
(1) All BGA packages are 1.0-mm FineLine BGA packages.

Table 7. MAX 3000 CPLDs

Device	Macrocells	Pin/Package Options	I/O Pins	Supply Voltage	Speed Grade
EPM3032A	32	44-Pin Plastic J-Lead Chip Carrier (PLCC)/TQFP	34	3.3 V	-4, -7, -10
EPM3064A	64	44-Pin PLCC/TQFP, 100-Pin TQFP	34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-Pin TQFP, 144-Pin TQFP, 256-Pin BGA *(1)*	80, 96, 98	3.3 V	-5, -7, -10
EPM3256A	256	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*	116, 158, 161	3.3 V	-7, -10
EPM3512A	512	208-Pin PQFP, 256-Pin BGA *(1)*	172, 208	3.3 V	-7, -10

Note to Table 7:
(1) 1.0-mm pitch FineLine BGA package.

Table 8. MAX 7000 CPLDs

Device	Macrocells	Pin/Package Options	I/O Pins	Supply Voltage	Speed Grade
EPM7032S EPM7032AE EPM7032B	32 32 32	44-Pin PLCC/TQFP 44-Pin PLCC/TQFP 44-Pin PLCC/TQFP, 49-Pin BGA *(2)*	36 36 36, 36	5.0 V 3.3 V 2.5 V	-5, -6, -7, -10 -4, -7, -10 -3, -5, -7
EPM7064S EPM7064AE EPM7064B	64 64 64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP 44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin BGA *(1)* 44-Pin TQFP, 49-Pin BGA *(2)*, 100-Pin TQFP, 100-Pin BGA *(1)*	36, 68, 68 36, 68, 68 36, 41, 68, 68	5.0 V 3.3 V 2.5 V	-5, -6, -7, -10 -4, -7, -10 -3, -5, -7
EPM7128S EPM7128AE EPM7128B	128 128 128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP 84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA *(1)*, 144-Pin TQFP, 256-Pin BGA *(1)* 100-Pin TQFP, 100-Pin BGA *(1)*, 144-Pin TQFP, 256-Pin BGA *(1)*	68, 84, 100 68, 84, 84, 100, 100 84, 84, 100, 100	5.0 V 3.3 V 2.5 V	-6, -7, -10, -15 -5, -7, -10 -4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-6, -7, -10
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S EPM7256AE EPM7256B	256 256 256	208-Pin PQFP/RQFP 100-Pin TQFP, 100-Pin BGA *(1)*, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)* 100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA *(2)*, 208-Pin PQFP, 256-Pin BGA *(1)*	164 84, 84, 120, 164, 164 84, 120, 141, 164, 164	5.0 V 3.3 V 2.5 V	-7, -10, -15 -5, -7, -10 -5, -7, -10
EPM7512AE EPM7512B	512 512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*, 256-Pin BGA 144-Pin TQFP, 169-Pin BGA *(2)*, 208-Pin PQFP, 256-Pin BGA *(1)*, 256-Pin BGA	120, 176, 212, 212 120, 141, 176, 212, 212	3.3 V 2.5 V	-7, -10, -12 -5, -7, -10

Notes to Table 8:
(1) 1.0-mm pitch FineLine BGA package.
(2) 0.8-mm pitch Ultra FineLine BGA package.

Table 9. ACEX Devices

Device	Gates	Pin/Package Options	I/O Pins	Supply Voltage	LEs	RAM Bits
EP1K10	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*	66, 92, 120, 136	2.5 V	576	12,288
EP1K30	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*	102, 147, 171	2.5 V	1,728	24,576
EP1K50	50,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA *(1)*, 484-Pin BGA *(1)*	102, 147, 186, 249	2.5 V	2,880	40,960
EP1K100	100,000	208-Pin PQFP, 256-Pin BGA *(1)*, 484-Pin BGA *(1)*	147, 186, 333	2.5 V	4,992	49,152

Note to Table 9:
(1) Space-saving FineLine BGA package.

Table 10. Mercury Devices

Device	Gates	Pin/Package Options	I/O Pins	Supply Voltage	CDR Channels	LEs	RAM Bits
EP1M120	120,000	484-Pin BGA *(1)*	303	1.8 V	8	4,800	49,152
EP1M350	350,000	780-Pin BGA *(1)*	486	1.8 V	18	14,400	114,688

Note to Table 10:
(1) Space-saving FineLine BGA package.

continued on page 18

Table 11. APEX 20K Devices

Device	Gates	Pin/Package Options	I/O Pins	Supply Voltage	LEs	RAM Bits
EP20K30E	30,000	144-Pin TQFP, 144-Pin BGA *(1)*, 208-Pin PQFP	92, 93, 125	1.8 V	1,200	24,576
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA *(1)*, 208-Pin PQFP, 324-Pin BGA *(1)*, 356-Pin BGA	92, 93, 148, 196, 196	1.8 V	2,560	32,768
EP20K100 EP20K100E	100,000 100,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA *(1)*, 356-Pin BGA 144-Pin TQFP, 144-Pin BGA *(1)*, 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA *(1)*, 356-Pin BGA	101, 159, 189, 252, 252 92, 93, 151, 183, 246, 246	2.5 V 1.8 V	4,160 4,160	53,248 53,248
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA *(1)*	88, 143, 175, 271, 316	1.8 V	6,400	81,920
EP20K200 EP20K200E EP20K200C	200,000 200,000 200,000	208-Pin PQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA *(1)* 208-Pin PQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA *(1)*, 652-Pin BGA, 672-Pin BGA *(1)* 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA *(1)*	144, 174, 277, 382 136, 168, 271, 376, 376, 376 136, 168, 271, 376	2.5 V 1.8 V 1.8 V	8,320 8,320 8,320	106,496 106,496 106,496
EP20K300E	300,000	240-Pin PQFP, 652-Pin BGA, 672-Pin BGA *(1)*	152, 408, 408	1.8 V	11,520	147,456
EP20K400 EP20K400E EP20K400C	400,000 400,000 400,000	652-Pin BGA, 672-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)*	502, 502 488, 488 488, 488	2.5 V 1.8 V 1.8 V	16,640 16,640 16,640	212,992 212,992 212,992
EP20K600E EP20K600C	600,000 600,000	652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	488, 508, 588 488, 508, 588	1.8 V 1.8 V	24,320 24,320	311,296 311,296
EP20K1000E EP20K1000C	1,000,000 1,000,000	652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)* 652-Pin BGA, 672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	488, 508, 708 488, 508, 708	1.8 V 1.8 V	38,400 38,400	327,680 327,680
EP20K1500E	1,500,000	652-Pin BGA, 1,020-Pin BGA *(1)*	488, 808	1.8 V	51,840	442,368

Note to Table 11:

(1) Space-saving FineLine BGA package.

Table 12. APEX II Devices **Note (1)**

Device	Pin/Package Options	I/O Pins	Supply Voltage	LEs	RAM Bits
EP2A15	672-Pin BGA *(2)*, 724-Pin BGA	492, 492	1.5 V	16,640	425,984
EP2A25	672-Pin BGA *(2)*, 724-Pin BGA	492, 536	1.5 V	24,320	622,592
EP2A40	672-Pin BGA *(2)*, 724-Pin BGA, 1,020-Pin BGA *(2)*	492, 536, 735	1.5 V	38,400	655,360
EP2A70	724-Pin BGA, 1,508-Pin BGA *(2)*	536, 1,060	1.5 V	67,200	1,146,880

Notes to Table 12:

(1) The ordering code for APEX II devices is based on the number of LEs; therefore, gate count numbers are not included.

(2) Space-saving FineLine BGA package.

Table 13. HardCopy Devices

Device	Pin/Package Options	I/O Pins	Supply Voltage	Estimated Logic Gates (K) *(1)*	LEs	RAM Bits
HC1S25	672-Pin BGA *(2)*	473	1.5 V	325	25,660	1,944,576
HC1S30	780-Pin BGA *(2)*	597	1.5 V	400	32,470	2,137,536
HC1S40	780-Pin BGA *(2)*	615	1.5 V	500	41,250	2,244,096
HC1S60	1,020-Pin BGA *(2)*	773	1.5 V	700	57,120	5,215,104
HC1S80	1,020-Pin BGA *(2)*	773	1.5 V	1,000	79,040	5,658,048
HC20K400	652-Pin BGA, 672-Pin BGA *(2)*	488, 488	1.8 V	200	16,640	212,992
HC20K600	652-Pin BGA, 672-Pin BGA *(2)*	488, 508	1.8 V	300	24,320	311,296
HC20K1000	652-Pin BGA, 672-Pin BGA1, 1,020-Pin BGA *(2)*	488, 508, 708	1.8 V	460	38,400	327,680
HC20K1500	652-Pin BGA, 1,020-Pin BGA *(2)*	488, 808	1.8 V	625	51,840	442,368

Notes to Table 13:
(1) Does not include digital signal processing (DSP) blocks or memories.
(2) Space-saving FineLine BGA package.

Table 14. Excalibur Devices

Device	Gates	Pin/Package Options	I/O Pins	Supply Voltage	LEs	RAM Bits	Embedded Processor
EPXA1	100,000	484-Pin BGA *(1)*, 672-Pin BGA *(1)*	186, 246	1.8 V	4,160	53,248	32-Bit ARM922T™
EPXA4	400,000	672-Pin BGA *(1)*, 1,020-Pin BGA *(1)*	426, 488	1.8 V	16,640	212,992	32-Bit ARM922T
EPXA10	1,000,000	1,020-Pin BGA *(1)*	711	1.8 V	38,400	327,680	32-Bit ARM922T

Note to Table 14:
(1) Space-saving FineLine BGA package.

Table 15. Serial Configuration Devices

Device	Pin/Package Options	Supply Voltage	Description
EPCS1	8-Pin SOIC *(1)*	3.3 V	1-Mbit serial configuration device designed to configure Cyclone devices up to the EP1C6 device
EPCS4	8-Pin SOIC	3.3 V	4-Mbit serial configuration device designed to configure Cyclone devices and Stratix II devices up to the EP2S15 device
EPCS16	16-Pin SOIC	3.3 V	16-bit serial configuration device designed to configure Cyclone devices and Stratix II devices up to the EP2S60 device
EPCS64	16-Pin SOIC	3.3 V	16-bit serial configuration device designed to configure Cyclone and Stratix II devices

Note to Table 15:
(1) SOIC: Small outline integrated circuit.

Table 16. Configuration Devices for Stratix, Stratix GX, Cyclone, APEX II, APEX, Excalibur, FLEX, Mercury & ACEX FPGAs

Device	Pin/Package Options	Supply Voltage	Description
EPC1441	8-Pin Plastic Dual-In-Line Package (PDIP), 20-Pin PLCC, 32-Pin TQFP	3.3 or 5.0 V	441-Kbit configuration device designed to configure all FLEX® and ACEX® devices
EPC1	8-Pin PDIP, 20-Pin PLCC	3.3 or 5.0 V	1-Mbit configuration device designed to configure APEX™, FLEX, and ACEX devices
EPC2	20-Pin PLCC, 32-Pin TQFP	3.3 or 5.0 V	In-system programmable 1.6-Mbit configuration device designed to configure Stratix, Stratix GX, Cyclone™, APEX II, APEX, FLEX, Mercury™, ACEX, and Excalibur™ devices
EPC4	100-Pin PQFP	3.3 V	In-system programmable 4-Mbit configuration device designed to configure Stratix, Stratix GX, Cyclone, APEX II, APEX, FLEX, Mercury, ACEX, and Excalibur devices
EPC8	100-Pin PQFP	3.3 V	In-system programmable 8-Mbit configuration device designed to configure Stratix, Stratix, Stratix GX, Cyclone, APEX II, APEX, FLEX, Mercury, ACEX, and Excalibur devices
EPC16	88-Pin BGA *(1)*, 100-Pin PQFP	3.3 V	In-system programmable 16-Mbit configuration device designed to configure Stratix, Stratix GX, Cyclone, APEX II, APEX, FLEX, Mercury, ACEX, and Excalibur devices

Note to Table 16:
(1) Ultra FineLine BGA package.

Bigger *and* faster.

Engine shown is from a Boeing 777.

Stratix® II The world's biggest and fastest FPGAs!

The revolutionary Stratix® II family has the highest density, highest performance, and most efficient architecture on the market. Built on an innovative new adaptable logic structure, Stratix II devices break speed barriers with 50% higher performance and more than twice the logic capacity of the award-winning Stratix FPGAs, all at a lower cost.

- Optimized for 90-nanometer technology
- High-performance DSP circuitry
- Flexible embedded memory blocks
- Low-skew clock structure and PLLs

Designs targeting the groundbreaking Stratix II family can migrate seamlessly to low-cost HardCopy® structured ASICs, allowing engineers to minimize costs while decreasing their development time.

Supported by QUARTUS® II

When you need a company to rely on, Altera delivers.

ALTERA®

The Programmable Solutions Company®

www.altera.com/stratix2

Leading through innovation.

ASIC Painkiller!

HardCopy. ASIC gain without the pain.

HARDCOPY™

Get to risk-free, high-volume production with HardCopy™ devices—the industry's only structured ASICs with a seamless FPGA prototyping capability. Designers can use an FPGA to minimize up-front investment, perform in-system verification, and get a head-start on system development and qualification, then move seamlessly to a HardCopy structured ASIC. This development flow bypasses the pain and expense of traditional ASIC development while still meeting cost, performance, and power requirements.

Start your high-volume design today with the HardCopy Starter Kit and experience ASIC gain without the pain.

- First-silicon success guaranteed
- 50% faster than FPGAs
- 40% less power consumption than FPGAs
- Fully supported by $2,000 Quartus® II design software
- Priced for high-volume, cost-sensitive applications

Supported by QUARTUS® II

ALTERA®

The Programmable Solutions Company®

www.altera.com/hardcopy

Cyclone Devices: The Fastest Ramping FPGAs Ever

The evolution of the semiconductor industry has fundamentally changed the applicability of FPGAs to include high-volume, low-cost applications. A few years ago, the closest an FPGA could get to low-cost applications was as an ASIC prototype. With the introduction of the Cyclone™ series, hardcore ASIC designers have jumped into the new reality: they can lower risk, accelerate time-to-market, and still maintain the low-cost benefits of an ASIC by using Cyclone FPGAs.

After 20 years of process and FPGA technology evolution, the crossover point for choosing an FPGA instead of an ASIC has arrived for the majority of ASIC design starts. This is driven by two things: the high cost to design and verify an ASIC and the availability of the low-cost Cyclone FPGAs. Even in many high-volume applications, the combined development and production costs of ASICs exceeds that of the Cyclone FPGAs. Cyclone devices are the right product at the right time to take advantage of this crossover from ASIC to FPGAs.

The success of Cyclone FPGAs in high-volume consumer applications has been extremely exciting for Altera. Consumers can go to their local electronics store and have choices of flat screen and DLP TVs, portable video recorder/players, DVD recorders, and a large variety of other equipment that includes Cyclone devices. Other consumer equipment that will have Cyclone devices includes satellite receivers, set-top boxes, and soon-to-be released home entertainment networking equipment.

Cyclone devices are being used for many innovative electronic applications spanning audio, video, wireless, and recreation. Dimension Technologies' 3D monitor allows viewers to see 3D images without special glasses (see Figure 1). Digidesign, a division of AVID, created an audio workstation card that enables high-end audio editing within a PC. Pinnacle has launched a USB- and Firewire-powered video interface that enables analog and digital video camcorders to easily interface to PCs (see Figure 2). Koolspan has a 256-bit AES wireless encryption device that significantly increases the security over conventional wireless ports (see Figure 3). Finally, watch out fish, Navman has released a high-performance color fish finder for sport fisherman (see Figure 4).

Figure 1. Dimension Technologies' 2D/3D Display

Figure 2. Pinnacle's USB-to-Video System

Figure 3. Koolspan's Wi-Fi Security System

Figure 4. Navman's Marine Navigation System

The amazing thing about these consumer applications, relative to the FPGAs traditional high-performance equipment applications, is that the time from device selection to high-volume production is very short. After little more than a year in the market, Cyclone FPGAs are in many end products that have ramped to tens of thousands of units a month with some forecasted to be over a million units a year. Altera has already shipped over 3 million Cyclone devices and this will dramatically grow throughout the year.

In our planning for the Cyclone family, we knew that to be successful we would have to reliably deliver high volumes of devices early in the product lifecycle. This drove one of our most important technology decisions, utilizing the 130-nm, 8-layer copper process from TSMC. Based on our successful launch and ramp to production of Stratix® devices on the same process node, we knew we could reliably deliver Cyclone FPGAs fast and in volume. In the low-cost, high-volume product category, vendors cannot tolerate supply issues as market windows are brief and explosive. As a result of our planning, Altera has not missed a single customer delivery of Cyclone devices.

So why has the Cyclone family taken off like no other FPGA in the industry? In the beginning of the development of the Cyclone series, the key objective was to build the lowest-cost FPGAs ever and make it easy to utilize in traditionally high-volume ASIC applications. Our product development process was based on extensive customer interaction in new markets that traditionally rely on ASICs due to cost concerns. Altera had to develop a brand new cost-optimized FPGA architecture from the ground up. Altera's customer-driven product definition process, initially developed to specify our performance-leading Stratix FPGA family, is now being used in all our product development efforts including Stratix II, HardCopy™, MAX® II, and Cyclone II devices, the Quartus® II software, and the Nios® II processor.

The Quartus II software has been a key contributor to the success of the Cyclone series. The objectives for Cyclone devices are to make them easy to use and easy to adopt. The Quartus II software makes designing for Cyclone devices extremely easy for new FPGA designers and experienced ASIC designers alike. Push-button design flows get new designers up and running fast while advanced scripting capabilities enable automation of complex tasks for expert designers. The Quartus II software comes in several versions, the most common being the free Quartus II Web Edition software. To facilitate the goal of developing the lowest cost FPGA, the Quartus II Web Edition software includes complete support for all Cyclone devices. In other words, free development tools are available to anyone who wants to design with Cyclone FPGAs.

The introduction of the Cyclone series leveraged another major innovation from Altera. The Nios processor is the industry's first soft processor designed for implementation onto an FPGA. With Cyclone devices, the cost structure of using the Nios II processor is only $2.00 for a 32-bit microcontroller while maintaining all the strong benefits inherent in an FPGA. The Nios development kit is based on a Cyclone EP1C20 device and has been identified as one of the top three processor development kits by any manufacturer according to independent user satisfaction surveys. As Altera rolls out Cyclone II devices and Nios II processors, the related capabilities will again go way up and the costs will go way down. When using a Nios II processor in a Cyclone device, a user can spend as little as $0.35 on logic.

The Cyclone family is the fastest ramping FPGA ever from any company. This, we believe, reflects both the huge opportunity available to use FPGAs instead of ASICs, as well as the successful implementation of Altera's customer-driven product development process. Every day we hear about new Cyclone-based applications that demonstrate the expanding reach of FPGAs.

CycloneBot Knocks Out the Competition with Cyclone & Nios 1-2 Punch

by Michael Hermann
Vice President of Engineering Operations
Nuvation Engineering

Company:
Nuvation Engineering

Industry:
Electronic Design Services

Altera Products:
Cyclone FPGAs
Nios Processor

Today's embedded programming environment is continually changing. One of these new forms of technology goes beyond the standard programming model. Traditionally, an engineer writes code, compiles it, and runs it all on a development board with a known, unchangeable, and defined processing platform. Today's technology now allows us to take this same model and apply it on a FPGA development board, but now we can change the platform repeatedly until we have the optimal balance between hardware and software. While it's easy to state, the implications are quite profound—Nuvation now has a programmable platform as well as a programmable application. To provide this exciting new capability Altera has built the Nios® Development Kit, which combines an FPGA-based embedded system development board with the Nios® processor, a soft intellectual property (IP) core available for most Altera® FPGAs, and its excellent development environment. Between the Nios processor itself, the software tools, and the board, Altera provides an excellent out-of-the box experience, enabling easy adoption for almost any user.

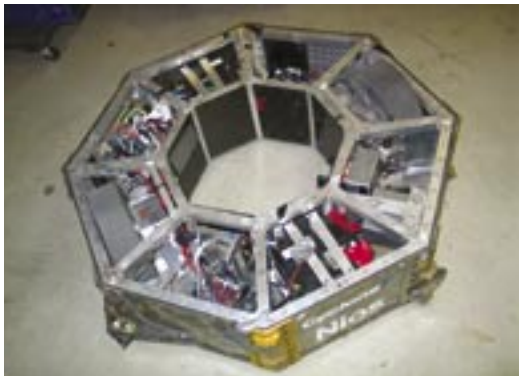
This article discusses the most interesting Nios application—CycloneBot. I'll take you through a brief explanation of our team and CycloneBot, a bit of CycloneBot's history, and then I'll take you on a bit more detailed walk through our electronics and firmware development cycle, and show you just how much of an impact our use of the Nios processor made.

CM Robotics is the name of Nuvation's engineering and building team. CM Robotics builds robots to beat up on other robots, and is supported by its team members and our sponsors, including Altera. Altera has been a wonderful corporate sponsor, enabling us to build a unique application around the Nios processor.

CycloneBot is CM Robotics' first robot in the 220 pound heavyweight fighting robot classification. Nuvation knew that CycloneBot was going to be a challenge. It was going to be complex, expensive, and, most importantly, it was going to be a true engineering challenge. It would be far more electronically advanced than most robots we compete against. To achieve this would involve bringing on new team members, creating new algorithms, and developing design concepts unheard of in the field.

CycloneBot's primary technological advantage comes from its drive system. Balanced on just two wheels, CycloneBot spins on its y-axis at over 400 rpm (see Figure 1). To induce directional movement, the speed of each wheel is constantly and controllably modified. Achieving controlled movement while spinning requires significant processing power to manage and update the motor speeds, to read the sensors that determine current heading (direction), and an algorithm to integrate these functions.

Figure 1. CycloneBot Interior Structure



Like any good engineering team, Nuvation started from a challenge and devised a practical and realistic model for defeating it. Nuvation established two prototype phases. The "C1" phase involved proving that the algorithm could work. It was implemented on a small wooden platform using an 8-bit processor programmed using a variant of BASIC, two small motors, and a toolbox as the electronics case. Nuvation was able to use a magnetometer to gather heading information, simple motor controllers to manage wheel speed, and a basic 8-direction control system to move while spinning. Nuvation had a controllable robot that could spin its entire body and move at the same time. This simple little robot proved the basic drive system challenge could be met.

The "C2" phase involved introducing the more powerful motors, complex motor controllers, multiple sensors, and the wireless communications we planned for the real CycloneBot. The original plan was for it to be electrically identical to the actual end robot design, with the exception of the battery power system. Nuvation started "C2" using a DSP-based control system. We were using a fairly advanced 16-bit DSP processor with standard motor-control peripherals (quadrature encoders and PWM generators in particular). Nuvation got some basic communications and controls running, but we often encountered sensor and motor interface limitations and certainly had our

share of development system challenges. Nuvation simply needed either more processing power, or better motor controllers, or better sensor interfaces, or a combination of all three. What we really needed was flexibility and we needed it fast.

At this point, we approached Altera about the Nios processor and Cyclone™ FPGA family. A number of us on the team work at Nuvation, a Certified Design Center partner of Altera, so we were familiar with the technology, and felt that the Nios and Cyclone combination could help us move enable our design to move forward faster, better, and with much more flexibility. Altera provided us with Nios Development Kits, Cyclone Edition, and access to excellent resources for design discussions and technical input.

The next stage for CM Robotics was to port the existing DSP code and algorithms and the sensor/motor interface setup onto the Altera platform. All told, it took about 15 person-hours to setup the development platform, port the code, adapt to the new register interfaces for control routines, and integrate the sensors and motor controls circuits to the development board. There were probably another 15 or so person-hours in the physical side of the change —mounting the new board inside the robot, changing the cables, updating connections, and so forth. Our port moved forward so successfully due to a combination of good starting code, the ability to quickly develop a custom Nios hardware system using SOPC Builder, the excellent Nios development tools, and the fact that everything worked right out of the box.

The process for porting our code from the DSP to the Nios processor was remarkably simple. We had already built our code in a three-layered modular system, all written in C, where we had the core application, the functional interface, and, at the lowest level, the hardware interface. The core application, consisting of modules for algorithm execution, motor coordination, and command execution, did not change significantly. At the next layer down we provided an interface for the application code for each of the major system functions, for example the magnetometer, the motor, the tachometer, the serial link, and so on. The key here was not passing on any hardware-specific elements from the lower level to the upper level when building the layer. We were relatively successful here, though sometimes we needed to change the interface exposed to the application to something more generic.

The lowest level, the hardware interface, is where we wrote routines and macros around the chip-specific registers. While it is essentially a total rewrite to change processor architectures and the peripherals, the quality of the documentation, reference code, and application notes from the vendor has a dramatic effect on the time and complexity completing the rewrite. Our DSP-based system had provided us with a very high-level hardware interface which they achieved by using a lot of C conventions for I/O devices. We decided to work directly with the peripheral registers because the Nios processor and its peripheral documentation was clear and concise, and the registers themselves were quite straightforward.

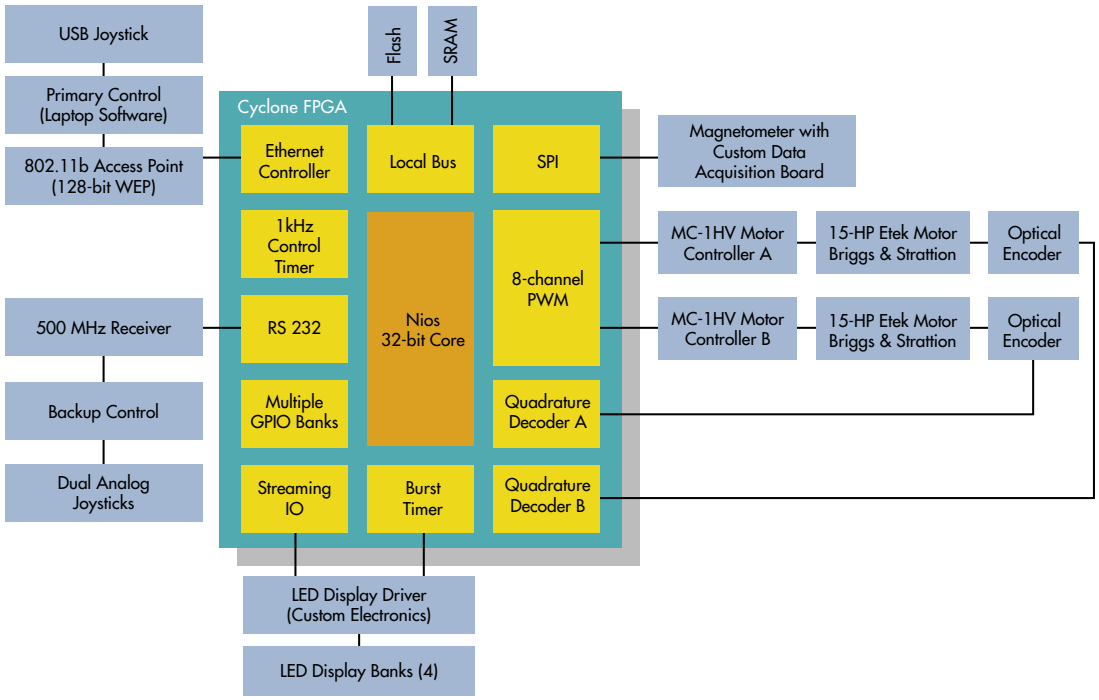
During our porting time we saw new solutions coming from the programmable Cyclone FPGA and soft-core Nios processor model. At one point, we needed to make a cable to match the motor controller and the Nios Development Board pinouts. We just let the electrical guys make the cable however it physically worked the easiest, and recompiled the processor subsystem with new pinouts to match the cable. In other words, we recompiled our processor to solve a physical problem, meaning the processor connections on the development board were no longer a constraint to be worked around. It certainly makes a lot of engineers happy when they can make wholesale changes by recompiling instead of rewiring.

The real CycloneBot (C3) is quite an advanced robot design. The electronics system diagram in Figure 2 shows a number of complex sub-systems, including wireless communication and the Nios Development board. The Nios processor subsystem we're using includes pulse width modulators (PWM), quadrature encoders, multiple timers, UARTs, SPI, general-purpose I/O pins, and on-chip and off-chip memory, and various other peripherals provided or created by us. This powerful, fully custom system is realized in a single Cyclone FPGA. Developing the custom systems as we advanced the design was easy through the use of Altera's SOPC Builder system development tool that is included with the Quartus® II software.

Our communications system uses a dual approach, with 802.11b for our primary system, and a robot-specific 900-MHz system for our backup system. At the data layer, both systems run the same custom command protocol; therefore, we can shift seamlessly to the backup should our primary system run into interference. This is an example of another part of our design philosophy—redundancy wherever possible.

continued on page 26

Figure 2. CycloneBot Intelligence



We've implemented a custom data acquisition board for the magnetometer that which provides us with the necessary filtering and analog-to-digital conversion. We implemented a custom peripheral to interface to the processor. We also have an LED array system that is used to print messages on the side of our robot while it is spinning. While toggling the LEDs on/off is simple, displaying a readable message while spinning requires either constant attention by the processor or a custom peripheral to change the stripe of LEDs once per revolution to make the eye see a full message scrolling. We chose a custom peripheral. This way we write the message to the peripheral, and peripheral manages the illumination of the LEDs without further processor interaction.

The drive system works today by a system not unlike our original "C1" prototype. To derive heading, we use quadrature encoders (custom peripherals) to gather data from optical encoders on the wheel, which is then used to determine how far we have driven. As we spin, this gives us a relative heading per revolution, which we correct and reconcile against a true heading using the compass heading from the magnetometer. This all derives a current heading that we update every millisecond. As we go through a rotation, the motor-control algorithm modulates the speed of each wheel as it travels its circular path. These modulations create our translational movement.

In addition to all this, we have CylconeBot running a mini-web server that we use to report run-time performance and status data. We can monitor the robot during battle and adjust our strategies. Using the web-server link, we can also change the hardware or the software configurations to handle magnetic or RF interference.

CycloneBot has been competing this past year and has continued to reach the semifinals. In each battle, we learn new things and make adjustments. We have never been beaten by the other robot—our losses have been due to internal failures of mechanical restraints or power systems. CycloneBot has qualified for and will be battling in the upcoming Robot Fighting League 2004 Nationals (**www.botleague.com**).

The next steps for CycloneBot are numerous, ranging across all of our mechanical, power, electrical, and control systems. As for the Nios system, we will move to the new Nios II embedded processor for its improved performance and will likely move to a two-Nios II system, allowing us to separate real-time controls from communications. Since all of our coding is in C, updating the system is a few clicks in SOPC Builder, and just a few lines of code away. Through the flexibility of soft-core CPUs in FPGAs we hope to meet our goal for CycloneBot to be ranked as the number 1 heavyweight fighting robot in the world.

Cyclone economics.

The lowest-cost FPGAs ever.
Available now.

Cyclone™

Powerful by nature. Low cost by design.

The Cyclone™ family is taking the industry by storm. Designed from the ground up based on extensive input from hundreds of customers, the Cyclone family offers the ideal combination of cost, density, features, and performance for volume-driven applications. Since introduction, thousands of customers have used Cyclone devices in applications ranging from plasma displays and wireless basestations to printers and hand-held radios. Cyclone devices are the lowest-cost FPGAs ever, making them a compelling alternative to costly ASICs for high-volume designs.

For high performance, fast time-to-market, and a price that will blow you away, contact us today at www.altera.com/cyclone.

ALTERA®

The Programmable Solutions Company®

http://www.altera.com/cyclone

Cyclone FPGAs Enable Affordable, High-Performance Media Storage

by Mike Anderson
CTO
Huge Systems

Company:
Huge Systems

Industry:
Broadcast

End Products:
Media Storage

Altera Product:
Cyclone FPGAs

The proliferation of affordable desktop video editing platforms combined with the coming dawn of high-definition (HD) content, is increasing the need for affordable, high-performance storage aimed at an emerging range of mid-level users. Until recently, however, the ability to meet this need was largely absent in the marketplace, as solutions were prohibitively expensive and physically large.

Huge Systems, based in Agoura, CA, is changing the storage paradigm for mid-level users in these arenas by developing a range of media storage products that combine the robust storage capacity of ATA/IDE disk drive technology with all of the advantages of Ultra320 SCSI at a price point less than half of the nearest competitor. The result is a compelling range of solutions that are future-proofed for high definition and allow users to tackle a range of content-reliant, high-resolution digital video applications.

The Altera Cyclone™ FPGA device contained in every Huge Systems MediaVault™ encompasses all the RAID and ATA logic on a single device. Huge Systems selected the Cyclone device because it can compactly contain all of the control directives and reduce the overall size of the hardware architecture that is necessary to derive the throughput rates required for high definition from only five IDE/ATA disk drives.

Huge Systems selected the Cyclone device because it can compactly contain all of the control directives and reduce the overall size of the hardware architecture that is necessary to derive the throughput rates required for high definition from only five IDE/ATA disk drives.

The Cyclone device directly drives five parallel ATA buses, each transferring data at 100 Mbits per second, fully in parallel. It also contains both the RAID 0 striping logic and the RAID 3 parity generation and reconstruction logic. Using a single device greatly reduces board space, heat, and power consumption while increasing reliability.

The result is a storage solution that requires fewer disk drives to achieve true HD rates, weighs less, and subsequently also needs less power. Because there are fewer drives, less heat is also generated, thereby reducing cooling requirements, and ultimately reducing cost. These all combine to provide a maximum return on investment for the user.

Huge Systems plans to also incorporate Altera's Cyclone II FPGAs in a new range of storage arrays using the Nios® embedded processor to supplement the processing power of the product and further increase system performance.

A variety of next-generation Huge Systems MediaVault U320-S (single channel), U320-S Dual (dual channel), and U-320-R (removable drive) storage arrays all feature an Ultra 320 controller and interface capable of sustaining over 200+ Mbytes per second sustained—more than enough to support even the most demanding HD applications. A single 5-drive Huge Systems MediaVault U320-R and each channel of the U320-S Dual can support 10-bit HD video and are available in a range of storage capacities ranging from 600 GB up to and incredible 2.5 TB. Dual fans and a hefty 200 watt power supply provide cooling and power to spare.

The MediaVault U320-S Dual is essentially two MediaVault U320-R disk arrays in a single chassis. Each disk array is independent with its own disk drives and U320 controller. The U320-S /Dual can be configured in RAID 0 (performance) or RAID 3 (protected) operation. In RAID 0 mode, all 5 drives are used for storage and maximum performance (200+ Mb/sec sustained). When in RAID 3 mode, one drive is used for "parity" information, so performance and capacities are reduced about 20%. In RAID 3 mode, even if a drive fails, the stored content will still be available and one can continue working with no degradation in performance.

The next-generation MediaVault U320-R also features an Ultra320 interface capable of sustaining over 200 Mb/sec in HDT mode (High Definition Turbo mode insures 200 Mb/sec data rate with a modest reduction in capacity). This makes the Huge Systems MediaVault U320-R the only storage array available that supports 10-bit HD capture and playback from a single 5-drive unit. The redesigned, industrial looking chassis supports five removable drives that are each hot swappable and is available in capacities from 600 GB up to 1.25 TB.

A variety of users in the film, video, and content creation arenas have welcomed the MediaVault U-320-R and U320-S/Dual's true plug-and-play capabilities. SCSI outputs provide for instant connectivity to Mac platforms running a variety of non-linear editing platforms, including Leitch Technology's VelocityQ, Blackmagic Design's Decklink HD, and Pinnacle's CinéWave 4.5. Each channel's next-generation onboard programmable RAID controller takes care of formatting, stripping, and all RAID functions —while appearing as one (U320-S) or two (U320-S Dual) Huge disk drive to the operating system. The controller also provides built-in diagnostics to monitor drive performance and health.

Cyclone FPGAs & Nios Processor Power Enhanced Capabilities in Automotive Diagnostic Tool

by Ivan Kotzig
Chief Engineer
Toolrama

Toolrama develops automotive diagnostic equipment for customers such as DiabloSport. Recently, Toolrama was asked to upgrade the performance of one of our designs, DiabloSport's Predator (see Figure 1), a state-of-the-art, high-performance tuning flash programmer that is used to advance a vehicle's timing and optimize the air/fuel ratio, as well as remap the transmission shift points in automatic transmissions. Predator communicates with the vehicle through an industry-standard OBDII interface. Specifically, Toolrama needed to increase the tool's computing power to enable a larger LCD with more attractive graphics, provide TCP/IP connectivity, and support an SD flash card with a FAT32 file system. Since we had already maximized the tool's hardware system, upgrading the tool was a challenge.

Toolrama's earlier design used the Motorola CPU32 family. Upgrading to a more powerful Motorola processor was not a viable solution, since the resulting increase in cost would have resulted in non-competitive pricing for next-generation Predator tools.

Toolrama was aware of Altera's Nios® embedded processor and recognized the potential it offered in terms of cost and hardware flexibility. Toolrama did not use the Nios processor for this application, but their engineers were so impressed with its capabilities that Ivan Kotzig and James Roth started Kros Technologies and created KROS, a Nios-native, small-footprint, real-time operating system (RTOS). Anticipating that Altera would be offering us a Nios platform that could compete price-wise with the Motorola processor, we rewrote our ANSI C software to run under our Kros RTOS and released the original version of Predator using the new software.

When it came time to upgrade the Predator tool, the Cyclone™ FPGA was available, providing us with the platform we needed to use the Nios processor in conjunction with our Kros RTOS. In January of this year, we initiated our Predator upgrade project with a block diagram. By early February we had the board in our hands and were ordering components. We had our assembled prototype by the end of that month, and from there it took just two days to have it up and working and another two to load the application software. When Altera talks about ease of design and implementation with its Cyclone FPGAs and Nios processor, they are not kidding! It cost us only $1,000 and 100 hours of engineering time to produce a functioning prototype. Altera's SOPC Builder design tool played a key role in facilitating this extremely short design cycle.

Our new Cyclone- and Nios-powered design offers much higher performance and includes both a 90 frame-per-second graphics controller and an SD flash card interface built into the Cyclone device, providing increased system integration. It also contains the desired TCP/IP connectivity and FAT32 file system, as well as a full GNU development environment. In addition, unlike the Motorola CPU-based design, which required the processor to manage the display, consuming considerable processing bandwidth, the new Predator version uses a dedicated LCD controller peripheral that makes very small demands on the processor. Since this peripheral is compliant with Altera's Avalon™ switch fabric, it was particularly easy to integrate it into the system using Altera's SOPC Builder tool.

In addition to the benefits described above, our Cyclone and Nios implementation provides us with an open upgrade path for future Predator systems. We intend to base all our future designs on the Cyclone and Nios platform and look forward to harnessing the cost and performance benefits of the Nios II embedded processor and the Cyclone II FPGA family.

Figure 1. DiabloSport Predator

Company:
Toolrama

Industry:
Automotive

End Products:
Automotive
Diagnostic Tool

Altera Products:
Cyclone FPGAs
Nios Processor

When Altera talks about ease of design and implementation with its Cyclone FPGAs and Nios processor, they are not kidding!

Cyclone FPGAs Drive Industry's First Low-Cost OEM Solution for High-Performance Data Streaming over GigE

by George Chamberlain
President
Pleora Technologies Inc.

Company:
Pleora Technologies

Industry:
Machine Vision

End Products:
Video-to-Gigabit Ethernet

Altera Product:
Cyclone FPGAs

Gigabit Ethernet (GigE) is the third generation of Ethernet, the dominant global protocol for local-area network (LAN) communications. Like earlier Ethernet generations, GigE equipment has 10 times more bandwidth than its predecessor and, as volumes grow, is becoming increasingly affordable.

But the GigE chapter of the 25-year Ethernet saga is also a bit different. With GigE, Ethernet now has enough bandwidth—Gbit per second—to serve as a viable communications platform for a host of applications outside its traditional LAN stronghold. GigE is a good fit for any application that streams data at high speeds, such as broadcasting, machine vision, automated imaging, and high-end surveillance systems.

Most of the systems used today for applications like these incorporate specialized, high-performance data transport and switching products, which are usually costly and difficult to integrate. GigE's high-speed data rate and low-cost platform make it an attractive alternative to specialized equipment. Moreover, GigE offers the ease-of-use and networking flexibility that helped make Ethernet the world's reigning LAN protocol.

The low pricing of Altera's Cyclone devices has helped Pleora achieve the price points needed to enter competitive markets in medical imaging, machine vision, intelligent traffic systems, and surveillance/military.

There are technical challenges, of course. Data that travels over GigE must be formatted as Internet Protocol (IP) packets. If the data is in another format—video, audio, or other data types—the system needs protocol conversion technology that can pump out IP packets at GigE rates. To deliver high-end performance, data must be transferred with low, predictable latency (or end-to-end delay). There can also be no risk of data loss.

Working with the Cyclone™ EP1C6 FPGA, Pleora Technologies has developed the industry's first low-cost GigE solution that meets these challenging requirements. Pleora's iPORT™ Connectivity Solution delivers wire-speed, low-latency data transport over standard GigE connections, while guaranteeing packet delivery.

Three-Part iPORT Solution

The iPORT Connectivity Solution has three elements. The heart of the solution is the iPORT PT1000-ST Protocol Engine, a small-footprint OEM board (see Figure 1) that integrates easily with a wide range of system architectures.

The iPORT engine efficiently converts almost any type of data, including voice and video, into IP packets for GigE transport. Driven by the Cyclone FPGA, it delivers the full 1-Gbit per second GigE data rate while achieving the lowest, most consistent latency in its class—typically less than 200 microseconds from data source to PC memory. The engine's interface captures data as wide as 24 bits at clock rates of up to 80 MHz. Since the solution is FPGA based, the interface can be customized for almost any application.

The second element of the solution is the iPORT IP Device Driver. This software loads quickly and easily onto standard PC network interface cards/chips, where it performs an advanced direct memory access (DMA) function. The driver streams data to PC memory using almost none of the machine's CPU, leaving about 99 percent of these resources available for running applications.

Pleora offers two versions of the driver. The iPORT High-Performance IP Device Driver delivers top performance for demanding applications. The iPORT Universal IP Filter Driver achieves high-throughput streaming with simultaneous access to corporate networks.

The third element is the iPORT Software Development Kit (SDK), which provides users with the building blocks needed to interface iPORT products to just about any custom application or third-party applications software, such as Labview.

Cyclone Helps Cap Pricing

As one of two core components in the PT1000-ST Protocol Engine, the FPGA dominates the cost of the board. The low pricing of Altera's Cyclone devices has helped Pleora achieve the price points needed to enter competitive markets in medical imaging, machine vision, intelligent traffic systems, and surveillance/military.

The Cyclone device has enough capacity to support Pleora's advanced application, and its flexible memory architecture has helped Pleora lower production costs by improving iPORT design efficiencies. In these respects, the Cyclone FPGA has been a key enabling technology for Pleora's success.

Pleora is also taking advantage of the Cyclone device's remote programmability to build good customer relationships. Many of Pleora's customers are developing custom systems, and requests for new features must be addressed quickly. Pleora meets this need cost-effectively by delivering new loads to Cyclone FPGAs in field-deployed iPORT engines over standard GigE connections.

Broader Architectural Options

In addition to providing a cost-effective alternative to specialized communications gear, the iPORT™ Connectivity Solution allows OEMs and systems integrators to improve efficiencies by leveraging GigE's unmatched networking flexibility and ease of use.

The PT1000-ST Protocol Engine supports most GigE networking topologies, including switched GigE interconnect between multiple devices and PCs, data multicasting to more than one PC, and distributed processing across more than one PC.

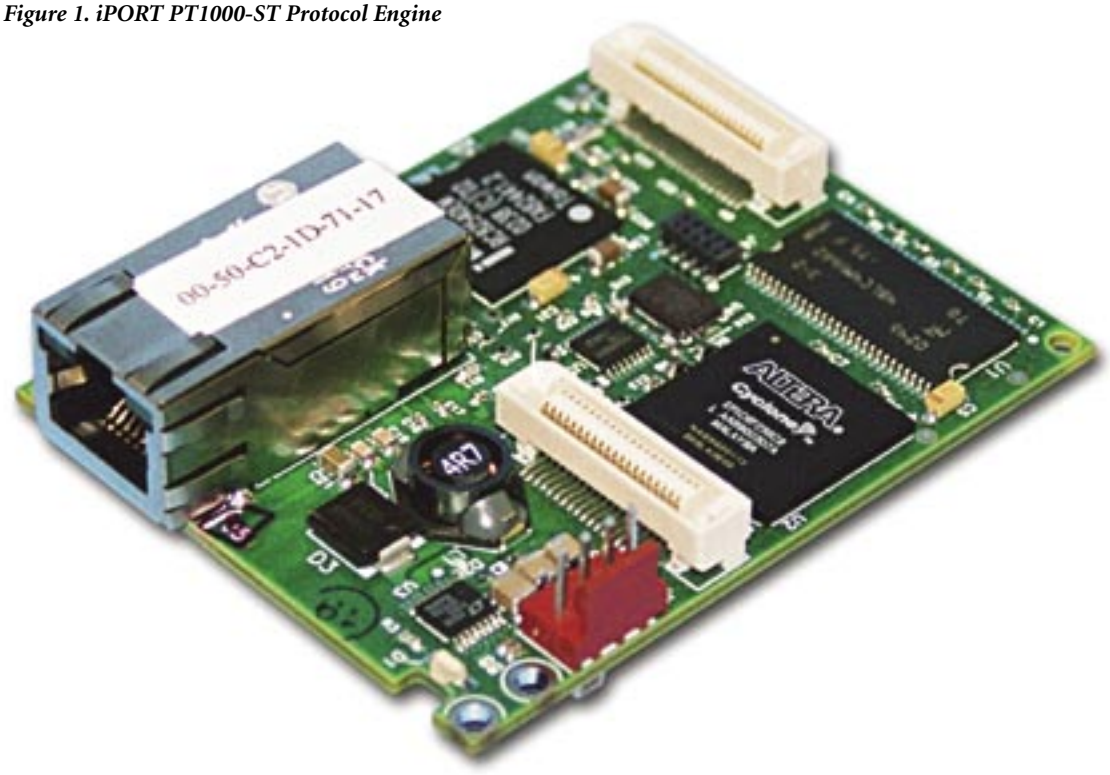
Furthermore, all GigE platforms—point-to-point links or packet-switched configurations—use well-understood, industry-standard equipment, such as Category 5 copper cabling, ordinary PC interface cards/chips, and straightforward LAN switches. This equipment is widely available and easy to integrate. By contrast, building systems with specialized gear is typically a slow, tedious process plagued by multi-vendor integration issues.

10GigE

The low-latency, wire-speed GigE transport solution offered by Pleora has one other key benefit, a migration path to even higher-speed solutions. The fourth Ethernet generation, 10GigE, which operates at the blazing speed of 10 Gbits per second, is already running over fiber. Meanwhile, work on a physical interface (PHY) for 10GigE over copper is proceeding nicely. Under the current timeline, the copper specification, known as IEEE 802 10GBASE-T, will be ratified in 2006. Pleora is already working on technology that will leverage this higher-speed commercial platform.

Pleora Technologies is a leading supplier of software and hardware products for high-performance data streaming over GigE networks. To contact Mr. Chamberlain, email **george@pleora.com**. For more information, visit **www.pleora.com**.

Figure 1. iPORT PT1000-ST Protocol Engine



National Instruments Announces Cyclone FPGA-Based Digital I/O Products Ideal for Industrial Measurement & Control Applications

by Rahul Kulkarni
Product Manager
(Industrial Data Acquisition and Control)
National Instruments

Company:
National Instruments

Industry:
Measurement & Automation

End Products:
PCI/PXI Data Acquisition Boards

Altera Product:
Cyclone FPGAs

With the advent of PC-based platforms for discrete, batch, and continuous automation applications, automation suppliers strive to provide customers with low-cost, PCI-based I/O modules (see Figure 1) with the safety and reliability features of a PLC. National Instruments (NI) recently released a new family of low-cost industrial digital I/O modules that delivers a high reliability industrial feature set using the Altera® Cyclone™ FPGA. These features, not all previously available for digital I/O modules on a single PCI module, include watchdog timers, change detection, input filters, and power-up states, all of which are programmable through software without jumpers. Many of the new products also feature isolated inputs and outputs for connecting to high-voltage, high-current, or high-noise signals.

Each of the modules feature an I/O connector, optocouplers for isolation, interface to PCI/PXI bus, and an Altera Cyclone FPGA to implement the industrial feature set (see Figure 2). Early in the development of the product incorporating these features on a PCI/PXI board seemed to be a daunting task, faced with tight deadlines, low target cost of the board, and a new development team.

Figure 1. NI's New FPGA Based Digital I/O Modules with High Reliability Industrial Features

"National Instruments has consistently set a price/performance standard for industrial measurement and control applications. We wanted to introduce powerful industrial features at the lowest cost in our new digital boards," noted Keith Winkeler, Engineering Section Manager for Data Acquisition and Control. "By using the Altera Cyclone FPGA and Quartus® II software tools, we were able to develop in a short time 12 new digital I/O products with superior industrial features and an aggressive price."

The following advanced features were implemented on the Altera Cyclone FPGA.

Input Filters

Input filters implemented on the Altera Cyclone FPGA help discard erroneous readings caused by a bouncing switch or chatter in relays. It does this by ignoring any pulses that are too small in width. You can programmatically select the minimum pulse width that is guaranteed to pass, thus eliminating chatter.

Power-Up States

With programmable power-up states, you can configure the initial output states of the board in software to ensure glitch-free operations when connected to industrial actuators such as pumps, valves, motors, and relays. You can configure each individual digital line as high-impedance input, high output, or low output. The digital I/O module stores the settings in on-board, non-volatile memory, and the Altera Cyclone FPGA implements the power-up states automatically after power is applied to the device.

Watchdog Timers

NI digital I/O watchdogs are an innovative technology that provide protection against a wide variety of fault conditions, including application failures or even a PCI bus failure. Watchdogs enable the digital outputs to go to a safe state when a fault condition is detected, allowing safe recovery. The Altera Cyclone FPGA monitors the software application and, if it fails to respond within the time limit, automatically sets the output lines to a user-defined safe state. The module remains in the watchdog state until the watchdog timer is disarmed by the application and new I/O values are written or until the computer is restarted.

Change Detection

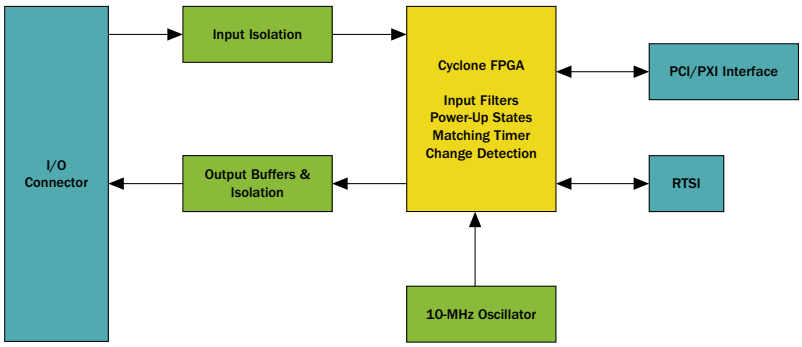
With change detection, you can automatically trigger your software application to perform a digital read operation upon a digital change of state. Change detection allows you to monitor for digital events with minimal processor usage.

The features implemented on the Altera Cyclone FPGA, coupled with integrated signal conditioning features like optical isolation and 24-V logic levels, have made these boards very attractive to industrial measurement and control engineers and machine builders. Not only do you get on-board intelligence for safety and reliability, but also integrated signal conditioning for direct connectivity to industrial sensors and actuators—all at a low price of $5 per channel.

About National Instruments

National Instruments (**www.ni.com**) is a technology pioneer and leader in virtual instrumentation—a revolutionary concept that has changed the way engineers and scientists approach measurement and automation. Leveraging the PC and its related technologies, virtual instrumentation increases productivity and lowers costs through easy-to-integrate software, such as the NI LabVIEW graphical development environment, and modular hardware, such as PXI modules for data acquisition, instrument control, and machine vision. Headquartered in Austin, Texas, NI has more than 3,100 employees and direct operations in 40 countries. In 2003, the company sold products to more than 25,000 companies in 90 countries. For the past five years, Fortune magazine has named NI one of the 100 best companies to work for in America.

Figure 2. NI Industrial Digital I/O Module Architecture



About the Author

Rahul Kulkarni is the product marketing manager for industrial data acquisition and control at National Instruments. He has contributed to many articles in professional publications including *Automation World*, *Control Engineering*, and *Product Design and Development*, and has authored several white papers. As a product marketing manager, he is responsible for worldwide marketing and product strategy for digital I/O and counter/timer product lines. Rahul holds a masters in mechanical engineering from Georgia Tech, Atlanta and a B.S. in mechanical engineering from VJTI, Mumbai.

DTI & Altera Displaying the Future in Real-Depth 3D

by Steven Goerlich
Senior Electronics Engineer
Dimension Technologies Inc.

Company:
DTI

Industry:
3D Graphics Display

End Products:
2D/3D Switchable Displays, Custom 3D Solutions

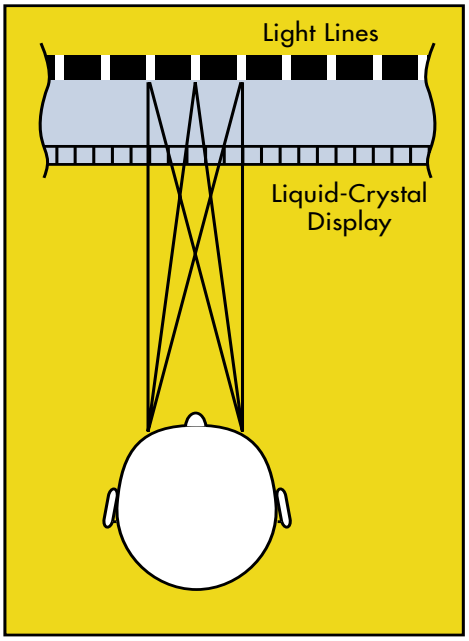
Altera Product:
Cyclone FPGA

Flat panel displays that show content in Real-Depth 3D™—without the use of glasses or other cumbersome headgear—were once the exclusive domain of specialized, high-cost, high-end applications such as military and space hardware. The familiar technology curve has recently changed that, driving this advanced technology into much more affordable consumer products such as desktop displays, cell phones, and laptops. This migration, of course, requires that 3D display systems keep pace in technology and cost. As the acknowledged world leader in this rapidly evolving technology, Dimension Technologies' 2D/3D switchable auto stereoscopic monitors use Altera® Cyclone™ devices and soft intellectual property (IP) cores for rapid, low cost, feature rich product development.

When viewing the real world, the human visual system uses different cues to construct an internal 3D model of what it is seeing. There are many such cues, including shadowing, the apparent size of objects, perspective, and others. The cue that provides a vivid sensation of depth that you see when looking at the real world or a DTI Real Depth® display is called binocular disparity. That is the term for the fact that the image that your left eye sees and the one that your right eye sees are slightly different from one another: your eyes see the world from two different locations, about 2.5 inches apart. The brain processes the differences in these two views (called a stereo pair) to provide an accurate representation of the shape and position of objects within the scene.

With the DTI no-glasses 2D/3D switchable flat panel display—as in the real world—your left eye sees the left eye view and your right eye sees the right eye view. This is accomplished with a special illumination pattern of light lines and optics behind the LCD screen that make alternate columns of pixels visible to the left and right eyes when you are sitting in front of the display, or in certain areas off to the side. As illustrated in Figure 1, the DTI system displays the left and right halves of stereo pairs on alternate columns of pixels on the LCD.

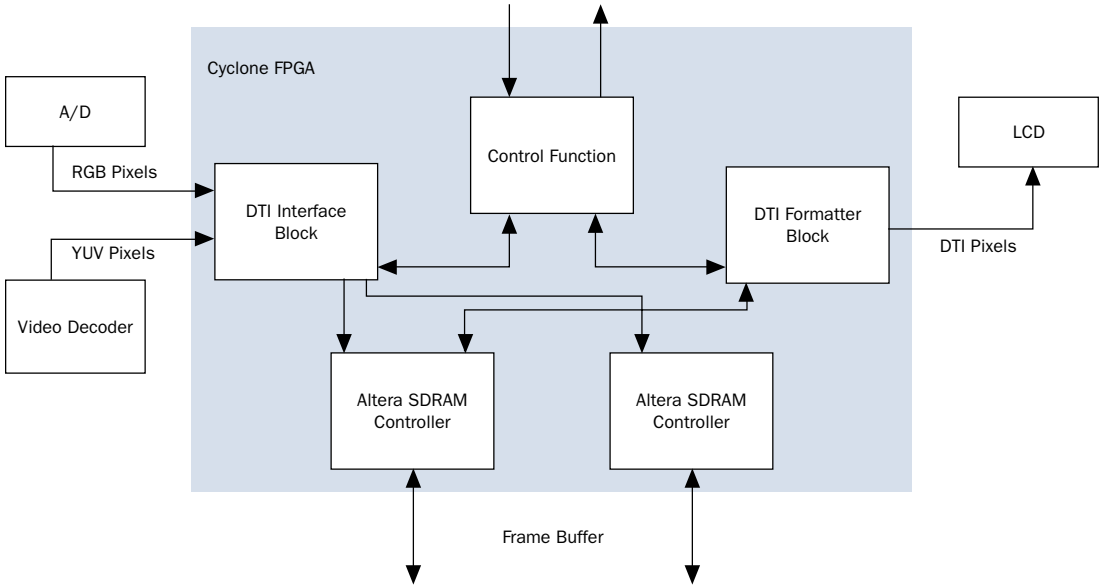
Figure 1. Alternate Columns of Pixels



To achieve the proper display image, a unique LCD data pattern is required. To generate this pattern, logic and memory resources are needed to buffer and manipulate the input data stream as well as implement the necessary control functions for the user interface and achieve the required output format. The Altera Cyclone FPGA is the centerpiece of the DTI Real-Depth 3D electronic subsystem. The FPGA handles all of the necessary processing as well as implementation of two SDRAM controllers, user interface sections, and unique control algorithms as shown in Figure 2.

DTI's decision to use Altera's Cyclone family was an easy one because it satisfies all of the design's requirements along with providing a significant cost savings. Our previous board used four FPGAs at a cost of $100/board, while Cyclone features have reduced that to $25/board for the base display. The high I/O pin, fine-pitch ball-grid array (BGA) package of the Cyclone FPGA also allowed a 75 percent printed circuit board (PCB) size reduction and increased functionality and flexibility. The increased functionality provides a better user experience with support for features such as additional resolutions and refresh rates, increased color spectrum, and more advanced video support, to name a few. The increased flexibility allows us to keep the same base PCB and system structure across products, reducing fabrication and assembly NREs, as well as reducing the different inventory required to produce our full line of Real-Depth 3D flat panel displays.

Figure 2. Cyclone Implementation Block Diagram



In addition to the production benefits, Altera also reduced the development time of our new 2D/3D switchable flat panel displays by providing soft IP cores and increased testing functionality. The soft IP cores provided were an SDRAM controller, first-in first-out (FIFO) buffers, and other Verilog HDL cores, through the MegaWizard® Plug-In Manager available in the Quartus® II and the SOPC builder software tools available with the Nios® processor. The increased test support was in the form of Altera's SignalTap® II logic analyzer available through the Quartus II software. The SignalTap II logic analyzer facilitates access into the innner part of the FPGA design for node watching, conditional triggering, and the other necessary debugging functions of a high-end logic analyzer without the additional equipment cost or I/O and test point penalty. The bottom line is that Altera's Cyclone FPGAs allow us to provide our customers with a better product at a reduced cost.

Conclusion

The familiar technology curve is unrelenting. Capabilities that were once wildly expensive and exotic regularly find their way into less expensive and more mundane consumer products. As display technology and content combine in more and more unique ways, the concept of Real-Depth 3D allows us to see more of our world on flat panels in the same way we see it in real life—with real depth, without the use of clunky glasses or other cumbersome devices. DTI and Altera are working together to provide industry professionals and consumers with a best-in-class product at an affordable price. See the world in Real-Depth 3D today.

Cadence Incisive Platform: The Industry's Fastest, Most Efficient Verification Platform

by Ray Salemi
Senior Product Marketing Manager
Cadence

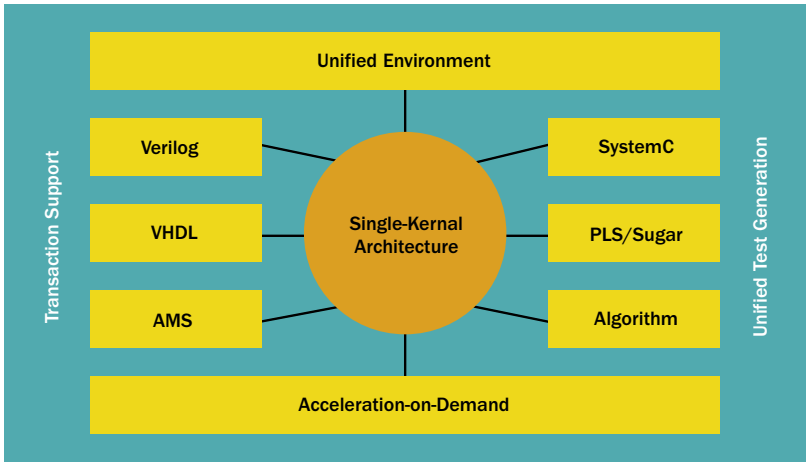
Attaining the speed and efficiency needed to functionally verify today's complex FPGA system designs require a unified verification methodology. The advent of 90-nm FPGAs such as Altera's Stratix® II devices creates new challenges for engineers developing system solutions, including:

- Designing embedded software in parallel with hardware to shorten design cycles
- Verifying intellectual property (IP) purchased from other companies or reused from previous projects
- Debugging functionality in the simulator rather than on the board

Today, many verification flows address these problems separately. Lacking a unified flow, they create separate silos of tools that can validate a small portion of the total design.

Without a unified approach to verification, your engineers must recreate almost everything at every stage. The Cadence® Incisive™ functional verification platform is the world's first single-kernel verification platform that supports a unified methodology from system design to system design-in for all design domains. With transaction-level support, unified test generation, and acceleration-on-demand, the Incisive platform delivers the fastest, most efficient verification in the industry. In fact, the Incisive functional verification platform can deliver 100× register transfer level (RTL) simulation performance throughout the design cycle and compress verification by 50 percent.

Figure 1. Incisive Verification Platform



New Technologies

Three new technologies are highlighted in the integrated Incisive platform:

- The Incisive unified simulator is the core of the Cadence Incisive verification platform. The world's first unified simulator for digital verification, the Incisive platform supports Verilog, VHDL, SystemC, SCV, PSL and OVL assertions, unified test generation, and full transaction-level support.
- Incisive XLD team verification is the flagship product of the Cadence Incisive platform, delivering comprehensive digital verification for up to 10 engineers. Incisive XLD includes Acceleration-on-Demand, which enables teams to choose either Incisive-unified simulation or 1 million gates of capacity on an Incisive XLD Base accelerator/emulator at runtime.
- Incisive XLD Base accelerated team verification includes Incisive XLD and a specially configured Cadence Palladium accelerator/emulator, which provides 100× to 10,000× the performance of RTL simulation.

All of these products can be expanded to include Incisive AMS to support analog/mixed-signal verification.

Getting To 100× RTL Performance

The Incisive unified simulator leads the industry in mixed-language RTL simulation performance and delivers 100× RTL performance in two ways. First, Incisive supports transaction-level models. By abstracting designs from the signal level to the transaction level, 100× simulation performance can easily be attained. Transaction-level models are accurate to the register level and fast enough for embedded software development concurrent with refinement to RTL. Once the transaction-level model is refined to RTL, Incisive delivers the industry's fastest hardware acceleration performance with Incisive XLD Base powered by Palladium, a massively parallel Boolean compute engine. Combining transaction-level modeling and hardware acceleration delivers 100× RTL simulation performance in a unified verification environment throughout the design cycle.

What does 100× performance mean? In less than a minute, you can accomplish what used to take an hour and a half. Four days of simulation can be completed over lunch. Over night, you can get results that would have taken a one-month-long simulation run, meaning more system design wins, faster time-to-market, and higher quality.

Learning To Implement a Unified Verification Methodology

As with most process improvements, implementing a unified verification methodology with the Incisive verification platform is best done with a little planning and preparation. You can begin with these steps:

1. Learn what is in Verilog 2001 and SystemC. Read through the first half of a good C++ book (such as *System Design with SystemC*, Kluwer Academic Publishers). This will help you understand what a class library is and that SystemC is simply a class library that extends C++ for system-level design and verification.
2. Start instantiating assertions into your RTL code using the PSL/Sugar property specification language. You might already be able to do this, as NC-Sim and the Incisive unified simulator both support dynamic assertion checking.
3. Try some verification examples with the open source SystemC verification library. Someone in your organization can start learning how SystemC testbench code can coexist with testbench code written in Verilog, VHDL, C, and E.
4. Read the Incisive acceleration policy checks and the application notes on simulation acceleration. Even if you have not purchased Incisive, the documentation is available to you. These guidelines make all the difference in the world when moving from a simulation-only methodology to one that includes hardware acceleration through the Incisive-XLD acceleration-on-demand technology.
5. Read application notes posted on cadence.com (**www.cadence.com/appnotes/verificationlibrary.asp**)
   - Accelerated Transaction-Based Co-Simulation
   - Creating a Functional Virtual Prototype
   - Creating Analog Behavioral Models
   - DSP and Communication Design and Verification
   - Incisive Simulation Acceleration Deployment
   - Reusing Functional Virtual Prototype (FVP) Components in a Testbench
   - The Role of Assertions in Verification Methodologies
   - Transaction-Level Models
   - Using Coverage

   These technical documents are full of beneficial ideas as you prepare to unify your verification methodology with the Incisive verification platform.
6. Lastly, familiarize yourself with the Incisive functional verification platform (**www.cadence.com/products/incisive.html**). The Cadence web site holds a wealth of knowledge, including brochures, data sheets, articles, and such featured white papers as:
   - It's About Time: Requirements for the Functional Verification of Nanometer-Scale Integrated Circuits (ICs)
   - A Unified Verification Methodology

Fast Signal Integrity Analysis with IEEE & IBIS Standards

by Gary Pratt
Product Manager, High-Speed Design Kits
Mentor Graphics

Signal integrity engineers used to use SPICE models to investigate the signal integrity aspects of their designs. Unfortunately, this method was painfully slow, complex, and exposed sensitive transistor-level intellectual property (IP) to the public. In response to the need for a better solution, a group of silicon vendors, EDA vendors, and end users worked together to create a standard to capture the critical I/O information in table format. This group became the IBIS committee, and continues to be the guiding force in signal integrity today.

The IBIS table model technique worked well for most applications for many years. Unfortunately, the latest generation of multi-gigabit serial communication technology such as PCI Express™, InfiniBand®, and XAUI began to prove difficult to model with traditional IBIS modeling techniques. Accuracy was difficult to achieve by modeling current-output serial devices with voltage control tables, and the configurable nature of high-speed serial devices (swing, pre-emphasis, equalization, etc.,) proved difficult to capture in a reasonable number of tables. In response, the industry began to revert to the SPICE solution of the past.

IBIS BIRD-75 Standard for Multi-Lingual Modeling

Fortunately, the IBIS committee anticipated the challenge of high-speed serial design, and began on standards to address the problem. The results of this effort was the creation and ratification of the IBIS BIRD-75 standard for Multi-Lingual Model Support. This standard provides the means for IBIS standard SI tools to accept models both in SPICE and behavioral modeling language formats. This standard was approved in early 2003 and incorporated into the IBIS 4.1 standard formally released in early 2004.

By accommodating SPICE models, the multi-lingual model standard immediately addressed the SPICE complexity problem by wrapping the complexity of the SPICE model in an IBIS file format. It allows that IBIS wrapper to be imported into and used in an signal integrity tool in exactly the same way as a traditional IBIS file. In this way, signal integrity engineers could continue to use familiar and optimized signal integrity tools for multi-gigabit serial designs for which there were no traditional IBIS models. Though this did solve the complexity issue, it failed to adequately address the SPICE IP protection problem, and completely failed to address the SPICE speed problem. With SPICE models, signal integrity engineers were no longer able to perform the complete printed circuit board (PCB) analysis of all process corners that they had been able to perform with IBIS table models.

Again, the IBIS committee anticipated and addressed this by providing for behavioral modeling in the multi-lingual addition to the IBIS 4.1 standard. Using a behavioral modeling language (such as the IEEE 1076.1 standard VHDL-AMS), modelers are able to abstract proprietary transistor-level information out of the model, and completely solve both the IP protection and speed issues. VHDL-AMS models provide simulation speeds hundreds of times faster than their transistor-level equivalents while providing equivalent accuracy, with a high level of flexibility and IP protection.

As a leader in signal integrity analysis, Mentor Graphics was an early supporter of the IBIS multi-lingual standard, and has incorporated native multi-lingual capabilities into its industry leading ICX environment.

The ICX Design Kit for Stratix GX

Altera and Mentor Graphics joined forces to use these new multi-lingual capabilities to create a Stratix® GX design kit that is fast and flexible in an environment that is highly optimized for signal integrity analysis (and familiar to many signal integrity engineers). The kit provides both Eldo-SPICE models for high accuracy, and IEEE standard VHDL-AMS models for accuracy and speed. The kit includes custom menus to allow signal integrity engineers to quickly explore the impact of different configurations, such as transmitter pre-emphasis and receiver equalization, as well as process corner cases. The kit contains all the necessary wrappers, examples, and documentation to provide fast and flexible analysis of Stratix GX high-speed serial interface (HSSI) I/O pins. The kit also provides the capability to use the multi-lingual facilities to wrap and simulate other devices such as s-parameter connector models.

Figure 1 shows a simple Stratix GX design captured in Mentor Graphics ICX, along with the custom menu created to accommodate the configuration flexibility of the Stratix GX HSSI. The custom menu makes it very easy for signal integrity engineers to the flexibility of the Stratix GX HSSI transmitter and receiver configurations.

ICX natively supports the SPICE models as well as the VHDL-AMS models. ICX also contains facilities for creating custom pseudo-random bit streams and the ability to view resulting eye diagrams with custom or standard eye masks. ICX provides for pre-layout what-if analysis in an actual physical layout environment, provides for a complete post-routing analysis including analysis-driven routing optimization, and will even perform multi-board analysis via connectors and/or cables (utilizing SLM, MLM, SPICE, or s-parameter format).

Figure 2 shows the results of the SPICE transistor-level simulation (green) verses its VHDL-AMS equivalent-simulation (yellow).

Simulations & What-If Scenarios

It is important for digital designers and signal integrity engineers to be able to test their design corners before committing to the final implementation. Using ICX, designers and engineers can simulate large designs in a short period of time and quickly perform what-if analysis on a variety of different permutations of transmitter and receiver configurations, including pre-emphasis and equalization settings, termination impedance, and voltage levels. The Stratix GX design kit allows designers to explore different scenarios in their designs and in turn, facilitate more first-time PCB design success.

Conclusion

The Stratix GX Design Kit for ICX supports both Eldo-SPICE and IEEE standard behavioral models. The VHDL-AMS models restore the speed, accuracy and ease of use signal integrity engineers have expected from their IBIS models. Models developed in this standard can be imported into a signal integrity tool with exactly the same ease as a traditional IBIS model and can be simulated at speeds hundreds of times faster than SPICE models. Furthermore, the Stratix GX design kit provides custom menus and examples to allow the signal integrity engineer to quickly get up-to-speed on multi-gigabit analysis, and quickly test various configurations of the serial link (pre-emphasis, voltage swing, termination, equalization, etc.). Signal integrity engineers are provided with the ability to perform full-board signal integrity analysis and what-if analysis. In addition, models developed with the IEEE standard VHDL-AMS will be fully compatible with any IBIS-compliant signal integrity simulator on the market now and into the future.

Figure 1. Stratix GX Design Captured in Mentor Graphics ICX

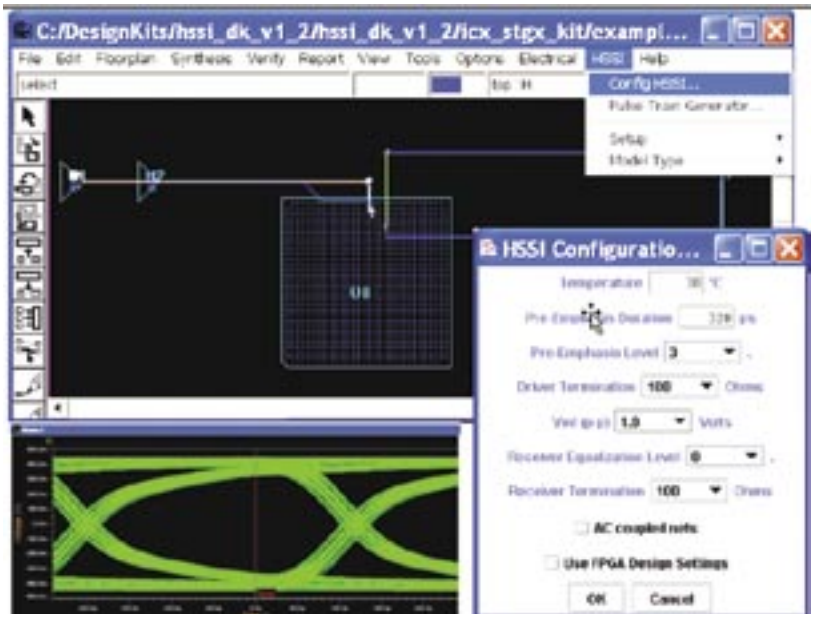
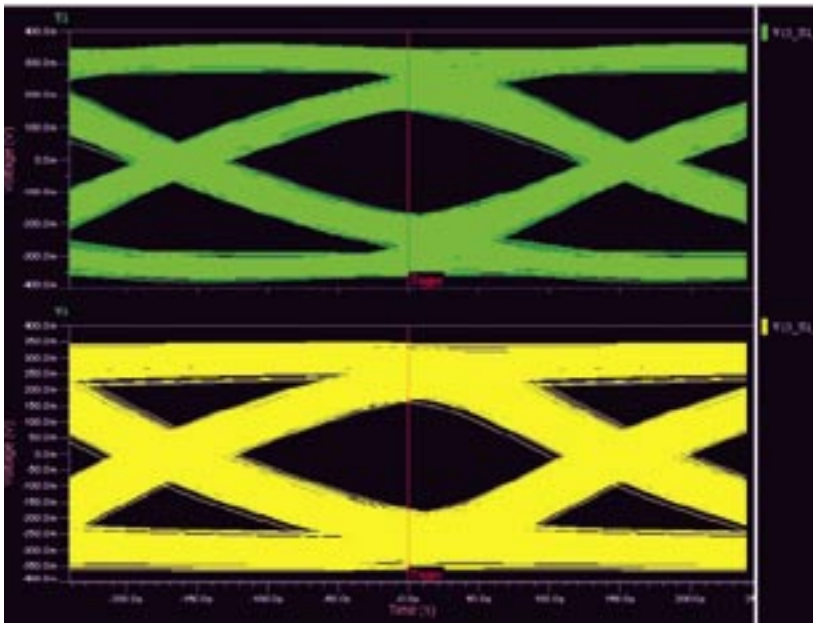


Figure 2. SPICE Transistor-Level Simulation vs. VHDL-AMS Equivalent



Maximize Your Tool Investment & Speed & Lower Device Cost with Design Compiler FPGA

by Greg Tanaka
Group Marketing Manager, FPGA Synthesis
Synopsys

Today's FPGA designers are challenged by complex designs with tight budget and time-to-market requirements. This dilemma is especially difficult for those who move between FPGAs and ASICs. Design Compiler® FPGA (DC FPGA) bridges the gap between custom and programmable logic design. DC FPGA is built on Synopsys' proven ASIC solution, Design Compiler, and also includes an all-new Adaptive Optimization™ technology.

FPGA Capabilities Equal Median ASIC Size

High-end FPGA capabilities have grown at such a rate that they can now implement the median ASIC design and match both the performance and capacity of an ASIC. FPGAs are being chosen for prototyping complex ASIC designs if the economics, power consumption, and timing performance are a fit. Altera® Stratix®, Stratix II, and Cyclone™ II FPGAs now provide the designer with over a million useable gates, almost approaching the median ASIC in complexity. If the aim is to be able to run the design at full speed so that system interfaces can be properly exercised, then the quality of results achieved for timing becomes paramount. As the majority (70 percent) of custom design re-spins are still due to functional errors, rapid verification of the programmable prototype can go a long way to ensure that the ASIC design is right the first time. DC FPGA provides a platform for software development, which continues in parallel with ASIC development and manufacture.

Today's FPGA Design Challenges Require an ASIC-Strength Solution

DC FPGA is based on an FPGA-optimized evolution of the industry-standard Design Compiler synthesis tool. The environment supports team-driven block-based design as well as top-down methodologies. The familiar Design Compiler user interface provides advanced levels of design controllability. Flexible formal verification is also a key feature of the ASIC-strength solution, and has proven to be a tremendous time-saver when it comes to signoff if the various implementation levels comply with the original source functional intentions.

FPGA Flows Lack ASIC-level Support

The FPGA flow is generally less supported than the ASIC flow. Where static timing analysis (STA) is supported, there is often a lack of the same level of supported features, such as case analysis. Similarly, formal verification is not supported even though equivalency checking has become a standard for ASIC design. Furthermore, gated clocks have to be manually translated to clock enables for the FPGA design to avoid clock skew problems.

Traditional FPGA to ASIC Design Flow Requires Error-Prone Manual Tasks

One of the key issues is that the majority of FPGA tools on the market today are not designed to facilitate large, complex programmable logic designs. Many existing tools restrict the design process to a top-down flow guided by a single user, although the complexity demands a team effort. Programmable designs that are of the order of a million gates require a block-based design flow, just like their ASIC counterparts.

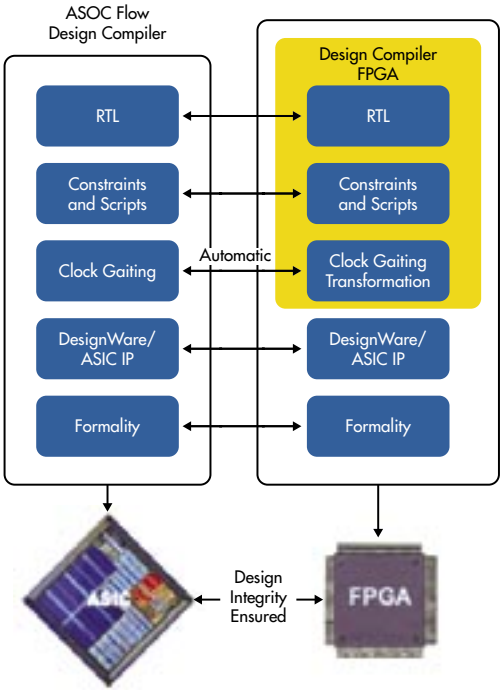
Ideally, the source register transfer level (RTL) for the designs would be identical for both the ASIC and FPGA. In practice, with today's FPGA flows, modifications are required to the RTL code to follow the FPGA vendor's recommended coding guidelines. Typically, areas that require re-coding include digital signal processing (DSP) algorithms and instantiated intellectual property (IP) or RAM blocks, due to differences in how the compilers handle these objects.

Often, the original RTL code intended for the ASIC will be taken by a separate design team and modified for the FPGA implementation. The manual modifications are time consuming and error prone, and can also lead to RTL "drift," where the two descriptions become so diverse that the functionality equivalence is jeopardized. In addition, different synthesis scripts, commands, and directives will be required for each flow. However, the formal flow mentioned earlier will help establish that this drift stays within the functional specifications.

Fastest Path to Initial Production

Since it is always necessary to keep a design on time and within budget, it is imperative that the initial production FPGA stage does not re-introduce time-to-market delays. Nowhere is this more difficult than moving between ASICs and FPGAs. Starting with DC FPGA, then moving to an ASIC is easier than ever before (see Figure 1). DC FPGA enables a single, common RTL source to be used for both the FPGA and the ASIC designs, so that designers can move easily between the ASIC and FPGA flows.

Figure 1. DC FPGA's Common ASIC to FPGA Flow



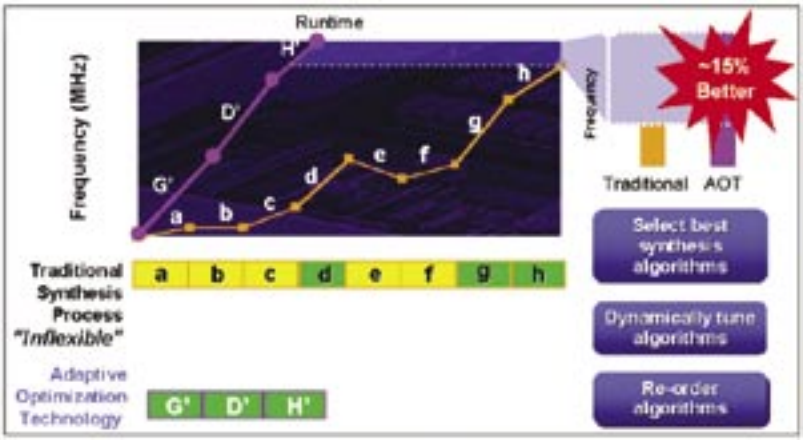
Get the Best Timing with Design Compiler FPGA's Adaptive Optimization Technology

One of the weaknesses in traditional approaches to FPGA synthesis is that often the designer is forced to use a fixed optimization strategy. DC FPGA provides Adaptive Optimization™ technology that automatically selects the best synthesis algorithm for the design, given the nature of the design and the applied constraints. Once the high-impact algorithms have been automatically chosen, DC FPGA goes on to tune the algorithms as they are applied to the design, and if necessary, change the order in which they are applied. The resulting circuits produced by DC FPGA operate more efficiently than traditional FPGA synthesis tools.

When targeting advanced FPGAs, such as Altera's Stratix II devices, you can save 25 percent of your cost by meeting target frequencies in a lower speed grade device. DC FPGA helps you meet critical timing in a lower speed grade part to significantly reduce the FPGA device cost by achieving on average 15 percent better performance than your pervious design flows.

Figure 2 shows how the Adaptive Optimization technology provides a one speed grade advantage resulting in 25% FPGA cost savings.

Figure 2. Adaptive Optimization Technology



Design Once: Fastest Path to ASIC or FPGA Prototype

Since it is always necessary to keep a project on time and within budget, it is imperative that moving the design between an FPGA or ASIC does not introduce time-to-market delays. With DC FPGA, moving to an ASIC or FPGA is easier than ever before, as shown in Figure 1. DC FPGA enables a single, common RTL/script source to be used for both FPGA and ASIC designs, so that designers can move easily between the ASIC and FPGA flows. DC FPGA eliminates most of the time consuming manual steps previously need to reconcile the two different flows.

Summary

DC FPGA merges the production-proven technology of Design Compiler with FPGA-specific optimizations and the Adaptive Optimization Technology to produce three unique benefits. First, DC FPGA provides an industry-standard ASIC-strength solution to solve the toughest FPGA design challenges with technologies like equivalence checking. Second, with Adaptive Optimization Technology, DC FPGA provides the best timing post-place and route versus any other synthesis tool. Finally, by sharing the DC infrastructure, designers can design once for both their ASIC and FPGA and thus save months of design time.

For more information on DC FPGA, visit **www.synopsys.com/products/dcfpga/dcfpga.html**.

Layer 2 Switch Implementation with Altera FPGAs

by Francois Balay
MorethanIP

This article describes how a system-on-a-programmable-chip (SOPC) architecture with a 32-bit Nios® or ARM® RISC processor and a Layer 2 (L2) Ethernet switch can be implemented in an FPGA. This implementation provides increased flexibility when compared to standard L2 switching ASSPs.

L2 Switching Overview

An Ethernet switch is used to interconnect a number of Ethernet local area networks (LANs), forming a large Ethernet network. Different ports of the switch are connected to different LAN segments. The purpose of the switch is to forward the packets intelligently only to the desired destination segment of the network whenever possible, instead of flooding the network for every frame. The switch stores the MAC addresses observed from frames received through each port and uses this information to learn which MAC belongs to which segment of the network. With this information, the switch can forward the frames from the source network segment to only the destination, instead of forwarding the frame to all the connected ports, reducing the network load.

SOPC Advantage vs. ASSP

Standard multi-port Ethernet switch ASSPs are widely available from different vendors and can be used to meet the requirements of a large number of applications. However, standard parts are designed for typical networking applications and may not provide a good solution for applications that require specific features.

For example, standard Ethernet switches typically implement physical Ethernet interfaces such as Medium Independent Interface (MII) (fast Ethernet ports) or Gigabit MII (GMII) (gigabit Ethernet ports) and therefore require an adaptation device if one or multiple ports need to be connected (e.g., a PCI bus, a SONET / SDH framer for packet over SONET/SDH (POS) for Ethernet over SONET/SDHEOS (EOS) applications, or voice over internet protocol (VoIP) applications).

In addition, standard Ethernet switches typically implement a large number of ports (12, 24) and implement a fixed distribution of ports (e.g., eight 10/100 Ethernet ports plus one Gigabit Ethernet port) and therefore can provide a solution that is not adapted for applications that require only a few ports or a different repartition of ports.

Also, with standard devices, it is not possible to implement non-standard Ethernet ports such as a 2-gigabits per second (Gbps) port.

To overcome the limitations of standard devices, MorethanIP has developed a flexible Ethernet switching engine which provides a unique solution that allows designers to implement any additional function (e.g., PCI interface, POS-PHY/SPI packet interfaces) to complement the Ethernet switch and to provide connectivity to a large number of standard parts (e.g., SONET/SDH framers, VoIP processors) or systems (e.g., Proprietary backplane, host computer via PCI / PCI-X) with a single device solution.

The switch can also be implemented in Altera® Stratix® devices which provide an on-board configuration capability that can be used to change the switch functionality.

L2 Switch Architecture

The MorethanIP switch is implemented as an SOPC solution. It embeds a hardware switch engine to provide high performance and a 32-bit Nios processor that performs the table management tasks (e.g., learning, aging, and migration). Using an embedded processor also allows designers to implement any other high-level networking functions such as Spanning Tree algorithm or any user-specific task.

The switch implements a programmable number of ports, which are physically implemented with the Altera® Atlantic™ interface (simple master/slave first-in first-out (FIFO)-based interface) on which any Layer 1 application or standard board-level interface can be connected.

The MorethanIP programmable switch provides 6-Gbps switching capability, which can be used as required in a custom application. For example, designers can configure the switch to implement 4 Gigabit Ethernet ports and 12 fast Ethernet ports or non-standard configurations such as a 2-Gbps port with multiple 200 megabits per second (Mbps) ports.

The switch does not require any external device apart from a Flash device to boot the embedded processor, reducing the solution cost and improve system level integration.

Functional Description

Frame switching is based on a two-stage hash code look-up associated with linear searching. This solution provides high performance and enough flexibility to extend the maximum number of MAC addresses supported by the standard implementation of the switch (2,048 addresses). To provide maximum performance and a non-blocking operation, frame switching is performed at wire speed without any software or firmware overhead.

To manage the switch look-up table (LUT), a 32-bit Nios processor is implemented in the switch. To control the switch, a firmware is developed and performs the following tasks:

- MAC Address Learning
- LUT entry aging
- Port migration
- Hash code and table management

The hardware and software parts of the switch have been designed for performance and therefore tightly coupled.

Frame Switching

The 48-bit destination MAC of each frame received by the switch on any of its interfaces is extracted by the de-queuing hardware and provided to the look-up engine together with the physical interface number.

If the received frame is a Unicast frame, a three-stage switching process is implemented. The three-stage look-up engine first calculates the 8-bit hash value from the MAC address 24-bit serial number. The 8-bit hash code is used as an entry to the switch LUT. The look-up function provides three results with three different associated actions performed by the switch hardware:

1. The address is in the table and associated with a correct port number. The switch forwards the frame only to that port.
2. The address is in the table, but is associated with the port on which it was received. The switch discards the frame and does not forward it to any port.
3. The address is not found in the table. The switch engine sends the received frame to all ports except the port on which it was received.

If a broadcast or a multi-cast frame is received, the switch hardware sends the received frame to all output ports, except the one from which it was received.

Learning

The switch frame de-queuing hardware extracts the destination MAC address of each frame received on each of the switch ports and sends it via a hardware queue to the switch firmware, which implements the learning task. The task is executed as follows:

1. For every frame received, the source address is compared with the previously stored entries in the LUT. If it does not match any of the previous entries, it is stored in the table. The following information is stored for each entry:
   a. MAC address: the 48-bit address is stored in the table.
   b. Time stamp: a 10-bit value, used to determine the age of an entry.
   c. Port number: a 4-bit value, which indicates the port through which the frame was received.
   d. Status: a 2-bit value. One bit indicates whether the entry is valid or invalid. The other is reserved.
2. If there is no more space in the tables for new entry, the oldest entry is removed and replaced by the new record.

Conclusion

L2 switches are an essential building block in today's telecommunication systems. With the availability of high-performance, high-integration Stratix FPGAs, new integration possibilities are now available. Complex programmable system devices can be designed to replace standard devices, achieve higher integration, and design devices highly optimized for a particular application.

5 x 5 Real-Time Monochrome Convolution Function Implemented with Altera Cyclone FPGAs

by Paul Nickelsberg
President
Orchid Technologies Engineering and Consulting, Inc.

The convolution function is a versatile image processing building block. Designers can use convolution functions to perform image filtering operations such as image blurring, edge enhancement, smoothing, shifting, embossing, and compensation. The convolution function filters an image by replacing each pixel in the source image with the weighted sum of the pixels in the neighborhood surrounding the source pixel. The neighborhood size and weightings define the convolution. A monochrome convolution function is described in this article. For color images, each color plane can be processed independently.

The basic convolution function is determined by two primary parameters: the neighborhood size (kernel size) and the coefficient, divisor, and offset values. Convolution function operation may be imagined as the moving of a coefficient window across the source image. Each movement of the coefficient window produces one output pixel.

Orchid Technologies used an Altera® Cyclone™ FPGA in its implementation of a generic 5 × 5 convolution function for 640 × 480 monochrome images. The Cyclone architecture offers a rich set of high-speed programmable logic resources in a low-cost package. Convolution function implementation made good use of the Cyclone on-chip phase locked loops (PLLs), the on-chip memory elements, and the high-speed multiply and accumulate logic.

Orchid Technologies began convolution function implementation by breaking down the convolution function task into three primary areas:

- Clock Management
- Input Image Line First-In First-Out (FIFO)
- Mathematics State Machine

Using on chip PLLs, Orchid first defined its clocking hierarchy. The on-chip clock structure was locked to the incoming pixel clock. Multi-phase on-chip clocks are derived from the single incoming pixel clock. The convolution function operates in a pipelined manner.

Orchid Technology's next step was to implement a source image line FIFO buffer. The purpose of the source image line FIFO is to buffer six full lines of source video data. The oldest five of these lines are used to hold the source image kernel data. Altera Cyclone FPGAs support configuration of on-chip synchronous SRAM as dual port memory. Dual Port Memory A was configured as write-only and used for source image storage. Dual Port Memory B was configured as read-only and used for source image kernel access. Kernel processing began once the first five complete image lines were stored in the FIFO buffer. While line six of the FIFO buffer is filling, the convolution state machine operates on the data set producing a new output image line.

Last to be implemented was the multi-step, 32-bit-wide mathematics state machine. Altera's Quartus® II software facilitates the construction of user-definable state machines and mathematics functions. Working with the read-only side of the input line FIFO buffer, the mathematics state machine performed the rapid-source kernel data access, multiply/accumulate functions, and final division scaling. A 5 × 5 convolution function requires 25 multiply operations, 24 addition operations and one shift (division) operation. Thirty-two-bit-wide data paths are employed to avoid truncation during the calculation steps.

Implemented on the Cyclone EP1C6 device, the entire 5 × 5 convolution function requires only:

- 1,516 logic elements
- 32,768 memory bits
- 1 PLL

This is a very comfortable fit, leaving plenty of additional resource on the Cyclone FPGA for other image processing functions.

Conclusion

The implementation of general-purpose convolution functions on Altera Cyclone FPGAs enables the designer to implement a complex, real-time image filter as an embedded element within a larger imaging application. Learn more about Orchid Technologies' use of Altera FPGAs on their board-level product designs by visiting **www.orchid-tech.com**.

It's Showtime for Stratix Devices in Video Processing

Stratix® devices are finding a growing audience in the video and image processing world. A leading imaging systems innovator recently cast Vanteon Corporation (**www.vanteon.com**), a leading design services company and Altera® Certified Design Center, to set the stage for additional research and development in video and image processing.

The Backdrop

Vanteon's customer outlined requirements for a new platform for video processing development, searching for a setting where they could mix the latest video interfaces and image processing algorithms on a highly flexible platform that would run at full video scan speeds.

Vanteon was called on to implement these requirements in a hardware and software solution. It was quickly agreed that a programmable logic solution was the best possible choice for performance and flexibility. In particular, Stratix® device features and tools available from Altera addressed the requirements of the project.

The design needed to input and output imaging data in multiple formats, including RGB, DVI, and unencoded TTL. The system also needed the ability to integrate with other development systems using USB and I^2C. Because of the large amount of image data being managed, a large, high-speed memory buffer was required to handle the pre- and post-processing data. The ability to expand the system to additional I/O interfaces was an attractive plus.

Spotlight on Digital Visual Interface

Digital visual interface (DVI) is a display industry standard developed for moving data digitally between graphics controllers and displays. The specification is promoted by the members of the Digital Display Working Group (**www.ddwp.org**), and outlines the hardware interfaces and the software protocols used to move high- speed data between devices.

A key benefit of the technology is the ability to move large amounts of digital image data, while reducing the electromagnetic interference (EMI) generated in the signaling. This is done in two ways. In hardware, the DVI interface takes advantage of the latest technology in low-voltage differential signaling and clock recovery. In the protocol, DVI makes use of special encoding and decoding techniques to reduce the amount of signal transitions, thus reducing the amount of EMI generated.

Bicubic Interpolation

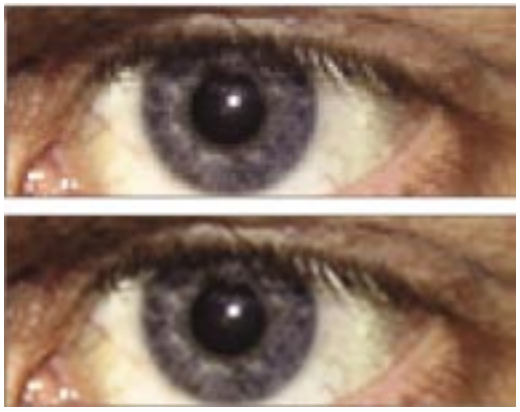
Image processing is very demanding. Bicubic interpolation is a good example of this, and it is a key imaging algorithm used in many applications. Using mathematical techniques, an image can be increased or decreased in resolution or size. In the case of bicubic interpolation, the output pixel being generated will use 16 of the nearest pixels in a 4×4 array. This process must be done on every output pixel in the image, and requires a large amount of digital signal processing (DSP) horsepower. Now, when this process is applied to progressive scan video, each pixel must be calculated 60 times a second.

On an XGA screen running at 60 Hz, the pixel rate quickly adds up:

1,024 pixels × 768 pixels × 60 frames/sec
= 47 MegaPixels/sec

Here is an example of what bicubic interpolation can do when increasing an image's resolution. See Figure 1.

Figure 1. Bicubic Interpolation Before & After



Stratix Devices, Quartus II Software & DSP Builder are Center Stage

This video processing application takes advantage of Altera's Stratix devices, Quartus® II software, and DSP Builder.

Stratix DSP blocks are ideal for many imaging algorithms. In the case of the bicubic interpolation, the new pixel values are calculated by completing an array of multiply and accumulate using neighboring pixel data. The bicubic calculation can be done at full video rates using fewer logic resources in the device.

continued on page 46

When running imaging algorithms on video data, it is important to have high-speed access to RAM for frame buffers. Once a video frame is brought in, calculations can be done on the frame itself, or on frames that occur before and after that frame. In compression algorithms, they look at data from both. To be able to access many frames of data quickly, the video application would have to rely on a quad data rate (QDR) SRAM interface. In this application, over four GigaBytes/second of image data need to be transferred between the Stratix device and the external SRAM. The I/O structures of the Stratix device supports these high-speed clocking and registered interfaces.

Because of all the possible applications for this project, it was hard to determine all the potential clocking resources that would be needed for the inputs, outputs and data crunching. The beauty of the Stratix device is the flexibility of the phase-locked loops (PLLs). With a few base frequencies and the PLLs, the design can generate all of the most common frequencies needed in video. Synchronization is much easier with the Stratix resources.

Altera Tools

The Quartus II software and DSP Builder made it much easier to take imaging algorithms from concept to implementation. Integration of the Altera tools with third-party tools was also a bonus. Simulation, synthesis, and modeling can be used from a number of vendors.

Altera Certified Design Centers

Armed with the latest tools, technology, and training from Altera, Vanteon quickly and cost effectively designed a solution. In this case, Vanteon combined Stratix features with both off-the-shelf and custom intellectual property (IP) to get the customer what was needed for advanced video processing development. Vanteon supplied a custom designed board with the Stratix EP1S80 device, enabling Vanteon-developed IP to interface the RGB, DVI, QDR Memory, USB, I^2C, and expansion buses.

Conclusion

Vanteon's Design Services enabled the development of custom programmable logic, hardware, and software solutions to meet its client's needs, and Altera continues to steal the show with new devices and tools to make it all possible.

About Vanteon

Vanteon's Embedded Software and Electronics Hardware Lab provides architecture consulting, design, prototyping, testing, and certification services to help our clients speed embedded products to market. For more information, visit the Vanteon web site at **www.vanteon.com**.

Free IP to Quartus II Subscribers

For the first time, Altera delivers all released MegaCore® functions on two convenient CDs: the MegaCore IP Library CD and the Nios® II Embedded Processor Evaluation Edition CD. These CDs contain more than 40 Altera® intellectual property (IP) MegaCore functions and are the fastest, easiest way for designers to install megafunctions and jump-start their designs.

To help designers build a stronger design base, Altera is also offering Quartus® II subscribers free licenses[1] to the IP Base Suite, which includes Altera's three most popular IP MegaCore functions—a value of over $9K (see Table 1). The IP Base Suite MegaCore functions are available on the MegaCore IP Library CD, which will be shipped along with the Quartus II software version 4.1 package in August 2004. All active Quartus II subscribers will automatically be granted these free licenses on August 1, 2004.[2]

Here's how you can receive your free IP Base Suite MegaCore functions and licenses:

1. Install the MegaCore IP Library CD.
2. After August 1, 2004, update your license file by visiting **www.altera.com/licensing**.

If you're not already an active Quartus II subscriber, please contact your local Altera representative before August 1, 2004.

About Altera MegaCore IP Library

All MegaCore functions included on the MegaCore IP Library CD support the OpenCore® Plus evaluation feature, which allows you to parameterize megafunctions, generate and simulate a VHDL and Verilog HDL model, and generate a time-limited FPGA programming file. A full and active license is required only when you take your design to full production. For more information on Altera IP MegaCore functions, visit **www.altera.com/ipmegastore**.

Table 1. IP Base Suite Contents

IP MegaCore Functions	Description	List Price
FIR Compiler	Over 12 major FIR filter architectures that can be used across all digital signal processing (DSP) applications. Maximum clock frequency over 300 MHz in Stratix® II FPGAs.	$2,999
NCO Compiler	Optimized for digital phase-locked loop (PLL) and digital interface functions. Supports multiple NCO architectures.	$2,495
DDR SDRAM Controller	High-performance DDR SDRAM memory interface controller with integrated SOPC Builder support. Includes complete system timing analysis and automatic constraints setting.	$3,995

Notes:

(1) The free IP Base Suite includes full perpetual licenses with support and upgrades until August 1, 2005.

(2) This is a one-time promotion exclusively for active Quartus II subscribers (FIXEDPC, FLOATPC, FLOATNET, and FLOATLNX). The promotion will expire on August 1, 2005. Altera Corporation reserves all rights to change the terms and conditions or discontinue the promotion at any time.

Stay Up to Date on the Latest News from Altera: Subscribe to Altera's Free e-Newsletters

Stay current on the latest news about Altera® FPGAs, CPLDs, structured ASICs, software, and intellectual property (IP).

To subscribe to these e-Newsletters visit: **www.altera.com/subscribe**.

- *Inside Edge, Altera's Monthly e-Newsletter*: Get all the news every month about Altera's products, solutions, and more.
- *Net Seminar e-Newsletter*: Stay current on Altera's leading-edge solutions with this monthly calendar of upcoming and archived net seminars.
- *Code:DSP e-Newsletter*: Receive this quarterly update on Altera's comprehensive digital signal processing (DSP) solutions for implementing reconfigurable DSP designs in leading-edge FPGAs.

Cyclone II Questions & Answers

Q *What is the Cyclone II device family?*

A The Cyclone™ II device family is the second-generation family in Altera's low-cost Cyclone series. Cyclone II FPGAs offer 30 percent lower cost and more than three times the logic density of first-generation Cyclone devices. Based on TSMC's proven 90-nm process technology with low-k dielectric, Cyclone II devices are the lowest-cost FPGAs in the industry.

With densities ranging from 4,608 to 68,416 logic elements (LEs), Cyclone II devices also offer new and enhanced features including up to 1.1 Mbits of embedded memory, up to 150 embedded 18 × 18 multipliers, phase-locked loops (PLLs), and support for external memory interfaces and differential and single-ended I/O standards.

Q *Which markets does the Cyclone II device family address?*

A The Cyclone II device family is the optimum low-cost solution for high-volume applications in a wide variety of markets, including consumer electronics, advanced communications and wireless, computer peripherals, industrial, and automotive. Cyclone II devices contain a number of new and enhanced features, such as embedded memory, embedded multipliers, PLLs, and low-cost package offerings, optimized for volume applications such as video displays, digital TVs (DTVs), digital set-top boxes (DSTBs), DVD players, DSL modems, residential gateways, and mid-range and low-end routers.

Q *Why are Cyclone II devices an ideal alternative to ASICs?*

A The Cyclone II family provides a flexible, risk-free option without up-front non-recurring engineering (NRE) charges or minimum order quantities. In addition to a cost structure unmatched by any other FPGA, Cyclone II devices offer advanced features such as embedded 18 × 18 multipliers for high-performance digital signal processing (DSP) applications, and support for memory interfaces such as DDR2 (up to 334 Mbps) and QDRII (up to 688 Mbps).

Q *How do Cyclone II devices compare with Cyclone devices?*

A Cyclone II devices offer lower prices and higher densities than the first-generation Cyclone devices. Cyclone II FPGAs are built on 90-nm process technology, while the Cyclone family uses 0.13 µm. The second-generation devices also offer more features, such as embedded multipliers, more PLLS, support for more I/O standards, and interface to newer memory devices.

Q *Are Cyclone II devices pin compatible with Cyclone devices?*

A No, Cyclone II devices are not pin compatible with Cyclone devices. Cyclone II design goals prioritized low cost as the primary objective. Pin compatibility between families adds undesirable die size.

Q *What type of embedded multipliers do Cyclone II devices have?*

A Cyclone II devices offer up to 150 embedded 18 × 18 multipliers capable of running at 250 MHz. The embedded multipliers can also be configured as two 9 × 9 multipliers, offering up to 300 9 × 9 multipliers. These multipliers are capable of efficiently implementing multiplication operations commonly found in DSP applications. Embedded multipliers in Cyclone II FPGAs can boost overall system performance and decrease system costs for cost-sensitive DSP applications.

Q *What type of embedded memory and memory features do Cyclone II devices have?*

A The Cyclone II embedded memory consists of columns of 4-Kbit M4K RAM blocks, each capable of data transfer rates of over 250 MHz. Each M4K RAM block can implement various types of memory, including true dual-port, simple dual-port, and single-port RAM, ROM, and first-in first-out (FIFO) buffers. Each block also includes extra parity bits for error control, mixed-width mode, and mixed-clock mode support.

Q *What type of system clock management solution is offered in Cyclone II devices?*

A Cyclone II devices provide a global clock network and PLLs with on- and off-chip capabilities for a complete system clock management solution. Cyclone II devices have up to sixteen dedicated clock input pins that feed the global clock network lines directly.

Q *What does the global clock network consist of, and what can it be used for in Cyclone II devices?*

A The global clock network in Cyclone II FPGAs consists of sixteen global clock lines accessible throughout the entire device. It is optimized to minimize skew, providing clock, clear, and reset signals to all resources within the device.

Q *How many PLLs are available in Cyclone II devices? What PLL features are available?*

A Cyclone II devices offer up to four PLLs. These PLLs provide general-purpose clocking management capabilities such as multiplication and phase shifting, programmable duty cycle, programmable bandwidth, spread spectrum input clocking, lock detection, as well as outputs for differential I/O support. The external clock outputs (one per PLL) can be used to provide clocks to other devices in the system, eliminating the need for other clock-management devices on the board.

Q *What versions of the Quartus II design software support Cyclone II devices?*

A The Quartus® II software version 4.1 and the free Quartus II Web Edition software both offer design capability for Cyclone II devices. Programming file generation for Cyclone II devices will be supported in a subsequent software release.

Q *What configuration devices are available to support Cyclone II devices?*

A To offer the lowest total solution cost, Altera created a low-cost serial configuration device family for the Cyclone II device family. On average, these serial configuration devices are priced for volume applications as low as 10 percent of the price of the corresponding Cyclone II device. Four serial configuration devices (1-Mbit, 4-Mbit, 16-Mbit, and 64-Mbit) are offered in space-saving 8-pin and 16-pin small-outline integrated circuit (SOIC) packages.

Q *Is the Nios II family of embedded processors supported in Cyclone II devices?*

A Yes, Cyclone II devices support Nios® II embedded processors, Altera's obsolescence-free, user-configurable general-purpose RISC soft embedded processor family. Second-generation Nios II processors extend Altera's soft embedded processor leadership with better performance, lower cost, and the most complete set of software development tools available anywhere. The Cyclone II family can incorporate multiple Nios II processors in one device, providing savings in cost, footprint, and power efficiency. Cyclone II devices provide designers with maximum flexibility, balance performance needs, and device resource usage by supporting three distinct Nios II cores, each optimized for a particular price and performance range. All three cores support a single instruction set architecture, making them 100 percent code-compatible.

Q *Will Altera support Cyclone II migration to HardCopy structured ASICs?*

A No, there are no plans to support a migration path from Cyclone II devices to HardCopy™ structured ASICs. The Cyclone II architecture has already been optimized to provide the lowest-cost implementation for these densities. Moving forward, Cyclone II and HardCopy devices will complement each other perfectly, because HardCopy devices will support densities that exceed the range of Cyclone II devices, providing designers with access to cost-optimized solutions across the entire density spectrum.

Contact Information

It is now easier than ever to get information and services from Altera. The table below lists some of the ways you can reach Altera.

Information Type	U.S. & Canada	All Other Locations
Product Literature	**www.altera.com**	**www.altera.com**
Altera Literature Services *(1)*	**lit_req@altera.com**	**lit_req@altera.com**
News & Views Information	**www.altera.com/literature/nview.html** **n_v@altera.com**	**www.altera.com/literature/nview.html** **n_v@altera.com**
Non-Technical Customer Service	(800) 767-3753	(408) 544-7000
Technical Support	**www.altera.com/mysupport**	**www.altera.com/mysupport**
	800-800-EPLD (3753) 7:00 a.m. to 5:00 p.m. Pacific Time	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	(408) 544-7104	(408) 544-7104 *(2)*
	www.altera.com	**www.altera.com**

Notes:

(1) The Quartus® II Installation and Licensing, Introduction to Quartus II, and MAX+PLUS II Getting Started manuals are available from the Altera® web site. To obtain other MAX+PLUS® II software manuals, contact your local distributor.

(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for the latest listing.

MAX II The lowest-cost CPLDs ever.

Altera's groundbreaking MAX® II architecture changes the CPLD industry with huge improvements in cost, power consumption, performance, and density. Featuring a 0.18-micron low-power flash process, MAX II devices minimize the cost and board space of your applications.

This instant-on, non-volatile device family offers the lowest-cost solution available for CPLD applications. By delivering cost and power improvements in higher densities than competing products, MAX II devices can easily replace many ASSPs and standard logic devices.

Use MAX II CPLDs to make big changes to your design today.

- 1/10 the power consumption
- 2X the performance
- 4X the density
- 3.3-, 2.5-, or 1.8-V power supply

Supported by QUARTUS® II

ALTERA®
The Programmable Solutions Company®

www.altera.com/max2

Leading through innovation.

Innovation to the power of II.

The world's biggest and fastest FPGAs.

The lowest-cost FPGAs ever.

The lowest-cost CPLDs ever.

The world's most versatile processor.

ALTERA®

The Programmable Solutions Company®

www.altera.com

Leading through innovation.