

News & Views

Winter 2005 Issue

Newsletter for Altera Customers

Design to Win

Quartus II Software Version 4.2

- Performance Leadership
- Power Management
- System-Level Design
- Winning Partnerships

187 Designs Conclusively Validate Altera's Performance Advantage

Altera® devices lead the industry in performance, beating competing devices by 39% to 60%. Data supporting this performance advantage includes third-party benchmark and analysis data for 187 designs using methodology endorsed by industry experts including Kevin Morris, Editor of the FPGA and Programmable Logic Journal and Russell Tessier, Associate Professor of Electrical and Computer Engineering at the University of Massachusetts, Amherst. The results, based on 187 designs evaluated with a third-party, industry-expert-endorsed benchmarking methodology, shows that:

- Stratix® II devices outperform Virtex-4 devices by 39%
- Cyclone™ and Cyclone II devices outperform Spartan-3 devices by 60%

Russell Tessier commented on the methodology. "To evaluate its FPGAs, Altera has created a benchmarking methodology which fairly considers the intricacies and optimizations of its competitors' tools and devices, as well as its own. Experiments which consider a variety of end-user operating conditions have been run on a suite of industrial benchmark circuits. The results of these experiments have been analyzed to accentuate experimental variations and to clearly identify result trends. I am convinced that the experimental methodology that has been used fairly characterizes appropriate user expectations for Altera's devices in terms of area utilization and speed versus their competitors."

According to Kevin Morris. "Altera has created an impressive methodology for measuring and monitoring key performance characteristics of theirs and competitors' devices and tools. Designing a fair and accurate test methodology that yields reasonable metrics is a daunting task...Their system includes a comprehensive and representative test suite, automatic compensation for technology and IP differences between various FPGA families, and automatic generation of design constraints to get optimal results from synthesis and layout tools."

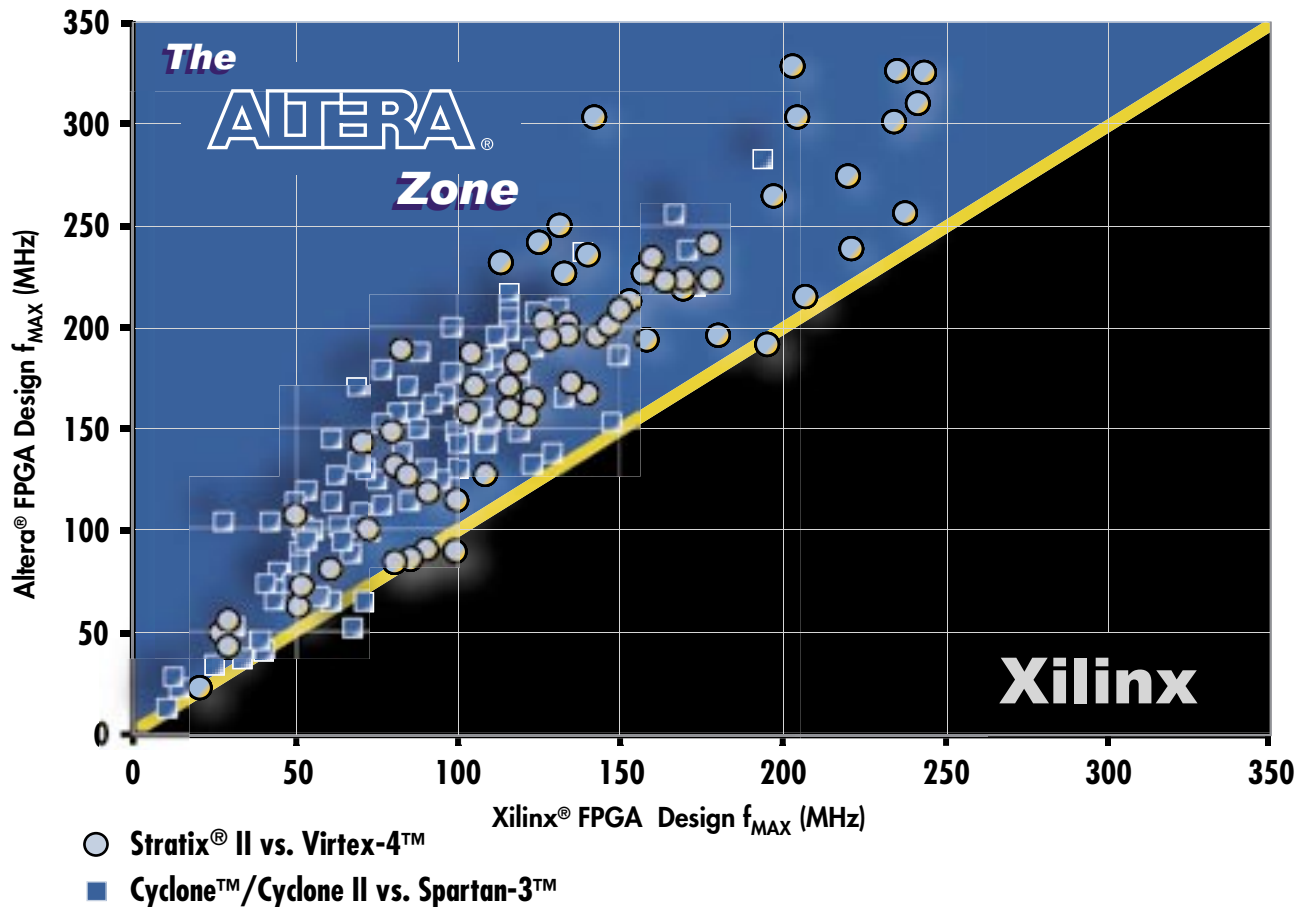
You can experience this performance advantage yourself by downloading Altera's free Quartus® II Web Edition software today.

Results based on 77 designs targeting Stratix II and Virtex-4 FPGAs and 110 designs targeting Cyclone/Cyclone II and Spartan-3 FPGAs. Benchmark development tools include Synplify's Synplify Pro 7.7, Altera's Quartus II, and Xilinx's ISE tools. For details, see Altera's FPGA Performance Benchmarking Methodology White Paper.



If Performance Matters, There's Only One Solution

187 Designs Conclusively Validate Altera's Performance Advantage



Don't Stay in the Dark—Get Into the Altera Zone

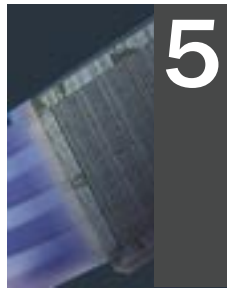
www.altera.com/alterazone

77 Designs Target Stratix II & Virtex-4; 110 Designs Target Cyclone/Cyclone II & Spartan-3 FPGAs
Benchmarking Methodology Endorsed by Third-Party Experts—See www.altera.com/alterazone for Details
For Details on Methodology, See Altera's *FPGA Performance Benchmarking Methodology* White Paper



The Programmable Solutions Company®

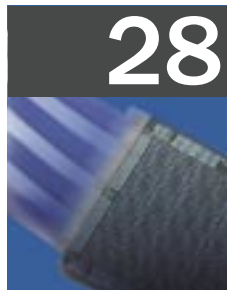
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Performance Leadership



Quartus II Expertise



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Quartus II Software Technology Leadership Delivers Highest FPGA & CPLD Performance

The Quartus® II design software's technology leadership delivers the highest available performance for high-density FPGA designs, low-cost FPGA designs, and CPLD designs, as shown in Table 1. These metrics, which use a third-party, industry-expert-endorsed benchmarking methodology, conclusively validate Altera's performance leadership for FPGA and CPLD designs.

Software Development Methodology Helps Optimize Silicon

Traditional programmable logic device development techniques optimize silicon hardware architectures and then go back and develop software tool chains to support that architecture. Altera uses Quartus II software modeling tools and unique Altera-developed device modeling tools to experiment with thousands of device and software algorithm parameters. Using this information, Altera concurrently develops optimal silicon architectures and software support.

This process enabled Altera to develop Stratix II devices with a new and innovative logic structure that offers higher performance and higher density at a lower cost than comparable FPGAs. Because of the concurrent silicon and software development process, high-performance software support for Stratix II devices was available before silicon.

FPGA Vendor-Integrated Physical Synthesis Technology

The Quartus II software includes the only integrated physical synthesis optimization technology available from an FPGA vendor. Quartus II physical synthesis options are applied during the fitting stage of the compilation process and can be applied regardless of the synthesis tool used.

Faster Timing Closure

Quartus II software users can take advantage of powerful timing closure flow features to optimize designs beyond push-button results. Quartus II software's timing closure flow includes integrated physical synthesis tools and a rich set of graphical analysis and editing tools supported by unmatched cross-probing capabilities.

Easy-to-Use Design Optimization Technology

The Quartus II software satisfies timing requirements using a push-button design flow for most designs. When you need to go beyond push-button results,

Device Category	Device Comparison	Winner	Winning Margin
High-Density FPGA (90 nm, Estimate)	Stratix® II vs. Xilinx Virtex-4	Quartus II	39%
Low-Cost FPGA (90 and 130 nm)	Cyclone™ II vs. Spartan-3	Quartus II	60%
CPLD	MAX® II vs. CoolRunner-2	Quartus II	50%

Note to Table 1:

(1) The *Programmable Logic Performance Leadership* section of the Altera web site includes technical details, timing analysis techniques, and exact benchmarking methods.

The Quartus II software now includes exclusive tools to make design optimization simple:

- Design space explorer (DSE) uses automated technology to increase average register-to-register f_{MAX} design performance by 21 percent.
- The timing optimization advisor tool gives you a virtual field application engineer inside the Quartus II software, providing specific advice on optimizing design timing performance based on the current design project settings and assignments.

Maintain Performance When Implementing Late-Arriving Design Changes

A traditional problem with programmable logic design software has been maintaining performance as later design changes are introduced. However, the Quartus II software makes it easy to implement late-arriving design changes. New fine-grained incremental design editing and compilation technologies give designers the best support for post-place-and-route design changes. These technologies include:

- Quartus II Chip Editor
- Ability to lock down placement and routing in LogicLock™ regions

Parallel Development for FPGAs & Structured ASICs

Only the Quartus II software provides seamless migration between FPGA design and structured ASIC design. By enabling compilation for HardCopy® Stratix devices, the Quartus II software provides a path to higher performance and lower device costs. HardCopy Stratix structured ASICs further strengthen the Stratix device family's 130-nm performance leadership by offering an average of 50 percent higher performance than Virtex-II Pro FPGAs.

Quartus II Software Version 4.2—Performance Leadership & Advanced Power Management

The Quartus® II software version 4.2 demonstrates leadership in performance and power management. New benchmarks demonstrate that Altera delivers clear, complete performance superiority across all 90-nm FPGAs, as well as CPLDs. The Quartus II software's new PowerPlay power analysis and optimization technology as well as a wide range of new features enhance Quartus II software's technology leadership position.



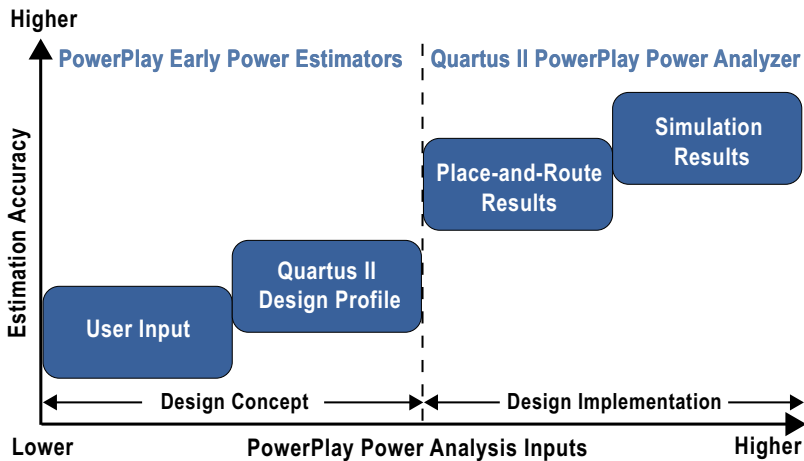
In recognition of software technology leadership, *FPGA Journal* recently gave the Quartus II software its *Highest Reader/Customer Satisfaction With an FPGA Vendor's Tools* award.

The Quartus II software delivers the highest performance for high-density FPGA, low-cost FPGA, and CPLD design segments. Recent benchmarks show that the Quartus II software version 4.2 delivers an average of 39 percent higher performance than when the same design is compiled with Xilinx ISE software for Virtex-4 devices. See the Quartus II performance leadership article on page 5 for more information.

PowerPlay Technology: Power Analysis & Optimization

Quartus II PowerPlay technology is designed to enable designers to accurately analyze and optimize both dynamic and static power consumption. Quartus II software version 4.2 includes the PowerPlay power analysis features that produce detailed reports. Users can use these reports to optimize thermal power dissipation on a block-type or design-hierarchy basis. An industry first, automated Quartus II PowerPlay optimization features will be introduced in 2005.

Figure 1. PowerPlay Power Analysis



Power Analysis From Design Concept Through Implementation

The new PowerPlay power analysis tools in the Quartus II software version 4.2 give designers the ability to estimate power consumption from early design concept through design implementation, as shown in Figure 1.

PowerPlay Early Power Estimators

Designers can use the PowerPlay Early Power Estimator spreadsheets to estimate static and dynamic power consumption during the design concept stage. Early Power Estimation spreadsheets can be filled out manually or populated directly from the Quartus II software. Power estimations are refined during design implementation using the new Quartus II PowerPlay Power Analyzer feature.

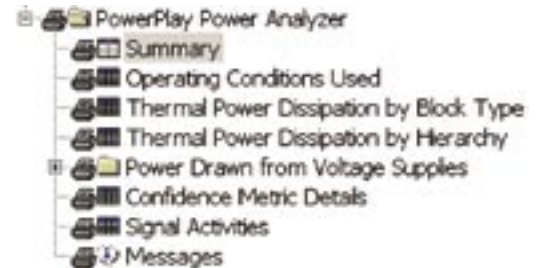
PowerPlay Power Analyzer

The Quartus II software now includes the PowerPlay Power Analyzer feature. This feature improves the accuracy of power consumption estimations given by the Early Power Estimator spreadsheets by:

- Accounting for device resource usage and place-and-route results
- Accounting for functional and timing simulation input/output stimuli
- Performing statistical analysis of expected design-node activity rates when simulation vector inputs are not available

The Quartus II PowerPlay Power Analyzer produces detailed reports that can pinpoint which device structures, and even design hierarchy blocks, are dissipating the most thermal power. Figure 2 lists the PowerPlay Power Analyzer reports available. Quartus II users can now use these reports to optimize designs for lower power consumption.

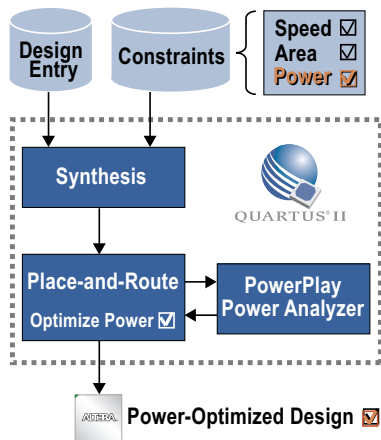
Figure 2. PowerPlay Power Analyzer Report Tabs



Push-Button Power Optimization

Up to this point, FPGA and CPLD design tools can optimize designs for performance and area utilization automatically, but still leave power management largely to the designer. In 2005, push-button PowerPlay power optimization technology will be included in Quartus II software releases. PowerPlay power optimization technology will help you optimize power consumption in addition to speed and area constraints in FPGA, CPLD, and structured ASIC designs, as shown in Figure 3.

Figure 3. PowerPlay Power Optimization Design Flow



The combination of Quartus II PowerPlay power analysis and optimization technology, Altera's advanced silicon design techniques, and partnerships with leading power management component suppliers gives Quartus II software users an edge in delivering high-performance, power-optimized designs on 90-nm and smaller process technologies.

Ease-of-Use & Productivity

Version 4.2 adds several new features that improve ease-of-use and increase productivity:

- **New Versions of Altera MegaCore® Functions:** Altera subscriptions include the MegaCore intellectual property (IP) Library CD and the Nios® II embedded processor, evaluation edition, CD. These CDs allow you to evaluate all of Altera's MegaCore design-ready IP functions in hardware before purchasing a license for the IP.
- **Early Timing Estimate Fitter Option:** This feature provides very quick estimates of design performance without performing a full place-and-route. Estimates are within 10-15 percent of final timing results with about 5-6× less fitter time. The time savings go up more dramatically for larger designs, up to 20× on some of the largest Stratix® II and Stratix designs.
- **Soft LVDS Megafunction:** Simplifies implementing LVDS communication with Cyclone™ II and Cyclone devices.
- **Incremental Synthesis and 20 Percent Faster Run-Times for Quartus II Integrated Synthesis):** Incremental synthesis provides designers more control over design changes and improves synthesis run-times. Other enhancements to the Quartus II integrated synthesis feature shorten average run-times by 20 percent even when not using the incremental synthesis feature.

SOPC Builder

SOPC Builder is exclusive technology included in the Quartus II software to automate system integration and generation. The following new features are added to the Quartus II software version 4.2 release.

- **Clock Domain Crossing Circuitry:** SOPC Builder can now automatically add specialized circuitry to support transactions between peripherals operating on different clock domains.
- **Component Editor:** New feature to better support integrating customer user logic into SOPC Builder systems.

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Verification

New verification features allow Quartus II software users to analyze and control clock skew, model clock jitter, and enable better analysis and optimization of control signals. Beginning with version 4.2, the Quartus II software also supports new register transfer level (RTL)-to-gates functional equivalency checking with the Cadence Conformal LEC formal verification software. This is in addition to the Gates-to-Gates Conformal LEC checking supported by earlier Quartus II software releases.

OS Support

The Quartus II software version 4.2 is now officially supported on Microsoft Windows XP SP2 and Sun Microsystems Solaris 9. The Quartus II software continues to be supported on Windows XP, Windows 2000, Windows NT 4.0, Solaris 8, Red Hat Linux 7.3, 8.0, and Enterprise WS 3.0, and HP-UX 11.0.

Expanding Quartus II Device Support

The Quartus II software version 4.2 adds programming support for EPCS64 configuration devices and adds pin-out support for Cyclone II devices.

Start Using the Quartus II Software Version 4.2 Today

All customers with active software subscriptions will automatically be sent the Quartus II software version 4.2 in December. Quartus II Web Edition software version 4.2 is available for downloading from the Altera® web site now at www.altera.com.

Which Quartus II Software is Best for Me?

The free Quartus II Web Edition software includes most of the features included in the Quartus II software subscription and everything needed to design for Altera's latest CPLD and low-cost FPGA families. The Quartus II Web Edition software also includes support for entry-level members of Altera's high-density FPGA families.

In addition to Quartus II Web Edition features, Quartus II subscription software offers:

- Support for all Altera high-density FPGAs
- Support for the HardCopy® series of structured ASIC devices
- ModelSim®-Altera simulation software
- Additional productivity features
- Support on Linux, Solaris, and HP-UX operating systems in addition to PC versions

For a complete comparison, visit the Altera web site and click on the comparison link on the Quartus II Web Edition page.

Learn How to Become a Quartus II Software Expert

The Quartus® II software features unique advantages in design flow methodology support, place-and-route technology, timing closure methodology, and in-system verification technology. Furthermore, Quartus II software is the only tool that supports FPGA, CPLD, and structured ASIC designs.

Altera provides the resources to get up and running quickly as well as help on how to utilize the Quartus II software's technology advantages to get the most out of your designs in the shortest time possible.

Table 1 shows some of the many resources available for designers of varying knowledge levels of the Quartus II software.

Table 2 lists resources to become an expert using Quartus II LogicLock™ block-based design methodology to shorten your design cycles.

Resources for all of the Quartus II software features are available to familiarize designers of all levels, and allows experienced designers to take full advantage of these features to maximize their design performance and minimize their design cycles.

Table 1. General Quartus II Resources

Resource	Location	Experience
Quartus II Online Demonstrations	www.altera.com/quartusdemos	Beginner Expert
Altera Design Software Web Page	www.altera.com/products/software/products/quartus2web/sof-quarwebmain.html	
Quartus II Tutorials	Choose Tutorial (Help Menu)	
Introduction to Quartus II Manual	www.altera.com/literature/manual/intro_to_quartus2.pdf	
Quartus II Handbook	www.altera.com/literature/lit-qts.jsp	
Altera Technical Training	https://buy.altera.com/etraining/etraining.asp	
Altera Net Seminars	www.altera.com/education/net_seminars/ns-index.html	

Table 2. Resources for Gaining Expertise in the Quartus II LogicLock Block-Based Design Methodology

Resource	Location	Experience
Quartus II Demonstrations	www.altera.com/education/demonstrations/online/design-software/flows/onl-design-flows.html	Beginner Expert
LogicLock Block-Based Designs	www.altera.com/products/software/products/quartus2/design/qts-logiclock.html	
Quartus II LogicLock Tutorial	Choose Tutorial (Help Menu)	
Introduction to Quartus II Manual (Chapter 6)	www.altera.com/literature/manual/intro_to_quartus2.pdf	
Quartus II Handbook (Chapter 1, Volume 1)	www.altera.com/literature/hb/qts/qts_qii51001.pdf	
Using Quartus II: LogicLock Regions Training Course	https://buy.altera.com/etraining/etraining.asp	
Hierarchical Design & New ECO Flows Simplify High-Density FPGA Design Net Seminar (Archived)	www.altera.com/education/net_seminars/past/ns-hi_design.html	
Using Third-Party Synthesis Software with the LogicLock Design Methodology (Section III, Quartus II Handbook)	www.altera.com/literature/lit-qts.jsp	

Take Advantage of Free Quartus II On-Line Software Training

A new series of in-depth on-line trainings teach you to take advantage of the latest Quartus II software features. Topics include power analysis, command line operation and tool command language (Tcl) scripting, and timing analysis. Visit the training section of the Altera web site to access the free training sessions at mysupport.altera.com/etraining.

FPGA Journal Awards Quartus II Tools Highest Marks in Reader & Customer Satisfaction Survey



Continuing its history of innovation, Altera has been awarded the highest marks from *FPGA Journal* for its Quartus® II software. This award, which is based on reader feedback, measures customer satisfaction with the quality, performance, and feature set of software tools.

FPGA Journal described the results: “You told us that Altera has made great strides in its tool suite over the past two years, particularly with the performance and quality of the Quartus II place-and-route tools. They (Altera) also got high marks from many for SOPC Builder embedded system tools working with their Nios® embedded processor.”

This award reflects Altera’s commitment to customers and to making its products easy to use while ensuring the highest performance and using the most advanced technology. Altera listens to customers throughout the product development cycle, which is largely driven by customer feedback. By delving into customer design needs and experiences, Altera identifies critical customer issues and then funnels that knowledge back into software engineering to deliver the products customers are looking for.

The results measuring customer satisfaction are based on formal reader surveys *FPGA Journal* conducted throughout the year on choosing devices, tools, and vendors for FPGA projects. The data for the results came from engineers who completed FPGA projects within the past year.

Quartus II Development Software Handbook

The three-volume Quartus II Version 4.2 Handbook guides you through the programmable logic design cycle from design to verification. It details the benefits of using various features of the Quartus II software, and when and where each feature is best applied in the design cycle. This handbook also covers third-party EDA vendor tool interfaces in appropriate sections. Go to the Altera® web site at www.altera.com/literature/lit-qts.jsp to download the entire handbook, or any constituent volume, section, or chapter. For a general introduction to features and design flow in the Quartus software, see the Introduction to Quartus II Manual.

You can order your own hard copy of the Quartus II Development Software Handbook by clicking the Buy Now icon on www.altera.com/literature/lit-qts.jsp.

Low-Cost Programmable Logic Drives Innovation in Consumer Electronics

by Bernd Riemann
 Director of Hardware Engineering
 Pinnacle Systems, Inc.

The current state of the consumer electronics (CE) market is forcing product developers to re-evaluate their existing development models. The traditional methods of relying on ASSPs or custom ASICs to achieve the lowest cost are proving inadequate to the demands for rapid innovation and increased product differentiation. Instead, CE product developers are increasingly turning to programmable logic-based solutions to enable them to respond to rapidly changing needs of consumers and deliver new features and capabilities, a trend that has been encouraged by the recent proliferation of low-cost FPGA offerings.

Successful products in the CE market will quickly face a flood of competitive products from a variety of manufacturers. This swift reaction causes rapid price erosion and frustrates CE product developers' attempts to derive significant revenue from their products during their increasingly shorter life cycles. In addition, the rise in popularity of digital media formats for audio and video (A/V) content has resulted in a growing interest in appliances and methods to deliver this content to consumers. However, consumers have varying degrees of investment in analog and legacy A/V equipment, which CE product developers must take into account. The result is that the CE developers appear to have a great opportunity before them, but the exact nature, capabilities, and price points of the products that will be successful in this area are not well understood.

These conditions require greater flexibility and agility in product development than are provided by ASSPs and ASICs. CE product developers often use ASSPs for a wide variety of functions, including A/V encoding/decoding, connection interfaces, format translations, and conversions. However, relying on ASSPs exclusively does not allow developers to significantly differentiate their products from others. Also, ASSPs are seldom available for the most current functions, and as a result, CE developers often turn to custom ASICs to deliver their intellectual property (IP) to their customers and differentiate their products.

ASICs also have the advantage of providing very low per-component prices, but unfortunately, the long development times that they require run counter to the need to innovate and quickly offer distinguishing features in markets that are saturated with similar products or that are otherwise changing. The high

non-recurring engineering costs needed for custom ASICs are also a significant barrier for developers who either cannot make such investments or who are unwilling to take such a financial risk in a market where the requirements for a successful product are still in flux. As a result, CE developers are coming to the realization that programmable logic-based solutions, which enable rapid, flexible development and additional product innovation with a minimum of additional engineering resources, are increasingly desirable for their products.

Low-cost programmable logic devices (PLDs) are currently being employed in a wide variety of CE products, including digital televisions, DVD players, handheld media players, set-top boxes, "smart home" networks, and computer peripherals. The flexibility of a low-cost PLD can serve the CE product developer in a variety of ways. CE product manufacturers who incorporate programmable logic into the right areas in their products can rapidly develop new features simply by modifying the PLD design. This capability enables them to offer multiple versions of the same product at introduction, affords them the option to develop new products in response to changing market demands with a minimum of additional engineering effort, as well as provide upgrades to existing products in the field. In this way, CE product developers can take advantage of low-cost ASSPs for well-established functions, while relying on programmable logic to deliver the differentiating capabilities of their product. These differentiating capabilities can include features such as video or audio enhancements, security functions, user-programmable functions, or even completely different modes of operation.

An example of this kind of innovation is the Studio MovieBox Deluxe from Pinnacle Systems. The MovieBox Deluxe is a device that allows multiple video formats from both analog and digital sources to be imported into a PC for editing with Pinnacle Studio 9 software. Many consumers have video content stored on analog tapes, and others have content stored in digital video (DV) format using a device—such as a DV camcorder—that includes a IEEE 1394 (or FireWire) interface, but they do not have an IEEE 1394 interface on their PC. The MovieBox Deluxe can connect all of these disparate types of video sources to a PC using a universal serial bus (USB) 2.0 interface. After editing, the MovieBox Deluxe can provide the connection between the PC and a TV, VCR, or digital camcorder for movie playback and/or storage.



Company:
 Pinnacle
 Systems, Inc.

Industry:
 Digital Video
 Solutions

Altera Products:
 Cyclone™ FPGAs

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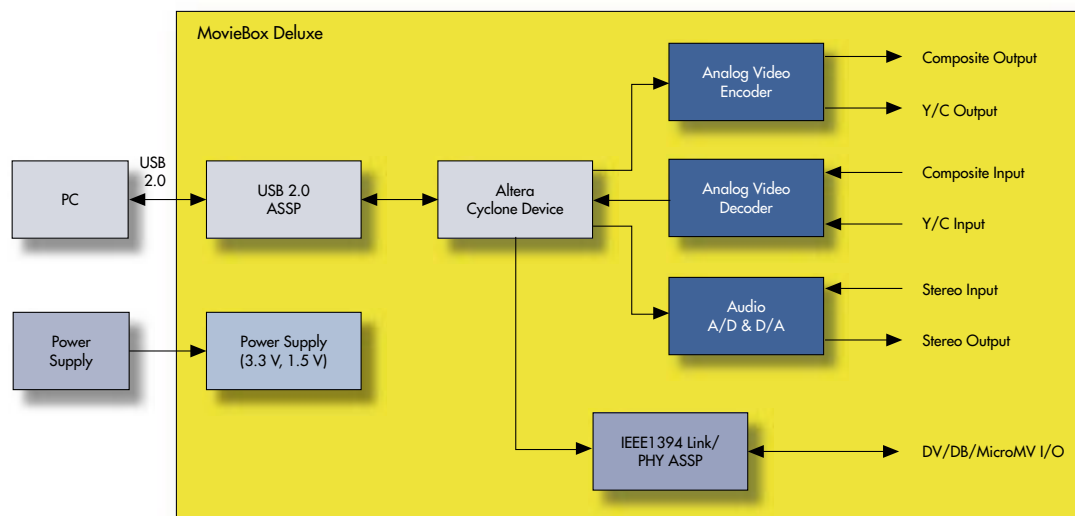
Pinnacle's MovieBox Deluxe includes several interfaces, including RCA and S-video inputs and outputs for analog devices, as well as IEEE 1394 for digital devices. These are all interfaced to the PC via the unit's USB 2.0 connection, and ASSPs are inside the MovieBox Deluxe to handle these interfaces. A single Cyclone FPGA handles the interaction between these ASSPs. Figure 1 shows a block diagram of the MovieBox Deluxe design.

The MovieBox Deluxe operates in one of a limited number of modes, depending on which video source is being used. Because the device only needs to operate in one of these modes at any given time, Pinnacle decided to leverage the FPGA reconfigurability such that the design configures the Cyclone device to function only in the required mode, depending on which cables are connected to the appliance. The time required to reconfigure the FPGA, which happens on the order of milliseconds, is undetectable by the user, compared to the time it takes to plug the cables into the MovieBox Deluxe. The resulting FPGA design

uses far fewer logic resources (nearly one-third the amount) than it would have if Pinnacle had used a non-reconfigurable device. Pinnacle was able to use the smallest Cyclone FPGA, the cost of which was only about one-fifth of the total bill of materials, and well within their budget.

To further reduce costs, the Pinnacle engineering team decided to host the configuration files for the FPGA in the PC device driver for the MovieBox Deluxe. This scheme eliminated the need to include configuration memory devices in the MovieBox Deluxe hardware itself, reducing board space, device count, and corresponding costs. By taking advantage of FPGA reconfigurability in these innovative ways, Pinnacle kept their manufacturing costs to a minimum. Pinnacle's comprehensive evaluation of the alternatives revealed that no other device solution would have enabled them to achieve either their cost targets or meet their aggressive development schedule better than their Cyclone FPGA-based design.

Figure 1. Pinnacle's MovieBox Deluxe



Pinnacle's MovieBox Deluxe automatically reconfigures the integrated Cyclone FPGA to operate only in the required mode, reducing logic utilization and lowering costs.

Introducing Nios II.



The world's most versatile processor!

Nios® II The ultimate in design flexibility.

The world's most popular soft-core processor just got better! Altera introduces the Nios® II family of embedded processors, featuring three CPU cores offering unprecedented performance and cost options. With Nios II processors, designers can define the exact features, performance, and cost they need in Altera's high-performance Stratix® series, low-cost Cyclone™ series, and HardCopy® device families.

The Nios II development kits provide a complete, easy to use tool set including the new Nios II integrated development environment to accelerate software design. Try the Nios II processor today and experience the ultimate in design flexibility.



- Over 200 DMIPs performance
- Consumes as little as \$0.35 of logic
- Supports multi-processor systems
- Library of over 60 programmable peripherals
- Industry's most complete development kits
- Royalty-free & obsolescence-proof

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Creating Hardware Accelerators for SOPC-Builder in C

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By compiling from C to hardware, embedded systems designers can create hardware accelerators and connect them to other components in an FPGA-based system without the need to write low-level hardware description language (HDL) code. The combination of Impulse CoDeveloper and SOPC Builder makes this possible, and allows designers to use the Avalon™ interface for hardware/software communication. For example, the designer of an imaging application can:

- Describe a streaming image filter (e.g., for edge detection, color conversion, etc.) in C
- Debug the code using Visual Studio, GDB, or another standard environment
- Accelerate the code by increasing system-level parallelism (multiple processes operating simultaneously) and by using automated compiler optimizations (e.g., loop unrolling)
- Automatically generate equivalent hardware and integrate it with the rest of the system via SOPC Builder and the Avalon interface

Using this approach, algorithm accelerations in excess of 300× over processor-based equivalent algorithms have been demonstrated.

Hardware Acceleration

Accelerating software algorithms involves partitioning the application, perhaps multiple times, to find a balance between hardware resources, hardware/software bandwidth limitations, and overall system performance. At its simplest, acceleration may mean replacing a single software-critical function with a functionally equivalent hardware module that takes advantage of the low-level parallelism inherent in hardware structures. Greater acceleration levels may be achieved through a multi-process approach, in which data streaming and system-level pipelines have a more important role. The latter approach (which is normally combined with the first) represents a communicating process programming model. Three elements make this programming model particularly effective for system-on-a-programmable-chip (SOPC) designs:

- Independently synchronized processes allow the programmer to create localized units of high-speed computation
- Streams provide a unifying model for high-bandwidth, and low-latency communication between independently synchronized processes (either hardware or software)
- Signals allow processes to synchronize and coordinate their use of external resources, including shared memory resources

Interfacing to such a hardware-accelerated module is similar to calling a software function, the only difference being that the function now resides in hardware as a persistent object (which typically operates on a stream of data or via direct memory access) and is orders of magnitude faster than an equivalent processor-based function.

Optimization for Performance

To squeeze out the highest possible performance, it is best to evaluate a given application as a whole and find higher levels of parallelism (system-level parallelism), as well as focus on more fine-grained parallelism with a given function or process. For this purpose, it helps to use a programming model that will allow an application to be described, simulated, and compiled to hardware or software targets as a collection of independent processes. Once partitioned in this way, it is relatively easy to experiment with moving some or all of the processes into hardware. Using such a programming model makes it possible to describe applications that are by nature parallel, and makes hardware/software partitioning easier. At the level of individual processes (which are analogous to subroutines in C), the types of parallelism that can be automated by software include:

- Instruction-level parallelism, in which one or more statements of untimed C code are collapsed into a single clock cycle
- Pipelining, which generates higher effective throughputs for many types of repetitive operations
- Loop unrolling, which generates parallel structures for repetitive operations (e.g., array computations)

Image Filter Example

Opportunities for accelerating image filters via parallelism exist both at the system level and at the level of statements with individual processes. To create an edge-detection filter, for example, n -by- n windows of pixel data must be assembled from an input data

stream and processed to create an output stream. Two pipelined hardware processes can be described in C for this function: one process generates three offset rows of pixels from the source image, and a second process accepts results of the first and apply a convolution to each pixel window, resulting in a single stream of convoluted pixels appearing on the output of the second process. The processes and streams can be declared and read/written using C-compatible stream I/O routines provided in the Impulse C™ libraries. If the image filter is to process pixel data directly from an image buffer, additional pipelined processes may be created at the front and back of the filter to read and write the pixel data, respectively, as shown in Figure 1.

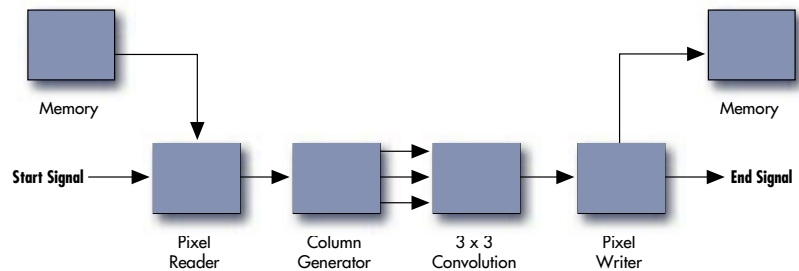
This algorithm has been described in ANSI C with the addition of Impulse C library calls to set up and manage the processes, signals, and streams. A software test application has also been developed using Microsoft Visual Studio that exercises the image algorithm in a desktop simulation environment. This test application combines the four hardware processes associated with the image convolution function along with a software test bench application that reads data from a TIFF format file for processing (this software test bench application can be compiled and run as either the PC-based desktop application or as an embedded application running on the Nios® II embedded processor). This test was set up and run using standard desktop debugging tools and the CoDeveloper Application Monitor. In this way, the algorithm results could be verified before going to the next step and compiling for the target FPGA platform.

Compiling to Hardware

After simulating the functionality of the image filter in software, we were ready to implement the application on a mixed FPGA/processor for actual hardware testing, using an embedded processor as a test generator. The Altera® Nios II development kit includes all the hardware and software needed to compile and synthesize hardware and software applications, which in this case consists of the automatically generated HDL source files representing the hardware processes, and the C source files representing the software test process that will run on the Nios II processor.

To generate hardware for the image filter, Impulse selected the Altera Nios II Platform Support Package from within the CoDeveloper tools and processed the relevant Impulse C source files. This generated approximately 1,200 lines of register transfer level (RTL) code and related SOPC Builder hardware/software interface source files.

Figure 1. Four Pipelined Hardware Processes Used to Assemble & Process Streams of Pixel Data



Next, a project was created using the Altera SOPC Builder tools. As part of this process, a Nios II processor core was generated that included the necessary peripherals for testing. The generated hardware and software files were exported from CoDeveloper to the newly-created SOPC Builder project. Then, using the Altera block diagram tools Impulse connected the generated hardware processes to the Nios II processor via the Avalon™ interface.

The complete system, including the Nios II processor and the generated image filter hardware were synthesized using Quartus® II software. The software portions of the application (consisting primarily of the test producer and consumer functions, including the main function) were also imported into the Nios II development environment and compiled using the supplied Nios II compiler. Lastly, a bit file was generated using the Quartus II software and downloaded to the platform via the provided parallel port interface cable, where it came up and ran as expected. In this example, the explicit pipelining of the four image filter processes, combined with automatically generated pipelines generated by the CoDeveloper hardware compiler, resulted in a best-case image processing rate of one pixel for every two FPGA clock cycles, which translates to a processing speed of approximately 10 ms for a full 512-by-512 image.

Impulse CoDeveloper is compatible with Visual Studio, GCC, CodeWarrior, and Eclipse. CoDeveloper is compatible with Quartus II and Synplify software. Full-featured CoDeveloper begins at \$2,000 (annual license, Altera only). Contact info@ImpulseC.com today for a free evaluation license or visit www.ImpulseC.com.

Design Custom SOPC Builder Components & Streamline Integration

by Chris Sullivan
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Efficiently designing and integrating algorithms into a system FPGA presents designers with interesting challenges. Intellectual property (IP) reuse using Altera's SOPC Builder tool goes a long way toward addressing these challenges, but the issue of custom IP generation and its integration into the system remains. Hence the question, how can designers take a custom algorithm, create a unique SOPC Builder component, and eliminate the integration effort? The answer lies in Celoxica's DKAccelerator design tool for system-on-a-programmable-chip (SOPC) development.

DKAccelerator allows you to create unique SOPC Builder components from algorithms already described in C. Without additional coding, they are automatically integrated into the design as library components. These could be specialized digital signal processing (DSP) functions, components on the local side of peripheral component interconnect (PCI), or other software algorithms and custom instructions that would benefit from acceleration in hardware. To illustrate this process, this article presents a straightforward 3D digital image and video processing design example.

Design Process Overview

Because DKAccelerator was expressly built for Altera's SOPC Builder tool, the design process is driven using the familiar SOPC Builder methodology.

DKAccelerator augments the SOPC Builder flow, and is used for the generation and automatic integration of custom components that are not already available in the SOPC Builder library. DKAccelerator handles the detail of the Avalon™ interface and SOPC Builder integration, meaning to concentrate your effort on the functionality of the custom component. The following steps apply to each new component based on an existing or custom designed C algorithm:

1. Define the required external (non-Avalon interface/custom instruction) I/O signals.
2. Describe the desired functionality (e.g., from existing C software code or a C implementation of a higher-level algorithm).
3. Define the register map for the address space of the component.
4. Implement the desired register map behavior.

Design Example: Digital Image & Video Processing

In this design example (summarily discussed on pages 26 and 27 of the third quarter 2004 issue of *News & Views*), the custom-designed application consists of three dynamically rendered and textured spheres that move across the screen (see Figure 1), bouncing off any edges they touch. Each sphere has a set of control registers that define the following properties:

- Angular velocity (DTheta[10..0])
- Linear velocity components (VX[3..0], VY[3..0])
- Surface color components (R, G, B)

From the SOPC Builder library, Celoxica used a general-purpose I/O pins, UART, on-chip memory, and a Nios® II processor. To complete the design, Celoxica then followed its four-step design process.

Define External I/O Signals

The output signals are VGA display signals (R, G, B, VSync, HSync, etc.). The signals are exported using the following code:

```
unsigned 8 vgaR;
ExportSOPCSignal(r, vgaR);
```

This code produces an 8-bit wide bus to carry red intensity information. vgaR can be used throughout the design as any variable would be used in C. For example: vgaR = 0xff; would produce full-intensity red.

Figure 1. Celoxica's Custom Designed Application



Describe the Desired Functionality

With system integration into the system automated by DKAccelerator, you can concentrate on describing the functionality of the component. Throughout the design phase, development remains at the C level of design abstraction by using DKAccelerator's system-level design capabilities. DKAccelerator uses C algorithms augmented with hardware constructs to create efficient hardware implementations. For example, the `par` statement inserted into the code allows true concurrency in a design, with `par` block assignments being executed in parallel (Figure 2). The `chan` statement (Channels) is used to communicate between and synchronize parallel processes.

This design example requires complex rendering, which uses a series of real-time rendered 3D Perlin noise functions, Phong shading, and lighting effects, all combined with axial rotations and linear translations.

The image is generated as follows:

1. In parallel, the functions

$$\begin{aligned} X &= \text{ScanX} - \text{SphereX}; \\ Y &= \text{ScanY} - \text{SphereY}; \\ R^2 &= X^2 + Y^2 \end{aligned}$$

are calculated for each sphere. This allows the determination of whether the current scan position is within each sphere (i.e., is $R^2 \geq \text{SphereR}^2$).

2. For the active sphere, the value Z is calculated

from square root ($\text{SphereR}^2 - R^2$). The square root is pipelined. This gives a Cartesian point (X, Y, Z) on the surface of the rotated sphere.

3. This point is inverse rotated through two axes by angles Phi and Theta (different for each sphere). Sine and Cosine are calculated through a fixed look-up table (LUT). This gives a Cartesian point (X, Y, Z) on the surface of the unrotated sphere.
4. This point is then passed into a series of 3D Perlin noise functions with different spatial frequencies. See www.noisemachine.com. These values are summed together to give a texture value for the current pixel.
5. The normal surface of the sphere at a given point is equal to (X/R, Y/R, Z/R). As the spheres are a fixed-power-of-two size, this calculation is trivial. By computing the dot-product with a fixed vector and adding a small ambient light value, the diffuse lighting value of the current pixel can be calculated. Multiplying this with the texture value gives the underlying shade of the current pixel. The specular component of the lighting is computed with a further dot-product and lookup in a table providing a Phong shading model. The diffuse and specular components are added together and the result is saturated. This gives the final output value for each pixel that lies on a sphere.
6. The spheres are moved by their current velocity. If the spheres impinge on the edge of the screen, a new velocity and rotational speed is randomly generated.

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Figure 2. Executing Sequential Code in Parallel

Software Implementation

```
void gen_table (void) /* build the crc table
*/ {
  unsigned long crc, poly;
  int i, j;
  poly = 0xEDB88320L;
  for (i = 0; i < 256; i++) {
    crc = i;
    for (j = 8; j > 0; j--) {
      if (crc & 1)
        crc = (crc >> 1) ^ poly;
      else
        crc >>= 1;
    }
    crc_table[i] = crc;
  }
}
```

Hardware Implementation

```
macro proc CRCGenTab (Poly, Index) {
  unsigned 32 CRC;
  static unsigned 3 Bit = 0;
  do {
    CRC = 0 @ Index;
    do {
      par // execute statements in parallel
      {
        if (CRC[0] & 1)
          CRC = (CRC >> 1) ^ Poly;
        else
          CRC >>= 1;
        Bit++;
      }
    } while (Bit != 0);
    par {
      CRCRam[ Index ] = CRC;
      Index++;
    }
  } while (Index != 0);
}
```

Define the Register Map

Our custom image-processing component has three textured spheres, and each sphere holds motion and color information in registers. To connect the component to software, we simply define the register map. Table 1 shows the register map chosen for this example. Each sphere has a 32-bit register, with motion and color information packed into it.

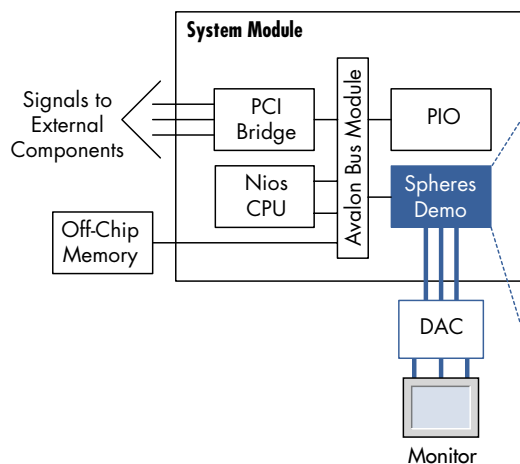
Offset	Register Name	Read/Write	21...11	10...7	6...3	2	1	0
0	Spheres(0)	RW	DTheta	VX	VY	R	G	B
1	Spheres(1)	RW	DTheta	VX	VY	R	G	B
2	Spheres(2)	RW	DTheta	VX	VY	R	G	B

Implement the Desired Register Map Behavior

For this example, the register map implementation unpacks 32-bit data values written to the component and places them in the relevant sphere control registers. Reading does the reverse, concatenating the smaller control registers into a single 32-bit value to return to a master on a read.

Figure 3 shows how the component fits into the system, along with a code snippet showing the register map implementation. The style of coding should be familiar to anyone familiar with C, though with some added operators (the @ operator performs bit concatenation).

Figure 3. System Overview



Building the Component

With our four steps completed, the component is ready to be built and integrated into SOPC Builder. DKAccelerator builds and optimizes the EDIF netlist for the target device and automatically integrates the component into the system. The supplied integration libraries and tools automatically generate the required Avalon signals in the EDIF and the SOPC Builder component description file.

The new component appears in SOPC Builder, and the remaining design effort is the same as for any SOPC Builder system.

Conclusion

DKAccelerator allows you to rapidly move from a high-level concept to a functional component integrated into the SOPC Builder framework. Combined with SOPC Builder, Celoxica's proven C-based design and synthesis technology provides a C-based design flow for the generation of unique and custom, SOPC Builder components from ANSI C source. The integration effort is streamlined and dramatically reduced.

For more information email info@celoxica.com or visit www.celoxica.com/dka and see the online demonstration.

```

/*
 * Avalon bus macros.
 * Handle reads and writes to/from the component.
 */
macro proc WriteData(Offset, WriteData, ByteEnable, Ready)
{
    // 32-bit data --
    // DTheta (11)
    // DPhi (11)
    // VX (4)
    // VY (5)
    // R (1)
    // G (1)
    // B (1)

    Sphere[Offset <- 2].DTheta = WriteData[21:11];
    Sphere[Offset <- 2].VX = WriteData[10:7];
    Sphere[Offset <- 2].VY = WriteData[6:3];
    Sphere[Offset <- 2].Red = WriteData[2];
    Sphere[Offset <- 2].Green = WriteData[1];
    Sphere[Offset <- 2].Blue = WriteData[0];

    Ready = 1;
}

macro proc ReadData(Offset, ReadData, Ready)
{
    ReadData = 0
    @Sphere[Offset<-2].DTheta
    @Sphere[Offset<-2].VX
    @Sphere[Offset<-2].VY
    @Sphere[Offset<-2].Red
    @Sphere[Offset<-2].Green
    @Sphere[Offset<-2].Blue;
    Ready = 1;
}

```


A Comprehensive Management Process for High-Performance FPGA Design

by Darron May
Mentor Graphics

The continuing evolution of FPGAs has enabled design teams to develop larger and more complex designs. The increases in design size and complexity are enabled in part by CPUs and other cores that are not developed in-house. The broad availability of these rich resources places greater demands on design and verification teams.

The flexibility to use bigger and faster FPGAs also strains the capabilities of design creation, simulation, synthesis, and place-and-route tools. Each design start may require unique tool resources, placing a premium on the ability to change and adopt new tools in your flow. Changes can be influenced by many factors. For example, the required intellectual property (IP) may be in a different hardware description language (HDL). The chosen IP may be supported by a specific subset of tools, or a new verification language may be introduced into your methodology.

The time has come for a new class of design methods and tools that enable more thorough design entry, simulation, and implementation, as well as the management of these tasks. Ideally, the comprehensive process of FPGA design creation to realization should be managed from a single, flexible user interface, enabling a seamless design and verification flow for significant productivity gains.

Solutions for FPGA Design Challenges

The ability to adapt to ever-changing customer needs and the necessity to improve productivity—plus the need to do both without impacting the other—are ubiquitous in the electronics industry. Because they are ideally suited to meeting these requirements, the market for FPGAs has grown rapidly.

Yet success brings its own set of new challenges. For example:

- How do you integrate and debug IP delivered in a different HDL?
- How can you train a new designer in your team to be productive sooner?
- How do you manage multiple synthesis tools as you attempt to target different devices or speed requirements?

Every successful team has the experience to meet these challenges, but not necessarily the tools and methodology. This has prompted Mentor Graphics® to develop a new Windows-based design environment

for FPGAs, providing an easy-to-use, advanced-feature solution for FPGA design. This technology, called ModelSim® Designer (see Figure 1), combines the industry-leading capabilities of the ModelSim logic simulator with a built-in design creation engine. It is plug-in ready for the synthesis and place-and-route tools of your choice. The ability to easily manage the interconnection of the entire development flow gives you improved productivity in design creation, simulation, debug, synthesis, and place-and-route.

Figure 1. ModelSim Designer



A Flexible Methodology Conforms to Designer Intent

Designers can freely mix text entry of VHDL and Verilog HDL code with graphical entry using block and state diagram editors. A single design unit can be represented in multiple graphical or abstract views. The management of compilation and simulation at all levels of abstraction is a single click away. This freedom to design according to the way you think extends to debugging, providing both graphical and text capabilities.

Alternatively, some teams choose a purely graphical approach to ensure a consistent coding style. This also facilitates design reuse and maintenance. Graphical editors use an intuitive methodology that shortens the learning curve, improving the time required for new designers to become productive. This method is also useful for designers who are migrating to HDL methodologies or changing their primary design language.

Design implementation tasks are achieved through tight integration with the most popular FPGA synthesis and place-and-route tools in the industry. The user can either run these tools directly in the simulator graphical user interface (GUI) or externally via scripts. Either way, the design data is maintained and used in a common and consistent way.

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To improve throughput and the distribution of design tasks, an intuitive mechanism to compile the necessary vendor libraries for post place-and-route simulation must be provided. With ModelSim Designer, the compiler detects which FPGA vendor tools have been installed and automatically compiles the necessary libraries as soon as the tool is launched. Engineers have access to the library compiler in case they want to compile additional vendor libraries.

Designers can automatically view or render diagrams from HDL code in block diagrams or state machines. When the design code changes, the graphical diagram can be updated instantly, thus ensuring its accuracy. This also helps designers understand legacy designs and aids in the debugging of current designs.

Synthesis & Place-&-Route Integration

The industry's popular synthesis tools from Mentor Graphics, Synplicity, Altera, and others can be integrated into this solution with push-button convenience. The Altera® Quartus® II place-and-route software is fully integrated. Together with the ModelSim simulator, Quartus II software delivers an improved flow for power estimation and optimization. Place-and-route results, together with SDF information, are automatically re-read into ModelSim Designer after the process is complete, making it ready for post-place-and-route, gate-level simulation.

Intelligent GUI for Enhanced Productivity

An intelligently engineered GUI makes efficient use of desktop real estate. An intuitive layout of graphical elements (windows, toolbars, menus, etc.) makes it easy to step through the design flow. Wizards help set up the design environment and make the design process seamless and efficient.

A memory window enables flexible viewing and switching of memory locations. VHDL and Verilog HDL memories are auto-extracted in the GUI, delivering powerful search, fill, load, and save functionality. The memory window allows pre-loading of memories, saving the time-consuming step of initializing sections of the simulation to load memories. All functions are available via the command line, making them available for scripting.

Creation wizards walk users through the construction of VHDL and Verilog HDL design units, using either text or graphics. In the case of the graphical editor, HDL code is generated from the graphical diagrams created. For text-based design, VHDL and Verilog HDL templates and wizards help engineers quickly

develop HDL code without having to remember the exact language syntax. The wizards show how to create parameterizable logic blocks, testbench stimuli, and design objects. Novice and advanced HDL developers alike benefit from timesaving shortcuts.

A flexible and powerful project manager feature allows easy navigation through a design to understand design content. During compilation and simulation, the project manager stores the unique settings of each individual project and displays their hierarchy and dependencies in a separate pane.

Active Design Visualization Enhances Simulation Debugging

During live simulation, design analysis capabilities are enhanced through graphical design views. From any diagram window, simulations can be fully executed and controlled. Enhanced debugging features include graphical breakpoints, signal probing, graphics-to-text-source cross-highlighting, animation, and cause analysis. The ability to overlay live simulation results in a graphical context speeds up the debug process by allowing faster problem discovery and shorter design iterations.

Automated Testbench Creation

ModelSim Designer offers an automated mechanism for testbench generation. The testbench wizard generates VHDL or Verilog HDL code through a graphical waveform editor, with output in either HDL or a tool command language (Tcl) script. Users can manually define signals in the waveform editor or use the built-in wizard to define the waveforms. Either way, it is intuitive, easy-to-use, and saves considerable time.

PowerPlay Support

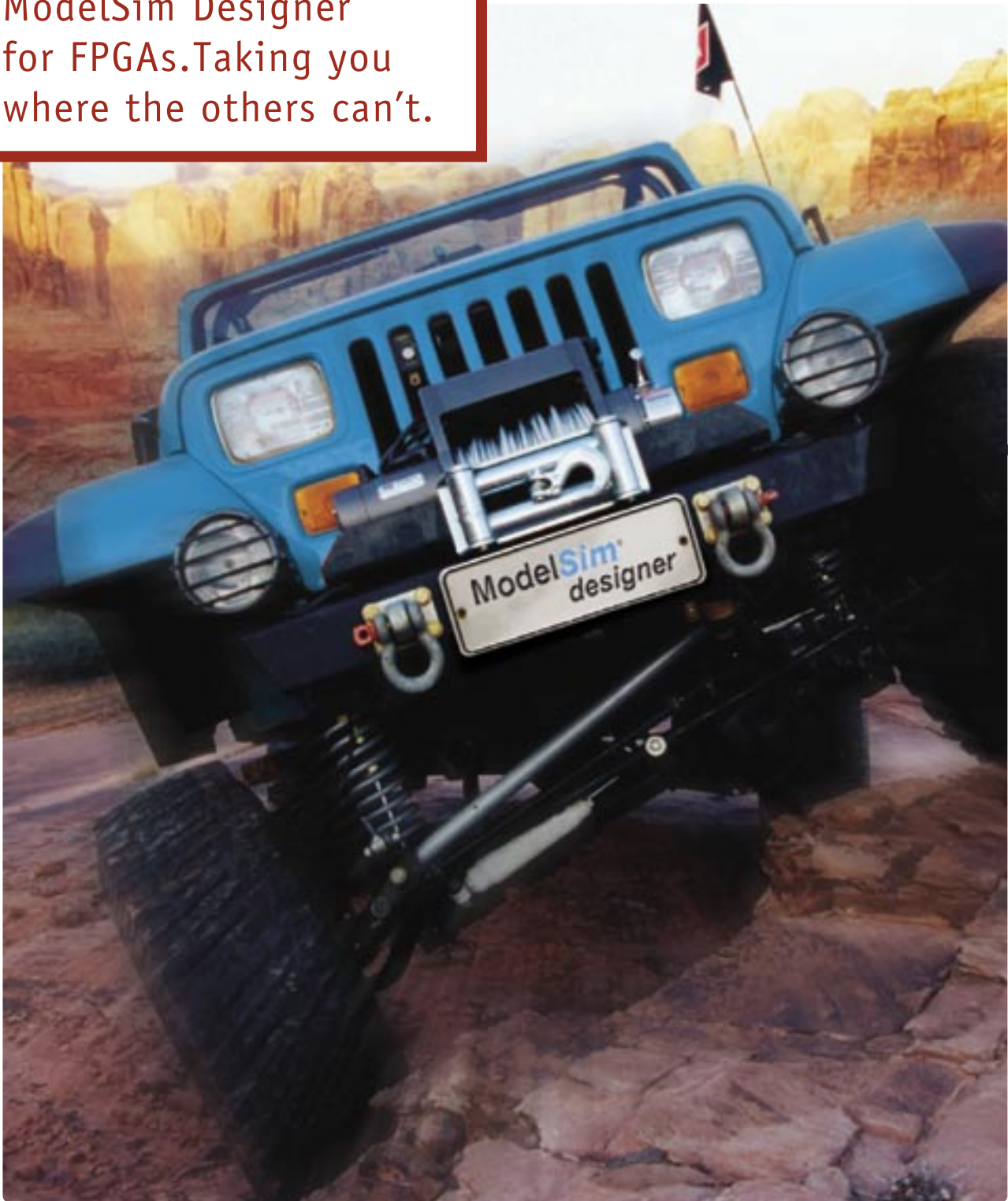
Quartus II software version 4.2 includes a new feature called PowerPlay. By importing the results of functional and timing simulation from the ModelSim software into Quartus II software, users can accurately analyze power consumption and optimize both dynamic and static power consumption for their FPGA designs.

Conclusion

ModelSim Designer supports the entire FPGA design and verification flow from creation through simulation, synthesis, place-and-route, and post place-and-route simulation. It is a straightforward process with a large number of steps performed automatically. ModelSim Designer combines easy-to-use, flexible creation with a powerful verification and debug environment.

ModelSim Designer
for FPGAs. Taking you
where the others can't.

From Creation to Realization



ModelSim® Designer | Imagine how far you can go without roadblocks. Try our Windows®-based, integrated design environment for managing FPGA design. Featuring proven technology from Mentor Graphics®, the ModelSim Designer tool offers VHDL, Verilog, mixed-language and graphical design entry, management, and simulation. Push-button support for the leading FPGA synthesis tools and tight integration with leading place-and-route software makes the ModelSim Designer tool the ideal tool for demanding FPGA designers. It also delivers high-performance all the way through post place-and-route gate-level simulation. For more information visit: model.com/modelsimdesigner or call 1-877-435-4255 and request your free 30-day evaluation. Go where you want to go.

**Mentor
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Improving Bit-Error-Rate Performance in Serial Digital Multi-Gigabit Communication Systems With Error Correction Coding

by David T. Carney
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&

Edward W. Chandler
MSOE

Altera® Stratix® GX devices contain multi-gigabit serial transceivers for use in custom applications or standard protocols such as PCI-Express. Interconnection in digital systems has evolved from synchronous parallel buses to very high-speed, point-to-point serial interconnections with a switch-fabric-based architecture. This article discusses the application of the concepts of error correction coding to these new multi-gigabit serial systems.

Model of Bit-Error-Rate vs. Jitter

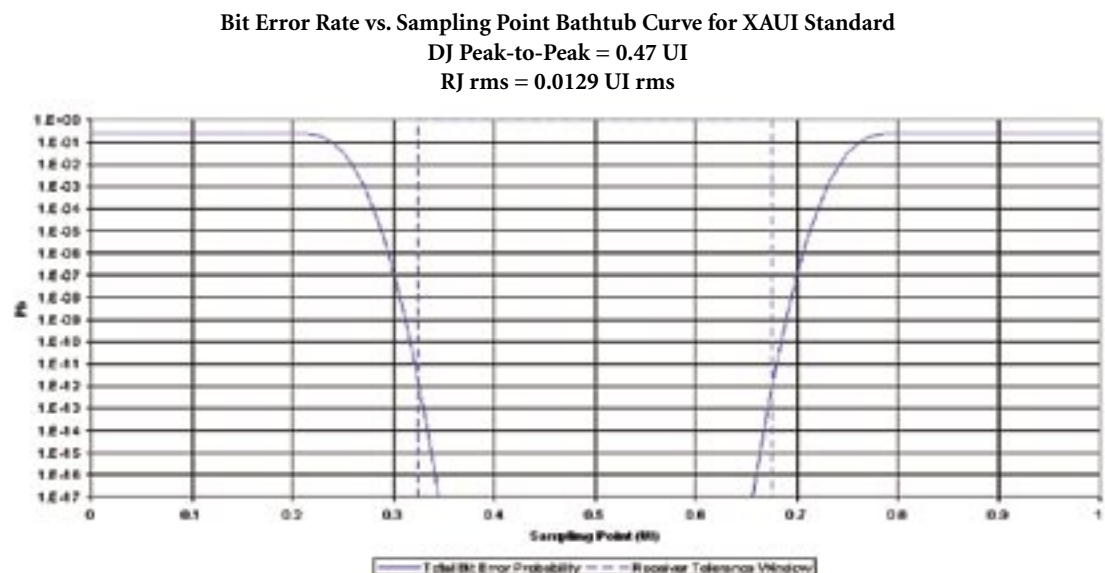
The fundamental measure of performance in a digital communication system is the bit-error-rate. Most of the current generation of standards for serial digital multi-gigabit communication systems specify a bit error rate of 10^{12} (e.g., PCI-Express, Fibre Channel, and XAUI, [1][2][3]). In many digital communication systems, it is customary to plot the bit-error-rate as a function of Gaussian signal-to-noise ratio (E_b/N_0). In wired digital communications systems, the National Committee for Information Technology Standards (in its Fibre Channel organization) has specified a different methodology for characterizing performance. This methodology plots the bit-error-rate vs. receiver sampling point in unit intervals (UI)

of time on a plot called a bathtub curve [4]. If the receiver is guaranteed to make a correct decision within some sample threshold, the bit-error-rate of the system can be determined from these bathtub curves at that point. For example, Stratix GX devices have a receiver jitter tolerance of 0.65 UI or a threshold window of 0.35 UI. The Fibre Channel organization specifies how these bathtub plots are created using random and deterministic jitter numbers, and an example using the jitter specifications for the XAUI specification is shown in Figure 1. The jitter is specified in two components, random and deterministic. Random jitter is assumed to have a Gaussian distribution and it is unbounded. Deterministic jitter has a defined distribution and a peak-to-peak value. Systems are designed with deterministic jitter specified to be less than the receiver jitter tolerance. Therefore, deterministic jitter by itself does not cause bit errors, but the unbounded random jitter added to the deterministic jitter leads to bit errors.

Error Correcting Code Design

There are many considerations in choosing an error correcting code (ECC) for a serial digital multi-gigabit communication system. One of the most important is the maximum run length (MRL) of the code. The code must be able to meet the maximum run length requirements of the transceivers (80 bits for the Stratix GX devices) and also perform well in an AC-coupled system in which most serial digital multi-gigabit communication systems exist. The coding used

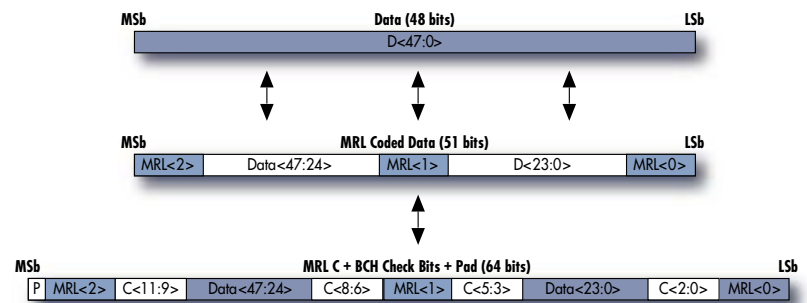
Figure 1. XAUI Probability of a Bit Error Curve



in most existing systems is 8B/10B coding which maps 8-bit input data words into 10-bit code words. This code has excellent maximum run length performance and limits the maximum running disparity between 0s and 1s to allow good performance in AC-coupled systems where DC balance is important. However, the 8B/10B coding does not provide any mechanism for error correction. Using 8B/10B coding in addition to error correction coding would also be undesirable because it already has a code rate of 0.8 and error correction coding would add even more overhead. Additionally, there is the question of what order to perform the 8B/10B coding and the error correction coding. Ideally, the MRL coding would be performed inside of ECC because the ECC will likely upset the maximum run length constraints of the MRL code if done in the opposite order. However, if this order is used and errors occur, the MRL decoder could multiply a single bit error into multiple bit errors, which could overwhelm the error correcting capability. 8B/10B coding is particularly sensitive to this multiplying of bit errors. A better way to design an error correcting code for these systems is to perform the ECC inside of the MRL coding [5].

The ECC chosen in this design is a two-error correcting primitive BCH code of length $2^6 - 1$. This code accepts a 51-bit input word and adds 12 parity bits to it for a total code word of 63 bits [6]. The MRL coding chosen is a scheme that maintains a running disparity count of the transmitted data including the parity bits from the ECC code [7]. The MRL code accepts 48 input data bits and adds 3 MRL code bits. Based on the running disparity and the disparity of the next input data word, the MRL code will either invert or not invert the incoming data in an attempt to force the running disparity toward 0. Two of the three MRL code bits indicate whether the data has been inverted or not and are set to 00 or 11. The third MRL code bit is a forced transition (1 or 0 depending on what the other two MRL bits were). This MRL code provides a means to minimize the running disparity, although it doesn't provide a guaranteed bound on running disparity like the 8B/10B coding does, and it also meets the maximum run length constraint by forcing a transition every 63 bits. It is inconvenient to connect 63 bits to the Stratix GX transceiver since it supports data word sizes of 8, 10, 16, and 20 bits. The solution is to add one extra pad bit to make the code word 64 bits, an even multiple of 16 bits. This pad bit could be used by a higher-level protocol as a frame or synchronization bit. The organization and order of the coding is shown in Figure 2. The code has a rate of 0.75, similar to the 8B/10B coding commonly used, with the advantage of being able to correct any two bit errors in each received code word.

Figure 2. MRL + ECC Code Design



Implementation

The design was implemented using an Altera Stratix GX (EP1SGX25F1020) device in a -5 speed grade. The size of the encoder is 450 logic cells (LCs) with 181 register LCs. The encoder design is pipelined in two stages, one stage for MRL encoding, and the second stage for ECC encoding. The maximum parallel clock frequency at which the design will operate is 67.79 MHz.

The size of the decoder is 989 LCs with 306 LC registers. The decoder design is pipelined into four stages, one stage for syndrome computation, one stage for error location polynomial coefficient calculation, one stage for error search, and a stage for MRL decoding. The maximum parallel clock frequency at which the design operates is 105.33 MHz. It may be possible to remove one pipeline stage to improve the latency performance since the decoder operates so much faster than the encoder.

The maximum serial data rate for the encoder and decoder would be 4.34 Gbps, which is beyond the capabilities of the Stratix GX transceivers. The design works at any data rate supported by the Stratix GX transceivers.

Performance

The performance of the coding design was simulated using ModelSim® with two different data patterns, a $2^{11} - 1$ PRBS pattern and a $2^{31} - 1$ PRBS pattern. All possible single-, double-, and triple-bit-error patterns were inserted between the encoder and decoder. The design corrected all single- and double-bit-error patterns. The code was able to detect 52.4% of the triple-bit-error patterns, while the others were decoded incorrectly. The maximum running disparity values for the $2^{11} - 1$ PRBS pattern simulated with 1,172 pattern repeats were 34 and -42. The maximum running disparity values for the $2^{31} - 1$ PRBS pattern simulated with 2 pattern repeats were 62 and -83.

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The improvement in bit-error-rate performance is shown on a bathtub curve in Figure 3. Figure 3 shows the coding gain for a system operating with 0.47 UI of deterministic jitter and 0.0129 UI rms of random jitter. The coding gain at a bit-error-rate of 10^{-12} in this system is 0.033 UI of jitter. The coding gain is better for systems with more random jitter, and for a system with 0.0464 UI rms of random jitter and no deterministic jitter, the gain is 0.118 UI of jitter at a bit-error-rate of 10^{-12} .

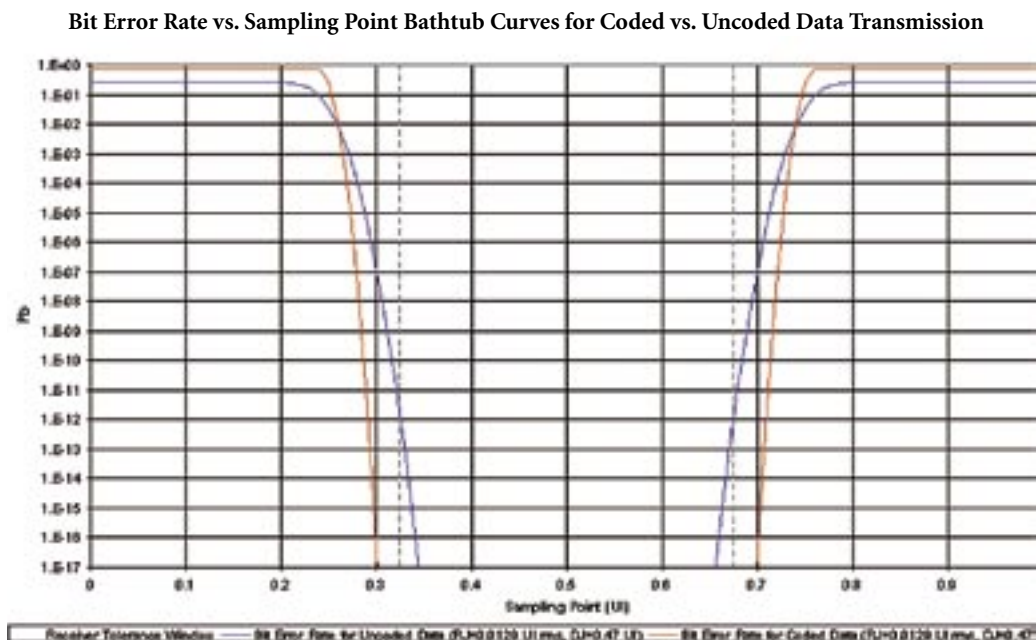
Conclusion

The coding scheme discussed will provide some coding gain for serial digital multi-gigabit communication systems. The code rate is similar to 8B/10B coding, so lower bit error rates can be realized by systems currently using 8B/10B coding, with a small amount of added overhead. The latency performance on the decode side of four parallel clock cycles is reasonable for interconnection applications where serial digital multi-gigabit communication is common.

References

- [1] PCI-SIG. PCI Express Base Specification, Rev 1.0a. PCI Special Interest Group, Portland, OR, April 15, 2003.
- [2] IEEE Computer Society. IEEE Std 802.3ae - 2002 (Amendment to IEEE Std 802.3 - 2002). The Institute of Electrical and Electronics Engineers, New York, NY, August 30, 2002.
- [3] National Committee for Information Technology Standards. Information technology- Fibre Channel - Physical Interfaces (FC-PI). ANSI INCITS 352-2002, November 19, 2002.
- [4] National Committee for Information Technology Standards. Information Technology- Fibre Channel - Methodologies for Jitter Specification. INCITS TR-25-1999, September 1, 1999.
- [5] A. J. van Wijngaarden and K. A. Schouhamer. "Maximum Runlength-Limited Codes with Error Control Capabilities." IEEE Journal on Selected Areas in Communications, Vol. 19 (4), April 2001, pp. 602-611.
- [6] Shu Lin and Daniel J. Costello. Error Control Coding: Fundamentals and Applications Second Edition. Prentice Hall, New Jersey, 2004.
- [7] A. Coles and D. Cunningham. "Low Overhead Block Coding for Multi-Gb/s Links." HP Labs Technical Reports, Extended Enterprise Laboratory HPL-98-168, October 1998.

Figure 3. Coding Gain for ECC



Cyclone II FPGAs & Nios II Embedded Processor Offer Low-Cost Performance Advantages

Building on the success of its industry-leading, low-cost Cyclone™ FPGA family and Nios® soft embedded processor, Altera has now launched the second generation of each product. Cyclone II devices offer customers increased densities and new, performance-enhancing hardware features at a 30 percent lower cost than the previous generation. These new devices are more than 50 percent faster and cost up to 50 percent less than competitive FPGAs. In addition, the Nios II soft core embedded processor is more powerful and occupies fewer logic elements (LEs) than the original Nios processor.

ASIC & ASSP Design Limitations

Today's design engineer is routinely tasked with providing products that offer the level of performance and selection of features needed to maintain a competitive edge, while also dealing with ever-tighter budgets and shrinking market windows. In the past, the challenge of meeting advanced performance requirements for high-volume products have been most cost-effectively met using either an ASIC or a suitable ASSP. While ASICs have historically offered the lowest-cost path to achieving the highest level of performance, that benefit has been offset by a lack of design flexibility, lengthy time to market and high development risks. ASSPs, on the other hand, are lower risk in terms of time-to-market, and development success, but still lack the flexibility offered by programmable logic.

Off-the-shelf ASSPs and microcontrollers can have an additional liability: obsolescence. Most hard embedded processors become obsolete over time and are discontinued. As a result, manufacturers who are using obsolete processors are forced into costly and time-consuming hardware redesigns and software application rewrites. Such a redesign may even require a complete change in the instruction set architecture from one family of processors to the next, leading to a even greater investment in time and money. Soft embedded processors, such as Altera's new Nios II processor, help prevent this kind of system obsolescence because they can be ported to future FPGA families, ensuring that the end user's software code will remain compatible across many generations of hardware.

Altera is focused on providing its customers with industry-leading programmable logic devices (PLDs), powerful embedded processors, a rich portfolio of intellectual property (IP) and a powerful suite of development tools to enable customers to create the exact design they need to meet a particular system requirement as quickly and as easily as possible. At the same time, the flexibility in Altera's offerings allows customers to easily expand a design's performance or

features to meet changing system parameters, thereby avoiding the risk of obsolescence.

Cyclone II & Nios II Benefits

Combined with the first-generation Nios processor, Cyclone devices delivered a cost-effective system-on-a-programmable-chip (SOPC) solution. The Cyclone II FPGA and Nios II processor combination takes this to the next level, enabling designers to build SOPC designs that can now effectively compete with mid-density ASICs and ASSPs. As a result, designers can now leverage the flexibility, time-to-market, and cost benefits of programmable logic in a host of new applications that were previously the domain of ASICs and ASSPs. A combined Nios II/Cyclone II design can implement a complete embedded processing system for as little as \$0.35 of logic, with performance of more than 100 Dhrystone million instructions per second (DMIPS).

The Nios II family includes: a high-performance core (Nios II/f, "fast"); a low-cost core (Nios II/e, "economy"); and a performance/cost balanced core (Nios II/s, "standard"). All three cores share a common 32-bit instruction set architecture (ISA) and are 100 percent binary-code compatible. All three cores are available under a single, royalty-free license to enhance design flexibility and minimize development cost. In addition, all the cores are capable of implementing custom instructions that allow critical software subroutines to be implemented in the FPGA, under operational control of the Nios II embedded processor. These instructions, which take multiple clock cycles in a hardware implementation, can be completed using a Nios II processor in as little as a single clock cycle, thereby increasing system performance and data throughput.

Design Flow

Recognizing that its customers, especially in consumer markets, face critical time-to-market windows and short product life cycles, Altera has developed a suite of tools—including SOPC Builder, the Nios II integrated design environment (IDE) and Quartus II development software—designed to speed the development of the hardware and software required to implement a complete programmable-logic-based SOPC solution. In line with this approach, customers licensing the Nios II processor receive a development kit that includes the soft processor core and the set of software tools needed to implement Nios II designs in an Altera® FPGA.

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SOPC Builder is the key tool used to implement IP in an Altera FPGA. This system-level tool uses Altera's MegaWizard® technology to automatically generate an Avalon™ switch fabric that connects the various functional blocks within a design. SOPC Builder also generates a custom software development kit providing the appropriate software header files, as necessary, for the functional blocks controlled by the Nios II processor. Using SOPC Builder frees designers from the time-consuming task of manually connecting and verifying the register and memory-mapped architecture within a design, freeing them to focus on optimizing critical system functions while also helping to reduce development time.

The Nios II IDE is the primary development tool for the Nios II soft processor and provides an integrated design environment for software development. It includes a graphical user interface (GUI) that provides project management, code development, and Joint Test Action Group (JTAG)-based debug capabilities for the simplest to the most complex Nios II processor-based designs. Additional tool capabilities include an instruction set simulator to enable code debug without requiring a debug development board, a MicroC/OS-II real-time operating system, and a light-weight TCP/IP protocol stack.

The industry-leading Quartus II software provides design capture, synthesis, simulation, and place-and-route functions for hardware development. Quartus II software offers unmatched levels of performance and ease-of-use that help designers achieve their design goal, while also speeding their time-to-market. As a result, Quartus II software is the most cost-effective FPGA development suite available.

Design Example

A look at an Internet appliance system design example highlights the benefits that can be derived from a design combining Cyclone II FPGAs and Nios II processors. Internet appliances include products such as video game consoles, some set-top boxes, smart refrigerators, and alarm systems. Such a system would communicate over an Ethernet link and perform some data processing. It would include some custom peripherals, the necessary system functionality, glue logic, and a user interface.

The traditional way to design such a system involves using a digital signal processor, an Ethernet MAC/PHY, a small microcontroller, and an FPGA. While this approach would provide all the desired system functionality, it would require multiple I/O pins to interface between the FPGA and the digital signal processor, complicating the design. In addition, such a design requires a minimum of 4 components,

consuming unnecessary amounts of valuable board real estate.

With the introduction of the Cyclone II device family and the Nios II embedded processor, the options for implementing this system change dramatically. It is possible, for example, to implement the digital signal processing (DSP) functionality using the Nios II embedded processor core, thereby eliminating a quarter of the previously required components. For more intensive DSP applications, a designer could leverage the Nios II processor's custom instruction capability to implement certain functions that can be run more efficiently in hardware.

If even more advanced DSP performance is required, the entire DSP function could be implemented in hardware using a combination of Altera's IP cores and custom hardware. The embedded multipliers available in Cyclone II devices, for example, could be used to perform math-intensive instructions much more quickly than even high-end digital signal processors. The Nios II processor would be used in such an implementation to handle all the control functions normally performed by a digital signal processor.

Because Cyclone II devices have triple the density of first-generation Cyclone devices, they are capable of integrating a wider array of functions, enabling increased system integration and reliability, while helping to reduce system costs. The Nios II processor also offers enhanced capabilities, a real time operating system (RTOS), and middleware, making it possible to use the processor to run a web server to provide Internet-enabled control and monitoring for equipment in the field.

Finally, a second Nios II core can be implemented in the same Cyclone II FPGA to handle the keypad and LCD driver, providing a man/machine interface (MMI) processor. This second processor typically operates at a slower speed than the digital signal processor. Using two processors prevents the slower MMI processor from interfering with DSP performance.

Conclusion

The introduction of the Nios II processor and the Cyclone II FPGA has expanded the choices available for designers who have previously required low- to mid-density ASICs to meet system performance requirements. Using Altera's powerful suite of development software and rich IP portfolio, designers can now leverage the flexibility and time-to-market advantages of programmable logic by implementing SOPC designs for cost-sensitive applications using a Nios II processor in a Cyclone II FPGA.

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Power Analysis for Efficient Power Planning

As designs grow larger and process technologies continue to shrink, power becomes an increasingly important design consideration. When designing a printed circuit board (PCB), the power consumed by a device needs to be accurately estimated to develop an appropriate power budget and to design the power supplies and cooling system. The Quartus® II software version 4.2 introduces PowerPlay power analysis and optimization technology to assist with power planning.

Power Planning

The factors affecting power in FPGAs are Device selection, environmental conditions and resources used by the design. Understanding of these factors allow you to effectively use the PowerPlay Power analysis tools to accurately estimate and plan for your device power consumption. Power analysis meets two essential planning requirements:

- **Thermal Planning:** The designer must ensure that the cooling solution is sufficient to dissipate the heat generated by the device. In particular, the computed junction temperature must fall within normal device specifications.
- **Power Supply Planning:** Power supplies provide adequate current to support device operation.

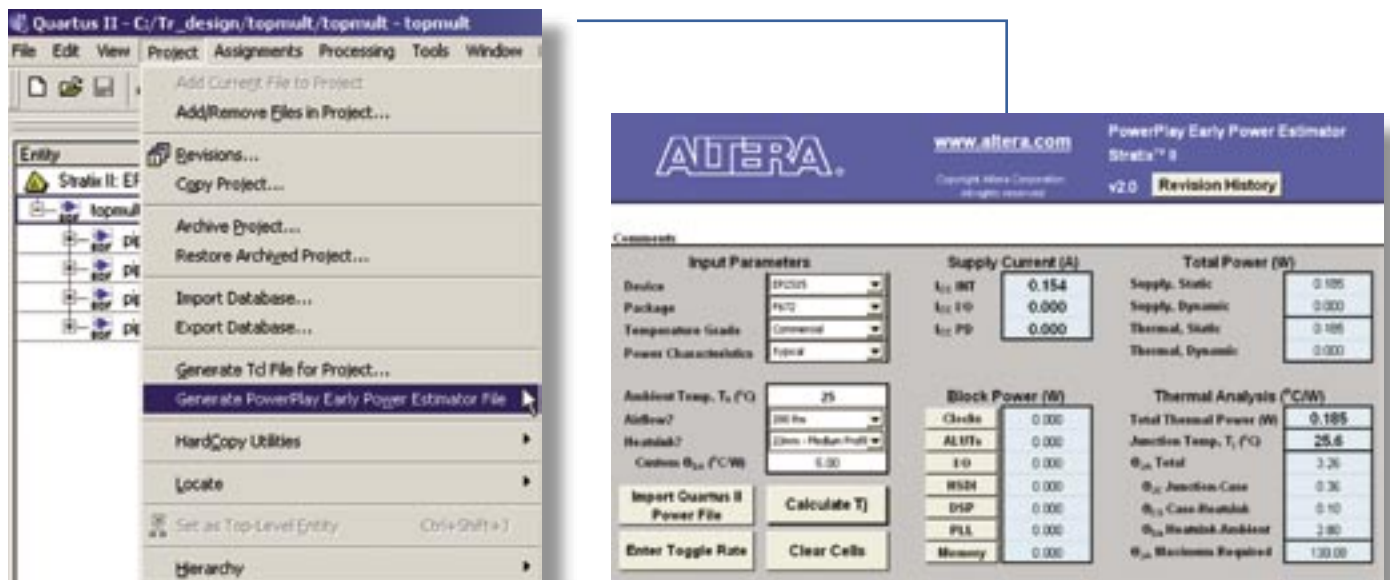
Power Estimation & Analysis

You can estimate power at different stages of your design cycle. Depending where you are in your design cycle and the accuracy of the estimation required, you can either use the PowerPlay Early Power Estimator spreadsheet available as a download from the Altera web site or the PowerPlay Power Analyzer Tool in the Quartus II software.

PowerPlay Early Power Estimator

Because FPGAs provide the convenience of a shorter design cycle and faster time to market, the board design often takes place during the FPGA design cycle, which means the power planning for the device must happen before the FPGA design is complete. If the FPGA design has not yet begun or is not complete, an estimate of the power consumption for the design can be made using the Early Power Estimator spreadsheets. See Figure 1. Separate spreadsheets are available for each device family.

Figure 1. PowerPlay Early Power Estimator



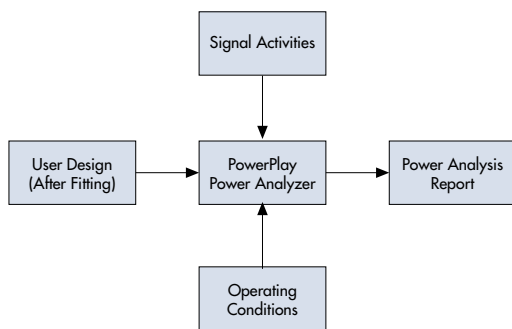
PowerPlay Power Analyzer

When the FPGA design is complete, accurate device power consumption can be estimated with the PowerPlay Power Analyzer tool in Quartus II software. Run the Power Analyzer after synthesis and place-and-route are completed, which provides detailed information on the design implementation and enables high-quality power estimates. See Table 1.

PowerPlay Power Analyzer Flow

The PowerPlay Power Analyzer supports accurate and representative power estimation by letting you specify all the important factors affecting power. Figure 2 illustrates the high-level Power Analyzer flow.

Figure 2. PowerPlay Analyzer High-Level Flow



Note to Figure 2:

(1) Operating conditions are available only for the Stratix® II and MAX® II device families.

Signal Activities

The most important factor in estimating power consumption is the behavior of each signal in the design. The two vital statistics are the toggle rate and the static probability. The toggle rate of a signal is the average number of times that signal will change value per unit of time. The units for toggle rate are transitions per second, and a transition is a change from 1 to 0 or 0 to 1. The static probability of a signal is the fraction of time that the signal will be logic 1 during the period of device operation that is being analyzed.

The Power Analyzer provides a flexible framework for specifying signal activities. This reflects the critical importance of using representative signal activity data during power analysis. The data sources are:

- Simulation results
- User-entered node, entity and clock assignments
- User-entered default toggle rate assignment
- Vectorless estimation (available for Stratix II and MAX II device families)

Table 1. Comparison of PowerPlay Early Power Estimator & PowerPlay Power Analyzer		
Characteristic	PowerPlay Early Power Estimator	PowerPlay Power Analyzer
Phase in the Design Cycle	Anytime	After Fitting
Tool Requirements	Spreadsheet Program/ Quartus II Software	Quartus II Software
Accuracy	Medium	Medium to Very High
Data Inputs	<ul style="list-style-type: none"> ■ Resource Usage Estimates ■ Clock Requirements ■ Environmental Conditions 	<ul style="list-style-type: none"> ■ Design after Fitting ■ Clock Requirements ■ RTL Simulation Results (optional) ■ Post-Fitting Simulation Results (optional) ■ Signal Activities per Node or Entity (optional) ■ Signal Activity Defaults ■ Environmental Conditions
Data Outputs (2)	<ul style="list-style-type: none"> ■ Total Thermal Power Dissipation ■ Thermal Static Power ■ Thermal Dynamic Power ■ Off-Chip Power Dissipation ■ Voltage Supply Currents (1) 	<ul style="list-style-type: none"> Total Thermal Power Thermal Static Power Thermal Dynamic Power Thermal Power by Design Hierarchy Thermal Power by Block Type Off-Chip (Non-Thermal) Power Dissipation Voltage Supply Currents (1)

Notes to Table 1:

(1) Available only for Stratix® II and MAX® II device families.

(2) Early Power Estimator output varies by device family; some features may not be available.

The Power Analyzer lets you mix and match the signal activity data sources on a signal-by-signal basis. Using simulation results is the most accurate way to generate signal activities, which is used to accurately estimate the power of your design. The PowerPlay Power Analyzer reads the results generated by the Quartus II simulator and other third-party EDA simulators. This flow provides the highest accuracy, as all node activities reflect actual design behavior, provided that supplied input vectors are representative of typical design operation.

Operating Conditions

Operating conditions can be specified for the Stratix II and MAX II device families, including device power characteristics (typical or maximum), environmental conditions, and junction temperature. The Power Analyzer can automatically compute the junction temperature based on the specified ambient temperature and cooling solution. You may select from a prepared list of sample cooling solutions. For a more accurate analysis, you can directly enter the thermal resistance of your exact cooling solution.

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Power Analysis Optimization

The PowerPlay Power Analyzer provides a comprehensive power consumption report. The report is divided into different sections for detailed information.

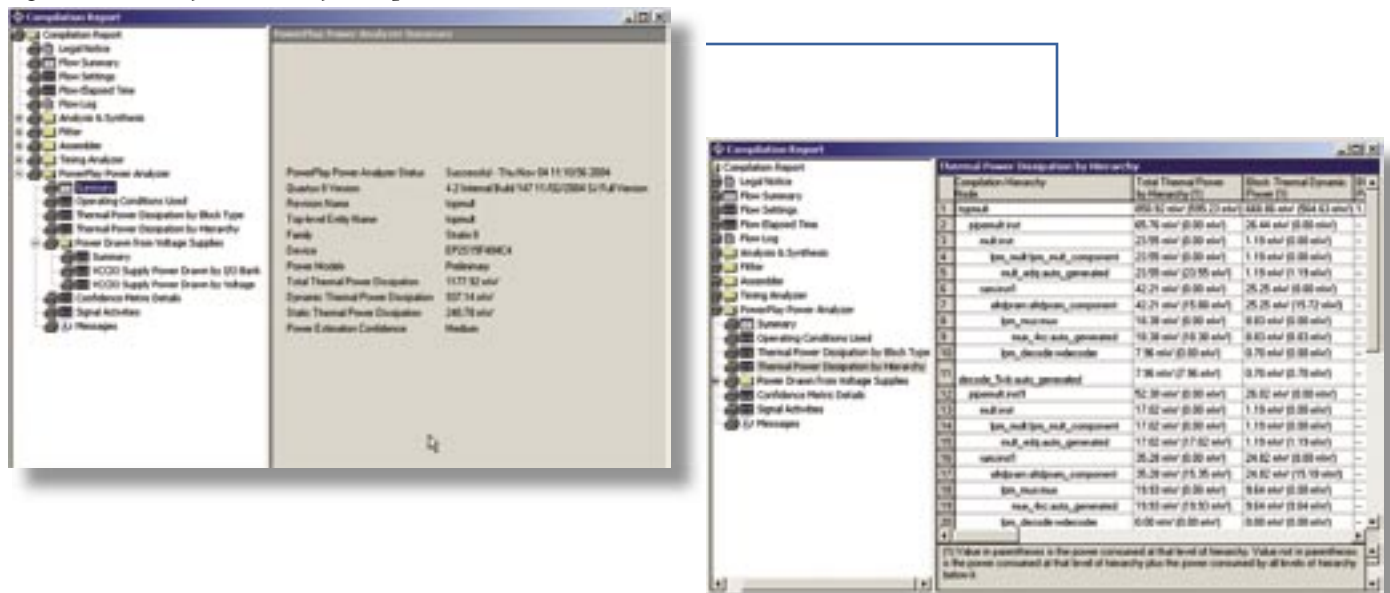
1. The “Summary” section of the report provides an estimated total thermal power consumption of your design. This includes the dynamic power, static power, and the routing power consumption.
2. The “Operating Conditions Used” section provides device characteristics, voltages, and cooling solution, if any, that were used during the power estimation.
3. The “Thermal Power Dissipation by Block Type” section provides the estimated thermal dynamic power and thermal static power consumption categorized by block types.
4. The “Thermal Power Dissipation by Hierarchy” section shows an estimated thermal dynamic power and thermal static power consumption categorized by design hierarchy and is further categorized by the dynamic and static power that was used by the blocks and routing within that hierarchy. This is very useful in locating modules that consume high power in your design and use this information to optimize it for low power consumption (see figure 3).

5. The “Power Drawn from Voltage Supplies” section supports power supply planning. It lists the power that was drawn from each voltage supply.
6. The “Confidence Metric Details” section provides information about the quality of the signal activity data sources.
7. The “Signal Activities” section lists toggle rate and static probabilities assumed by power analysis for all signals with fan-out and pins.

Conclusion

Advancement in semiconductor technology has led to smaller dimensions of transistors, and devices with higher density, higher performance, low voltage, and low power dissipation. At the same time, designs have also become larger and more complex, causing devices to consume more power. This makes it vitally important to accurately estimate the power for your design. Altera provides PowerPlay Power Analysis tools to estimate the power consumption of your design throughout the design cycle.

Figure 3. PowerPlay Power Analyzer Report



Altera Development Kits

In 1999, Altera introduced the SOPC Development Board. This first-of-its-kind system development platform featured the high-density (at that time) APEX™ EP20K400 device, and was designed to appeal to all types of programmable logic designers. Intended as a catch-all intellectual property (IP) and system development platform, the board featured a variety of components and connectors including: RS-232, 1394, 1284, PS2, and USB ports; SRAM and SDRAM; EEPROMs and flash memory; BNC, PMC, CMC, and VGA connectors; LEDs; and push buttons. The board was used internally to test IP functions in hardware, and could also be used as a development platform by Altera's customers. The SOPC Development Board enjoyed a moderate level of success, reinforcing the idea that customers recognized the benefit of hardware development platforms. However, it soon became apparent that while prototyping hardware was useful, customers really wanted more focused development platforms.

Optimum development board features vary with technology focus. Embedded systems, digital signal processing (DSP), and high-speed interface design-

ers require different combinations of connectors and memories. Embedded system designers simply want to run their software code on the hardware without having to wait for their custom hardware development to be complete. DSP designers want a faster method of verification. Given the variety of situations that DSP designs must be prepared to handle, software simulations are just not practical. Thus, DSP system designers need hardware verification platforms to effectively debug these complex DSP designs. Having identified the need for more focused development hardware, Altera started to identify those specific markets that warranted a specialized development kit.

Three major technology areas were identified: DSP, embedded systems, and high-speed interfaces. With those markets in mind, Altera developed more targeted kits, such as the Stratix® PCI and DSP development kits, and the various Nios® II kits. Building upon the success and momentum of these development kits, Altera has recently developed four new kits to support the new low-cost MAX® II CPLD family and the high-performance Stratix II FPGA family.

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Figure 1. Altera Development Boards (From Left to Right, MAX II, Nios II, Stratix II DSP, & Stratix II High-Speed Development Boards)



Although the MAX II Development Kit is a full-featured development platform that enables customer prototyping and debugging, it is the ability to demonstrate MAX II features in a hands-on, “seeing is believing” environment that has been identified as the critical requirement for the kit. As a result, the MAX II Development Kit uniquely focuses on demonstrating the capabilities of the device as the top priority. The MAX II Development Kit ships with the industry leading Quartus® II software and several demonstrations and reference designs, each of which is targeted to show a particular MAX II feature, as well as introduce new users to the Altera® design flow.

The three Stratix II development kits combine the focused features and advanced development software customers need to take full advantage of the Stratix II FPGA family’s industry-leading performance and features. Each kit includes a Stratix II development board, a CD containing documentation and reference designs, a power supply, a USB Blaster™ download cable, and other cables. The kits also ship with Altera’s Quartus II software and the complete library of Altera MegaCore® functions.

Some details about each kit follow:

- The Stratix II High-Speed Development Kit delivers a comprehensive platform for designs requiring high-speed interfaces. Included in the kit are the Stratix II EP2S60F1020 device and DDR2 SDRAM DIMM modules for high-speed memory transfers. The kit also supports high-speed I/O protocols such as, SPI-4.2 with dynamic phase alignment (DPA), SFI-4, 10-gigabit 16-bit interface (XSBI), HyperTransport™, RapidIO®, PCI and PCI-X interfaces, and LVDS.
- The Stratix II DSP Kit delivers a complete DSP development environment with a DSP development board, the DSP Builder development tool, and MATLAB/Simulink DSP system modeling software. The development board features the Stratix II EP2S60F1020 device along with analog interfaces to enable high-performance wireless, video, and audio applications. These analog interfaces include two 125 MSPS ADCs, two 165 MSPS DACs, a

video DAC, and a 96-KHz stereo audio codec. Additionally, the board contains support for external memory, including 16 MB of SDRAM, 1 Mbyte SRAM, and 32 Mbytes of compact flash. Finally, the board has a connector for interfacing to the Texas Instruments’ external memory interface (EMIF) to speed development of FPGA co-processors.

- The Nios II Development Kit, Stratix II Edition provides designers with the resources needed to begin developing embedded processor systems on Stratix II FPGAs, including a full license for the Nios II family of processors, the Nios II integrated development environment (IDE), and a full-featured development board. In addition to the Stratix II device, the development board also features 16 Mbytes of SDRAM and 1 Mbyte of SRAM, a 10/100 Ethernet port, two serial ports, a Mictor connector for software trace debug, and two expansion headers.
- The MAX II Development Kit features an instant-on, reprogrammable MAX II device (EPM1270F256C5), along with a USB MAC and PHY, a SPI temperature gauge, one Mbit of SRAM, a unique power-up sequencing circuit, power-measuring circuitry, LEDs, and push buttons. The kit ships with the free Quartus® II Web Edition software, a USB type A-to-B cable, and a ByteBlaster™ II download cable for device programming. The kit also features reference designs and demonstrations that highlight the unique features of the MAX II CPLDs.

Pricing & Availability

All three Stratix II Development Kits and the MAX II Development Kit are available for ordering through Altera’s distributors and sales representatives. The MAX II Development Kit can also be ordered on Altera’s web site at www.shopaltera.com. Pricing is \$1,995 for the High-Speed and DSP Development Kits, \$995 for the Nios II Development Kit, and \$150 for the MAX II Development Kit. Find out more at www.altera.com/devkits.

Upcoming Events

Altera takes part in and sponsors a wide variety of trade shows, seminars, and conferences on an ongoing basis. Table 1 lists upcoming events. For more information, visit www.altera.com.

Table 1. Upcoming Events Calendar			
Date	Event Name	Location	Altera Presence
January 6 to 9, 2005	International Consumer Electronics Show	Las Vegas, Nevada	Exhibitor Booth
January 31 to February 3, 2005	DesignCon West	Santa Clara, California	Exhibitor Booth, Conference Papers
February 4, 2005	High-Speed Design Symposium	Santa Clara, California	Altera-Hosted Seminar
February 15 to 17, 2005	Texas Instruments Developers Conference	Houston, Texas	Exhibitor Booth
February 22 to 24, 2005	Embedded World	Nürnberg, Germany	Exhibitor Booth, Conference Papers
February 28 to March 2, 2005	Intel Developers Forum	San Francisco, California	Exhibitor Booth
March 7 to March 10, 2005	Embedded Systems Conference	San Francisco, California	Presenting 2 Conference Papers
March 7 to March 11, 2005	DATE	Paris, France	Partner Booths
March 8 to March 9, 2005	CMP Design Seminar Series	San Francisco, California	Presenting 2 Conference Papers
March 21 to March 23, 2005	China Cable Broadcasting Network 2005	Beijing, China	Exhibitor Booth

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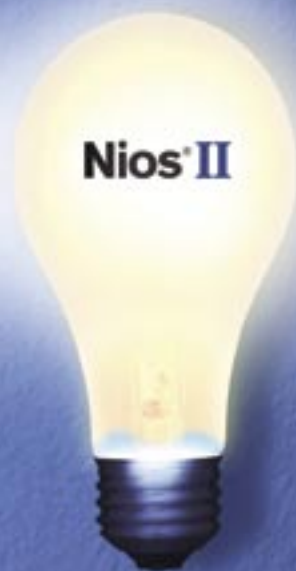
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Altera FPGA Matrix: New Devices

Density & Speed	Stratix II (1.2 V) High Density, High Performance						Cyclone II (1.2 V) Low Cost, High Volume					
	EP2K15	EP2K30	EP2K60	EP2K90	EP2K30	EP2K180	EP2C5	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
Adaptive Logic Modules (ALMs)	6,240	13,552	24,176	36,384	53,016	71,760	-	-	-	-	-	-
Adaptive Look-Up Tables (ALUTs)	12,480	27,104	48,352	72,768	106,032	143,520	-	-	-	-	-	-
Logic Elements (LEs) ¹	15,600	33,880	60,440	90,960	132,540	179,400	4,608	8,256	18,752	33,216	50,528	68,416
Total RAM Bits (K) ²	419	1,370	2,544	4,520	6,748	9,383	120	166	240	484	594	1,152
M512 RAM Blocks (512 bits + 64 parity bits)	104	202	329	488	699	930	-	-	-	-	-	-
M4K RAM Blocks (4 Kbits + 512 parity bits) ³	78	144	255	408	609	768	26	36	52	105	129	250
M-RAM Blocks (512 Kbits + 65,536 parity bits) ³	0	1	2	4	6	9	-	-	-	-	-	-
Speed Grades (fastest to slowest)	-3, -4, -5	-3, -4, -5	-3, -4, -5	-3, -4, -5	-4, -5	-4, -5	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8
Available Embedded Processor	Nios® II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II
DSP Blocks	12	16	36	48	63	96	-	-	-	-	-	-
18x18-bit/9x9-bit Embedded Multipliers	48 / 96	64 / 128	144 / 288	192 / 384	252 / 504	384 / 768	13 / 26	18 / 36	26 / 52	35 / 70	86 / 172	150 / 300
I/O Registers per I/O Element	6	6	6	6	6	6	3	3	3	3	3	3
True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Global & Regional Clock Networks	48	48	48	48	48	48	8	8	16	16	16	16
Phase-Locked Loops (PLLs)/Unique Outputs	6 / 28	6 / 28	12 / 56	12 / 56	12 / 56	12 / 56	2 / 6	2 / 6	4 / 12	4 / 12	4 / 12	4 / 12
Design Security ⁴	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HardCopy™ Devices Support	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Industrial & Lead-Free Device Support	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Configuration File Size (Mbits)	5.0	10.1	17.1	27.5	39.6	52.4	1.23	1.99	3.93	7.07	9.13	10.25
Number of EPC1 Devices (1 Mbit)	-	-	-	-	-	-	1	-	-	-	-	-
Number of EPC4 Devices (4 Mbits)	1	-	-	-	-	-	1	1	1	-	-	-
Number of EPC16 Devices (16 Mbits)	1	1	1	-	-	-	1	1	1	1	1	1
Number of EPC64 Devices (64 Mbits)	1	1	1	1	1	1	1	1	1	1	1	1
Number of EPC2 Devices (1.6 Mbits)	2	4	7	11	16	21	1	1	2	4	5	7
Number of EPC4 Devices (4 Mbits)	1	-	-	-	-	-	1	1	1	-	-	-
Number of EPC8 Devices (8 Mbits)	1	1	-	-	-	-	1	1	1	1	1	1
Number of EPC16 Devices (16 Mbits)	1	1	1	-	-	-	1	1	1	1	1	1
I/O Voltage Levels Supported	1.5V, 1.8V, 2.5V, 3.3V						1.5V, 1.8V, 2.5V, 3.3V					
I/O Standards	LVDS, LVPECL, HyperTransport, Differential SSTL-18 (I & II), Differential SSTL-2 (I & II), 1.5-V Differential SSTL-2 (I & II), 1.8-V Differential SSTL-2 (I & II), 1.5-V Differential SSTL-18 (I & II), 1.8-V Differential SSTL-18 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, PCI-X 1.0, LVTTTL, LVCMOS											
External Memory Device Interfaces	QDRII, DDR2, RDRAM II, DDR, SDR											
True-LVDS™ Maximum Data Rate (Mbps)	1,000	1,000	1,000	1,000	1,000	1,000	-	-	-	-	-	-
True-LVDS Channels (Receive/Transmit)	42 / 38	62 / 58	84 / 84	118 / 118	156 / 156	156 / 156	-	-	-	-	-	-
Medium-Speed LVDS Data Rate (Mbps) (Receive/Transmit)	-	-	-	-	-	-	805 / 622	805 / 622	805 / 622	805 / 622	805 / 622	805 / 622
Medium-Speed LVDS Channels	-	-	-	-	-	-	60	79	136	209	197	265
RDS Maximum Data Rate (Mbps) (Transmit)	-	-	-	-	-	-	170	170	170	170	170	170
Mini-LVDS Maximum Data Rate (Mbps) (Transmit)	-	-	-	-	-	-	170	170	170	170	170	170
Embedded Dynamic Phase Alignment (DPA) Circuitry	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Series On-Chip Termination	✓	✓	✓	✓	✓	✓	-	-	-	-	-	-
Differential On-Chip Termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Programmable Drive Strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes: ¹For Stratix II, the values represent the number of equivalent logic elements (1 ALM = 2.5 LEs); ²K=1,000; ³Kbit=1,024 bits; ⁴Design Security for Cyclone II available with MAX® II handshaking solution

Altera FPGA Matrix: New Devices

- Device Available Now in Commercial (0 to 85° C) & Industrial (-40 to 100° C) Temperatures.
- Device Available Now in Commercial Temperature; Contact Altera for Industrial Temperature
- Vertical Migration (Same VCC, GND, ISP & Input Pins)

	Stratix II (1.2 V) High Density, High Performance					Cyclone II (1.2 V) Low Cost, High Volume				
	EP2S15	EP2S30	EP2S60	EP2S90	EP2S180	EP2C8	EP2C20	EP2C35	EP2C50	EP2C70
Thin Quad Flat Pack (T)										
Plastic Quad Flat Pack (Q)										
FineLine BGA (F)	144-Pin TQFP					89	110 ¹			
	208-Pin PQFP					142	152			
	256-Pin FBGA					171 ¹	315	322	294	
	484-Pin FBGA	342	342	334				475	450	422
Hybrid FineLine BGA (H)	672-Pin FBGA	366	500	492						
	780-Pin FBGA			534 ¹						
	896-Pin FBGA				742					622
	1,020-Pin FBGA		718	758	742					
1,508-Pin FBGA			902	1,126	1,170					
484-Pin HFPGA			308 ¹							

Notes: ¹ User I/O counts are preliminary and subject to change.

	TQFP	PQFP	FBGA	HFPGA
Package Statistics				
Number of Pins	144	208	780	484
Nominal Length x Width (mm)	22 x 22	30.6 x 30.6	29 x 29	40 x 40
Maximum Surface Area (mm ²)	493	952	853	1,616
Maximum Height (mm)	1.60	4.10	3.50 ¹	3.50 ¹
Nominal Lead Pitch (mm)	0.50	0.50	1.00	1.00
Maximum Lead Width (mm)	0.27	0.27	0.70	0.70

Note: ¹ Altera's maximum height specification is 2.6mm. The 3.5mm maximum height specification shown reflects the JEDEC specification.

	Configuration Devices						
	EP2	EP4	EP8	EP16	EP31	EP64	EP128
8-Pin SOIC					✓		
16-Pin SOIC						✓	
20-Pin PLCC	✓						
32-Pin TQFP	✓						
88-Pin UBGA*				✓			
100-Pin PQFP		✓	✓	✓	✓	✓	✓
Reprogrammable	✓	✓	✓	✓	✓	✓	✓
Data Compression	✓	✓	✓	✓	✓	✓	✓
Page Mode		✓	✓	✓			

*UBGA: Ultra FineLine BGA

Altera FPGA Matrix: Production Devices

Density & Speed	Stratix (1.5 V) High Density, High Performance							Stratix GX (1.5 V) 3.125-Gbps Transceivers							Cyclone (1.5 V) Low Cost, High Volume				
	EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80	EP1SGX10C	EP1SGX10D	EP1SGX25C	EP1SGX25D	EP1SGX25F	EP1SGX40D	EP1SGX40G	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
	Available Now							Available Now							Available Now				
Logic Elements (LEs)	10,570	18,460	25,660	32,470	41,250	57,120	79,040	10,570	10,570	25,660	25,660	25,660	41,250	41,250	2,910	4,000	5,980	12,060	20,060
Total RAM Bits (K) ¹	920	1,669	1,944	3,317	3,423	5,215	7,427	920	920	1,944	1,944	1,944	3,423	3,423	60	78	92	240	295
M512 RAM Blocks (512 bits + 64 parity bits)	94	194	224	295	384	574	767	94	94	224	224	224	384	384	—	—	—	—	—
M4K RAM Blocks (4 Kbits + 512 parity bits) ²	60	82	138	171	183	292	364	60	60	138	138	183	183	183	13	17	20	52	64
M-RAM Blocks (512 Kbits + 65,536 parity bits) ²	1	2	2	4	4	6	9	1	1	2	2	4	4	4	—	—	—	—	—
Speed Grades (fastest to slowest)	-5, -6, -7	-5, -6, -7	-5, -6, -7, -8	-5, -6, -7, -8	-5, -6, -7, -8	-5, -6, -7, -8	-5, -6, -7, -8	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-5, -6, -7	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8	-6, -7, -8
Available Embedded Processor	Nios [®] II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II	Nios II
DSP Blocks	6	10	10	12	14	18	22	6	6	10	10	10	14	14	—	—	—	—	—
18x18-bit / 9x9-bit Embedded Multipliers	24 / 48	40 / 80	40 / 80	48 / 96	56 / 112	72 / 144	88 / 176	24 / 48	24 / 48	40 / 80	40 / 80	40 / 80	56 / 112	56 / 112	—	—	—	—	—
I/O Registers per I/O Element	6	6	6	6	6	6	6	6	6	6	6	6	6	6	3	3	3	3	3
True Dual-Port RAM	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Global, Regional & Fast Clock Networks	36	36	36	40	40	40	40	40	40	40	40	48	48	48	8	8	8	8	8
Phase-Locked Loops (PLLs) / Unique Outputs	6 / 32	6 / 32	6 / 32	10 / 40	12 / 52	12 / 52	12 / 52	4 / 26	4 / 26	4 / 26	4 / 26	8 / 42	8 / 42	8 / 42	1 / 3	2 / 6	2 / 6	2 / 6	2 / 6
HardCopy [®] Device Support	—	—	✓	✓	✓	✓	✓	—	—	—	—	—	—	—	—	—	—	—	—
Industrial Device Offering	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Lead-Free Device Offering	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Configuration File Size (Mbits)	3.53	5.90	7.89	10.38	12.39	17.54	23.83	3.58	3.58	7.95	7.95	12.53	12.53	0.63	0.93	1.17	2.32	3.56	
Number of EPC1 Devices (1 Mbit)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	1	1	1	—	—
Number of EPC4 Devices (4 Mbits)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Number of EPC2 Devices (1.6 Mbits)	3	4	5	7	8	11	15	3	3	5	5	8	8	1	1	1	2	2	
Number of EPC4 Devices (4 Mbits)	1	1	—	—	—	—	—	1	1	—	—	—	—	—	1	1	1	1	
Number of EPC8 Devices (8 Mbits)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Number of EPC16 Devices (16 Mbits)	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
I/O Voltage Levels Supported	1.5V, 1.8V, 2.5V, 3.3V							1.5V, 1.8V, 2.5V, 3.3V							1.5V, 1.8V, 2.5V, 3.3V				
I/O Standards Supported	LVDS, LVPECL, HyperTransport [™] , 3.3-V PCML, Differential SSTL-2, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), SSTL-3 (I & II), 1.8-V HSTL (I & II), PCI, Compact PCI, PCI-X 1.0, AGP (1x & 2x), GTL, GTL+, CCT, LVTTTL, LVCMOS							LVDS, LVPECL, HyperTransport, 3.3-V PCML, 1.5-V PCML, Differential HSTL, SSTL-18 (I & II), SSTL-2 (I & II), SSTL-3 (I & II), 1.5-V HSTL (I & II), 1.8-V HSTL (I & II), PCI, Compact PCI, PCI-X 1.0, AGP (1x & 2x), GTL, GTL+, CCT, LVTTTL, LVCMOS							LVDS, RSDS, Differential SSTL-2, SSTL-2 (I & II), SSTL-3 (I & II), PCI, LVTTTL, LVCMOS				
External Memory Device Interfaces	QDR II, DDR2, R1DRAM II, QDR, ZBT, DDR, SDR							QDR II, DDR2, R1DRAM II, QDR, ZBT, DDR, SDR							DDR, SDR				
True-LVDS [™] Maximum Data Rate (Mbps)	840	840	840	840	840	840	840	1,000	1,000	1,000	1,000	1,000	1,000	1,000	—	—	—	—	—
True-LVDS Channels (Receive / Transmit)	44 / 44	66 / 66	78 / 78	80 / 80	80 / 80	80 / 80	80 / 80	22 / 22	22 / 22	39 / 39	39 / 39	39 / 39	45 / 45	45 / 45	—	—	—	—	—
Medium-Speed LVDS Maximum Data Rate (Mbps)	—	—	—	462	462	462	462	—	—	—	—	—	—	—	640	640	640	640	640
Medium-Speed LVDS Channels (Receive / Transmit)	—	—	—	2 / 2	10 / 10	36 / 36	56 / 72	—	—	—	—	—	—	—	34	129	72	103	129
RSDS Maximum Data Rate (Mbps)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	311	311	311	311	311
Transceiver (SERDES) Maximum Data Rate (Gbps)	—	—	—	—	—	—	—	3.1875	3.1875	3.1875	3.1875	3.1875	3.1875	3.1875	—	—	—	—	—
Transceiver (SERDES) Channels	—	—	—	—	—	—	—	4	4	8	8	16	8	20	—	—	—	—	—
Embedded Dynamic Phase Alignment (DPA)	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—
Series & Differential On-Chip Termination	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	—	—	—	—	—
Programmable Drive Strength	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes: ¹K=1,000; ²Kbit=1,024 bits

Altera FPGA Matrix: Production Devices

Device Available Now in Commercial (0 to 85° C) & Industrial (-40 to 100° C) Temperatures.

Device Available Now in Commercial Temperature; Contact Altera for Industrial Temperature.

Vertical Migration (Same V_{CC}, GND, ISP & Input Pins)

	Stratix® (1.5 V) High Density, High Performance						Stratix GX (1.5 V) 3.125-Gbps Transceivers						Cyclone™ (1.5 V) Low Cost, High Volume						
	EP1S10	EP1S20	EP1S25	EP1S30	EP1S40	EP1S60	EP1S80	EP1SGX10C	EP1SGX10D	EP1SGX25C	EP1SGX25D	EP1SGX25F	EP1SGX40D	EP1SGX40G	EP1C3	EP1C4	EP1C6	EP1C12	EP1C20
Thin-Quad Flat Pack (T)																			
Plastic Quad Flat Pack (Q)																			
Ball-Grid Array (B)																			
FineLine BGA® (F)																			
	100-Pin TQFP																		
	144-Pin TQFP																		
	240-Pin PQFP																		
	672-Pin BGA	345	426	473															
	956-Pin BGA				683	683	683												
	256-Pin FBGA																		
	324-Pin FBGA																		
	400-Pin FBGA																		
	484-Pin FBGA	335	361																
	672-Pin FBGA (Wirebond)	345	426	473															
	672-Pin FBGA (FlipChip)																		
	780-Pin FBGA	426	586	597	597	615													
	1,020-Pin FBGA			706	726	773	773												
	1,508-Pin FBGA					822	1,022												

Note: Lead-free devices are offered in all device/package combinations except for the 672-pin and 956-pin BGA packages.

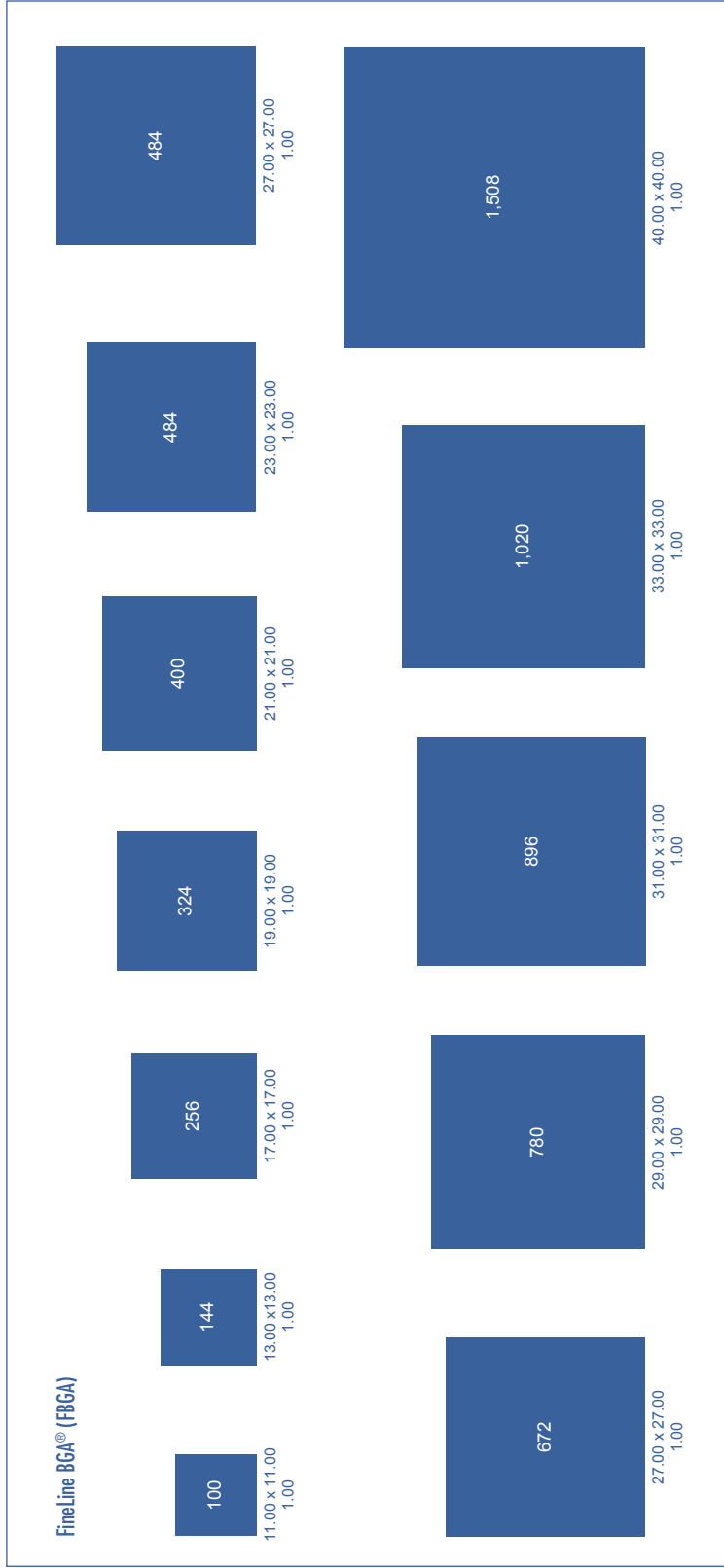
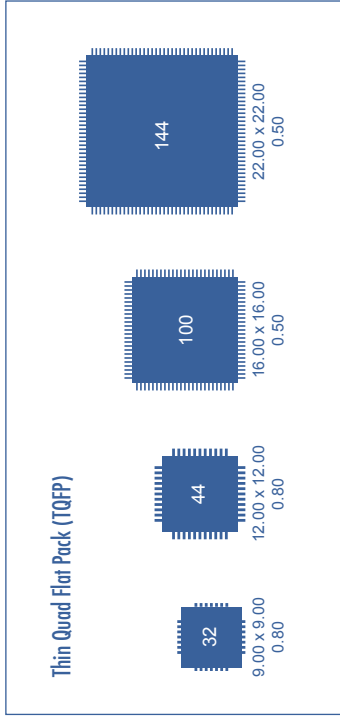
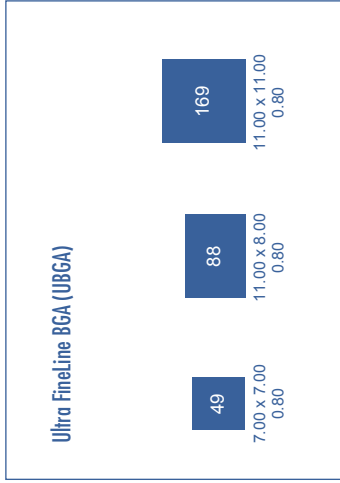
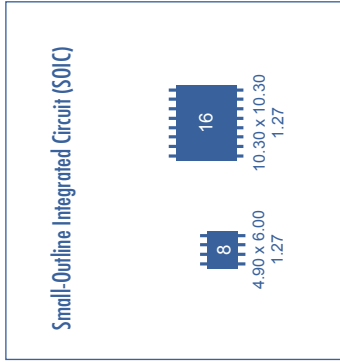
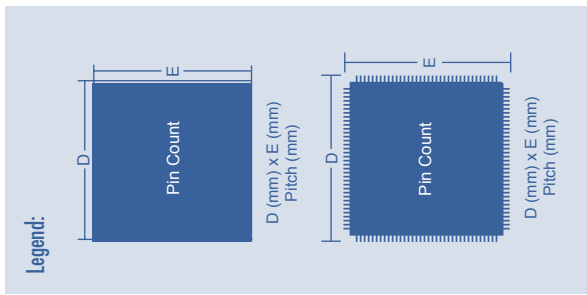
Package Statistics	TQFP		PQFP		BGA		FBGA					
	Wirebond	FlipChip	Wirebond	FlipChip	Wirebond	FlipChip	Wirebond	FlipChip	Wirebond	FlipChip	FlipChip	
Number of Pins	100	144	240	956	256	324	400	484	672	780	1,020	1,508
Package Technology	Wirebond	Wirebond	Wirebond	FlipChip	Wirebond	Wirebond	Wirebond	FlipChip	Wirebond	FlipChip	FlipChip	FlipChip
Nominal Length x Width (mm)	16x16	22x22	34.6x34.6	40x40	17x17	19x19	21x21	23x23	27x27	29x29	33x33	40x40
Maximum Surface Area (mm ²)	262	493	1,215	1,616	296	369	449	538	740	853	1,102	1,616
Maximum Height (mm)	1.20	1.60	4.10	3.50	2.60	2.60	2.60	3.50	2.60	3.50	3.50	3.50
Nominal Lead Pitch (mm)	0.50	0.50	0.50	1.27	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Maximum Lead Width (mm)	0.27	0.27	0.27	0.90	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70

	Configuration Devices					
	EPIC2	EPIC4	EPIC8	EPIC16	EPIC31	EPIC34
8-Pin SOIC						
20-Pin PLCC	✓					
32-Pin TQFP	✓					
88-Pin UBGA*				✓		
100-Pin PQFP				✓		
Reprogrammable	✓	✓	✓	✓	✓	✓
Data Compression		✓	✓	✓	✓	✓
Page Mode		✓	✓	✓	✓	✓

* UBGA: Ultra FineLine BGA

Features	MAX II 3.3 V, 2.5 V, 1.8 V		MAX 3000A 3.3 V				MAX 7000B 2.5 V				MAX 7000AE 3.3 V				MAX 7000S 5.0 V									
	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05	Now	Q2 '05				
User Flash Memory (Kbit)																								
Boundary Scan JTAG		8																						
JTAG In-System Programmability (ISP)		✓																						
Fast Input Registers		✓																						
Programmable Register Power-Up		✓																						
Programmable Ground Pins		✓																						
Open-Drain Outputs		✓																						
Programmable Pull-Up Resistors		✓																						
Bus Hold		✓																						
JTAG Translator		✓																						
Real-Time ISP		✓																						
Core Voltage (V)		1.8																						
MultiVolt™ Core (V)		3.3, 2.5, 1.8																						
MultiVolt I/O (V)		3.3, 2.5, 1.8, 1.5																						
I/O Power Banks		2, 2, 4, 4																						
Maximum I/O Pins		80, 160, 212, 272																						
Maximum Output Enables		80, 160, 212, 272																						
TTL (5.0-V Tolerance)		-																						
LVTTL/LVCMOS		✓																						
32-bit, 33-MHz PCI Compliant		-																						
GTL+/SSTL-2, SSTL-3, All Class I & II		-																						
Schmitt Triggers		✓																						
Programmable Slew Rate		✓																						
Programmable Drive Strength		✓																						

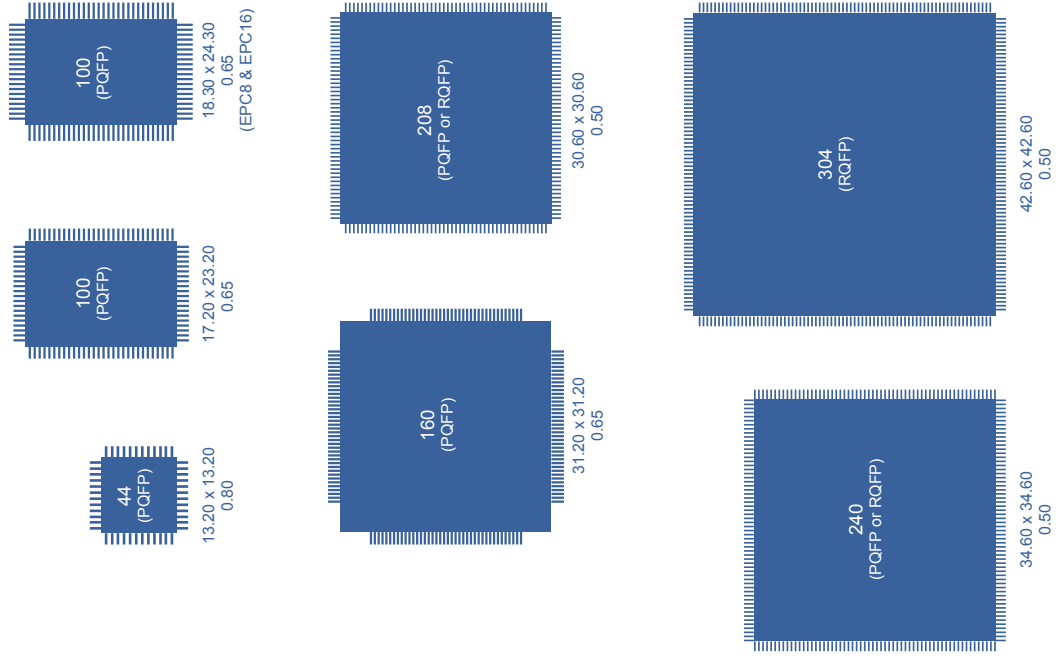
¹An external series resistor must be used for 5.0-V tolerance.



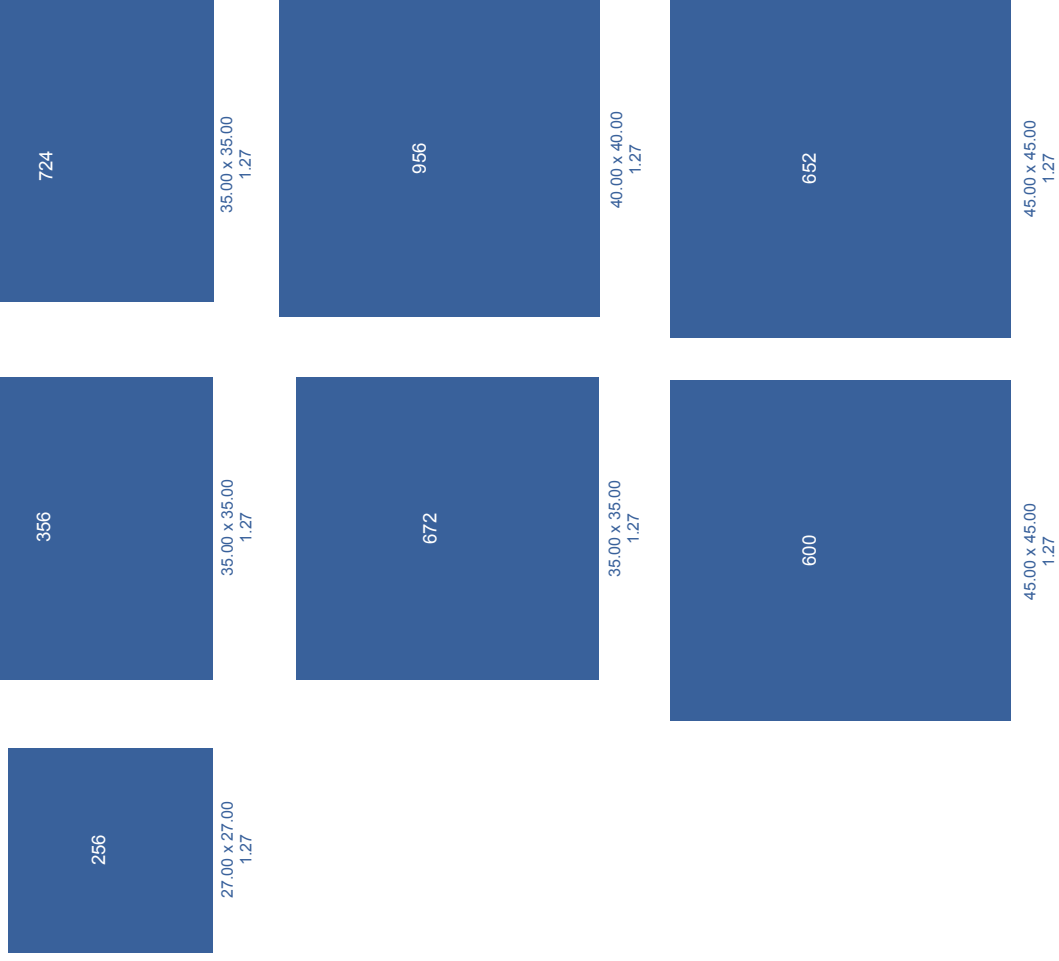
Note: Outermost dimensions are "D" and "E" for both array and peripheral package families.

Altera Packaging Dimensions

Plastic Quad Flat Pack (PQFP) Power Quad Flat Pack (PQFP)



Ball-Grid Array (BGA)



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