The Altera Advantage News & Views

Newsletter for Altera Customers ◆ Third Quarter ◆ August 1996

ClockLock & ClockBoost Circuitry for High-Density PLDs

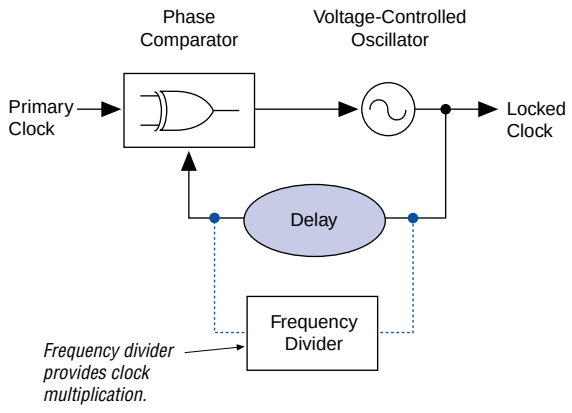
Altera is introducing two new options for high-density programmable logic devices (PLDs). The ClockLock feature uses a phase-locked loop (PLL) to minimize clock delay and skew within a device, significantly increasing performance. The ClockBoost feature can increase clock frequencies by as much as four times the incoming clock rate, improving system performance. Combined, these enhancements provide significant breakthroughs in system performance and bandwidth. See Figure1.

Faster System Performance

As PLDs increase in density, clock delay and skew have a greater impact on performance. Historically, to shield designers from the effects of clock skew, critical parameters such as setup and clock-to-output delays (t_{SU} and t_{CO}) were padded. In contrast, the ClockLock circuitry uses a PLL to synchronize clock lines, thereby minimizing clock delay and skew. With the easy-to-use ClockLock feature, Altera can reduce the clock delay and skew in programmable logic specifications, significantly improving performance. For example, by using the ClockLock circuitry in an EPF10K100GL503-3DX device, designers are likely to see a worst-case t_{SU} and t_{CO} of 7 ns and 3.6 ns, respectively, increasing the expected system performance by more than 60%. This performance increase will help designers meet the high-speed bus interface requirements of the future. See Figure 2 on page 3.

Figure 1. Phase-Locked Loops (PLLs)

A PLL maintains a phase delay between an input clock and an internal oscillator. Dividing the feedback signal can provide clock multiplication.



Increased System Bandwidth & Reduced Area

The ClockBoost circuitry enables clock multiplication in Altera devices. Popularly used in microprocessors, clock multiplier circuits allow an external clock frequency to be "multiplied" inside the device. With the ClockBoost feature, designers have access to both a clock doubling option and clock frequencies that can be tripled and quadrupled in some Altera devices. See Figure 3 on page 3. ClockBoost allows designers to run the internal logic of the device up to four times faster than the input clock frequency. This option can be useful in digital signal processing (DSP) designs and data compression algorithms, where complex data manipulation is performed at very high speeds.

Through a technique called time-domain multiplexing, the ClockBoost feature allows the designer to enhance device area efficiency via resource sharing within the device. For example, a design that requires a

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32-bit data path function running at 40 MHz can be implemented with a 16-bit data path function running internally at 80 MHz, achieving the same functionality with nearly half the logic resources and I/O requirements.

Software Support

Software support of both the ClockLock and ClockBoost features is planned for MAX+PLUS II version 7.0. To enable the ClockLock or ClockBoost circuitry, designers will use a parameterized function (named `CLKLOCK` in MAX+PLUS II) that permits specifications for input frequency and frequency multiplication factors. After design compilation, the designer can use the MAX+PLUS II software for functional and timing simulation as well as timing analysis. EDA support for the ClockLock and ClockBoost circuitry—through Verilog HDL and VHDL models—will also be available with MAX+PLUS II version 7.0.

Availability

Initially, the ClockLock and ClockBoost features will be available for FLEX 10K devices only. The EPF10K100 will be the first device to incorporate these options (planned for release in September 1996), followed by additional FLEX 10K devices. MAX 7000S devices will be introduced with the ClockLock feature in 1997.

Figure 2. ClockLock Feature

The ClockLock feature improves clock-to-output times by 33% because clock delay and skew are eliminated.

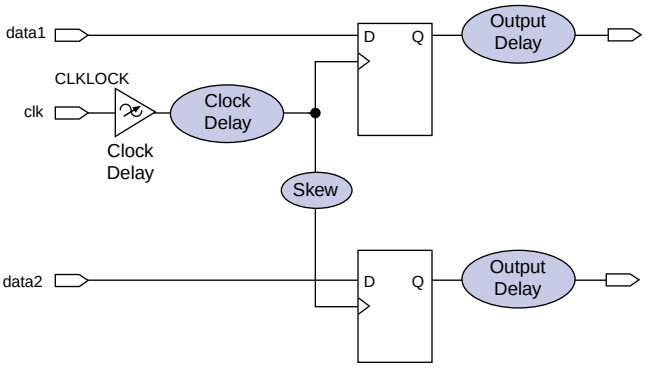
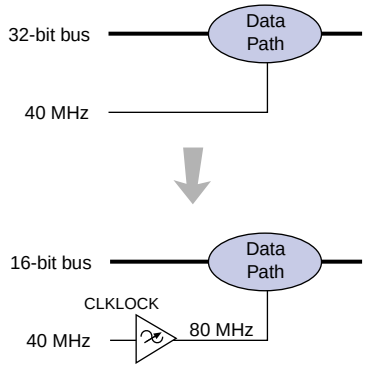


Figure 3. ClockBoost Feature

A clock multiplier increases the bandwidth of the data path without increasing the board-level clock speed.



Introducing the ByteBlaster Download Cable

Designers who require the fastest performance during in-system programming can use the newest Altera programming hardware, called the ByteBlaster. The ByteBlaster connects to a standard 25-pin parallel port on PCs and downloads programming or configuration data directly to the target device. The ByteBlaster is fully compatible with existing printed circuit boards that use the BitBlaster for device programming.

The ByteBlaster programs MAX9000 and MAX 7000 devices and configures FLEX 10K and FLEX 8000 devices. You can also use the ByteBlaster with the PLDshell Plus software to program or configure FLASHlogic devices. The following table compares the features of the ByteBlaster and BitBlaster. For more information on the ByteBlaster, refer to the *ByteBlaster Download Cable Data Sheet*.

ByteBlaster & BitBlaster Comparison

Feature	ByteBlaster	BitBlaster
Platforms supported	PC	PC and workstation
In-system programming time (for EPM7128S)	~5 seconds	~20 seconds
In-circuit reconfiguration time	Fast	Fast
Data port	25-pin parallel port	RS-232 serial port

Devices & TOOLS

FLEX 10K

Altera Improves FLEX 10K Performance

Altera has improved the performance of FLEX 10K devices. Devices in a -3 speed grade are now available, and devices in -4 speed grades contain performance improvements. The FLEX10K device family leads the industry in density, with devices densities up to 100,000 gates. With the new performance enhancements, FLEX 10K devices also offer speed leadership similar to FLEX8000A devices.

Altera used the following methodology to demonstrate the high-performance characteristics of the FLEX 10K family:

1. Selected nine circuits that represent typical programmable logic device (PLD) designs.
2. Implemented the circuits until the device was filled.
3. Determined the performance with the MAX+PLUSII software.

The test results are shown in the table "Performance Characteristics for FLEX 10K Devices" below.

EPF10K30 Ships in 240-Pin RQFP Package

Altera is now shipping the EPF10K30 device in 240-pin power quad flat pack (RQFP) packages. The EPF10K30 embedded array—which contains 12,288 bits of memory—can be used to implement on-chip RAM or complex logic functions without affecting resource utilization or logic array speed.

FLEX 10K -3 Speed Grade Device Availability

EPF10K10, EPF10K30, and EPF10K100 devices are available today in -3 speed grades. EPF10K50 and EPF10K20 devices in -3 speed grades are scheduled for the fourth quarter of 1996. The EPF10K40 and EPF10K70 are scheduled for the first quarter of 1997. Contact your local Altera representative for information on pricing, or for further information on the FLEX 10K family. The following table summarizes device availability for FLEX10K devices in the -3 speed grade.

FLEX 10K Device -3 Speed Grade Availability

Device	Availability
EPF10K10	Now
EPF10K20	October 1996
EPF10K30	Now
EPF10K40	Q4 1996
EPF10K50	Now
EPF10K70	Q1 1997
EPF10K100	Now

New EPF10K10 Packages

The EPF10K10 will be available in 84-pin plastic J-lead chip carrier (PLCC) and 144-pin thin quad flat pack (TQFP) packages later this year. For pricing information, contact Altera Customer Marketing.

Performance Characteristics for FLEX 10K Devices

Logic Benchmark	Performance for -3 Speed Grade Devices (MHz)						
	EPF10K10	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70	EPF10K100
Data path	131	156	143	141	135	125	117
Timer	73	70	66	66	64	63	62
State	85	84	79	78	72	69	67
Large state machine	46	47	42	41	33	36	33
Arithmetic circuit	39	39	38	37	36	35	34
16-bit accumulator	82	78	79	79	78	77	76
16-bit counter	104	103	104	104	103	103	104
Pre-scaled counter	263	215	207	204	165	174	159
Memory map	54	53	50	48	47	45	44
Average performance	**97**	**94**	**90**	**89**	**81**	**81**	**77**

FLEX 8000

Altera Introduces First 144-pin TQFP Package

The EPF8820A is the first Altera device offered in a 144-pin TQFP package. With 8,000 usable gates and 104 I/O pins, the EPF8820ATC144 can support PCMCIA designs requiring higher density or more I/O pins than are available with the EPF8282A or EPF8452A devices in 100-pin TQFP packages. The compact TQFP package is an ideal solution for tight board designs that cannot accommodate a 160-pin QFP package. Initial quantities of the EPF8820A in A-4, A-3, and A-2 speed grades will be available in early October. Production volumes will be available later this year.

New Industrial-Temperature FLEX 8000 Devices

The following industrial-temperature devices were recently added to the FLEX 8000 family. All of the devices are offered in the A-3 speed grade, providing 95-MHz, 16-bit counter performance.

New Industrial-Temperature FLEX 8000 Devices

Device	Usable Gates	Package
EPF8282ATI100-3	2,500	100-pin TQFP
EPF8452AQI160-3	4,000	160-pin PQFP
EPF81188AQI208-3	12,000	208-pin PQFP
EPF81500ARI240-3	16,000	240-pin RQFP

FLEX 8000 Prices Reduced up to 55%

Maintaining leadership as the industry's most cost-effective programmable logic family, Altera has reduced the price of FLEX 8000 devices up to 55%. The new 100-unit pricing is listed below.

Examples of Reduced FLEX 8000 Pricing

Part Number	Old 100-Unit Price	New 100-Unit Price *(1)*	Percent Decrease
EPF8282ALC84-4	$17.50	$11.00	35%
EPF8452ALC84-4	$38.00	$17.00	55%
EPF8636ALC84-4	$58.00	$25.00	55%
EPF8820AQC160-4	$75.00	$37.00	50%
EPF81188AQC208-4	$89.00	$55.00	35%
EPF81500ARC240-4	$149.00	$79.00	45%

Note:
(1) Price in U.S. dollars for OEM direct orders and suggested resale.

The metal-intensive architecture of the FLEX 8000 family utilizes a 0.5-micron, triple-layer metal SRAM process to provide the high-performance and low-cost required in today's low-end ASIC designs.

MAX 9000

EPM9560 Available in 208-pin RQFP Package

The EPM9560 device will be available in 208-pin RQFP packages in the third quarter of 1996. The 208-pin RQFP package is a replacement for the existing 208-pin ceramic quad flat pack (CQFP) package. EPM9560 devices in 208-pin RQFP packages are form, fit, and functionally equivalent to EPM9560 devices in 208-pin CQFP packages.

Pricing for EPM9560 devices in 208-pin CQFP packages will be the same as EPM9560 devices in RQFP packages. The ordering codes affected by the package substitution are shown below.

MAX 9000 Ordering Code Changes

Existing Ordering Code	New Ordering Code
EPM9560WC208-20	EPM9560RC208-20
EPM9560WC208-15	EPM9560RC208-15
EPM9560WC208-20C	EPM9560RC208-20C
EPM9560WC208-15C	EPM9560RC208-15C

EPM9560 Prices Reduced by 10%

On July 1, Altera reduced the cost of selected speed grades of the EPM9560 device by 10%. These price reductions reflect the continuous improvement made possible by increased sales volume.

MAX 7000

MAX 7000S Availability

Altera is now shipping production quantities of the EPM7192S device. Additional MAX 7000S devices are available as engineering samples and can be obtained from your local Altera sales representative. MAX 7000S device availability is shown below. Contact your local Altera sales representative for release dates for other MAX 7000S devices.

MAX 7000S Device Availability

Device	Engineering Samples	Production Availability
EPM7256S	Now	Q4 1996
EPM7192S	–	Now
EPM7128S	Now	October 1996
EPM7064S	Now	Q1 1997

EPM7192S Now Shipping

Production quantities of the EPM7192S device in 160-pin plastic quad flat pack (PQFP) packages are

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EPM7192S Ships
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now shipping. The EPM7192S is available in both 10-ns and 15-ns speed grades for an introductory 100-unit price of $115.00 and $82.00, respectively. The EPM7192S, like all MAX 7000S devices, supports in-system programmability (ISP) through the industry-standard JTAG test ports. Additionally, the device has an open-drain output option and is pin- and programming file-compatible with the EPM7192 and EPM7192E devices.

MAX 5000 & Classic

Exchange Your MAX 5000 Programming Adapter for Free

Altera has qualified a 0.65-micron EPROM process for MAX 5000 devices and is migrating existing 0.8-micron MAX 5000 devices to a 0.65-micron process. This change will facilitate long-term support for the MAX5000 family.

This migration will not change MAX 5000 ordering codes or the MAX 5000 timing parameters shown in the *MAX 5000 Programmable Logic Device Family Data Sheet*. However, new programming adapters are required to program the 0.65-micron devices.

Altera will exchange existing EPM5032, EPM5064, and EPM5130 programming adapters for new adapters *for free*. These new adapters are backwards-compatible and support all existing die revisions. The table below lists the existing adapters that can be exchanged for new adapters. Altera has already completed an exchange program for EPM5128 and EPM5192 programming adapters.

Contact Altera's Customer Service Department or your local Altera sales representative for more information.

MAX 5000 Replacement Adapters

Existing Adapter	New Adapter
PLED5032	PLMD5032A
PLMD5032	PLMD5032A
PLEJ5032	PLMJ5032A
PLM5032	PLMJ5032A
PLES5032	PLMS5032A
PLEJ5064	PLMJ5064A
PLMJ5064	PLMJ5064A
PLEG5130	PLMG5130A
PLEJ5130	PLMJ5130A
PLMJ5130	PLMJ5130A
PLEQ5130	PLMQ5130A
PLMQ5130	PLMQ5130A

Product Transitions

Altera is migrating existing MAX 5000 and Classic devices from a 0.8-micron process to a 0.65-micron process. To evaluate or qualify devices manufactured on the new process, obtain an evaluation packet (containing device samples, data sheets, process change notices, and reliability data) from a local Altera sales representative. Altera recommends verifying that your third-party programming hardware vendor has modified its programmers for devices that have migrated to the new 0.65-micron process. The table below outlines the migration schedule:

Product Migration Schedule

Description *(1)*	Reference	Device	Date
MAX 5000 devices fabricated on a 0.65-micron process *Note (2)*	PCN 9407 ADV 9515 ADV 9606	EPM5032	Q1 1997
		EPM5064	Q2 1997
		EPM5128	Complete
		EPM5130	May 1, 1997
		EPM5192	October 1, 1996
Classic devices fabricated on a 0.65-micron process	PCN 9510 ADV 9607	EP6*xx*	Complete
		EP9*xx*	September 1, 1996
		EP18*xx*	March 1, 1997

Notes:

(1) This process transition will not result in any changes to data sheet parameters or ordering codes.

(2) Devices containing the new die must be programmed with new programming adapters. For information on how to obtain the adapters, see "Exchange Your MAX 5000 Programming Adapter for Free" on this page.

MAX+PLUS II

MAX+PLUS II Version 7.0 Available in September

MAX+PLUS II version 7.0 will be available in late September. In addition to support for new FLEX 10K, FLEX 8000, MAX 9000, and MAX 7000S devices and packages, this version will provide support for Altera's ClockLock and ClockBoost features, which are currently available in EPF10K100 devices.

MAX+PLUS II version 7.0 will also contain improved interfaces to EDA tools. Specifically, the timing models used by Synopsys for performance prediction will be improved to generate more accurate results. In addition, the release will support the Mentor Graphics QuickVHDL simulator.

MAX+PLUS II version 7.0 can maximize your design efficiency. For pricing information or for details on software maintenance agreements, contact your local Altera representative.

Discontinued Devices

In recent months, Altera has announced that various products will be discontinued (see the table below). Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera sales representative. Selected ADVs and PDNs are also available on Altera's world-wide web site at **http://www.altera.com**. Rochester Electronics, an after-market supplier, offers support for many discontinued Altera products. Contact Rochester Electronics at (508)462-9332 for more information.

Discontinued Device Ordering Codes

Device Family	Device	Last Order Date	Last Shipment Date	Reference
FLEX 8000	Military products (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513 PDN 9517
MAX 7000	Military products (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513
FLASHlogic	EPX780 (all packages, temperature grades, and speed grades)	6/28/96	9/30/96	PDN 9601
	EPX740 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
MAX 5000	Military EPM5130W device	10/31/96	12/31/96	PDN 9513
	Selected MAX 5000 ordering codes	9/30/96	12/31/96	ADV 9609
	EPM5016 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
Classic	EP22V10, EP22V10E, EP310I, EP320I (all packages, temperature grades, and speed grades)	6/28/96	9/30/96	PDN 9516 PDN 9511
	Military products (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513
	EP220, EP224, EP312, EP324 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
	Selected EP6*xx* ordering codes	6/28/96	9/30/96	ADV 9518
	Selected EP9*xx* ordering codes	9/30/96	12/31/96	ADV 9608
	Selected EP18*xx* ordering codes	3/31/97	6/30/97	ADV 9608
Function-Specific	EPS448, EPC1213 military (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513 PDN 9517
	EPS448, EPS464 (all commercial and industrial temperature grades; military devices have earlier last order and last shipment dates)	3/31/97	9/30/97	PDN 9516

New Altera Publications

New Altera publications are available from Altera Literature Services, Altera Express, and the Altera world-wide web site. Document part numbers are shown in italics.

- **1996 Data Book** ***A-DB-0696-01***
  Provides comprehensive information about Altera's FLEX 10K, FLEX 8000, Configuration EPROM, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic device families as well as MAX+PLUS II development tools. The ***1996 Data Book*** also includes information on device operation, product reliability, device timing models, and package outlines.
- **AMPP Catalog** ***M-CAT-AMPP-01***
  Provides an introduction to the Altera Megafunction Partners Program (AMPP), a description of each AMPP megafunction, and a listing of corporation profiles and contact information for each AMPP partner.
- **Gate Array-to-Programmable Logic Conversion Kit User Guide** ***A-UG-GARP-01***
  Describes how to use the Gate Array-to-Programmable Logic Conversion Kit, including supported technologies, design flow, Library Mapping Files, design guidelines, installation, and MAX+PLUS II design processing.
- **FLEX 10K Embedded Programmable Logic Family Data Sheet Supplement, version 1.2** ***A-DSS-F10K-1.2***
  Provides updated timing parameters for the FLEX10K family.

Technical ARTICLES

Building Complex Logic with FLEX 10K EABs

Altera's FLEX 10K devices are the first programmable logic devices (PLDs) to contain embedded arrays, which allow designers to quickly create, prototype, and debug complex designs with as many as 100,000 gates. Unlike embedded functions in a gate array, the FLEX10K embedded array is fully programmable, giving the designer complete control over the functions programmed in the embedded array. The FLEX 10K embedded array is composed of a series of embedded array blocks (EABs), which can be used to implement both memory and complex logic functions. EABs can also be reconfigured on-the-fly, allowing designers to modify a portion of a design without disturbing the operation of the rest of the device.

This article provides two examples of how to implement complex logic functions in FLEX 10K EABs. However, many other functions can be implemented in the embedded array, including:

- Multipliers
- Constant multipliers/vector scalars
- Digital filters
- Two-dimensional convolvers
- State machines
- Transcendental functions
- Waveform generators
- 8 bit-to-10 bit encoders
- On-the-fly reconfigurable functions

For more detailed information on these applications, refer to *Product Information Bulletin 21 (Implementing Logic with the Embedded Array in FLEX 10K Devices).*

Implementing Logic in an EAB

Each EAB is a flexible block of RAM with optional input and output registers. An EAB can assume any of the following sizes with no speed penalty: 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1 bits.

Logic functions are implemented by programming the EAB during configuration with a read-only pattern, creating a large look-up table (LUT). The pattern can be reconfigured during device operation to change the logic function. The LUT contains the results of the functions rather than using algorithms to calculate them.

Example 1: Trancendental Functions & Waveform Generators

The EAB can be used to generate waveforms that repeat over time (e.g., sine waves). The waveform generator is implemented with a counter that drives the address input of the EAB, and the waveform output appears on the output of the EAB. Because an EAB can be up to 8 bits wide, 1 EAB can simultaneously generate 8 waveforms. Multiple EABs can be cascaded to generate additional waveforms. The waveform can be irregular within its period because it is created with a LUT. This example describes how to generate a sine wave using an EAB.

Transcendental functions—such as sine, cosine, and logarithms—are non-linear, so they are difficult to compute using algorithms. It is more efficient to implement transcendental functions by looking up the results in large LUTs, which can be implemented with EABs.

When using an EAB to implement a transcendental function, the input drives the address input of the EAB, and the output appears at the data output. Each address location in the EAB stores the result of its input (e.g., the result of the function implemented with input=10 is stored in address location 10).

Rather than duplicating entries for $+n$ and $-n$ in symmetric functions (e.g., $\cos(+n) = \cos(-n)$, and $\sin(+n) = -\sin(-n)$), transcendental functions use the sign bit to determine whether the output should be inverted. To compute the sine function, for example, the EAB stores the values for one quadrant of the function. Based on the value of the input, the logic element (LE) computes the results for the other quadrants by determining whether the inputs or outputs of the EAB should be inverted. Figure 1 shows how the values for one quadrant of the sine function can repeat for the rest of the function.

Computing transcendental functions with an EAB produces a high-resolution result, where resolution is the minimum change in input to change in output. An EAB produces high-resolution results because it can implement functions with high numbers of inputs, whereas LEs cannot easily implement such complex functions. The more entries that can be stored in the EAB, the higher the resolution. One EAB can store 256 8-bit entries. Therefore, an EAB used to calculate a symmetric function effectively has 1,024 8-bit entries because symmetric functions can use each entry in the EAB 4 times, once for each quadrant of the function. For example, computing a sine wave with an EAB produces a resolution of 0.35°.

To increase the precision and resolution on the output of the transcendental function, multiple EABs are used. To increase the precision, one EAB can look up the eight most significant bits (MSBs) while another EAB looks up the eight least significant bits (LSBs) of the result. To increase resolution, two EABs can be used to emulate a 512 × 8 ROM, which provides 2,048 8-bit entries and a resolution of 0.18°.

Figure 1. Computing the Sine Function

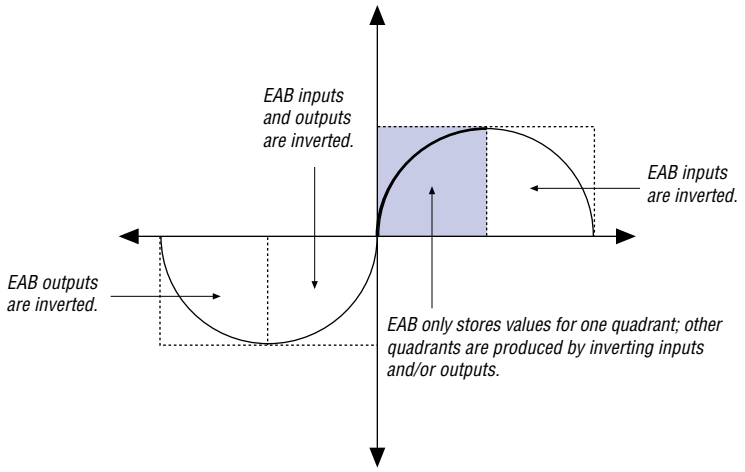
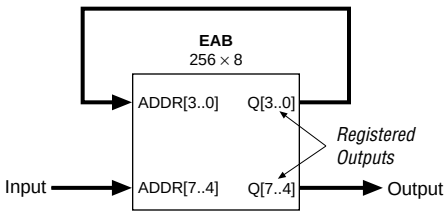


Figure 2. Implementing a Moore State Machine in an EAB



After a sine function has been implemented, the EAB can generate a sine wave. If a counter drives the input of the sine function, the output is a digitized sine wave. This digital output can be driven to a digital-to-analog converter. A sine wave can be used for various DSP functions.

Example 2: State Machines

The embedded array can be used to implement highly complex state machines. Generally, the more complex a state machine becomes (i.e., the more transitions it has), the more logic resources it requires. The number of EABs required to implement a state machine is a function of the number of states, inputs, and outputs of the state machine—regardless of complexity. Therefore, state machines with a different number of transitions but the same number of states, inputs, and outputs require the same number of EABs.

The address input to the EAB is a combination of bits representing the inputs to the state machine and the current state. For example, in a 16-state, 4-input, 4-output state machine, signals representing the 4 inputs to the state machine drive `ADDR[7..4]`, and signals representing the current state drive `ADDR[3..0]`. Each address input to the EAB contains two fields: the outputs for the current state and the state bits indicating the next state. A Moore state machine design uses the output registers of the EAB, whereas a Mealy state machine design uses LEs to register only the address bits representing the current state. Figure 2 shows the implementation of a 16-state, 4-input, 4-output Moore state machine.

The EAB can also be used to implement a sequencer, in which the state machine generates a sequence of signals. To implement a sequencer, a counter drives the address inputs of the EAB. The EAB defines the operation of the sequencer by storing the appropriate set of outputs for each count value. During operation, the outputs of the EAB are the outputs of the sequencer.

Figure 3 shows a state machine implemented in an EAB. The contents of the table control the behavior of the state machine. For example, in state 0 with state

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Using the EAB as RAM in VHDL Designs

FLEX 10K devices contain embedded array blocks (EABs) that can be configured as large blocks of RAM. You can use these EABs in a VHDL design with functions from the industry-standard library of parameterized modules (LPM). The MAX+PLUS II Compiler version 7.0 supports instantiation of LPM functions in VHDL, which allows you to implement RAM while preserving the architecture-independence of your design.

LPM functions are parameterized, i.e., you can quickly and easily change the size and/or the behavior of the RAM. The LPM functions have optional parameters that provide flexibility.

The following example shows how to instantiate the memory function `lpm_ram_dq` in a VHDL design. This example shows an instance of a RAM block with synchronous inputs and asynchronous outputs that is 4bits wide by 4 K (2^{12}) words deep. When you include the statements highlighted in blue, you do not have to declare the LPM function before using it.

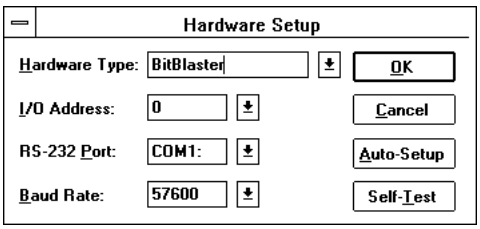
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
LIBRARY lpm;
USE lpm.lpm_components.ALL;

ENTITY ramexa IS
    PORT
    (
        inclock : IN STD_LOGIC;
        WE      : IN STD_LOGIC;
        datain  : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
        addr    : IN STD_LOGIC_VECTOR (11 DOWNTO 0);
        dout    : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
    );
END ramexa;

ARCHITECTURE a OF ramexa IS
BEGIN
    the_ram     : LPM_RAM_DQ
        GENERIC MAP (LPM_WIDTH => 4,
            LPM_WIDTHAD => 12, LPMOUTDATA =>
            UNREGISTERED, LPM_ADDRESS_CONTROL =>
            REGISTERED, LPM_INDATA => REGISTERED)
        PORT MAP (DATA => datain, inclock =>
            inclock, address => addr, WE => WE,
            Q => dout);
END a;
```

Troubleshooting Problems with ISP

You can program MAX 9000 and MAX 7000S devices in-system with MAX+PLUS II and the BitBlaster. The PC or workstation running MAX+PLUS II sends data to the BitBlaster via the serial port; in turn, the BitBlaster sends the data to the JTAG connector on your printed circuit board (PCB). The BitBlaster uses an EPM7064 device to perform data translation and to drive the four JTAG pins required for programming in-system (`TCK`, `TMS`, `TDI`, and `TDO`). The PCB supplies power to the BitBlaster; if power is applied correctly, the POWER status light will turn on.

Perform the following steps to program devices with the BitBlaster and MAX+PLUS II.

1. Choose **Programmer** (MAX+PLUS II menu).
2. Choose **Hardware Setup** (Options menu). The following dialog box appears:



3. For in-system programmability (ISP), use the following settings:

Hardware Type	BitBlaster
I/O Address	Not required for programming devices in-system with the BitBlaster.
RS-232 Port	Select the appropriate COM port for the BitBlaster.
Baud Rate	Select the baud rate that corresponds to the BitBlaster setting, or choose **Auto-Setup** to have MAX+PLUSII set the baud rate for you.

Serial ports share interrupts: COM1 shares with COM3 and COM2 shares with COM4. Therefore, if you have installed other hardware that uses COM1, selecting COM3 as the BitBlaster RS-232 port—or selecting COM2 when other hardware uses COM4—causes a conflict. To avoid conflicts, verify that other hardware is not using a port that shares interrupts with the BitBlaster.

For correct configuration using **Auto-Setup,** the RS-232 port settings must be correct and the BitBlaster must be powered from the your PCB.

After you have configured MAX+PLUS II and the BitBlaster, you can begin programming. If problems occur with the BitBlaster or the PCB (e.g., noise), MAX+PLUS II issues an error message. Use the following table to determine the possible cause for the message and the solution.

Programming Error Messages & Solutions

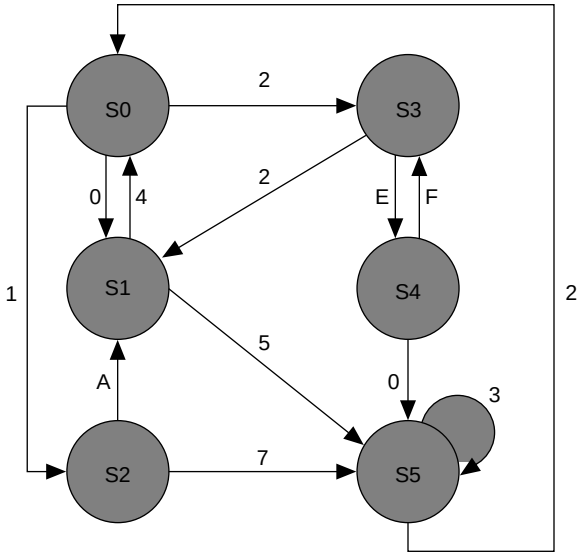
Error Message	Possible Cause	Solution
`Programming hardware is busy`	The BitBlaster is not receiving power.	Provide power to the BitBlaster through its 10-pin header on the PCB.
	There is an RS-232 port conflict.	Select a different COM port or disconnect any conflicting hardware.
	The baud rate selected in MAX+PLUS II does not match the BitBlaster setting.	Ensure that the baud rate in MAX+PLUS II matches the BitBlaster dipswitch setting. Use **Auto-Setup** to match the baud rates.
	The selected baud rate is not supported by the operating system.	The maximum baud rates supported are: Windows NT/95 115,200 Windows 3.11 57,600 Workstation 38,400
`Unrecognized device or socket is empty`	The `TDO` pin is stuck high or low.	Probe `TDO` to verify that signal levels are acceptable.
	The `TCK`, `TMS`, or `TDI` pins have noise.	Probe `TCK`, `TMS`, and `TDI` for valid signal levels and noise. If necessary, terminate `TCK`. Refer to *AN 75 (High-Speed Board Designs)* for more information.
`Device version is not enabled`	The device specified in the MAX+PLUS II Programmer does not match the device on the PCB.	In the Programmer, change the device to match the device on the PCB.
	Your version of MAX+PLUS II does not support the chosen device, or requires a password to program the device.	Use the latest version of MAX+PLUS II or obtain a password to program the device.
`Verify Error`	The `TDO` pin is stuck high or low.	Probe `TDO` to verify that signal levels are acceptable.
	The `TCK`, `TMS`, or `TDI` pins have noise.	Probe `TCK`, `TMS`, and `TDI` for valid signal levels and noise. If necessary, terminate `TCK`. Refer to *AN 75 (High-Speed Board Designs)* for more information.
	The `GOE` pin is not tied to VCC during programming.	Ensure that the `GOE` pin is held at VCC during programming.

Building Complex Logic with FLEX 10K EABs continued from page 9

machine inputs equal to 0, the state machine transitions to state 1; in state 1 with state machine inputs equal to 5, the state machine transitions to state 5. These transitions are indicated in Figure 3 as well as the first and fifth rows of the table below.

Figure 3. State Machine Inputs

State machine input and output values are shown in hexadecimal radix.



The values for each state in Figure 3 are shown in the following table.

State Machine Values

State	Inputs ADDR[7..4]	Current State ADDR[3..0]	Outputs Q[7..4]	Next State Q[3..0]
S0	0	0	0	1
S0	1	0	0	2
S0	2	0	1	3
S1	4	1	3	0
S1	5	1	4	5
S2	A	2	1	1
S2	7	2	A	5
S3	2	3	C	1
S3	E	3	7	4
S4	0	4	2	5
S4	F	4	F	3
S5	3	5	2	5
S5	2	5	4	0

The size of the state machine's required memory is calculated from its memory width and memory depth. Memory width is a function of the number of outputs and the number of states; memory depth is a function of the number of inputs and the number of states.

If the required memory space is too large to fit into one EAB, the MAX+PLUS II development software can cascade multiple EABs to create the required memory space.

Design Entry

Altera's MAX+PLUS II design software provides two methods of placing logic in an EAB. You can manually assign logic to one or more EABs by selecting a piece of logic and turning on the *Implement in EAB* option. This method provides maximum control over the design implementation. You can also direct MAX+PLUS II to automatically place logic into one or more EABs by turning on the *Automatic Implement in EAB* option in the **Global Project Logic Synthesis** dialog box (Assign menu). A variety of logic functions can also be implemented with Altera-provided macrofunctions.

Conclusion

FLEX 10K devices are the first PLDs to contain embedded arrays. The FLEX 10K embedded array, composed of a series of EABs, enables designers to implement complex logic functions in a single level of logic. Using EABs to implement logic functions results in higher device utilization and performance. The flexibility of an EAB makes it adaptable to a variety of specialized logic applications and combinatorial functions.

Altera VIEWPOINT

MegaCore Functions Complete the Picture

by Jack Ogawa
Development Tools Marketing Manager

The density and complexity of programmable logic devices (PLDs) and ASICs have outpaced improvements to the design process, widening the "design gap." Designers require the right tools to efficiently create designs for large devices. Specifically, design tools must address the following needs:

- *Design flow*—The design tools should be integrated, requiring minimal overhead and providing maximum flexibility.
- *Compilation performance*—Each design iteration should be completed as fast as possible.
- *Increased design abstraction*—When using high-density devices, designers often need to move away from explicit, gate-oriented design to high-level descriptions. Design abstraction requires a less verbose, more explicit description of logic, which permits more gates to be designed over a period of time. Consequently, high-level hardware description languages (HDLs) such as VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL) have become increasingly popular.

However, HDLs alone are not sufficient to bridge the design gap. For large designs to be practical, another level of abstraction at the design level is required. Large building blocks, such as megafunctions, provide this next level.

Altera Provides Value

Many functions are reusable. Designers usually associate these reusable functions with digital design building blocks, such as 74-series TTL functions. Over time, however, these reuseable functions have grown in complexity, far beyond the scope of 74-series functions. With large, complex megafunctions—such as peripheral component interconnect (PCI) interfaces, microprocessor peripherals, and microprocessors—the design process is faster and more efficient.

Because of the lack of commercially available megafunctions, some companies develop functions internally during the course of normal design activity, and provide these functions to other design engineers within the same company. However, other companies do not have the resources to develop megafunctions in-house. Altera addresses this need by providing the following functions:

- *MegaCore functions*—These Altera-provided functions are internally developed, fully tested, and supported by MAX+PLUS II as well as third-party EDA tools.
- *Altera Megafunction Partners Program (AMPP) functions*—AMPP partners are intellectual property (IP) vendors who develop, market, and support megafunctions. The partners target select, fully-tested functions for Altera devices, such as high-level system functions, which can be used for different architectures. AMPP functions are supported by MAX+PLUS II and third-party EDA tools.

MegaCore Functions & AMPP Functions

MegaCore functions and AMPP functions seemingly overlap because they address the same market. However, Altera chooses to develop megafunctions that complement Altera's core architectures; MegaCore functions focus on specific areas and can only be targeted for Altera devices. In contrast, the AMPP functions cover a broader range of functional areas, can be retargeted to a variety of architectures, and provide a migration path for the designer.

MegaCore Functions

Altera plans to offer MegaCore functions in two ways: in a kit comprised of related functions and as stand-alone functions. The first available functions will be:

- 8237 DMA controller
- 6402 UART
- 16450 UART
- 8251 UART

continued on page 19

Customer APPLICATION

Altera Delivers Speed for GigaNet ATM Protocol Engine

"We needed a single toolset that was well integrated with our Viewlogic WorkView Plus board-level simulator."
— David Follett
Project Architect

Industry:	*Communications*
End Product:	*Intel Paragon Supercomputer*
Design Application:	*ATM OC-12c Protocol Engine*
Altera Products:	*EPF81188A, EPM7032, EPM7128E, EPM7160E, EPM7192E, EPM7256E, MAX+PLUS II*

GigaNet develops high-performance ATM-based protocol engines that interface to supercomputers. The OC-12c Protocol Engine was designed for use in the Intel Paragon supercomputer to allow customers to communicate with ATM networks at OC-12c, OC-48, and OC-192 rates. Speed for this design was critical because the interface needed to run at OC-12c rates under worst-case conditions. The designers also wanted the flexibility to scale the design to OC-192 rates through parallel implementations.

GigaNet OC-12c Protocol Engine

Choosing a Programmable Logic Vendor

The GigaNet design team implemented much of the design in programmable logic to meet flexibility and time-to-market demands. They chose the specific devices based on speed and density requirements.

"We needed a register-intensive product for calculating TCP/IP checksums at 400MB per second (MBPS), and we needed a macrocell architecture to incorporate the wide state machines and deep pipelines of the higher-level protocol algorithms," says David Follett, the architect of the project.

In addition, having a single programmable logic vendor was essential because "we needed a single toolset that was well integrated with our Viewlogic WorkView Plus board-level simulator," says Follett.

Altera Provides the Answer

All programmable logic vendors were considered during the selection process, but Altera was the only supplier that met GigaNet's speed, density, and tool requirements. The final design incorporated 24 Altera devices using clock frequencies from 50 to 100 MHz.

"The FLEX 8000 architecture was ideal for implementing the fast checksum with its multiple high-speed adders. Implementing the ATM algorithm at our required speed was particularly tricky due to the large state machines, but MAX 7000 devices helped us meet the challenge," says Follett.

Benefits of Tool Integration

The GigaNet designers expected to use Altera's MAX+PLUS II software for chip design and some multi-chip functional simulation while using WorkView Plus to verify the larger blocks and the entire board. In the end, however, they used the MAX+PLUS II Simulator extensively for functional and timing simulation because it is so well integrated with the MAX+PLUSII design entry tools.

"The integration of the tools is the best I've seen," says Follett. "The timing simulator provided very accurate information that allowed us to modify the design and obtain our mandated speed."

The multi-chip simulation capability also allowed the GigaNet team to simulate one functional block with nine chips and verify both functionality and timing parameters. The timing information from MAX+PLUS II was then imported into WorkView Plus for board-level simulation.

A Winning Solution

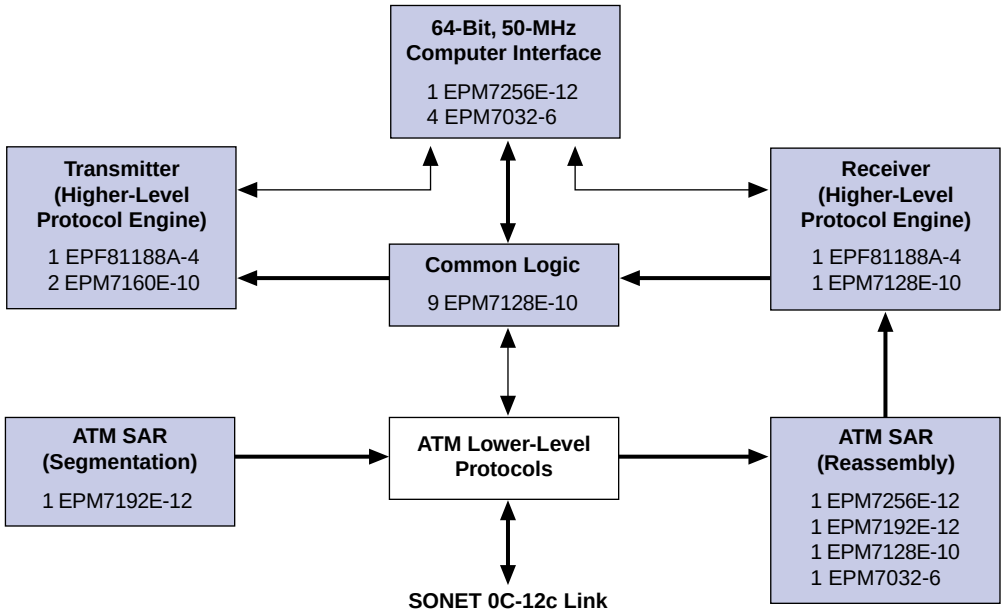
FLEX 8000 and MAX 7000 devices, together with MAX+PLUS II software, provided the winning solution for GigaNet.

"Altera was the only supplier that met our demand for high density, blazing speed, and well-integrated tools. And MAX+PLUS II enabled us to verify functionality, integrate many of the elements, and validate the aggressive speed requirements."

"The integration of the tools is the best I've seen," says Follett. "The timing simulator provided very accurate information that allowed us to modify the design and obtain our mandated speed."

GigaNet ATM OC-12c Protocol Engine

In the ATM OC-12c Protocol Engine, the transmit side processes the data received from the computer, segments it into 53-byte ATM cells, and sends it to the network link. The receiver then reassembles the ATM cells received from the network link, processes the data, and sends it on to the computer.



Questions & ANSWERS

Q The DSP Design Kit I received includes a CD-ROM, but I don't have a CD-ROM drive. How do I install the DSP Design Kit files?

A To install the reference designs on the DSP Design Kit CD-ROM, perform the following steps:

1. Insert the CD-ROM into a computer that does have a CD-ROM drive.
2. Insert a blank diskette into drive **a:**.
3. Type the following command at the DOS prompt:

```
c:\> copy <CD-ROM drive>:
   \pc\install.exe a:
```

4. Remove the first diskette and insert a second into drive **a:**.
5. Type the following command at the DOS prompt:

```
c:\> copy <CD-ROM drive>:
   \pc\install.w02 a:
```

You can then use the first diskette to begin installation of the DSP Design Kit files.

Q Which FLEX 10K device packages support 3.3-V I/O pins with a 5.0-V core?

A The following packages support 3.3-V I/O pins with a 5.0-V core.

- All FLEX 10K devices in pin-grid array (PGA) packages
- All ball-grid array (BGA) packages
- 208-pin plastic and power quad flat pack (PQFP and RQFP, respectively) packages
- 144-pin TQFP packages

FLEX 10K devices in 84-pin PLCC or 240-pin RQFP packages do not support this feature.

Q Which Altera programming adapter should I use to program an EPC1 Configuration EPROM in an 8-pin DIP or 20-pin PLCC package?

A You can use the PLMJ1213 programming adapter with the MPU to program all Configuration EPROMs in the 8-pin DIP or 20-pin PLCC packages, including the EPC1.

*Q I would like to assign a constant in my Graphic Design File (**.gdf**). How do I assign a constant in a GDF?*

A You can use the function `lpm_constant` from the library of parameterized modules (LPM) to make a constant value available in a schematic. This function has one output, which is the constant that you define. The constant value is defined as the parameter `LPM_CVALUE`; the width of the constant value is defined as the parameter `LPM_WIDTH`.

You can also use the `CONSTANT` primitive to specify a constant and its value used in a GDF.

Q How can I control the length of carry chains used in an LPM function such as `lpm_counter` or `lpm_add_sub`? For example, I have a 32-bit adder that I would like to implement as two 16-bit carry chains.

A You can control the length of carry chains implemented in LPM functions on a function-by-function basis by performing the following steps.

1. Select the function in the MAX+PLUS II Text Editor, Graphic Editor, or Hierarchy Display.
2. Choose **Logic Options** (Assign menu).
3. Choose **Individual Logic Options**. In the **Individual Logic Options** dialog box, select *Auto* in the *Carry Chain* drop-down menu box. Then, you can type a value in the *Max. Auto Length* box for the maximum carry chain length.

This adjustment will apply only to the selected function—not to all functions in the design.

Q How can I take advantage of the device-wide clear and device-wide output disable options in FLEX10K devices?

A In FLEX 10K devices, one pin has the ability to clear all registers or tri-state all pins on the device. To access these features, perform the following steps:

1. Select FLEX10K as the device family by choosing the **Device** command (Assign menu) and choosing *FLEX 10K* in the *Device Family* box.
2. Choose **Device Options** to open the **FLEX10K Individual Device Options** dialog box.

You can also set these features globally in the **FLEX10K Global Project Device Options** dialog box (Assign menu) after selecting FLEX 10K as the device family.

To use the device-wide clear option, turn on the *Enable Chip-Wide Reset* option. When this option is turned on, MAX+PLUS II adds a pin called `DEV_CLRn` to the design. When this pin is driven low, all registers on the device are cleared, as if the device had just powered up. MAX+PLUS II may print the following message during compilation: `Some registers may power-up at VCC.` Any registers that power-up at VCC are preset by the device-wide clear signal.

To use the device-wide output disable, turn on the *Enable Chip-Wide Output Enable* option in the **FLEX 10K Individual Device Options** dialog box. MAX+PLUS II will add a pin called `DEV_OE` to the design. When this pin is driven low, all pins on the device will be tri-stated. This option electrically removes the device from the circuit, which is useful for debugging a board without physically removing the device.

Q *When would I use the Altera **genmem** utility with a hardware description language (HDL) simulator and/or Synopsys tools for timing-driven synthesis?*

A The **genmem** utility produces a file that behaviorially describes a memory function (with extension **.v** for Verilog HDL or **.vhd** for VHDL). You can use this file in an HDL simulator to functionally verify the circuit. However, if you do not plan to use an HDL simulator, this file is not required.

The **genmem** utility also produces a file with the extension **.lib**, which contains timing information that the Synopsys tools use to synthesize a design with a timing constraint. This file should be added to the technology library for the Altera device you are using. However, if you are not using Synopsys tools for timing driven synthesis or if accurate timing information—using the **report_timing** command in Synopsys tools—is not necessary, then you do not need to add the **.lib** file to the technology library.

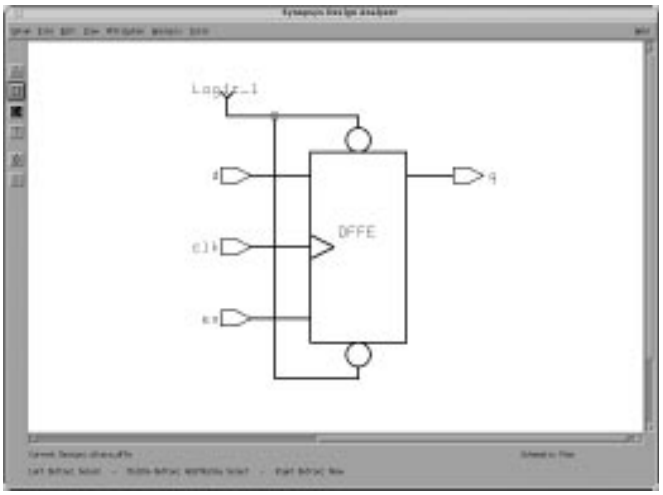
When you instantiate the behavioral description of the memory that **genmem** creates, you must use the same name that **genmem** assigns to the description. MAX+PLUS II uses the name to map the memory function to the appropriate LPM memory function. For example, **syn_ram_64x8_iror.v**, a Verilog HDL module, is mapped to `lpm_ram_dq` with parameters `LPM_NUMWORDS` = 64 and `LPM_WIDTH` = 8. In the file name, **iror** signifies that both inputs and outputs are registered.

Q *I am creating a design for a FLEX 10K device using Synopsys tools. How do I ensure that when I compile my design with the Synopsys Design Compiler, the* `DFFE` *primitives are correctly mapped to* `DFFE` *primitives in the FLEX 10K device?*

A For devices that contain `DFFE` primitives implemented in silicon (FLEX10K, MAX9000, and MAX7000 devices), you can add code in an HDL that synthesizes to `DFFE` primitives. For example:

```
always @ (posedge clock)
     IF(enable)
       q = d;
     ELSE
       q = q;
```

The primitives will map correctly as shown in the following figure.



Q *Are JTAG boundary-scan description language (BSDL) files available for Altera devices?*

A JTAG BSDL files are required to describe the JTAG circuitry within a device. Altera provides BSDL files for FLEX8000, MAX9000, MAX7000S, and FLASHlogic devices. You can download the self-extracting executable with JTAG BSDL files, called **jtagbsdl.exe**, from the Altera FTP site (**ftp.altera.com**) or the Altera BBS. BSDL files for FLEX 10K devices are under development.

Advantages of Hybrid I/O For Mixed-Voltage Systems

Hybrid I/O capability enables the device inputs and outputs to support the electrical requirements of both 5.0-V and 3.3-V devices. Because programmable logic devices often act as the "glue" that ties the various devices on a board together, high-performance programmable logic devices with hybrid I/O capability provide the ideal interface solution for mixed-voltage systems. The hybrid I/O capability of FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, and FLASHlogic devices makes these families an excellent choice for mixed-voltage interfacing. See Figure 1.

Most 5.0-V FPGAs Cannot Drive 3.3-V Devices

Because most 5.0-V field-programmable gate arrays (FPGAs) do not offer hybrid I/O, they may produce undesirable results when driving 3.3-V devices. Some FPGAs have true CMOS outputs with a high-level output voltage (V_{OH}) range of 3.86 V to 5.0V. However, the maximum high-level input voltage (V_{IH}) for any 3.3-V device is 3.6 V. Thus, the outputs of these FPGAs exceed the maximum V_{IH} specification. Providing an option for TTL outputs is not a foolproof solution because the V_{OH} may reach 3.7 V in TTL mode, violating the V_{IH} specification.

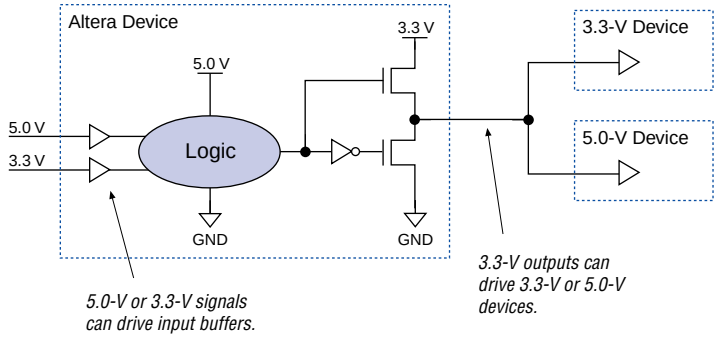
The most severe penalty for violating the V_{IH} specification is latch-up, which can destroy a 3.3-V device. Additionally, excess current can flow from the 5.0-V power supply to the 3.3-V power supply through the 5.0-V and 3.3-V devices, potentially raising the 3.3-V power bus to a higher level and damaging other 3.3-V devices connected to the bus. Finally, driving an input voltage higher than the specified value can adversely affect the long-term reliability of the device. See Figure2.

One solution when using FPGAs is to place a 150-Ω resistor between the two devices to minimize the current flow. While this patchwork solution may help limit the current, it cannot ensure reliable operation because the V_{IH} specification is still not met. Furthermore, placing extra resistors on the board is an inconvenient solution that can require the designer to change the board layout.

3.3-V FPGAs Are Not 5.0-V Tolerant

Although some FPGA vendors are promoting "pure" 3.3-V devices, customers designing mixed-voltage systems may run into problems with these devices because the inputs are not 5.0-V tolerant. Regardless of whether the driving 5.0-V device has a CMOS or an NMOS output, the maximum V_{OH} (5.0 V or 3.7 V, respectively) may exceed the maximum V_{IH} of 3.6 V for the device. Once again, the V_{IH} specification is violated, and consequently, this

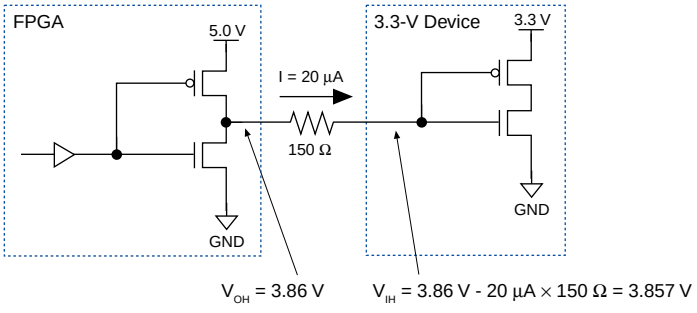
Figure 1. Altera Two-Way Mixed-Voltage Interfacing



configuration may have the same latch-up, current flow, and reliability issues as previously discussed. See Figure 3.

While Altera's current 3.3-V devices have similar limitations, the hybrid I/O capability of Altera 5.0-V devices offers the flexibility to interface with inputs and outputs of both 3.3-V and 5.0-V devices. Furthermore, future 3.3-V devices from Altera will offer 5.0-V tolerant inputs, making them suitable for mixed-voltage systems.

Figure 2. 5.0-V FPGAs with CMOS Output Cannot Drive 3.3-V Devices

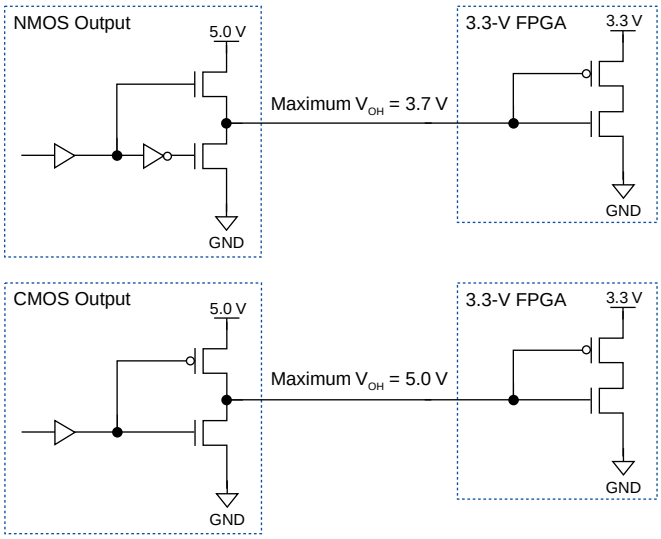


Altera Provides Mixed-Voltage Flexibility

Altera provides the broadest mixed-voltage product offering with the FLEX10K, FLEX 8000, MAX 9000, MAX 7000, and FLASHlogic device families. The inputs of these devices can easily accommodate both 3.3-V and 5.0-V signals, and the outputs of these devices can safely drive both 3.3-V and 5.0-V devices without violating the V_{IH} specification. Thus, this hybrid I/O capability provides a superior interface between 5.0-V and 3.3-V devices.

Figure 3. 3.3-V FPGAs Are Not 5.0-V Tolerant

V_{OH} for CMOS or NMOS outputs exceeds the maximum V_{IH} of 3.6 V.



MegaCore Functions Complete the Picture continued from page 13

- 6850 asynchronous communications interface adapter
- 8255 parallel I/O controller

These functions will be offered together as the Microperipheral MegaCore Library, priced at $7,995. Maintenance agreements are available, providing the designer with access to improvements and new library elements at no additional charge.

Conclusion

Altera MegaCore functions, in conjunction with AMPP functions, provide designers with a viable "make or buy" option for large, complex digital systems. This option is important for designers who want to use 100,000-gate PLDs, but who are faced with increasingly stringent time-to-market demands. Altera is committed to providing designers a complete solution for high-density programmable logic design and expanding the PLD design capability beyond 100,000 gates.

Now Available: VHDL-Synthesizable LPM Functions

Altera has provided synthesizeable VHDL models of functions from the library of parameterized modules (LPM). With the LPM, a designer can create architecture-independent designs without sacrificing silicon efficiency. The VHDL models of the LPM functions are available through the Electronic Design Interchange Format (EDIF) world-wide web site at **http://www.edif.org**.

LPM: A Powerful Tool

The industry-standard LPM contains 25 different functions—including adders, multipliers, and memory functions—that can be easily placed in a logic design and modified to expand in many dimensions. Designers can use the LPM to duplicate the functionality of other design libraries that contain hundreds of functions, which greatly simplifies design and debugging tasks.

The LPM allows designers to create architecture-independent designs while still maintaining silicon efficiency. Designers can specify the architecture-independent LPM functions in schematics or instantiate them in hardware description language (HDL) files. EDA software recognizes each LPM function and uses architecture-specific design techniques to create the most efficient design.

Altera Increases Effectiveness

Because a generic synthesizeable description of LPM functions was not previously available, the use of the LPM was limited to tools that supported LPM natively. With the VHDL models, EDA tools and silicon vendors that do not support the LPM can process a design containing LPM functions. Designers can use EDA tools to synthesize, optimize, and simulate designs implementing the behavioral descriptions.

The VHDL description of the `lpm_counter` function is shown below.

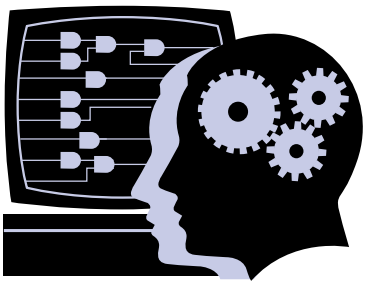
```
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE work.lpm_components.ALL;

ENTITY count4 IS
   PORT   (
      data : IN STD_LOGIC_VECTOR
         (3 DOWNTO 0);
      clock  : IN STD_LOGIC;
      clk_en : IN STD_LOGIC;
      cnt_en : IN STD_LOGIC;
      updown : IN STD_LOGIC;
      sload  : IN STD_LOGIC;
      sset   : IN STD_LOGIC;
      sclr   : IN STD_LOGIC;
      aload  : IN STD_LOGIC;
      aset   : IN STD_LOGIC;
      aclr   : IN STD_LOGIC;
      eq     : IN STD_LOGIC;
      q      : OUT STD_LOGIC_VECTOR
         (3 DOWNTO 0)
   );
END count4;

ARCHITECTURE lpm OF count4 IS

BEGIN

   U1: LPM_COUNTER
      GENERIC MAP (LPM_WIDTH => 4)
      PORT MAP (data => data, clock =>
         clock, clk_en => clk_en,
         cnt_en => cnt_en, updown => updown,
         sload => sload,
         sset => sset, sclr => sclr,
         aload => aload, aset => aset,
         aclr => aclr, q => q);
END;
```

Current Software Versions

The latest versions of Altera software products are shown below:

- MAX+PLUS II version 7.0, available September 1996
  (PC, Sun SPARCstation, HP 9000 Series 700, and IBMRISC System/6000 platforms)
- PLDshell Plus version 5.1 (PC only)

New Customer Training Courses



The Altera Customer Training Program enables designers to maximize the benefits of Altera devices, including time-to-market benefits and lower system cost. One key to lower cost is increased silicon efficiency. Altera's training classes show you how to efficiently use silicon resources, which often permits additional logic to be placed into a device, eliminating other devices and their associated costs. Alternatively, a design may fit into a smaller, less expensive device, providing reduced overall system cost.

Altera is offering two new customer training classes: a FLEX 10K class and a FLEX 10K & Synopsys class.

FLEX 10K Training

This one-day course introduces the FLEX 10K family and describes how to use MAX+PLUS II to access FLEX 10K device features. The class provides an in-depth description of the FLEX 10K architecture and explains how you can use the architecture to optimize your design to meet area and performance requirements. Lab excercises are used to demonstrate how to implement logic in FLEX 10K embedded array blocks (EABs).

Prerequisites
Prerequisites include completion of the PLT-INTRO course or a good working knowledge of MAX+PLUSII.

Agenda
The FLEX 10K course covers the following topics.

- FLEX 10K basics
- FLEX 10K architecture
  - Logic element
  - Embedded array block (EAB)
  - Interconnect structure (row and column composition)
- Description of library of parameterized modules (LPM) and megafunctions
- Alternative design methods
- Lab session

FLEX 10K & Synopsys Training

This one-day course teaches you how to use Synopsys tools to design efficiently with FLEX 10K devices. The class provides an in-depth description of the FLEX 10K architecture. You are shown how optimization features in Synopsys and MAX+PLUS II can be used to improve the area and performance of a design. You will use the latest features in Synopsys tools and MAX+PLUS II. Lab exercises are used to demonstrate these concepts.

Prerequisites
Prerequisites include completion of the PLT-INTRO course or a good working knowledge of MAX+PLUSII. Working experience with the Synopsys design environment is required.

Agenda
The FLEX 10K & Synopsys course covers the following topics.

- FLEX 10K basics
- FLEX 10K architecture
  - Logic element
  - Embedded array block (EAB)
  - Interconnect structure (row and column composition)
- Design guidelines and lab session
- Lab session 1: How to use RAM and compile using Synopsys tools
- Lab session 2: Compiling in MAX+PLUS II
- Lab session 3: DesignWare
- Lab session 4: Logic functions in EABs
- Lab session 5: I/O optimization
- Lab session 6: Pipelining
- Lab session 7: State machines

Classes are offered regularly in multiple locations in each region. The training class schedule and course catalog are available on Altera Express at (800)5-ALTERA and on the Altera world-wide web site at **http://www.altera.com**.

Creating AMPP Megafunctions

Megafunctions produced as part of the Altera Megafunction Partners Program (AMPP) are targeted for specific Altera device architectures. The targeting process typically involves setting compilation and synthesis options to achieve optimum density and performance. The megafunctions are then refined until they are as fast and small as possible.

Megafunction Development Flow

The development of AMPP megafunctions is summarized below:

1. The megafunction begins as a high-level design created in VHDL, Verilog HDL, or schematic capture with a third-party design tool or MAX+PLUS II.
2. The megafunction design is modified or updated to take advantage of the features of the target Altera architecture (e.g., embedded array blocks (EABs) in FLEX 10K devices, carry and cascade chains in FLEX devices).
3. Logic synthesis options are applied so that the synthesis engine invokes certain rules or algorithms to achieve specific design objectives (e.g., high speed, high density, parallel vs. serial implementation, pipelining). These options can be set in third-party synthesis tools or in MAX+PLUSII.
4. The AMPP partner performs iterative design processing using MAX+PLUS II to maximize performance and minimize resource usage. Some functions provide a range of size and speed options and can be offered in different versions to suit target design requirements.
5. Once optimal specifications are met, the AMPP partner generates a post-synthesis Altera Hardware Description Language (AHDL) file in MAX+PLUS II, and encrypts the file using software provided by Altera. AMPP partners can also provide megafunctions in VHDL, Verilog HDL, or AHDL.
6. The final megafunction is tested, proven, documented, and added to the AMPP product availability list.

Available Formats

The AMPP partners can provide megafunctions in the following formats:

- VHDL
- Verilog HDL
- Altera Hardware Description Language (AHDL)
- Post-synthesis AHDL

Post-synthesis AHDL files, provided by most AMPP partners, reduce the possibility of unexpected changes occurring during the design process. For more information on available design file formats, contact the AMPP partners directly.

Megafunction Package Contents

Each packaged megafunction includes some or all of the following information, depending on the vendor:

- Encrypted post-synthesis AHDL file (<*function name*>**.tdf**) or design file in VHDL, Verilog HDL, or AHDL
- Symbol File (<*function name*>**.sym**) for use in MAX+PLUS II schematics
- List of critical timing parameters
- Documentation
- Authorization key(s)

In addition, some AMPP partners supply simulation models and verification suites that can be used in third-party EDA tools prior to MAX+PLUSII design processing, or with test vectors to check design functionality. Each partner offers a different level of design verification support. Designers should contact the AMPP partner directly for more information.

Encryption

AMPP megafunctions are typically shipped in encrypted format to protect the partners' intellectual property. Megafunction decryption is performed by the MAX+PLUSII software. MAX+PLUSII must be authorized to process a particular megafunction before design processing; the decryption key is supplied to customers when they license the megafunction from the AMPP partner.

Licensing Terms

Each AMPP partner specifies the megafunction licensing terms, such as:

- Authorization codes and installation instructions
- Time-period during which access to the megafunction will be granted
- Access to the source code for the megafunction

For more information on AMPP or AMPP megafunctions, contact Altera Customer Marketing.

Target Applications Support Growing Strong

The Altera target applications program provides tools for improving design cycles and supporting customer time-to-market. These tools include megafunctions, reference designs, design kits, and documentation. Currently, the target applications program focuses on three areas: digital signal processing (DSP), peripheral component interconnect (PCI), and communications.

DSP

DSP support includes megafunctions from the Altera Megafunction Partners Program (AMPP) and Altera MegaCore functions. The table below summarizes the DSP AMPP megafunctions. DSP megafunctions that are planned for 1996 include two color space converters (RGB-YUV and YUV-RGB) and round, saturate, and accumulate functions.

DSP AMPP Functions

Partner	Megafunction
Integrated Silicon Systems Ltd.	Programmable FIR filter
	1-dimensional symmetric FIR filter
	1-dimensional median filter
	2-dimensional FIR filter
	IIR biquad filter
	Laplacian sharpening filter (3 × 3)
	Laplacian edge detector (3 × 3)
Synova Incorporated	JPEG decoder
	JPEG encoder
	Fast Fourier transform function

PCI

Two AMPP partners, Logic Innovations and Eureka Technology, have announced PCI megafunctions supporting both target and master/target interfaces. MegaCore function support for a 32-bit PCI target/master megafunction will be available in the fourth quarter of 1996.

Communications

Communications support includes 14 AMPP megafunctions that provide significant value to network designers. These functions are listed in the following table.

Communications AMPP Functions

Partner	Megafunction
SIS Microelectronics, Inc.	Speedbridge
3Soft Corporation	M16C450 UART
	M16550A UART
Object Oriented Hardware	RF-G704 synchronous framer/deframer
	RF-G721 ADPCM transcoder
	RF-HDLC controller
	RF-BRIM basic rate interface
	GF-RSC Reed Solomon CODEC
	GF-LILAC linked list access controller
Logic Innovations, Inc.	ATM cell delineation
	ATM cell translation and routing
	ATM cell HEC generator/checker
	ATM switch
	UTOPIA interface

Up-to-date information on target applications is available on the Altera world-wide web site at **http://www.altera.com**.

Altera at PCI Spring Show

Altera presented two papers at the PCI spring show held in San Jose, California, April 30 to May2. Leo Wong, an Altera Applications Engineer presented "A Design Foundation for Flexible and Rapid PCI Interface Development" at the CAD Tools panel and "A VHDL Design Approach to a Master/Target PCI Interface" at the Semicustom Logic Implementations panel. Both presentations were well received.

The Altera Dream Team Delivers Big at DAC

The crowds around Altera's booth at the recent Design Automation Conference (DAC) in Las Vegas showed the growing popularity of the Dream Team solution for programmable logic designs. Over 1,000 engineers and managers viewed Altera's presentation or participated in software or hardware demonstrations.

The Altera Dream Team has five players:

- *FLEX10K device family* —Provides the anchor of the Dream Team. With 100,000 gates, the EPF10K100 is the largest programmable logic device commercially available today.
- *MAX+PLUS II development system*—Combines the strengths of Altera devices with EDA tools and megafunctions to create a total programmable logic solution for ASIC design challenges.
- *Altera Commitment to Engineering Solutions (ACCESS) program*—Provides a partnership with over 30 EDA vendors and focuses on ensuring compatibility with Altera architectures.
- *Altera Megafunction Partners Program (AMPP)*—Ensures a constant flow of megafunctions optimized for Altera devices.
- *MegaCore functions*—Provides megafunctions hand-crafted by Altera.

The Dream Team provides a complete solution, focused on improving productivity and reducing product development cycles.

Teamwork Ensures Success

Altera offered numerous demonstrations using Altera devices and tools from Altera's EDA partners. Altera and third-party tool companies shared responsibility for the hands-on demonstrations throughout the show.

The total design solution is successful because the hardware and software work together seamlessly. For example, one demonstration showed synthesis using Synopsys tools combined with simulation with Cadence tools for an EPF10K50 device, taking a design from concept to silicon. Other demonstrations included Autologic II, Quicklogic, and WorkView Office with MAX+PLUS II. In addition, communications designers were shown how digital signal processing functions fit into the 50,000-gate EPF10K50 device.

Special Announcements

During DAC, Altera invited AMPP and ACCESS partners to discuss key issues surrounding the use of megafunctions. Although the discussion focused on simulation file encryption for protecting intellectual property, many other issues were discussed. As a result, a group of companies who develop and sell intellectual property have joined to form the industry's first association: RAPID (Reusable Application-Specific Intellectual Property Developers). The intellectual property vendors also intend to create an advocacy organization to preserve their companies' interests as the intellectual property industry advances.

Altera began distributing the ***AMPP Catalog*** at DAC. The catalog summarizes the current AMPP functions (10 are currently available and more than 30 are under development) and provides a corporate profile of each AMPP partner. For a copy of the ***AMPP Catalog***, contact Altera Literature Services; up-to-date AMPP information is available on the Altera web site at **http://www.altera.com**. The number of AMPP megafunctions is expected to grow to 50 by year-end.

During DAC, Altera announced that VHDL versions of functions from the library of parameterized modules (LPM) are available in the public domain. The Altera descriptions can be obtained on the Electronic Design Interchange Format (EDIF) world-wide web site at **http://www.edif.org**. With the VHDL models, EDA tools and silicon architectures that do not support the LPM can process a design containing LPM functions. For more information, see "Now Available: VHDL-Synthesizeable LPM Functions" on page 20.

Also at DAC, Synopsys announced FPGA Express, a new PC-based synthesis tool targeted for the programmable logic industry. Altera and Synopsys have worked closely to develop interfaces to the Synopsys Design Compiler and FPGA Compiler. This process will continue for FPGA Express.

Winning at DAC

The success of DAC was due in large part to the active participation of Altera partners and vendors. Altera is committed to providing not only the most advanced devices, but also design tools and megafunctions that help designers increase productivity and reduce product development cycles.

In Every ISSUE

Altera Device Selection Guide

All current information for the Altera FLEX 10K, FLEX 8000, MAX 9000, and MAX 7000 devices is listed here. Information on other Altera products is given in the Altera ***1996 Data Book***. Contact Altera or your local sales office for current product availability.

FLEX 10K Devices

	Typical Gates	Pin/Package Options	I/O Pins *(1)*	Temp.	Speed Grade	Flip-flops	Logic Elements	RAM Bits
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	C	-3	720	576	6,144
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	C, I	-4	720	576	6,144
EPF10K20	20,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C	-3	1,344	1,152	12,288
EPF10K20	20,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C, I	-4	1,344	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	C	-3	1,968	1,728	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	C, I	-4	1,968	1,728	12,288
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C	-3	2,576	2,304	16,384
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C, I	-4	2,576	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	C	-3	3,184	2,880	20,480
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	C	-4	3,184	2,880	20,480
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	C, I	-5	3,184	2,880	20,480
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	C	-3	4,096	3,744	18,432
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	C, I	-4	4,096	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	C	-3	5,392	4,992	24,576
EPF10K100	100,000	503-Pin PGA	406	C, I	-4	5,392	4,992	24,576

(1) Six I/O pins are dedicated inputs.

continued on page 26

Altera Device Selection Guide
continued from page 25

FLEX 8000 Devices

	Usable Gates	Pin/Package Options	I/O Pins *(2)*	Temp.	Speed Grade	Flip-flops	Logic Elements
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C	A-2	282	208
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-3	282	208
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-4	282	208
EPF8282AV *(1)*	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C	A-4	282	208
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C	A-2	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C, I	A-3	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C, I	A-4	452	336
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 110, 136	C	A-2	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 110, 136	C	A-3	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 110, 136	C, I	A-4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	120, 152	C	A-2	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	120, 152	C	A-3	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	120, 152	C, I	A-4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C	A-2	1,188	1,008
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-3	1,188	1,008
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-2	1,500	1,296
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C, I	A-3	1,500	1,296
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-4	1,500	1,296

(1) V indicates 3.3-V voltage supply.
(2) Four I/O pins are dedicated inputs.

MAX 9000 Devices

	Macrocells	Pin/Package Options	I/O Pins *(1)*	Temp.	Speed Grade
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA	60, 132, 168	C	-12
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA	60, 132, 168	C	-15
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA	60, 132, 168	C, I	-20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-12
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-15
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C, I	-20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C	-15
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C, I	-20
EPM9560	560	208-Pin CQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP	153, 191, 216	C	-15
EPM9560	560	208-Pin CQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP	153, 191, 216	C, I	-20

(1) Four I/O pins are dedicated inputs.

MAX 7000 Devices

	Macrocells	Pin/Package Options	I/O Pins *(2)*	Temp.	Speed Grade	t_{PD} (ns)	f_{CNT} (MHz)
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-5	5	178.6
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-6	6	150
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-7	7.5	125
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C, I	-10	10	100
EPM7032	32	44-Pin PLCC/TQFP	36	C, I	-12	12	90.9
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C, I	-15	15	76.9
EPM7032V *(1)*	32	44-Pin PLCC/TQFP	36	C	-12	12	90.9
EPM7032V *(1)*	32	44-Pin PLCC/TQFP	36	C	-15	15	76.9
EPM7032V *(1)*	32	44-Pin PLCC/TQFP	36	C, I	-20	20	62.5
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-6	6	150
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-7	7.5	125
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C, I	-10	10	100
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-12	12	90.9
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C, I	-15	15	76.9
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-6	6	150
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-7	7.5	125
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C, I	-10	10	100
EPM7096	96	68-Pin PLCC, 64-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-12	12	90.9
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C, I	-15	15	76.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-7	7.5	125
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-10(P)	10	100
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12	12	90.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-15	15	76.9
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20	20	62.5
EPM7128SV *(1)*	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 100	C	-10	10	100
EPM7128SV *(1)*	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 100	C	-15	15	76.9
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 104	C	-7	7.5	125
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 104	C, I	-10(P)	10	100
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12	12	90.9
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 104	C, I	-15	15	76.9
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20	20	62.5
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA	124	C	-7	7.5	125
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA	124	C	-10	10	100
EPM7192E	192	160-Pin PQFP/PGA	124	C	-12(P)	12	90.9
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA	124	C, I	-15	15	76.9
EPM7192E	192	160-Pin PQFP/PGA	124	C, I	-20	20	62.5
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C	-7	7.5	125
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C	-10	10	100
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C	-12(P)	12	90.9
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C, I	-15	15	76.9
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C, I	-20	20	62.5

(1) V indicates 3.3-V voltage supply.
(2) Four I/O pins are dedicated inputs.

Data I/O Programming Support

Data I/O provides programming hardware support for select Altera devices. Algorithms are supplied via Data I/O's Keep Current Express - Bulletin Board Service (KCE-BBS). Programming support for Configuration EPROM, MAX 9000, and MAX 7000 devices is shown below. All estimated availability dates are subject to change. Data I/O customers with a current maintenance agreement can obtain qualified algorithms electronically from the KCE-BBS.

The following Configuration EPROM devices are supported by the 2900 version 5.2, the 3900 version 5.2, and UniSite version 5.2 (Hex Files only).

- EPC1213P-8
- EPC1213L-20
- EPC1064P-8
- EPC1064L-20
- EPC1064T-20
- EPC1064VL
- EPC1064VT
- EPC1P-8
- EPC1LC-20

The following MAX 9000, MAX 7000, and FLASHlogic devices are supported by the 3900 version 5.2 and UniSite version 5.2.

MAX 9000 Devices

- EPM9320LC84
- EPM9320GC280
- EPM9320RC208
- EPM9400RC208
- EPM9400RC240
- EPM9480RC208
- EPM9480RC240
- EPM9560GC280
- EPM9560RC240
- EPM9560WC208
- EPM9560RC304

MAX 7000 Devices

- EPM7032L-44
- EPM7032Q-44
- EPM7032T-44
- EPM7032VL-44
- EPM7032VT-44
- EPM7064L-44
- EPM7064L-68
- EPM7064L-84
- EPM7064Q-100
- EPM7096L-68 (EPROM)
- EPM7096L-84 (EPROM)
- EPM7096Q-100 (EPROM)
- EPM7096L-68 (EEPROM)
- EPM7096L-84 (EEPROM)
- EPM7096Q-100 (EEPROM)
- EPM7128L-84
- EPM7128Q-100
- EPM7128Q-160
- EPM7128EL-84
- EPM7128EQ-100
- EPM7128EQ-160
- EPM7160L-84
- EPM7160Q-160
- EPM7160EL-84
- EPM7160EQ-100
- EPM7160EQ-160
- EPM7192G-160
- EPM7192Q-160
- EPM7192EG-160
- EPM7192EQ-160
- EPM7256G-192
- EPM7256W-208
- EPM7256M-208
- EPM7256EG-192
- EPM7256EG-160
- EPM7256ER-208

FLASHlogic Devices

- EPX880

Software Utilities

eau000.exe Overview of electronic utilities
eau003.exe EP310 to EP330 JEDEC File converter
eau005.exe JEDPACK JEDEC File compactor
eau007.exe JEDSUM JEDEC checksum generator
eau017.exe LEF2AHDL converts A+PLUS LEF files to AHDL
eau018.exe PLD2EQN PAL/GAL/PLA file converter
eau019.exe ABEL2MAX file converter
eau020.exe PASM2TDF PALASM file converter
eau022.exe PLA2PDS PLA to PALASM file converter

Utilities are available from the Altera BBS via modem at (408) 954-0104 and the Altera FTP site at **ftp.altera.com**.

Programming Hardware Compatibility

The following tables contain the latest programming hardware information. You should always use the software version shown in "Current Software Versions" on page 20 to ensure correct programming. PLM-prefix adapters can be used only with the Master Programming Unit (MPU).

Programming with the BitBlaster

Device	Package	Hardware
FLEX 10K devices	All packages	PL-BITBLASTER
FLEX 8000 devices	All packages	PL-BITBLASTER
MAX 7000S	All packages	PL-BITBLASTER
EPX880	All packages	PL-BITBLASTER, *(1)*
FLASHlogic devices	All packages	PL-FLDLC, PL-BITBLASTER, *Note (1), (2)*

Notes to tables:

(1) MAX+PLUS II version 6.0 and higher provides programming support for all FLASHlogic devices via the BitBlaster. The EPX880 can only be programmed with the BitBlaster.

(2) You can use the FLASHlogic Download Cable (PL-FLDLC) with PLDshell Plus to program and configure all FLASHlogic devices, except the EPX880.

(3) The hardware products for these devices are included with the FLEX Download Cable.

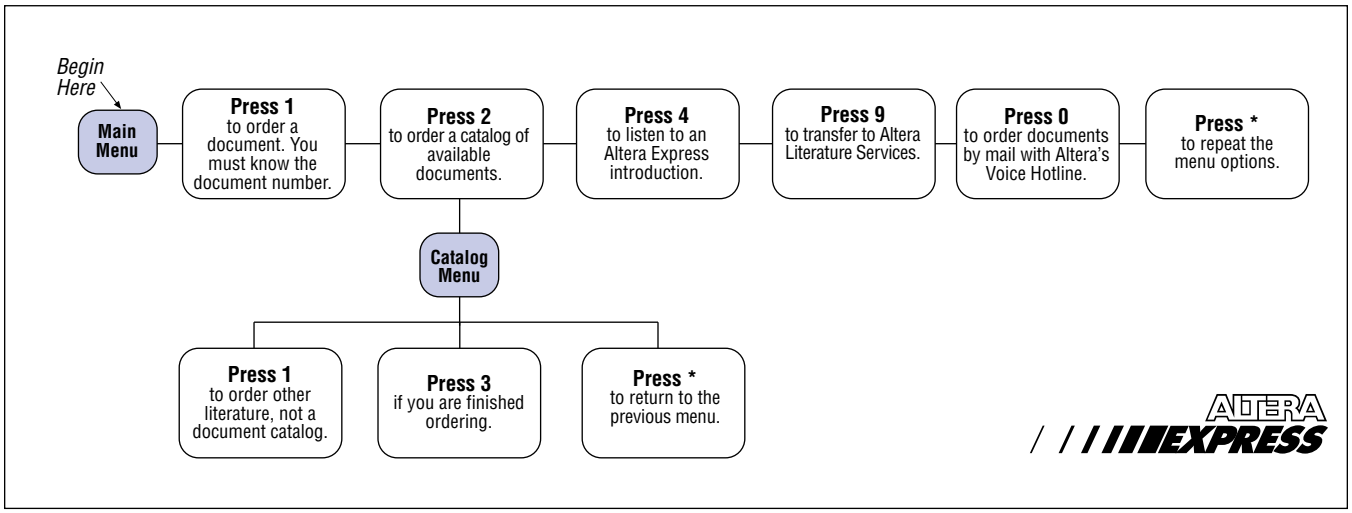
(4) Refer to the Altera ***1996 Data Book*** for device adapter information. Altera offers an adapter exchange program for 0.8-micron EPM5032, EPM5064, and EPM5130 programming adapters. See "Exchange Your MAX 5000 Programming Adapter for Free" on page 6 of this newsletter for more information.

Programming Adapters

Device	Package	Adapter
EPC1064, EPC1064V, EPC1213 (all FLEX 8000 devices), *Note (3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 (all FLEX 10K and FLEX 8000 devices), *Note (3)*	DIP J-lead	PLMJ1213 PLMJ1213
EPM9320	PGA J-lead (84-pin) RQFP (208-pin)	PLMG9000-280 PLMJ9320-84 PLMR9000-208
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	PGA RQFP (208-pin) RQFP (240-pin) RQFP (304-pin)	PLMG9000-280 PLMR9000-208 PLMR9000-240 PLMR9000-304
EPM7032, EPM7032V	J-lead PQFP TQFP	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7064	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160, EPM7160E	J-lead PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7192, EPM7192E	PGA PQFP	PLMG7192-160 PLMQ7192/7256-160
EPM7256E	PGA MQFP, RQFP PQFP	PLMG7256-192 PLMR7256-208 PLMQ7192/7256-160
EPX780	J-lead	PLMJ780-84
MAX 5000 devices	All packages	*Note (4)*
Classic devices	All packages	*Note (4)*
EPS448	All packages	*Note (4)*

How to Request Altera Publications

Altera publications are available through Altera Express, a 24-hour, 7-day-a-week, automated fax service. In the U.S. and Canada, call (800) 5-ALTERA; international callers can retrieve information by calling (408) 894-7850 from a fax phone. See the following figure. Documents can also be obtained from Altera Literature Services at (408) 894-7144 or the Altera world-wide web site at **http://www.altera.com**.



How to Access Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera:

Altera Contact Information

Information Type	Access	U.S. & Canada	All Other Locations
Literature	Altera Express	(800) 5-ALTERA	(408) 894-7850
	Altera Literature Services	(408) 894-7144 lit_req@altera.com	(408) 894-7144 *(1)* lit_req@altera.com
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 894-7000
	Fax	(408) 954-8186	(408) 954-8186
Technical Support	Telephone Hotline (8 a.m. to 5 p.m. Pacific Time)	(800) 800-EPLD (408) 894-7000	(408) 894-7000 *(1)*
	Fax	(408) 954-0348	(408) 954-0348 *(1)*
	Bulletin Board Service	(408) 954-0104	(408) 954-0104
	Electronic Mail	sos@altera.com	sos@altera.com
	FTP Site	ftp.altera.com	ftp.altera.com
	CompuServe	go altera	go altera
General Product Information	Telephone	(408) 894-7104	(408) 894-7104 *(1)*
	World-Wide Web	http://www.altera.com	http://www.altera.com

Note:

(1) You can also contact your local Altera sales office or sales representative. See the Altera ***1996 Data Book*** for a list of sales offices and representatives.

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