The Altera Advantage News & Views

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FLEX® Devices: The Gate Array Alternative

Altera's FLEX 10K and FLEX 8000 devices combine the flexibility of programmable logic devices (PLDs) with the density and efficiency of gate arrays. As PLD unit costs decline, Altera's FLEX devices demonstrate a clear cost advantage over gate arrays. Gate array design revisions, which can cost an average of $25,000 per revision (per Dataquest), are key to the PLD-gate array cost difference.

The Hidden Costs of Gate Arrays

FLEX 10K and FLEX 8000 devices allow the designer to avoid the hidden costs of gate arrays, which include non-recurring engineering (NRE) charges, higher development cost, and lost market opportunity. See Figure1.

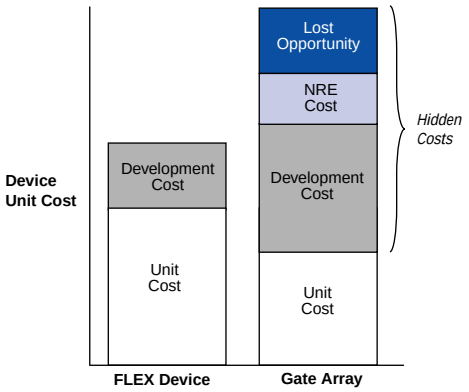
The most commonly overlooked hidden cost of gate arrays is NRE charges—the up-front, non-refundable charges for engineering, custom mask-making, and samples. Dataquest reports that gate array NRE charges typically cost $25,000 for each design revision—depending on the vendor, engineering services required, and number of mask layers. For automatic test vector generation, another $2,000 to $7,000 is added. All of these charges apply to each design iteration, and 40% of all gate array designs require at least two iterations. For example, Dataquest projects an NRE cost (netlist to prototype) of $45,000 for a 20,000-gate device.

In contrast, NRE costs are not incurred when designing with PLDs. Test vector generation—the most time-consuming part of the gate array design flow—is unnecessary with PLDs, which are fully tested before shipment. The fast prototyping capabilities of PLDs shorten functional simulation by enabling in-system testing earlier in the design cycle, providing a crucial time-to-market advantage (see Table 1).

Engineering & Re-Spin Costs

PLDs have shorter design cycles that reduce engineering costs. A designer can rapidly produce working prototypes, decreasing simulation time and enabling in-system testing earlier in the design cycle. In-system prototyping also ensures accurate timing simulation. In addition, programmable logic eliminates vendor interaction, a time-consuming gate array design phase that includes simulation, place-and-route iterations, and sign-off. According to a study by Integrated Circuit Engineering Corporation, gate array designs require a second iteration 40% of the time, which significantly adds to the time that an engineer spends on a design. When combined with other overhead, such as the computer hardware and software required to design gate arrays, the result is a significant financial impact.

Figure 1. Hidden Costs of Gate Arrays



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Total Cost Calculation

Unit costs, engineering costs, and hidden costs all add to the total cost of a design and affect the length of the development cycle. Table 2 shows a sample analysis based on 1998 projections.

Time-to-Market Advantages

The shorter PLD development cycle clearly benefits designer productivity. It also speeds time-to-market, thereby decreasing the risk of lost market opportunities. Getting designs to market quickly provides several advantages:

- Higher profit margins are gained because products benefit from economies of scale earlier in their design life cycle.
- Creates increased market share and customer loyalty.
- Adds a month to the product's sales life for each month cut from the product development cycle.

A study by Integrated Circuit Engineering Corporation found that a product released three months late in a market that lasts 24 months will lose 34% of its potential revenue—a loss that cannot be ignored in today's competitive market.

PLD Units Costs Are Declining

Historically, the price difference between PLDs and gate arrays caused managers to reject PLDs as a viable alternative. However, PLD prices have been declining about 30% annually (per Dataquest), and Altera will continue to develop advanced processes that will help to further reduce prices. For example, Altera projects a 1998 North American volume price of $8 for 20,000-gate EPF10K20 devices, a 76% drop from current prices. Altera also estimates that the price of the EPF10K100, with 100,000 programmable gates, will decline 82% by 1998. In contrast, the price of gate arrays of similar density should drop about 25% during the same period (per Dataquest).

Conclusion

Altera's FLEX 10K and FLEX 8000 families combine the advantages of gate arrays with the flexibility of PLDs. With reduced engineering and per-unit cost, these high-density PLDs now present an alternative to gate arrays for both prototyping and volume production applications.

Table 1. Gate Array vs. Programmable Logic Design Cycles

Design Stage	Gate Arrays (Weeks), *Note (1)*	PLDs (Weeks)
Design Specification	1	1
Design Entry	1.6	1.6, *Note (2)*
Functional Simulation	4	2.4, *Note (2)*
Test Vector Generation	6.4	0
Vendor Interface	1.6	0
Prototype Test	1.6	1.6
Prototype Lead Time	2 to 4	0
Production Lead Time	6 to 8	0
Total Design Cycle	**24 to 28**	**7**

Notes:
(1) Percentage of gate array time by task based on data from *ASIC Technology & News*.
(2) The use of megafunctions will reduce this number.

Table 2. Example of Gate Array vs. PLD Costs

Cost	Gate Array	PLD
Usable Gates	20,000	20,000
Unit Costs (20,000 Units), *Note (1)*	$4.00	$8.00
NRE, *Note (1)*	$44,000	$0
NRE per Unit	$2.20	$0
Typical Design Cycle	24 weeks	7 weeks
Cost per Engineer (at $3,000 per Week)	$72,000	$21,000
Number of Engineers on Team	3	3
Total Engineering Resource Cost	$216,000	$63,000
Engineering Costs per Unit	$10.80	$3.15
Re-Spin Costs	$0, *Note (2)*	$0
Lost Market Opportunities	$0, *Note (2)*	$0
Total Device Unit Cost	**$17.00**	**$11.15**

Notes:
(1) Projected 1998 gate array unit prices and NRE costs are from Dataquest; projected PLD costs are from Altera.
(2) No cost assumed; however, most gate array designs incur re-spin and/or lost market opportunity costs.

Devices & TOOLS

FLEX 10K

Altera Ships First FLEX 10KA Device

Altera recently announced the FLEX10KA family, with a 3.3-V operating voltage and densities ranging from 10,000 to 250,000 gates. Altera is now shipping the EPF10K50V, the 50,000-gate member of the FLEX 10KA family, in 240-pin power quad flat pack (RQFP) packages. EPF10K50V devices in 356-pin ball-grid array (BGA) packages are scheduled to ship in April 1997.

In May 1997, Altera plans to ship the 130,000-gate EPF10K130V. The 3.3-V EPF10K130V with 6,656 logic elements, 16 2-Kbit embedded array blocks, and 7,126 flipflops, offers reductions in power consumption. The table below summarizes the projected availablity of devices within the FLEX 10KA family.

FLEX 10KA Availability

Device	Density (Gates)	Availability
EPF10K10A	10,000	1998
EPF10K20A	20,000	1998
EPF10K30A	30,000	Second Half 1997
EPF10K40A	40,000	1998
EPF10K50V	50,000	Now
EPF10K70A	70,000	Second Half 1997
EPF10K100A	100,000	September 1997
EPF10K130V	130,000	May 1997
EPF10K250A	250,000	1998

Frequently Asked FLEX 10KA Questions

Q *What is the difference between the "V" and the "A" devices?*

A The FLEX10KA family includes two "V" devices: the EPF10K50V and the EPF10K130V. These devices are manufactured on a 0.35-micron, triple-layer-metal process. The "A" devices will be manufactured on a 0.35-micron, quad-layer-metal process. Altera plans to introduce 0.35-micron, quad-layer metal versions of these devices in 1998.

Q *Do I need to make any changes to my printed circuit board to migrate from a FLEX 10K device to a FLEX10KA device?*

A The FLEX 10KA family is pin-compatible with the FLEX 10K family. To connect the FLEX 10KA device, you simply connect the 3.3-V power plane of your printed circuit board to the power pins of the FLEX 10KA device.

Q *How does the timing of the FLEX 10KA family compare to the FLEX 10K family?*

A The performance of the 3.3-V FLEX 10KA family will be comparable to the 5.0-V FLEX 10K family.

More FLEX 10K Package Offerings

The following table summarizes newly shipping FLEX10K devices.

New FLEX 10K Devices Now Shipping

Device	Package
EPF10K10LC84-4	84-pin plastic J-lead chip carrier (PLCC)
EPF10K10LC84-3	84-pin PLCC
EPF10K20TC144-4	144-pin thin quad flat pack (TQFP)
EPF10K20TC144-3	144-pin TQFP
EPF10K20TI144-4	144-pin TQFP
EPF10K20RC208-3	208-pin quad flat pack (QFP)
EPF10K40RC208-4	208-pin QFP
EPF10K40RC240-4	240-pin QFP
EPF10K50RC240-3	240-pin QFP
EPF10K50RI240-4	240-pin QFP
EPF10K50GC403-3	403-pin pin-grid array (PGA)
EPF10K50BC356-3	356-pin BGA
EPF10K70GC503-4	503-pin PGA
EPF10K70GC503-3	503-pin PGA

EPF10K70 & EPF10K40 Ship

Altera is now shipping EPF10K70 devices in 503-pin pin-grid array (PGA) packages. The EPF10K40 is shipping in 240- and 208-pin QFP packages.

Configuration Support for 3.3-V FLEX 10KA Family

With the introduction of the 3.3-V FLEX 10KA family, Altera is extending the SRAM-based family to a projected 250,000 gates. To configure these 3.3-V devices, Altera provides the EPC1 Configuration EPROM, which can be used for 3.3-V or 5.0-V operation.

The EPC1 Configuration EPROM operates at either 3.3V or 5.0 V, depending on the setting of a configuration bit. The MAX+PLUS®II software version7.1 and higher automatically sets the bit when generating the Programmer Object File (**.pof**) for the EPC1. For example, if you compile your design for a 5.0-V FLEX 10K device, MAX+PLUSII ™ will not set the 3.3-V configuration bit, and the EPC1 will function as a 5.0-V device. If you compile your design for a 3.3-V FLEX 10KA device, MAX+PLUSII will set the 3.3-V configuration bit, and the EPC1 will function as a 3.3-V device. All EPC1 devices (including those that have already shipped) fully support both 3.3-V and 5.0-V operation.

To program an EPC1 for 3.3-V operation, you must use MAX+PLUSII version 7.1 or higher. Previous versions of MAX+PLUSII will not set the 3.3-V configuration bit in the POF.

FLEX 8000

Low-Cost 240-Pin QFP Ships

With the introduction of the 16,000-gate EPF81500A and 12,000-gate EPF81188A in 240-pin plastic QFP packages, FLEX 8000 continues to be the lowest-cost PLD family. These devices combine the flexibility of programmable logic with competitive pricing, providing the most cost-effective solution for designs that require high I/O pin counts.

Sample FLEX 8000 Pricing

Device	Package	Speed Grade	Current 100-Unit Price	Volume Price End 1997 *(1)*
EPF81188A	240-pin PQFP	-4	$32.50	$16.50
EPF81500A	240-pin PQFP	-4	$39.50	$17.50

Note:
(1) Projected price in U.S. dollars for OEM direct orders.

MAX® 9000

Enhanced ISP Support for MAX 9000 Devices Using Automated Test Equipment

With the latest MAX 9000 devices and MAX+PLUS II version 7.2 and higher, Altera is offering enhanced in-system programming support for automated test equipment (ATE). The following ordering codes should be used when devices are programmed in-system using ATE:

- EPM9320LC84-15F
- EPM9320RC208-15F
- EPM9560RC208-15F
- EPM9560RC240-15F
- EPM9560RC304-15F

New MAX 9000 Packages

The EPM9560 device is now available in 356-pin BGA packages, the first BGA package offered for the MAX9000 family. EPM9320 devices in 356-pin BGA packages will be available in March 1997.

Industrial-temperature-grade EPM9560 devices are now available in 208-pin power quad flat pack (RQFP) packages.

MAX 7000

MAX 7000S Availability

The MAX 7000S device availability is shown below:

MAX 7000S Device Availability

Device	Package	Speed Grade	Availability
EPM7064S	44-pin PLCC	-7, -10	Now
	44-pin TQFP	-7, -10	April 1997
	84-pin PLCC	-7	March 1997
		-10, -15	Q2 1997
EPM7128S	100-pin TQFP	-10, -15	Now
	100-pin PQFP	-7, -10, -15	Now
	160-pin PQFP	-7, -10, -15	Now
EPM7192S	160-pin PQFP	-10, -15	Now
EPM7256S	208-pin RQFP	-10	Q3 1997
	208-pin RQFP	-12, -15	Now

Contact your local Altera sales representative or Altera customer service for the most current MAX 7000S availability.

MAX 7000S Devices Now Programmable in Sockets

During the second quarter of 1997, Altera will introduce adapters that support traditional programming of MAX 7000S devices in QFP packages.

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These programming adapters will be available for design flows that require device programming before printed circuit board assembly, but require field upgrades using the in-system programmability (ISP) feature of the MAX 7000S family. The adapters have been specifically developed to provide programming in quad flat pack (QFP) packages without carriers. Contact your local Altera sales representative for more information. The ordering codes for these new adapters are shown below:

- PLMQ7000S-100NC
- PLMQ7128/160-160NC
- PLMQ7192/256-160NC
- PLMR7256-208NC

MAX 7000S Prices Reduced up to 49%

On January 1, Altera reduced the prices of the EPM7128S, EPM7192S, and EPM7256S devices by up to 49%. This price reduction is a result of continuing process improvements and increased production volumes. Examples of the new 100-unit pricing are shown below:

MAX 7000S Price Reductions

Device	New 100 Unit Pricing	Reduction
EPM7128SQC100-15	$18.75	43%
EPM7128STC100-15	$22.00	40%
EPM7192SQC160-15	$42.00	49%
EPM7256SRC208-15	$68.50	48%

MAX 5000 & Classic

Product Transitions

Altera is migrating existing MAX 5000 and Classic devices from a 0.8-micron process to a 0.65-micron process. Evaluation packets (containing device samples and documentation) are available from your local Altera sales representative. The table below outlines the process migration schedule:

Product Migration Schedule

Description *(1)*	Reference *(2)*	Device	Date
MAX 5000 devices fabricated on a 0.65-micron process *Note (3)*	PCN 9407 ADV 9515 ADV 9606	EPM5032	May 1, 1997
		EPM5064	July 1, 1997
		EPM5128	Complete
		EPM5130	July 1, 1997
		EPM5192	Complete
Classic devices fabricated on a 0.65-micron process	PCN 9510 ADV 9607 ADV 9621	EP6*xx*	Complete
		EP9*xx*	Complete
		EP18*xx*	Complete

Notes:
(1) This process transition will not result in any changes to data sheet parameters or ordering codes.
(2) Altera provides advisories and process change notices. Go to the Altera world-wide web site for these reference documents.
(3) Devices manufactured on the 0.65-micron process must be programmed with new programming adapters.

New Altera programming adapters are required to program the 0.65-micron MAX 5000 devices (0.65-micron Classic devices do not require new adapters). Altera will exchange existing EPM5032, EPM5064, and EPM5130 programming adapters for new adapters *for free*. These new adapters are backwards-compatible and support all existing die revisions. The table below lists the existing MAX 5000 adapters that can be exchanged for new adapters.

MAX 5000 Replacement Adapters

Existing Adapter	New Adapter
PLED5032	PLMD5032A
PLMD5032	PLMD5032A
PLEJ5032	PLMJ5032A
PLM5032	PLMJ5032A
PLES5032	PLMS5032A
PLEJ5064	PLMJ5064A
PLMJ5064	PLMJ5064A
PLEG5130	PLMG5130A
PLEJ5130	PLMJ5130A
PLMJ5130	PLMJ5130A
PLEQ5130	PLMQ5130A
PLMQ5130	PLMQ5130A

Discontinued Devices

In recent months, Altera has announced that various products will be discontinued (see the table below). Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's world-wide web site at **http://www.altera.com**. Rochester Electronics, an after-market supplier, offers support for many discontinued Altera products. Contact Rochester Electronics at (508)462-9332 for more information.

Discontinued Device Ordering Codes

Device Family	Device	Last Order Date	Last Shipment Date	Reference
FLEX 10K	EPF10K50 in -5 speed grades	3/31/97	6/30/97	ADV 9623
FLEX 8000	Selected speed grades (-6, -5, and -2A)	3/31/97	6/30/97	ADV 9622
FLASHlogic	EPX880 and EPX8160 (all packages, temperature grades, and speed grades)	6/30/97	6/30/98	PDN 9625
	EPX740 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
MAX 5000	EPM5032SC-15	6/30/97	12/31/97	PDN 9624
	EPM5016 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
Classic	EP220, EP224, EP312, EP324 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
	Selected EP18*xx* ordering codes	3/31/97	6/30/97	ADV 9608
Function-Specific	EPS448, EPS464 (all commercial and industrial temperature grades; military devices have earlier last order and last shipment dates)	3/31/97	9/30/97	PDN 9516

New Altera Publications

New Altera publications are available from Altera Literature Services and Altera Express. Individual documents are available on the Altera world-wide web site. Document part numbers are shown in italics.

- **LPM Quick Reference Guide** *A-CAT-LPM-01*
  Provides information on functions in the library of parameterized modules (LPM) and on custom parameterized functions created by Altera.
- **AMPP℠ Catalog** *M-CAT-AMPP-02*
  Provides the latest information on the Altera Megafunction Partners Program℠ (AMPP), including a description of the functions and a corporate profile for each partner.
- **Target Applications Selector Guide** *M-SG-TAPPS-01*
  Gives a complete listing of megafunctions, reference designs, and technical documentation.
- **Altera Target Applications CD-ROM** *M-CD-TAPPS-01*
  Supplies a complete library for target applications (e.g., digital signal processing, communications, and bus interfaces), including reference designs and documentation. New documentation in the ***Altera Target Applications CD-ROM*** includes:
  - **fft Fast Fourier Transform Data Sheet** *A-DS-FFT-01*
  - **Functional Specification 5: round Data Word Rounder** *A-FS-05-01*
  - **Functional Specification 6: saturate Data Word Saturator** *A-FS-06-01*
  - **Solution Brief 4: Complex Multiplier/Mixer Megafunction** *A-SB-004-01*
  - **Solution Brief 5: Numerically Controlled Oscillator Megafunction** *A-SB-005-01*
  - **Solution Brief 6: PCI Bus Target Megafunction** *A-SB-006-01*
  - **Solution Brief 8: ADPCM Megafunction** *A-SB-008-01*
  - **Solution Brief 9: Discrete Cosine Transform Megafunctions** *A-SB-009-01*
  - **Solution Brief 10: Digital Modulator Megafunction** *A-SB-010-01*
  - **Solution Brief 11: Linear Feedback Shift Register Megafunction** *A-SB-011-01*
  - **Solution Brief 12: Fast Fourier Transform MegaCore Function** *A-SB-012-01*
  - **Solution Brief 13: Speedbridge Megafunction** *A-SB-013-01*

Estimating FLEX 10K Design Performance

Although you can use MAX+PLUS II to calculate performance once a design is created, you may find it useful to approximate performance during design planning. Estimating performance in some programmable logic devices can be difficult because they have segmented routing channels and unpredictable timing. However, Altera devices—such as the FLEX 10K family—have a continuous routing structure that provides predictable timing, allowing designers to easily determine performance. Designers can calculate the clock performance of a FLEX 10K design by following the steps below:

1. Identify the synchronous source (the source register).
2. Identify the synchronous destination (the destination register).
3. Determine the number of intermediate combinatorial logic levels.
4. Calculate the sum of delays using the following equation:
   $t_{CO} + t_{D1} + t_{D2} + ... + t_{D(n-1)} + (n\text{-}1)\, t_{LE} + t_{LUT} + t_{SU}$
5. Compare the sum of delays to the desired clock period.

Figure 1 shows the critical path delays; the timing parameters are summarized in Table 1.

In Figure 1, the sum of the delays between the synchronous source, the output of the first register, the synchronous destination, and the input of the last register is:

$$t_{CO} + t_{D1} + t_{D2} + t_{LE} + t_{LUT} + t_{SU}$$

The sum of the path delays and logic delays determines whether the design meets performance requirements. If the critical path delay is roughly equivalent to the clock period, the design may meet performance requirements. If the sum of the delays is longer than the clock period, you can adjust the MAX+PLUS II Compiler's logic synthesis options (such as enabling carry chains) by choosing **Logic Options** (Assign menu).

The times for t_{D1} and t_{D2} depend on the relative placement of the logic elements (LEs). The FLEX 10K timing model incorporates the following three parameters to model the hierarchical interconnect structure. You can choose the appropriate parameter based on the placement of the LEs.

$t_{SAMELAB}$ The delay encountered when two LEs are in the same LAB.
$t_{SAMEROW}$ The delay encountered when two LEs are in different LABs in the same row.
$t_{DIFFROW}$ The delay encountered when two LEs are in different rows.

The $t_{SAMEROW}$ and $t_{DIFFROW}$ parameters model the delay for an LE with a fan-out of 4, i.e., driving across the entire row or device. As such, the delay is greater than the typical delay of a signal in a design. MAX+PLUS II takes fan-out and distance into account when computing delays in the Timing Analyzer, Simulator, and netlist extractors.

Using an EPF10K50 device in a -3 speed grade as the target device for the design in Figure 1, the calculations are:

$t_{D1} = t_{D2} = 0.4$ ns
$t_{LE} = t_{LUT} + t_{COMB} = 1.5 + 0.6 = 2.1$ ns

Figure 1. Critical Path Delays

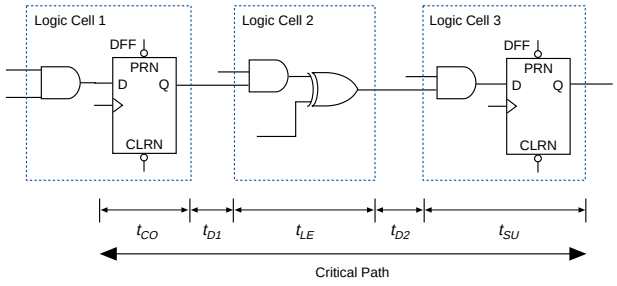


Table 1. Timing Parameters

Symbol	Parameter
t_{CO}	Register clock-to-output delay
t_{Dn}	Path delays (n = number of combinatorial logic levels)
t_{LE}	Delay through logic element ($t_{LUT} + t_{COMB}$)
t_{LUT}	Delay through combinatorial logic
t_{SU}	Register setup time

The total delay is shown in the following calculation:

$t_{CO} + t_{D1} + t_{D2} + t_{LE} + t_{LUT} + t_{SU} =$
$(0.2) + (0.4) + (0.4) + (2.1) + (1.5) + (2.2) = 6.8$ ns

Therefore, the minimum clock period for this path is 6.8 ns. The total path delay is less than the available resources for the circuit and thus the performance requirements are easily met. If the same design was implemented by logic elements from different rows, the signal paths would have additional row and column delays, causing a performance impact:

$t_{Dn} = t_{DIFFROW} = 10.2$ ns
$t_{CO} + t_{D1} + t_{D2} + t_{LE} + t_{LUT} + t_{SU} =$
$(0.2) + (10.2) + (10.2) + (2.1) + (1.5) + (2.2) = 26.4$ ns

FLEX 10K devices also contain embedded array blocks (EABs), which are represented in the timing model. The timing information for the EAB in the *FLEX 10K Embedded Programmable Logic Family Data Sheet* contains micro- and macroparameters. Microparameters break the EAB into smaller slices and can be used to compute timing for any possible configuration of the EAB. However, this mathematical exercise can become tedious to repeat for commonly used configurations of the EAB. Therefore, the data sheet also contains macroparameters—precomputed parameters for the most common configurations of the EAB. Macroparameters show the timing for asynchronous and synchronous uses of the EAB. Most FLEX 10K designers use the synchronizing registers of the EAB, which provide a much simpler timing analysis. The EAB structure permits the timing to remain consistent for different size configurations of the EAB. For example, the timing for a 256 ×8 RAM is the same as for a 512 ×4 RAM.

When analyzing the data path driving the EAB, you can simply substitute one of the EAB macroparameters for one of the LE parameters described previously. For instance, $t_{EABDATASU}$ is the parameter representing the setup time of the data or address register in the EAB. If an LE register drives through one LE into the EAB, the equation for the critical path delay (t_P) is $t_{CO} + t_{D1} + t_{D2} + t_{LE} + t_{EABDATASU}$. If the two LEs are in the same row as the EAB, the equation is:

$t_{D1} = t_{D2} = t_{SAMEROW}$
$t_{CO} + t_{D1} + t_{D2} + t_{LE} + t_{EABDATASU} =$
$(0.2) + (3.7) + (3.7) + (2.1) + (5.6) = 15.3$ ns

The $t_{EABDATACO}$ parameter models the clock-to-output delay for the output registers of the EAB. During timing analysis, the $t_{EABDATACO}$ parameter can replace the t_{CO} parameter in the above equations.

You can use cliques to group all logic on a speed critical path to ensure optimum speed. The example above shows how different implementations of the same design can affect performance. MAX+PLUS II calculates performance after you create a design, which allows you to quickly and easily obtain performance parameters. Refer to MAX+PLUS II Help or the *FLEX10K Embedded Programmable Logic Family Data Sheet* in the ***1996 Data Book*** for more information on design timing analysis.

FLEX 10K Pin Migration

Altera FLEX 10K devices offer extensive pin migration options, allowing you to change your design from a smaller device to a larger one with ease (see Table 1). For example, if you are designing with the EPF10K30, and find that you need more logic, you can simply migrate your design to an EPF10K40 in the same package. Pin migration capability increases design flexibility, shortening time-to-market.

Table 1. Pin Migration in FLEX 10K Devices *Note (1)*

Device	84-Pin PLCC	144-Pin TQFP	208-Pin QFP	240-Pin QFP	356-Pin BGA	403-Pin PGA	503-Pin PGA
EPF10K10	59	102	134				
EPF10K20		102	147	189			
EPF10K30			147	189	246		
EPF10K40			147	189			
EPF10K50				189	274	310	
EPF10K70				189			358
EPF10K100							406

Note:
(1) The value in each cell is the number of user I/O pins.

BGA: Packaging for the Future

As programmable logic devices (PLDs) grow to 250,000 gates and beyond, designers require more advanced, flexible packages. Ball-grid array (BGA) packaging, used by Altera, empowers designers by offering the technological benefits and flexibility needed to meet the challenges of the future. With the SuperBGA package from Amkor/Anam, Altera continues this leadership position by supplying designers with cutting-edge BGA packaging.

In BGA packages, the I/O connections are located on the interior of the device. Leads normally placed along the periphery of the package are replaced with solder balls arranged in a matrix across the bottom of the substrate. The final device is then soldered directly to the printed circuit board (PCB) using assembly processes virtually identical to the standard surface-mount technology preferred by system designers.

The advantages of BGA packaging are summarized below:

- Fewer damaged leads
- More leads per unit area
- Less expensive surface mount equipment
- Smaller footprints
- Enhanced thermal performance
- Integrated circuit speed advantages

Fewer Damaged Leads

The most important benefit offered by BGA packaging is a sharp reduction in damaged leads during PCB manufacturing and assembly. Instead of fine-pitched peripheral leads (FPPLs), BGA leads consist of solid solder balls which are less likely to suffer damage during handling. For example, solder joint defect levels for a 208-pin quad flat pack (QFP) package—which have 0.5-mm FPPLs—typically run 100 parts per million (PPM). Defect levels for BGA packages typically run 1.0 PPM, even as solder ball leads become more finely pitched.

More Leads Per Unit Area

Currently, lead counts are being increased by moving the solder balls closer to the edges of the package and by decreasing the pitch to 1.27 mm, or 50 mils. For example, 356 balls can be arranged in an interstitial pattern in the same substrate space as that occupied by 313 pin leads spaced 1.80 mm apart. Because the balls are not located underneath the die area, the solder joints are not affected by the local thermal expansion effects caused by the die.

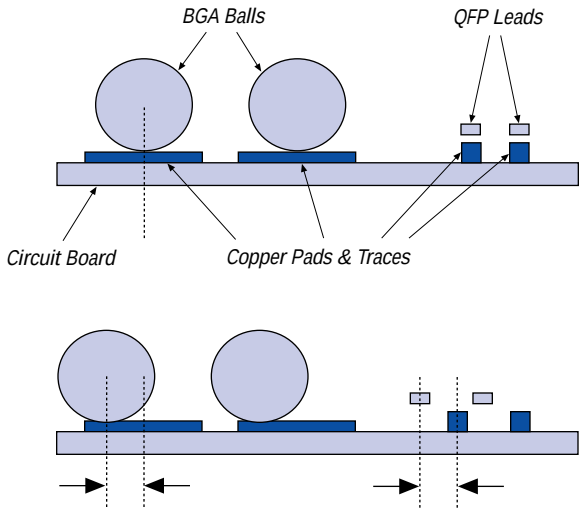
Less Expensive Surface Mount Equipment

BGA packages can tolerate slightly imperfect placement during mounting, requiring less expensive surface mount equipment. The solder balls on a BGA package sit directly on solder paste. When the balls melt, the surface tension pulls the solder into the smallest possible shape and aligns the package to the PCB substrate. This self-aligning capability of the BGA means less restrictive tolerances than QFPs and less expensive surface mount equipment. See Figure 1.

Smaller Footprints

The smaller footprints and lighter weight provided by BGA packages are ideal for digital signal processing (DSP) in portable communications and computing devices. BGA packages are also usually 20% to 50% smaller than QFPs, making BGA packages more attractive for applications that require high

Figure 1. BGA vs. QFP Mounting



performance and a smaller footprint. For example, Altera provides the 50,000-gate EPF10K50 device in a 35 × 35-mm package, which contains 274 I/O pins. A 27 × 27-mm BGA package, with 256 I/O pins, is only 1.4mm tall and weighs just 4.0 grams. This 27 × 27-mm package provides a 33% footprint savings over an equivalent QFP package.

Enhanced Thermal Performance

The latest BGA packages have enhanced thermal performance. The SuperBGA package from Amkor/Anam, for example, employs a copper heat spreader that distributes heat throughout the package. The copper "plate" also provides an EMI/RFI shield. Thus, a 356-pin, 35 × 35-mm device has a resistance (θ_{JA}) of 12.2 (°C/W) compared to a θ_{JA} of 35 (°C/W) for a 208-pin 28 × 28-mm QFP package.

Integrated Circuit Speed Advantages

As PLDs achieve increasingly higher speeds, selecting a package that offers optimal electrical performance is critical to successful integration between package and device. Poor electrical performance can result in switching noise, crosstalk, and other signal integrity problems.

The most advanced BGA packages, capable of operating well into the microwave frequency spectrum, achieve high electrical performance by using ground planes, ground rings, and power rings in the package construction. These features, when properly implemented, create current loops which yield minimum loop inductance.

Ground Plane

The effect of the SuperBGA ground plane can be seen by comparing the lead inductance of the SuperBGA with that of a QFP package. The typical signal lead self inductance for a 35 × 35-mm SuperBGA package is 2.95 to 6.45 nH (including bond wires) while that of a 40 ×40-mm 304-lead QFP package is 15.5 to 19.78 nH. The SuperBGA package achieves this advantage by positioning the ground plane 100 µm from the signal leads. No ground plane exists in the QFP package.

Ground Ring

In the SuperBGA package, bond wires connect die grounds to the ground ring, which is connected to the ground plane, a continuous sheet of metal on the side wall of the laminate (see Figure 2). This connection is formed by wrapping the metal around the internal cavity wall and onto the ground plane, creating a very low inductance interconnect. Multiple ground balls connected to the plane are strategically located on the periphery of the package to create efficient, low-inductance return paths for all signal and power traces. The resulting ground structure is 0.12 nH for a typical 35 × 35-mm package size.

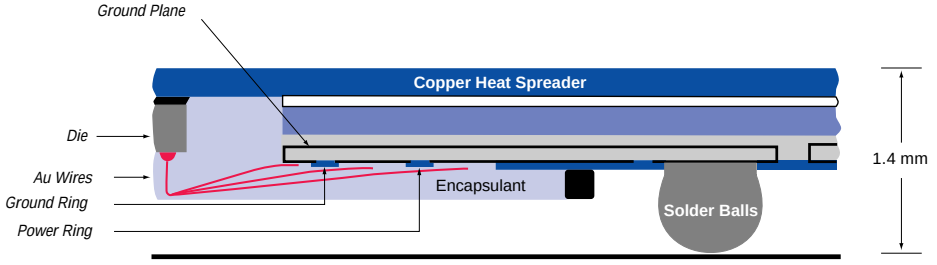
Power Ring

Power plane parasitics are reduced with the use of a power ring that is connected to traces in all four corners of the package. The traces are populated with several solder balls to ensure low-inductance interconnect to the PCB. Further power reduction is achieved with several interior traces connected to the first row of solder balls. The result is a low-inductance power network, which effectively creates mutual inductance with signal conductors. The typical inductance of the power network is 0.192 nH for a 35 ×35-mm package.

Conclusion

BGA packaging can improve any PLD design—offering advantages such as fewer damaged leads, smaller footprints, and improved electrical performance. By using BGA packaging, Altera gives designers the tools they need to face the challenges presented by higher density PLDs.

Figure 2. Ground Ring Diagram



Mapping LPM Parameters in VHDL

The library of parameterized modules (LPM) allows designers to create architecture-independent designs, while still maintaining silicon efficiency. Using LPM functions frees engineers to focus on adding value to their designs rather than spending days or weeks replicating standard logic functions. The LPM was created to allow a designer to:

- Create a complete design
- Permit architecture independence
- Separate the logical and physical portions of a design
- Support timing-driven synthesis

Designers can specify LPM functions in schematics or instantiate them in hardware description language (HDL) files. MAX+PLUS II recognizes LPM functions and uses architecture-specific design techniques to create the most efficient design. Figure 1 shows a sample VHDL Design File (**.vhd**) that includes an instance, `mymux`, of the LPM function `lpm_mux`. Each instance requires a separate entry in the VHDL code.

The `lpm_mux` function uses VHDL generics to map user-specified attributes to LPM parameters, such as size, width, and pipeline depth. VHDL generics (highlighted in blue) allow customization and pass instance-specific information to the multiplexer. For example, if additional multiplexers in this design were necessary, the designer could instantiate separate copies of the LPM multiplexer and assign appropriate parameter values of varying size, width, and depth to each copy.

In this example, the `sel` and `result` ports are only one bit wide. Because the LPM function has ports of type `STD_LOGIC_VECTOR`, you must implement `sel` and `result` as `STD_LOGIC_VECTOR` rather than `STD_LOGIC` .

For more information on how to instantiate LPM functions in VHDL, refer to MAX+PLUS II Help or ***MAX+PLUS II VHDL***.

Figure 1. Parameterized Multiplexer in VHDL

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
LIBRARY lpm;
USE lpm.lpm_components.ALL;

ENTITY  mux_ex IS
   PORT
   (
      data   : IN STD_LOGIC_VECTOR
               (1 DOWNTO 0);
      sel    : IN STD_LOGIC_VECTOR
               (0 DOWNTO 0);
      result : OUT STD_LOGIC_VECTOR
               (0 DOWNTO 0)
   );
END  mux_ex;

ARCHITECTURE lpm OF mux_ex IS

BEGIN
   mymux : lpm_mux
      GENERIC  MAP (LPM_SIZE => 2,
         LPM_WIDTHS => 1,
         LPM_PIPELINE => 0,
         LPM_WIDTH => 1)
      PORT MAP (data(0,0) => data(0),
         data(1,0) => data(1),
         sel => sel,
         result => result);
END lpm;
```

MAX+PLUS II Version 7.2 to Ship in March

Altera continues to offer new devices in new packages. By March 1997, Altera plans to ship an additional eight device/package combinations for FLEX 10K and MAX9000 devices, all of which will be supported by MAX+PLUS II version 7.2. Additional features of MAX+PLUS II version 7.2 include:

- Option to configure a chain of FLEX devices in-circuit with the BitBlaster or ByteBlaster
- Support for creating parameterizable macrofunctions in VHDL
- Improved support for FLEX 10K devices with the ClockLock™ and ClockBoost™ options

Altera's software maintenance program gives you up-to-date support for Altera devices, as well as the latest MAX+PLUS II features. For more information on how to purchase a software maintenance agreement, contact your local Altera representative.

Digital Modulator Megafunction

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The digital modulator megafunction from Nova Engineering contains a parameterized complex multiplier/mixer and quadrature output NCO. The NCO is a look-up table (LUT) that has a quadrature output, phase accumulator, and phase offset input port. The complex multiplier/mixer multiplies two user-defined inputs with the NCO outputs for amplitude modulation or frequency down conversion. Figure 1 shows a block diagram of the digital modulator megafunction.

Functional Description

The NCO contains sine and cosine LUTs that generate digital sine and cosine waveforms. The LUTs perform the following functions:

$F1[n] = \sin[2\pi n/N]$
$F2[n] = \cos[2\pi n/N]$
where: n = Address input to the LUT
N = Number of samples in the LUT
$F1[n]$ = Amplitude of sine wave at $[2\pi n/N]$
$F2[n]$ = Amplitude of cosine wave at $[2\pi n/N]$

Incrementing n from 0 to N causes the LUT to output one complete cycle of amplitude values for the sine and cosine functions. The value $2\pi n/N$ represents a fractional phase angle between 0 ($n = 0$) and 2π ($n = N$). The time (t) required to increment n from 0 to N, is the period of the sine and cosine waveforms produced by the NCO. Moreover, an m-bit phase input generates the addresses for the quadrature NCO. The LUT address increments once each system clock cycle by an amount equal to the phase input. The LUT address, or phase angle, is accumulated and stored in the phase accumulator register. The register's output is used to address the sine and cosine LUTs.

The frequency (f) of the system clock (f_{CLOCK}) is fixed. Therefore, the frequency of the sine and cosine waves produced by the NCO is:

$f = 1/T$
$= (f_{CLOCK} \times \text{phase}) \ / \ 2^m$
where: phase = Input phase angle

The `phase_offset` input modulates the NCO phase angle. The value from the `phase_offset` input is summed with the phase accumulator output. Both values, as well as the sum, are represented in two's complement format.

The complex multiplier/mixer can multiply two complex numbers represented in two's complement format. It uses a parallel-pipelined architecture that provides maximum speed. The complex multiplier/mixer performs the following function:

real + $j$imag = (a + jb) × (c + jd)
where: j = square root of -1
real = (a × c) – (b × d)
imag = (a × d) + (b × c)

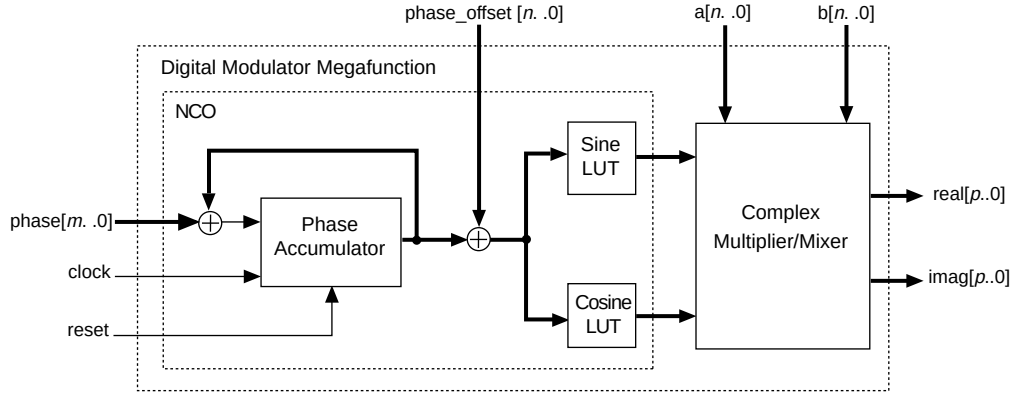
The total latency of the modulator from the phase input to the real output is 6 clock cycles. The output of the complex multiplier/mixer is registered to improve speed without increasing logic resource usage.

Parameters

Nova Engineering can customize the phase accumulator width, phase offset port width, the NCO's LUT output width, and the complex multiplier/mixer width to meet user specifications. The user can also request that functional blocks be removed or optionally bypassed. These custom-built parameters eliminate unnecessary logic and optimize the megafunction for specific applications.

continued on page 13

Figure 1. Digital Modulator Megafunction Block Diagram



Digital Modulator Megafunction
continued from page 13

Performance

Table 1 illustrates the device utilization and maximum clock frequency for a typical digital modulator function in an EPF10K20-3 device. Custom configurations will differ in logic cell usage and performance.

Table 1. Typical Device Utilization in an EPF10K20-3 Device

Implementation	Clock (f_{MAX})	Logic Cells	EABs
phase = 24 bits phase_offset = 10 bits a, b = 8 bits Outputs = 8 bits	35 MHz	662	2

Applications

The functional building blocks—the NCO, phase offset input port, and a complex multipler/mixer—allow the megafunction to implement a variety of modulators such as the amplitude, frequency, and phase.

Amplitude Modulation

The designer begins by setting the NCO to a desired frequency. To program the NCO, the designer should select the appropriate phase word and system clock and set the `phase_offset` value to zero. The NCO will generate the desired sinusoidal waveform. The complex multiplier/mixer combines the NCO output with the `a` and `b` inputs. The output signal at the `real` port is:

$$\texttt{real[p]} = (\texttt{a} \times \cos(n)) - (\texttt{b} \times \sin(n))$$

Input `b` should be set to zero. The resulting AM sinusoid appears in two's complement form at the `real` output. The user can apply binary data to the most significant bit (MSB) of port `a` to create amplitude shift keying (ASK).

Quadrature amplitude modulation (QAM) is accomplished in a similar manner, except ports `a` and `b` are used to input the complex vector to be transmitted. The QAM signal appears at the `real` output in two's complement format.

Frequency Modulation

FM requires the user to modulate the phase input to the NCO. To program the NCO to the desired center frequency, select the appropriate phase word and system clock and set the `phase_offset` value to zero.

The data source can modulate the NCO frequency in several ways. After the data signals are digitized, they are added to the `phase` input. Each time the data changes, the `phase` input changes, which consequently changes the NCO frequency. The FM deviation, or maximum frequency change, can be controlled by scaling the input data. The maximum data value should correspond to a numerical value that increases the NCO frequency to the desired upper frequency limit. The minimum data value should correspond to the two's complement of the upper frequency limit. FM deviation and symmetry are accomplished by scaling the digital data source.

In addition, binary data can change the NCO frequency by controlling the multiplexers. Binary frequency shift keying (FSK) requires two phase words and a 2-to-1 multiplexer. A binary 1 selects one phase word and a binary 0 selects the other phase word to apply to the NCO. The serial binary data stream toggles the multiplexer to select one of the two phase words. Each selected phase word controls a desired NCO frequency. The user can also create an *M*-ary FSK by combining several bits to select one of *M* phase words. For example, an *8*-ary FSK transmitter specifies one of 8 different frequencies to transmit on an 8-to-1 multiplexer using 3 select bits. The receiver then uses this frequency in a priority encoder to determine the 3 select bits.

Phase Modulation

Phase modulation is accomplished by imparting the data information onto the phase accumulator output. The `phase_offset` input port is provided for this purpose. To program the NCO to the desired frequency, select the appropriate phase word and system clock.

Binary phase shift keying (BPSK) is accomplished in the same way as FSK. That is, a 2-to-1 multiplexer selects one `phase_offset` word to apply to the `phase_offset` input port. In BPSK, the binary data transmitted can be applied to the MSB of the `phase_offset` input port. The user should set the `a` input to its maximum value and the `b` input to its minimum value (zero). The resulting BPSK waveform appears at the `real` output.

Quadrature phase shift keying (QPSK) is a composite of two BPSK waveforms in quadrature phase alignment. QPSK requires that the `a` and `b` inputs be set to the maximum value. It also requires a 4-to-1 multiplexer to select one `phase_offset` word to apply to the `phase_offset` input port. The resulting QPSK waveform appears at the `real` output port.

ADPCM Megafunction

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WWW http://www.ISS-DSP.com

The adaptive pulse code modulation (ADPCM) megafunction performs multi-channel duplex ADPCM coding in telecommunications applications. The main applications of the G.726 standard are in overload channels; i.e., carrying voice and data modem signals in DCME, particularly for modems operating in excess of 4,800 kbits per second. The main application of the G.727 standard is converting A- and µ-law PCM channels to and from variable rate embedded ADPCM channels. In this format, the megafunction is primarily used for packetized speech systems operating in accordance with the packetized voice protocol (PVP). The ADPCM megafunction is optimized for the Altera FLEX 10K architecture and combines the algorithm and architecture research of ISS with the performance and implementation advantages of the FLEX 10K family. The ADPCM megafunction is designed in a hierarchical manner to enable the high-quality implementation achieved in the lower-level blocks, such as multipliers and adders, to be carried through to the higher-level encoder and decoder blocks.

The megafunction ensures that products incorporating ADPCM can be delivered to market quickly and efficiently, and the parameterized feature ensures that the target application operating requirements are met. The megafunction can be utilized for multi-channel encoding, multi-channel decoding, and multi-channel duplex coding. See Figures 1 and 2.

Figure 1. ADPCM Decoder Block Diagram

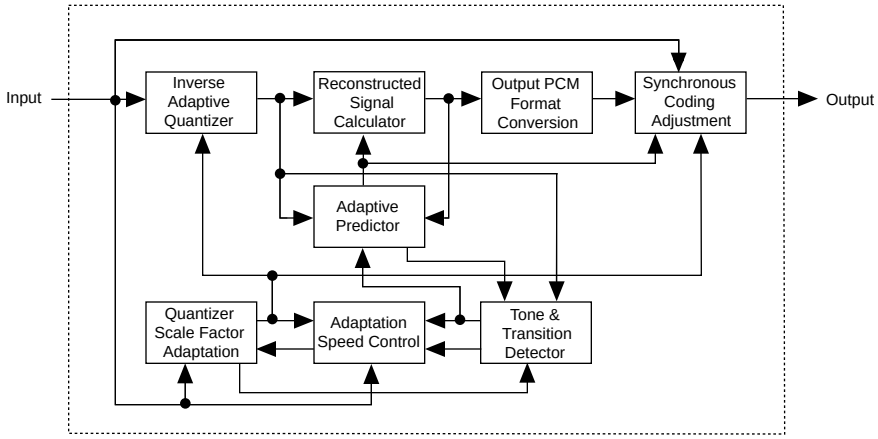
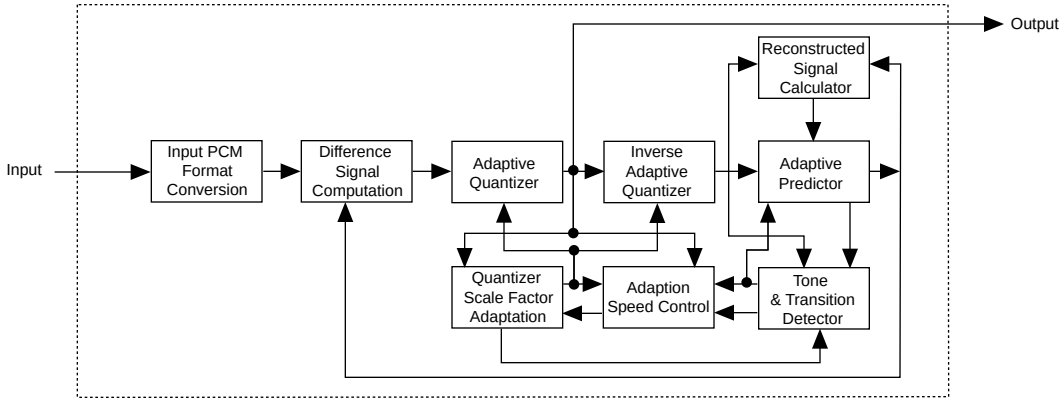


Figure 2. ADPCM Encoder Block Diagram



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Questions & ANSWERS

Q *How can a device drive a 5.0-V device with CMOS-level input pins if V_{CCIO} is 3.3 V?*

A If an Altera device drives 3.3-V and 5.0-V devices, V_{CCIO} must be connected to a 3.3-V source to ensure that the maximum V_{OH} is 3.3 V.

Most CMOS devices have TTL-level inputs, which require a V_{IH} of 2.0 V. To drive TTL-level inputs, connect V_{CCIO} to a 3.3-V or 5.0-V power supply.

For 5.0-V CMOS input pins that require a V_{IH} of 3.5 volts, use an open-drain pin to drive a trace that is pulled up to 5.0 V with a resistor. The open-drain pin will never drive high, only low or tri-state. Therefore, a connection will not exist between the 3.3-V power supply and the 5.0-V power supply (through the pull-up resistor). When the open-drain pin is active, it will drive low. When the open-drain pin is inactive, the trace will be pulled up to 5.0 V by the resistor. Because the pin can be driven at 5.0 V, the device will not be damaged.

Q *The MAX+PLUS II software guard is not recognized on my Windows NT PC. What is wrong?*

A The MAX+PLUS II software guard is not recognized because the Sentinel driver is not installed. To install the driver, follow the steps below:

Windows NT Version 3.51

1. Choose **Drivers** (Control Panel).
2. Choose **Add**.
3. Select *Unlisted or Updated Driver* from the *List of Drivers* list box and choose **OK**.
4. Type \<*path to MAX+PLUS II*>\`drivers` in the text box and choose **OK**.
5. Select *Sentinel for i386 systems* and choose **OK**.
6. Restart the PC.

Windows NT Version 4.0

1. Choose **Multimedia** (Control Panel).
2. Choose **Devices**.
3. Select *Unlisted or Updated Driver* from the *List of Drivers* list box and choose **OK**.
4. Type \<*path to MAX+PLUS II*>\`drivers` in the text box and choose **OK**.
5. Select *Sentinel for i386 systems* and choose **OK**.
6. Restart the PC.

Q *When using the Data I/O programmer to program an EPM5128 device, I receive an incorrect device ID error. What is wrong?*

A MAX 5000 devices have gone through a process change, and programming algorithms exist for devices on each process. For example, the programming algorithms for EPM5128 devices fabricated on the new process is 5128 NEW; the programming algorithm for devices fabricated on the old process is 5128.

If you are unable to determine the process on which your device was manufactured, try both algorithms. Using the wrong algorithm only provides the Data I/O programmer with the incorrect device ID and does not damage the device.

After selecting a new algorithm, the Programmer Object File (**.pof**) must be re-entered into the RAM of the Data I/O programmer. Failure to reload the POF will result in an incorrect checksum, and the device will not be programmed properly.

Q *How do I make logic assignments to individual nodes in an EDIF netlist file?*

A To make logic assignments to an individual node in an EDIF file, open the EDIF Input File (**.edf**) in MAX+PLUS II. In the Hierarchy Display, open all branches of the hierarchy tree. The hierarchy tree branches show a file name and icon for each subdesign in the hierarchy. To make a logic assignment, select a subdesign icon and choose the appropriate logic option from the Assign menu.

Q *What sockets are available for 403- and 503-pin pin-grid array (PGA) packages?*

A Altera does not manufacture sockets, but recommends that you use sockets from a third-party vendor. The following tables show available sockets, part numbers, and vendors for 403- and 503-pin PGA packages.

Zero-Insertion-Force Sockets for 403-Pin PGA Packages

Vendor	Part Number	Type	Phone Number
Yamaichi	NP-178-64401-KS14828	Open Top	(408) 456-0797
AMP	1-38230-7	Lever Arm	(800) 522-6752 (800) 331-9857 x05410
3M/Textool	2-0403-08450-390-019-002	Lever Arm	(800) 3M-HELPS (800) 421-2244

Zero-Insertion-Force Sockets for 503-Pin PGA Packages			
Vendor	**Part Number**	**Type**	**Phone Number**
AMP	382876-6	*Note (1)*	(800) 522-6752 (800) 331-9857 x05410
Yamaichi	NP-236-102002-AC01601	Lever Arm	(408) 456-0797
3M/Textool	2-0503-01357-050-002	Lever Arm	(800) 3M-HELPS (800) 421-2244

Low-Profile Printed Circuit Board Sockets			
Vendor	**Part Number**	**Type**	**Phone Number**
McKenzie	*Note (2)*	PZA Family	(510) 651-2700
Mil Max-Preci-Dip	*Note (2)*	518 Family	(516) 922-6000
Appros	*Note (3)*	*Note (3)*	(408) 567-1234

Notes:
(1) Although this socket was created for 560-pin PGA packages, it also works with 503-pin PGA packages.
(2) This socket has no standard part number. Contact the vendor for more information.
(3) Contact the vendor for more information.

Q *What Configuration EPROM should I use to configure FLEX 10KV and FLEX 10KA devices?*

You can use the EPC1 Configuration EPROM to configure FLEX 10KV or FLEX 10KA devices. Depending on how a particular Programmer Object File (**.pof**) configuration bit is set, you can program the EPC1 for 5.0-V or 3.3-V operation. MAX+PLUS II sets a configuration bit when generating the POF for the EPC1. If you compile for a FLEX 10KV or FLEX 10KA device, MAX+PLUS II will set the 3.3-V bit. If you compile for a 5.0-V device, MAX+PLUS II will not set the 3.3-V bit. Third-party programmers correctly program the EPC1 if the configuration bit is set in the POF.

Q *What happens when the preset and clear signals of a register in an Altera device are simultaneously enabled?*

A When the preset and clear signals for a register are simultaneously enabled, the output is undefined. If one of the two signals is then disabled, the other one will "win" and the register output will immediately reflect the appropriate result. This answer is true for all FLEX10K, FLEX 8000, MAX 9000, MAX7000, FLASHlogic, and MAX 5000 devices. Classic devices do not have a preset signal.

Q *Why doesn't the timing calculation using numbers from the FLEX 8000 Programmable Logic Device Family Data Sheet match the MAX+PLUS II timing calculation?*

When examining the timing for a design, you may find that the MAX+PLUS II timing calculation does not exactly match the number that you get from a computation using data sheet values. For example, you may compute the maximum registered performance to be 15 ns, while MAX+PLUS II calculates 13 ns.

This discrepancy occurs because the row and column interconnect delays change depending on fan-out and distance. A logic element (LE) in LAB A1 driving only one LE in LAB A2 may see a row delay of 2 ns, while an LE in LAB A1 driving 10 LEs—where the farthest is in LAB A20—may see a delay of 5 ns. The data sheet values for row and column delays are for a signal traversing the entire row or column with a fan-out of four, spread evenly across the row or column. A fan-out of four is used because the average fan-out of a signal is less than four. MAX+PLUS II computes the row or column delay as a function of distance and fan-out. In most cases, the MAX+PLUS II computed delay will be less than the delay calculated from data sheet values. The MAX+PLUS II calculation is always more accurate than an estimation using data sheet values.

Q *Which MAX 7000S pins are used for JTAG operation?*

A A pin-out diagram for MAX 7000S devices is available in *AB 145 (Designing for In-System Programmability in MAX 7000S Devices)*. This document is available from the following sources.

- ***Altera Digital Library*** CD-ROM
- Altera world-wide web site
- Altera FTP site

Q *Where can I find JTAG BSDL files for Altera devices?*

A Altera provides Joint Test Action Group (JTAG) Boundary-Scan Description Language (BSDL) files on the Altera FTP site (ftp.altera.com) and the Altera Bulletin Board Service (BBS) at (408) 954-0104. Files are available as a self-extracting executable for the PC (named **jtagbsdl.exe**) or as a UNIX file (named **jtagbsdl.tar**).

Q *How long should I bake dry-packed devices?*

A For information on baking dry-packed devices, go to *AN 71 (Guidelines for Handling J-Lead & QFP Devices)*, available in the Altera ***1996 Data Book, Altera Digital Library*** CD-ROM, or on the Altera world-wide web site.

Altera
VIEWPOINT

Behind the Scenes of High-Density Programmable Logic

Cliff Tong
Director, Product Marketing

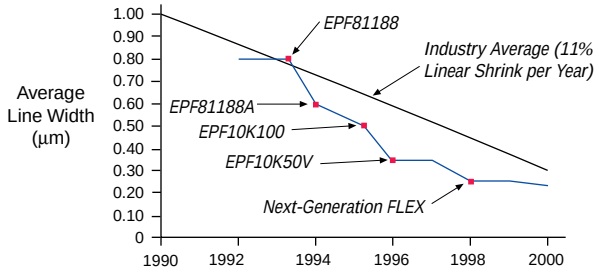
With the traditional benefits of fast time-to-market and risk reduction, high-density PLDs will increasingly become attractive as a gate array alternative for both prototyping and volume production. For the highest volumes and integration levels, designers increasingly choose standard cells, also referred to as cell-based integrated circuits (CBICs). In turn, leading ASIC suppliers have transitioned to CBICs exclusively for new product introductions. These tendencies lead to "the gate array squeeze," in which a traditional gate array no longer offers a significant density advantage compared to programmable logic nor a significant manufacturing lead time advantage compared to using a standard cell. Therefore, several industry analysts—including Dataquest—project growth of high-density programmable logic devices (PLDs) and CBICs to significantly outstrip the growth of gate arrays. See Table 1.

Table 1. The "Gate Array Squeeze"

Advantage	High-Density PLDs	Gate Arrays	Standard Cells
Time to market	✓		
Risk reduction	✓		
Integration density			✓
High-volume device cost			✓
Low-volume device cost	✓		
CAGR 1995 to 2000, *(1)*	30%	14%	25%

Note:
(1) Source: Dataquest

Figure 1. Process Technology Advancements



As PLD density increases, program-mable logic architectures must evolve. Through feedback from programmable logic users and ASIC designers, program-mable logic suppliers can make the correct decisions regarding device architecture, cost optimization, and development tools. Future users of high-density programmable logic are directly affected by these "behind-the-scenes" decisions, which involve the detail and intricacy of interconnect structures, manufacturing yields, and synthesis algorithms. While logic designers tend not to be interested in the details, they demand integration density, low cost, and ease-of-use.

Process & Interconnect Architecture: The Key Combination

Advancements in process geometry will always allow more transistors to be placed on a single device (see Figure 1). However, line widths alone provide only a partial solution to the task of creating an ideal high-density PLD. Combining advanced process technologies with device architecture has been and will remain the key element in the creation of high-density PLDs.

From the standpoint of silicon area, the most important aspect of device architecture is the interconnect structure. Interconnect consumes more die area than any other portion of the device. As a result, the challenge for PLD suppliers is to develop an interconnect structure that optimizes device fitting and routability, and minimizes delay and skew, while maintaining a die area and cost structure that meets customer requirements for volume applications. Silicon architects must realize that in order to meet the needs of the logic designer, the interconnect structure will require changes to address increasing device density.

The evolution of interconnect structure within Altera devices over the years illustrates this point. While the interconnect hierarchy has changed, the continuous nature of the interconnect remains constant (see Figure2). This continuous interconnect is fundamentally distinct from the FPGA segmented interconnect, which provides a reasonable scheme for devices of less than 10,000 gates. But, as device density grows, the segmented interconnect becomes a "rat's nest of wires" that increases die size and negatively impacts cost, device performance, and routability. Figure 3 compares the continuous interconnect structures for CPLDs to the segmented interconnect of FPGAs.

Embedded Architecture for Megafunction Integration

Increasing density drives architectural change. In addition to interconnect structure changes, logic structure changes may be needed due to the increasing level of system integration. From the ASIC world, we know that certain complex functions typically do not map well to the traditional look-up table (LUT) or product-term approach used in most PLDs. As densities grow larger than 10,000 gates, the need to integrate large blocks of on-chip RAM has accelerated. While some FPGA architectures have supported simple on-chip RAM functions, such as small FIFO functions, this approach has proven insufficient for most designs larger than 10,000 gates.

The requirement for large blocks of RAM and the integration of other megafunctions was the driving force behind the embedded architecture in Altera's FLEX 10K family. By combining embedded array blocks (EABs)—which can be used both for large RAM implementations as well as complex logic functions—with traditional logic array blocks (LABs), Altera was able to develop a high-density programmable logic architecture that could support the expanding integration needs of the system designer. Once again, a continuous interconnect structure was critical for maintaining efficiency in the connectivity between EABs and LABs. The result for the designer is system-level integration of large on-chip RAM blocks with speed and area efficiency, without the penalty of lost general-purpose logic resources.

The Question of Embedded Cores

The FLEX 10K family is the first example of a high-density, general-purpose PLD

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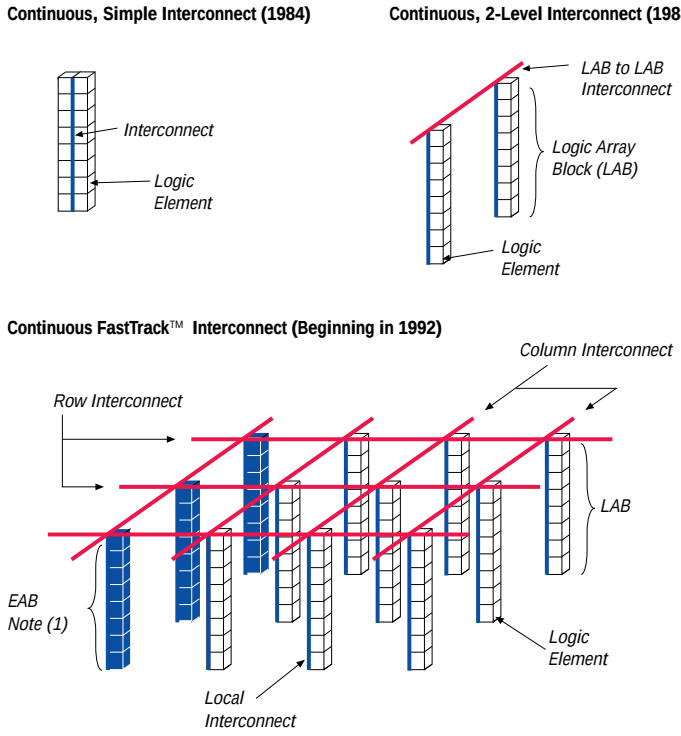
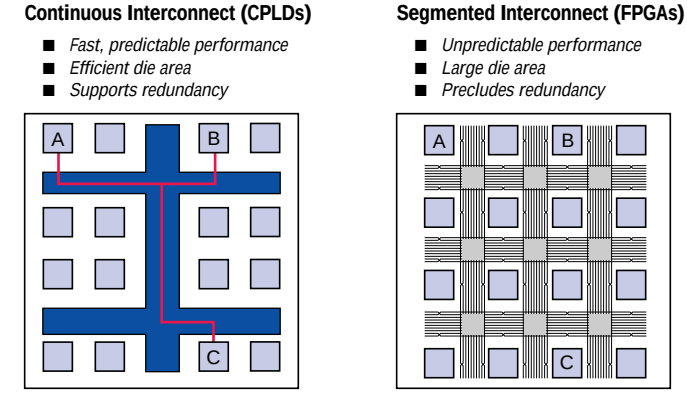
Figure 2. Evolution of Altera Device Interconnect



Note:
(1) Embedded array blocks (EABs) are only available in FLEX 10K devices, which were introduced in 1995.

Figure 3. Comparison of Continuous & Segmented Interconnects



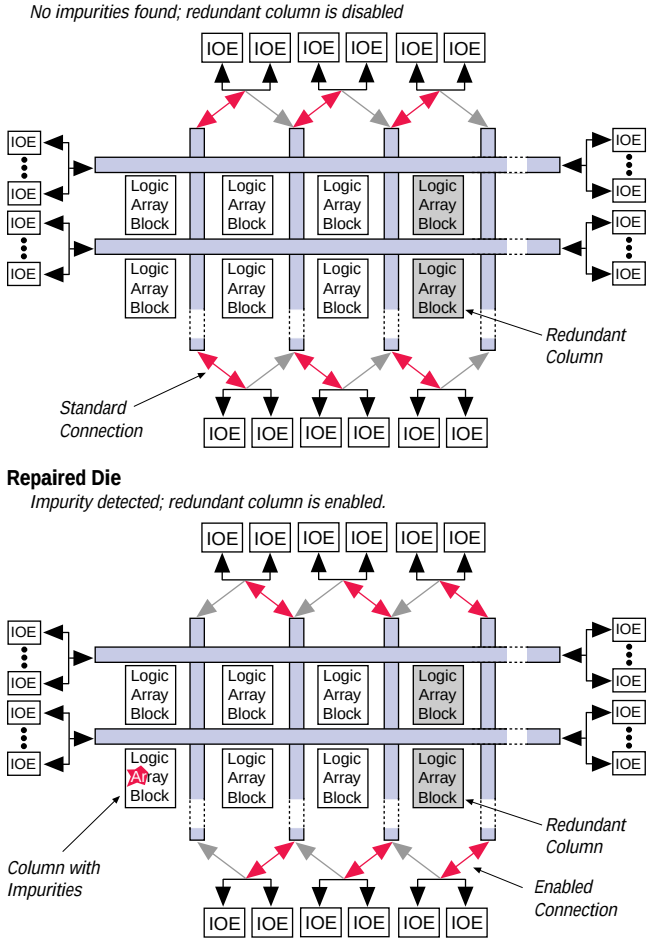
Behind the Scenes of High-Density Programmable Logic
continued from page 19

Where time-to-market and flexibility are the critical criteria, a high-density, general-purpose PLD such as a FLEX 10K device offers an architecture tailored for megafunction integration, while still allowing the system architect to modify the silicon to meet ever-changing system specifications.

with an architecture tailored for megafunction integration, but not specific to any single application. Seemingly, the next step in this integration process might be to include custom circuitry for a specific logic function and surround it with general-purpose programmable logic. Conceptually, this step seems attractive, and some PLD suppliers are beginning to posture in this direction. The resulting "embedded-core PLD" appears to "take the best of both worlds," namely, the efficiency of a custom core and the flexibility of programmable logic.

However, the key problem with this approach is that the end product would be neither a gate array nor a PLD, but it would have the downside of both. The embedded core would require metal-customization, eliminating the time-to-market advantages of a PLD. With programmable circuitry, the device would not have the lower cost of custom silicon for high-volume applications. Furthermore, the device truly becomes "application-specific" because it is "masked" for a specific application, forcing the designer to change system specifications to meet the silicon, instead of modifying the silicon to meet ever-changing system specifications. Embedded cores have their place, but are better suited for standard-cell designs where low cost and high volume are the foremost objectives. Where time-to-market and flexibility are the critical criteria, a high-density, general-purpose PLD such as a FLEX 10K device offers an architecture tailored for megafunction integration, while still allowing the system architect to modify the silicon to meet ever-changing system specifications.

Figure 4. Example of Redundant Circuitry



Cost Reduction & Redundancy

For many years, memory suppliers have pushed the leading edge of process technology by creating bigger and bigger memory devices. High-density PLDs are also created on leading-edge processes, i.e., PLD suppliers are putting as much logic density as possible on a single device, limited only by the size of the reticle that can be used in the wafer manufacturing equipment. With die size now approaching the size of a thumbnail, yielding a meaningful number of good die per wafer becomes a significant factor—not only in the cost of the device, but also in making the device widely available to a broad number of customers. One way to enhance effective die yield is by adding redundant circuitry to the device. Then, if manufacturing defects are detected on a circuit, the redundant circuit is enabled and yield recovery can be obtained (see Figure4). Circuit redundancy adds a small percentage to the actual die size, but the resulting yield recovery—on even the most advanced process technology—can be tremendous.

This technique is an effective means for yield recovery and cost reduction for memory suppliers. Altera holds numerous patents for redundancy techniques for high-density PLDs, and has used redundancy since the introduction of the MAX5000 family in 1988. Today, Altera employs redundancy on the larger members of the MAX 9000, FLEX 8000, and FLEX 10K families. Redundancy has allowed Altera to obtain better cost structures and availability for the highest density devices (see Figure 5). The continuous interconnect structure helps make redundancy applicable for high-density PLDs. In contrast, the segmented interconnect of FPGAs precludes the use of redundancy techniques.

Design Methodology

As devices grow in density, the needs of designers are changing. To help designers move towards an architecture-independent design flow, the high-density PLD industry must focus on supporting a high-level design methodology. Five years ago, designers only required EDA vendors to provide simple interfaces to PLD fitters. As device density and design complexity has grown, the requirements have expanded beyond the simple availability of an EDIF interface, to include compilation results. For example, Altera currently focuses on the quality and efficiency of hardware description language (HDL) synthesis, architectural mapping, and point tool integration. This focus is stimulated by a growing need for a more traditional ASIC design methodology and support for design re-use.

Megafunctions developed through the Altera Megafunction Partners Program℠ (AMPP℠) and Altera's own MegaCore™ functions provide a variety of intellectual property functions to a broad programmable logic user base. Megafunctions accelerate the time-to-market aspect of programmable logic and allow designers to focus on system enhancement and differentiation, instead of "reinventing the wheel."

Altera's ACCESS℠ program ensures that EDA vendors obtain the necessary information and training to support new programmable logic architectures. Strategic alliances such as the Altera/Synopsys partnership improve the melding of synthesis and fitting algorithms, ultimately leading to optimized results and an architecture-independent solution for the system designer (see Figure 6).

Conclusion

As Altera and other programmable logic suppliers create devices with ever-increasing density levels, critical decisions about architecture and design methodology have a far-reaching impact on the bottom-line issues that concern the logic designer. Higher densities will render previous architectures and software algorithms obsolete; old methods will need to be modified. Silicon architects must focus on an optimized and continuous interconnect structure combined with a programmable architecture that supports megafunction integration. Likewise, megafunction expertise and breadth—along with optimized synthesis and mapping algorithms—are necessary for an efficient design methodology. When these silicon and design methodology goals are met, high-density programmable logic users will fully obtain the advantages of low cost, fast time-to-market, and flexibility of change.

Megafunctions accelerate the time-to-market aspect of programmable logic and allow designers to focus on system enhancement and differentiation, instead of "reinventing the wheel."

Figure 5. Yield Improvements with Redundancy

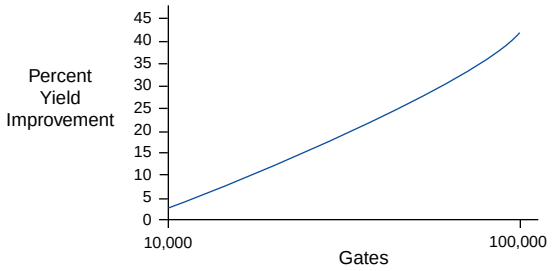
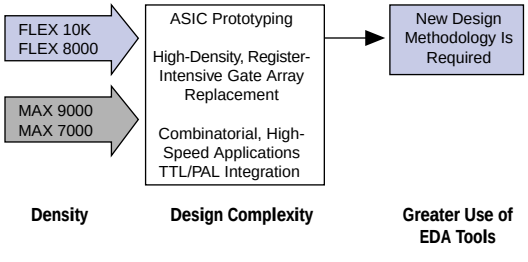


Figure 6. High-Density Design Methodology



Customer APPLICATION

FLEX DSP Maintains Intermec's Image as a World Leader

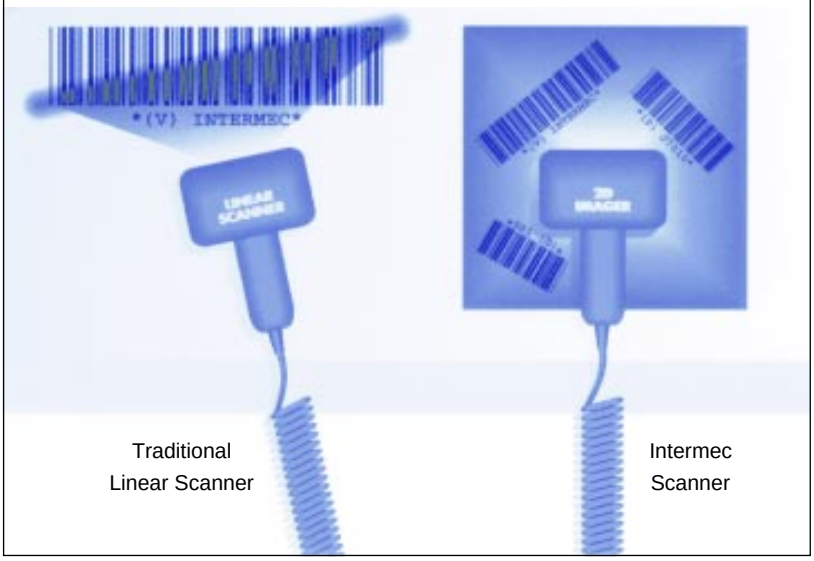
"I initially didn't think it was possible to achieve the kind of integration I needed using a programmable logic device—until I contacted Altera and discussed it with them."
—Ken Coffman, Intermec Design Engineer

Intermec Imaging Systems, an industry leader in automated data collection, maintains the world's largest installed base of omnidirectional CCD imaging technology. Intermec's CCD-based scanners can read information symbols in any orientation, ranging from familiar bar codes such as UPC, Postnet, and Code39 to two-dimensional codes such as PDF-417 and Data Matrix (see Figure1). As an industry leader, Intermec continuously researches and updates its products using the latest, most reliable, and cost-efficient technology. Accordingly, when Intermec designers were designing a new scanner, they chose Altera FLEX8000 devices to realize their goals.

Intermec Engineer Ken Coffman assisted in the design of the new scanner. One of his tasks included the implementation of an N × M transformation function that performs high-pass filtering to accentuate the edges in the captured image of an information symbol. Previously, this function was performed with an off-the-shelf filter device. Coffman was concerned with the long-term availability of the off-the-shelf filter, as well as the overall cost. For the redesign, Coffman wanted to reduce costs, use more readily available devices, and create a scaleable design that could be reused in future products. Therefore, he investigated the possibility of placing the filter design into a programmable logic device (PLD).

Figure 1. Intermec vs. Traditional Scanners

Advanced Intermec scanners read multiple signals omnidirectionally. In contrast, traditional linear scanners require careful alignment of the scanner to the symbol.



The Need for a Cost-Effective DSP Solution

Intermec's design, like most DSP filtering designs, multiplies the incoming image data by a set of filter coefficients and sums the results. Because multiplication is typically a resource-intensive function for implementation in programmable logic, Coffman was concerned about the amount of PLD device resources required by the filter design, and thus, the cost of the device.

Coffman decided to contact Altera for assistance. His local field applications engineer directed him to Altera's MegaCore design group—Altera engineers who develop large-scale building blocks for programmable logic. After a few discussions of the design needs and constraints, Coffman was convinced that he could successfully build a filter design that would more than satisfy his needs and use far fewer device resources than he had thought, resulting in an overall cost savings.

"I initially didn't think it was possible to achieve the kind of integration I needed using a programmable logic device—

until I contacted Altera and discussed it with them," Coffman stated.

Developing an Optimized Video Filter

The video filter in Intermec's new scanner implements a spatial finite impulse response (FIR) filter with a 3 × 3 filter kernel. The filter uses a center pixel (p5) and its eight neighbors (p1 through p4, p6 through p9) to calculate the value of a new pixel (see Figure 2).

Figure 2. Filter Matrices

Filter Coefficient Matrix (Kernel)

N

c1	c2	c3
c4	c5	c6
c7	c8	c9

M

Input Pixel Matrix

N

p1	p2	p3
p4	p5	p6
p7	p8	p9

M

The new pixel value, p(out), is calculated by multiplying the input pixels by the coefficients in their respective kernel positions and summing the results as shown in the following formula:

$$p(out) = (p1)(c1) + (p2)(c2) + (p3)(c3) + (p4)(c4) + (p5)(c5) + (p6)(c6) + (p7)(c7) + (p8)(c8) + (p9)(c9)$$

To illustrate this process, consider a mathematical average. In this case, the kernel coefficient matrix would contain the value 0.11 (1 divided by 9) in each position and the output pixel value would simply be the average of the nine input pixels. The filter kernel values can be changed to highlight or blur the differences in individual pixel values. For example, positive kernel values result in low-pass filtering, in which the value of a pixel's neighbors are summed and averaged, causing the image to become blurred and smoother. Negative numbers result in high-pass filtering, in which neighboring pixels subtract from the center value, resulting in a greater difference between pixels, thus a sharper image.

From inspecting the coefficient values in the filter kernel, the "intensity" of the filtering action can be judged. If the center has a large value compared to the neighbors, then the center dominates the output, and vice versa.

To reduce complexity of the logic in Intermec's filter, the resolution and range of the coefficient values were selected to fit in 4 bits with a resolution of 0.125.

Coffman worked with an Altera engineer to devise a programmable logic implementation scheme that would make the coefficient multiplication faster and less resource-intensive. The approach was based on the following facts:

- In binary mode, multiplication by integers that are powers of two is the equivalent of shifting the number to the left (i.e., multiplying by 2 = shift left by one place; multiplying by 4 = shift left by two places). Similarly, division by powers of two is the equivalent of shifting to the right.
- Any integer can be expressed in powers of two (i.e., $1 = 2^0$, $4 = 2^2$, $12 = 2^2 + 2^3$, etc.).
- The coefficients of the selected filter kernel were constrained to a range ±1.875 with 4 bits of resolution (0.125 per bit).

As a result, Coffman was able to replace all of the multipliers in the filter with shift registers and other logic, using far fewer resources. In fact, this design approach used about 60% fewer device resources than the traditional design method using full multipliers. "The Altera engineer showed me how I could design the filter such that it took up less than half of the resources I thought it would," Coffman explained.

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FLEX DSP Maintains Intermec's Image as a World Leader continued from page 23

Designing for the Future

Coffman's final goal for the video filter was to create a design that could be scaled and upgraded in the future. He created the design using the Altera Hardware Description Language (AHDL), which allowed him to define arrays of registers for the filter's shift operations with simple, in-line references. For example, the following reference sets up two groups of registers (D flipflops) and defines the logical relationship between them:

```
reg0_[9..0]:dff;
pix10_in[7..0]:dff;
reg0_[] = (gnd,pix10_in[],gnd) +
          (gnd,gnd,pix10_in[]);
```

The two register banks consist of a 10-bit register called `reg0` and an 8-bit register called `pix10_in`. The register `pix10_in` holds the tap value that is multiplied by the first coefficient of the filter kernel. The last line in the example above shows how the 8-bit value `pix10_in` is shifted (corresponding to the multiplication operation), "padded" with zeros (the `gnd` values), and summed with itself to become a 10-bit value that is stored in `reg0`. The size of these registers can be altered by changing the values in the first two lines of the example (i.e., 9 or 7), and the shifting operation can be controlled by changing the position of the tap values in the last line. These changes can be made in the future if the filter module must produce a value of higher precision, or if the filter kernel must be modified. Figure 2 provides a block diagram of the filter.

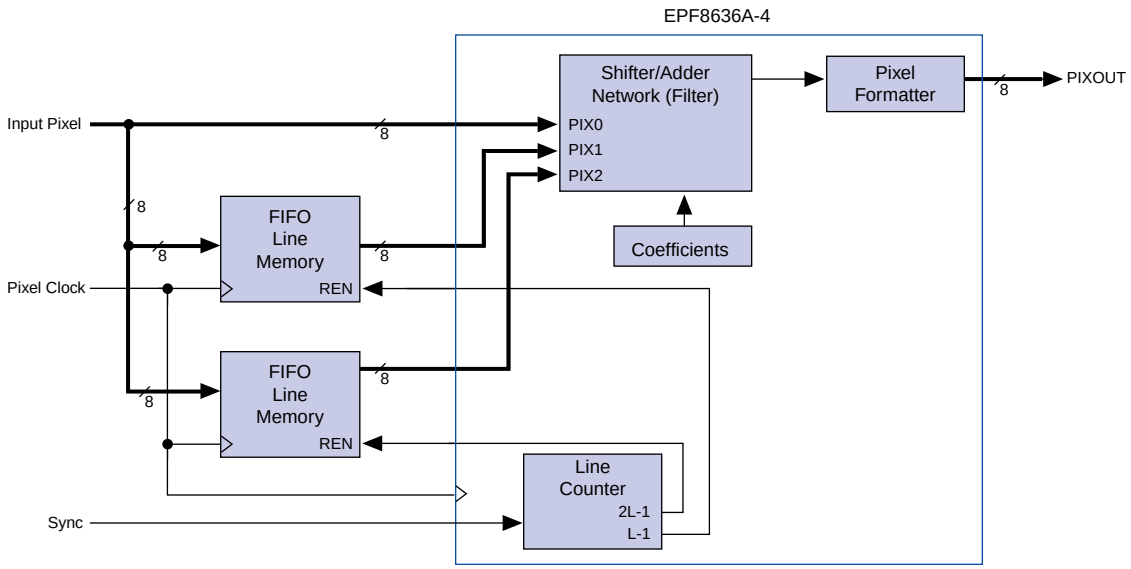
Currently, the filter operates at a speed easily achieved in the lowest speed grade of the target FLEX 8000 device (an EPF8636A-4). As a result, future redesigns could easily accommodate higher speeds. In addition to using a device in a higher speed grade, Coffman can transfer the video filter design to any Altera PLD. With Altera's MAX+PLUS II development software, retargeting a design for another Altera device is as simple as choosing the device name from a menu and recompiling the design.

Another enhancement considered by Coffman is the ability to choose between different sets of imaging coefficients to compensate for different lighting conditions. This feature can be added by creating different programming files for each coefficient set and downloading the appropriate file into the target device.

Conclusion

With Altera devices and software, Intermec was able to meet the goals of the scanner design. "Using FLEX 8000 devices resulted in a more cost-effective, smaller, and faster solution than using off-the-shelf video filters," Coffman said. "Combined with Altera's MAX+PLUS II software, it was the most painless way to get our design up and running."

Figure 2. Intermec Filter Block Diagram



Altera Technical Customer Support

Originating in 1984, the Altera technical support hotline staff has grown from a small core of individuals into a team of over 20 Applications Engineers, who provide prompt, courteous, and accurate technical support. To better support customers, Altera created the Applications Response Center (ARC), which is staffed by engineers who provide focused support for both hotline calls (800) 800-EPLD and e-mail messages (**sos@altera.com**). This article discusses the success Altera has had with the ARC and how Altera plans to enhance technical customer support in the future.

The Altera technical support team is dedicated to the following objectives:

- Fast customer access to an Applications Engineer
- Accurate responses
- Timely responses

Altera established a customer satisfaction survey to determine the effectiveness of these objectives. The survey is targeted for those using the hotline and **sos@altera.com**.

Fast Access to an Engineer

During 1996, the Altera technical suppport staff handled over 45,000 customer calls and 3,000 e-mail messages. Altera provides fast access to an engineer for hotline callers by extensive staffing in the ARC. In the survey, customers expressed satisfaction with how quickly they were able to get through to an engineer.

The wait experienced by hotline callers in the second half of 1996 is summarized below:

- 63% of the hotline callers reached an engineer immediately
- 86% of the callers reached an engineer within 2 minutes

Accurate, Timely Responses

In the survey, Altera asked customers to rate (on a scale from 1 to 10) their satisfaction with the accuracy of the answers received and the response times for problems that could not be resolved immediately over the telephone. The results for the second half of 1996 showed that:

- *Accurate responses*—Customer satisfaction with the response accuracy rose from 7.8 in the third quarter of 1996 to 8.4 in the fourth quarter.

- *Timely responses*—Customer satisfacton with response timeliness rose from 8.0 in the third quarter 1996 to 8.3 in the fourth quarter.

Expanded Hotline Hours

Beginning March 25, 1997, the hotline operating hours will be from 6:00 AM to 6:00 PM Pacific Time. The expanded hours will help Altera provide better service to customers in the eastern time zone of North America. The ARC is fully staffed with technical support engineers during all operation hours.

Reduced caller wait on the hotline and expanded operation hours are two examples of Altera's dedication to provide the most comprehensive and easily accessible technical support available.

You can use the following methods to contact Altera technical support:

Hotline	(800) 800-EPLD
E-mail	**sos@altera.com**
Fax	(408) 954-0348
Bulletin board service (BBS)	(408) 954-0104
FTP site	**ftp.altera.com**
World-wide web	**http://www.altera.com**

If you have any comments or questions concerning the quality of technical support you have received from Altera Applications, contact the Customer Support Manager at **daleh@altera.com**.

Introducing Altera Technical Support (Atlas) On-Line Service

The Altera Applications technical support staff is dedicated to providing the most comprehensive and easily accessible technical support available. On February 10, 1997, Altera deployed the Altera Technical Support (Atlas) service on the Altera world-wide web (WWW) site. The Atlas service provides:

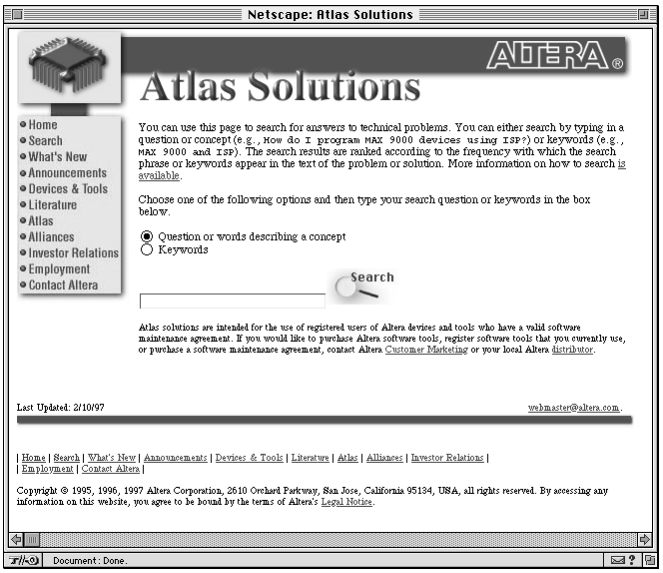
- Searchable knowledge-base of technical solutions with hyperlinks to related information
- Customer training information
- Searchable collection of technical articles

The highlight of the Atlas service is the technical solutions: 150 are currently available and the total will be expanded to 500 by July 1997. Altera plans to add example design files in April 1997.

Altera Applications engineers generate solutions from frequently asked customer questions. Solutions exist for all Altera device families, MAX+PLUS II software, third-party EDA tools, as well as Altera and third-party programming hardware. You can search the Atlas solutions via a keyword, question, or concept; the results are listed in order of confidence or by subject.

You can go to the Atlas solutions page to send feedback, ask for clarification on an existing solution, or e-mail a new question to the Altera technical support staff. All e-mail is promised a 24-hour response.

The Atlas solutions will be continually updated to ensure accurate, up-to-date information. For more information on Atlas, go to Altera's WWW site at **http://www.altera.com**.



Graduating Engineers with CPLD Design Experience

Altera partners with universities around the world to support quality education programs for engineering students. The Altera University Program provides engineering students with state-of-the-art development tools and programmable logic devices (PLDs) for designing, simulating, analyzing, and prototyping digital logic designs in a university environment. The newly launched "Certification in CPLD Design" program rewards students for their work in CPLD design. By participating in the program, students gain hands-on experience with Altera tools and devices, gaining the knowledge they need for success in today's competitive job market.

Certification confirms that a student is able to solve a significant design problem using Altera tools and devices. Students use MAX+PLUSII to create, compile, and verify a design, as well as to program or configure an Altera device, giving them experience in all phases of the design process. Students then submit information about their project, including an abstract, that is posted on Altera's world-wide web site.

For more information about the certification process or to view student abstracts, go to the University Program pages on Altera's world-wide web site.

Altera Target Applications

As the density of programmable logic devices (PLDs) moves toward 250,000 gates, high-performance, function-based building blocks become increasingly important. Altera addresses this need with the Target Applications program, which focuses on the following areas:

- FLEX DSP
  - DSP building blocks
  - DSP imaging
  - DSP wireless and broadband communications
- Bus interfaces
  - Peripheral component interconnect (PCI)
  - Universal serial bus (USB)
- Communications
  - Data communications and telecommunications
  - Asynchrous transfer mode (ATM)

FLEX DSP

Altera's DSP solution includes an abundance of new reference designs and megafunctions, including the ADPCM transcoder megafunction from Integrated Silicon Systems (ISS), an image processing library (also from ISS), as well as the `round` and `saturate` reference designs from Altera. DSP solutions are divided into two categories: DSP building blocks (generic functions that can be used in any DSP application) and application-specific DSP megafunctions that typically focus on imaging or wireless communications. See Table 1.

Wireless and broadband communications incorporate building blocks that enable system designers to optimize function performance early in the design cycle. Target applications for these solutions include CDPD, cellular basestation, PCS, ADSL, and cable modem functions. Building blocks include numerically controlled oscillators (NCOs), complex mixers, ADPCM, linear phase shift registers, and fast Fourier transform (FFT) functions (see Table 2). For the latest information, go to the Altera world-wide web site.

Bus Interfaces

PCI megafunctions are currently available from AMPP partners and Altera. Two AMPP partners (Eureka Technology and PLD Applications) have delivered PCI master/target megafunctions, both running at 33 MHz. Altera's combined PCI master/target MegaCore function is currently available as a beta product; production release is scheduled for April 1997.

Target Applications Selector Guide & CD-ROM

The new *Target Applications Selector Guide* provides you with a complete listing of megafunctions, reference designs, and technical documentation. The CD-ROM provides details about these applications, including reference designs and a variety of technical literature. For a copy, contact Altera Literature Services.

Table 1. DSP Building Blocks

Function	Source
Parallel FIR filters	DSP Design Kit, version 1, Altera Target Applications CD-ROM
Serial FIR filters	
Floating-point multiplier	
Floating-point adder/subtractor	
Integer divider	
3 × 3 video convolver	
Saturate	DSP Design Kit, version 2, Altera Target Applications CD-ROM
Round	
FFT MegaCore function	MAX+PLUS II migration product
Parameterized multiplier	MAX+PLUS II
Square root functions	ISS
Floating-point library	
Adaptive FIR filter	
IIR filter	
FIR filter library	
Image processing library	
ADPCM	
Reed-Solomon CODEC	ISS and Systolic Technology
Discrete cosine transform	ISS
JPEG encoder/decoder	ISS and Synova Inc.
Decimator	FASTMAN

Table 2. Wireless & Broadband Communications Megafunctions

Megafunctions	Source
FFT MegaCore function	MAX+PLUS II migration product
Reed-Solomon CODEC	ISS and Systolic Technology
NCO	Nova Engineering Inc.
Complex mixer/multiplier	
Linear feedback shift register	
Digital modulator	
Bit synchronizer	
Binary correlator	
Convolutional interleaver	Ktech Telecommunications
ADPCM	ISS
Adaptive FIR filter	
Decimator	FASTMAN

What's New with AMPP

Altera has taken a leadership position in providing megafunctions for use in programmable logic devices (PLDs). At the start of the Altera Megafunction Partners Program℠ (AMPP℠), intellectual property (IP) developers were invited into the program and megafunctions were targeted for development. As the program grew, Altera formalized the megafunction development process. The AMPP megafunction development process typically follows the sequence listed below.

1. Megafunctions are defined from the following broad categories:
   - Buses and interfaces
   - Processors and peripherals
   - Telecommunications and data communications
   - Digital signal processing (DSP) for imaging
   - DSP for communications
2. Key customers and Altera sales staff are surveyed to determine which megafunctions may be useful, offer a compelling market advantage, and have a fair chance of commercial success.
3. Each AMPP partner then selects a megafunction that fits its expertise. In many cases, the megafunction already exists, typically in register transfer level (RTL) form.
4. The megafunctions from each AMPP partner are promoted by Altera through focused marketing, such as the ***AMPP Catalog***, Altera web site, Target Applications, solution briefs, and in-person visits to potential customers by sales and technical staff.
5. Altera supports megafunction customers during implementation of megafunctions into their designs and provides expertise to solve fitting, timing, and similar problems.
6. Altera records user experiences and success stories and relays this information to the AMPP partners. AMPP customer input is crucial to the success of the program because it provides real-world feedback on which megafunctions are useful and successful. Altera will continue to use customer input to fine-tune AMPP and to provide quality megafunctions in a timely and cost-effective manner.

AMPP Training Program (AMPPCON)

Before developing Altera megafunctions, AMPP partners attend an aggressive training course, called AMPPCON. AMPPCON gives partners the knowledge they need to successfully implement their megafunctions in Altera PLDs. Generally, AMPP partners have an RTL background, so AMPPCON is their first exposure to programmable logic. Through two days of intensive, hands-on training at AMPPCON, and through follow-up by Altera factory and field engineering staff, Altera ensures that AMPP partners are thoroughly qualified. After the training, the partners prove to be excellent sources of creativity and feedback on Altera tools and architectures.

Now Available: AMPP Catalog Version 2

The ***AMPP Catalog*** version 2 is now available. Contact Altera Literature Services or your Altera sales representative for a copy. The ***AMPP Catalog*** is also available on the Altera world-wide web site.

Nova Engineering Discovers LFSR Compatibility

During recent megafunction development, AMPP partner Nova Engineering (Nova) discovered a special compatibility between the linear feedback shift register (LFSR) megafunction and the product-term-based MAX architecture.

Nova—a company that specializes in megafunctions that serve the communications industry—develops products that are primarily designed for the FLEX10K family because of the density and embedded memory of these devices. Nova also retargets their megafunctions for the MAX 9000 and MAX 7000 families to evaluate the megafunctions' performance in these product-term architectures. Typically, Nova megafunctions fit better and run faster in FLEX devices than in MAX devices. However, with the LFSR megafunction, Nova found that the function in MAX 9000 or MAX7000 devices far outperformed the FLEX devices. After some research, Nova discovered that the complex, combinatorial nature of product-term logic was a perfect fit for the LFSR megafunction.

The LFSR megafunction uses complex combinatorial logic and user-defined feedback to generate long sequences of random data, encryption sequences, and scrambling/descrambling patterns. These functions are performed using a linear feedback algorithm based on XOR/XNOR logic.

For example, the 32-bit LFSR fits into 103 macrocells and runs at 92 MHz in -10 speed grades of the EPM7128. Even at this small size, the user can program the initial value and define the pattern length and bit size. The product terms in the MAX architectures are ideally suited to implement this class of function. The same function in EPF10K10 devices in -4 speed grades requires 317 logic elements and runs at 86MHz, which provides good performance but is less resource-efficient.

Because of this discovery, Nova has gained greater understanding of the differences between product-term-based MAX devices and LE-based FLEX devices. Nova can use this information to tailor megafunctions for the strengths of either architecture.

AMPP partners use their knowledge and experience to improve the density and performance of their megafunctions. When AMPP partners share this type of knowledge, Altera is able to adjust the MAX+PLUSII software and the AMPP program to take advantage of the new information. In this way, the AMPP program benefits all users of Altera devices, not just those customers who are licensing AMPP megafunctions.

ADPCM Megafunction continued from page 15

Frequently-Asked Questions

Q *Can the megafunction be used for a number of different coding rates within one application?*

A The ADPCM megafunction supports all four coding rates (5-, 4-, 3-, and 2-bit), as well as six CCITT standards (G.721, G.723, G.726, G.726a, G.727, G.727a), and both A- and µ-law PCM formats. The control bits enable the user to select the operating format.

Q *Can the megafunction be used for a single coding rate, single PCM law, and single ADPCM coding standard?*

A When instantiating the ADPCM megafunction, the control bits can be used to select the desired coding rate. Depending on the coding rate selected, the function may use less logic. The Altera MAX+PLUS II software will automatically minimize the design, removing the unused logic.

Q *What is the difference between the G.726 and G.727 CCITT standards?*

A The G.726 standard is a fixed ADPCM algorithm for conversion to and from 64 kbits per second and 40, 32, 24, and 16 kbits per second. The algorithms of the G.727 standard quantize the signal into core and enhancement bits. The core bits are used for precision while the enhancement bits are used to reduce the quantization noise in the reconstructed signal. The core bits must reach the decoder, but the enhancement bits can be discarded to alleviate congestion. (The G.726a and G.727a represent modifications to the standards.)

Altera Device Selection Guide

All current information for the Altera FLEX 10K, FLEX 8000, MAX 9000, and MAX 7000 devices is listed here. Information on other Altera products is located in the Altera ***1996 Data Book***. Contact Altera or your local sales office for current product availability.

FLEX 10K Devices Note (1)

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	TEMP.	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin QFP	59, 107, 134	C	-3, -4	720	576	6,144
EPF10K10A		144-Pin TQFP, 208-Pin QFP	107, 134	I	-4			
EPF10K20	20,000	144-Pin TQFP, 208-Pin QFP, 240-Pin QFP	107, 147, 189	C	-3, -4	1,344	1,152	12,228
EPF10K20A		144-Pin TQFP, 208-Pin QFP, 240-Pin QFP	107, 147, 189	I	-4			
EPF10K30	30,000	144-Pin TQFP[1], 208-Pin QFP, 240-Pin QFP, 356-Pin BGA	107, 147, 189, 246	C	-3, -4	1,968	1,728	12,228
EPF10K30A		208-Pin QFP, 240-Pin QFP	147, 189	I	-4			
EPF10K40	40,000	208-Pin QFP, 240-Pin QFP	147, 189	C	-3, -4	2,576	2,304	16,384
EPF10K40A								
EPF10K50	50,000	240-Pin QFP, 356-Pin BGA, 403-Pin PGA *(2)*	189, 274, 310	C	-3, -4	3,184	2,880	20,480
EPF10K50V		240-Pin QFP	189	I	-4			
EPF10K50A								
EPF10K70	70,000	240-Pin QFP, 503-Pin PGA	189, 358	C	-3, -4	4,096	3,744	18,432
EPF10K70A								
EPF10K100	100,000	356-Pin BGA *(3)*, 503-Pin PGA, 596-Pin BGA *(3)*	274, 406, 406	C	-3, -4	5,392	4,992	24,576
EPF10K100A								
EPF10K130V	130,000	596-Pin BGA, 599-Pin PGA	470	C	-3, -4	7,126	6,656	32,768
EPF10K130A								
EPF10K250A	250,000	596-Pin PGA, 599-Pin BGA	C.F. *(4)*	C	-3, -4	C.F.	C.F.	C.F.

Notes:
(1)Contact Altera for FLEX 10KA device availability.
(2)Not available in FLEX 10KA devices.
(3)Available in FLEX 10KA devices only.
(4)Consult Altera for this information.

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS *(1)*	TEMP.	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C	A-2	282	208
		84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-3		
		84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-4		
EPF8282AV *(2)*	2,500	100-Pin TQFP	78	C	A-4	282	208
EPF8452A	4,000	160-Pin PQFP	120	C	A-2	452	336
		84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C, I	A-3		
		84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C, I	A-4		
EPF8636A	6,000	208-Pin PQFP	136	C	A-2	636	504
		84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	C	A-3		
		84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	C, I	A-4		
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	112, 120, 152	C	A-2	820	672
		144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	C	A-3		
		144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	C, I	A-4		
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C	A-2	1,188	1,008
		208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-3		
		208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-4		
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-2	1,500	1,296
		240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C, I	A-3		
		240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-4		

Notes:
(1)Four I/O pins are dedicated inputs.
(2)A "V" indicates a 3.3-V voltage supply.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS (1)	TEMP.	SPEED GRADE
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	C	-15
		84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	C, I	-20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C	-15, -20
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C	-15
		208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C, I	-20

Note:
(1)Four I/O pins are dedicated inputs.

MAX 7000 Devices

DEVICE	MACRO-CELLS	PIN/PACKAGE OPTIONS	I/O PINS	TEMP.	SPEED GRADE	t_{PD} (ns)	f_{CNT} (MHz)
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-5	5	178.6
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-6	6	150
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-7	7.5	125
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C, I (1)	-10	10	100
EPM7032	32	44-Pin PLCC/TQFP	36	C, I	-12 (2)	12	90.9
EPM7032	32	44-Pin PLCC/TQFP	36	C, I	-15 (2)	15	76.9
EPM7032V (2)	32	44-Pin PLCC/TQFP	36	C	-12	12	90.9
EPM7032V (2)	32	44-Pin PLCC/TQFP	36	C	-15	15	76.9
EPM7032V (2)	32	44-Pin PLCC/TQFP	36	C, I	-20	20	62.5
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC (2), 84-Pin PLCC, 100-Pin PQFP/TQFP (1)	36, 52, 68	C	-6	6	150
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC (2), 84-Pin PLCC, 100-Pin PQFP/TQFP (1)	36, 52, 68	C	-7	7.5	125
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC (2), 84-Pin PLCC, 100-Pin PQFP/TQFP (1)	36, 52, 68	C, I (1)	-10	10	100
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-12 (2)	12	90.9
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C, I	-15 (2)	15	76.9
EPM7096S	96	84-Pin PLCC, 100-Pin PQFP/TQFP	52, 64, 76	C	-6	6	150
EPM7096, EPM7096S	96	68-Pin PLCC (2), 84-Pin PLCC, 100-Pin PQFP/TQFP (1)	52, 64, 76	C	-7	7.5	125
EPM7096, EPM7096S	96	68-Pin PLCC (2), 84-Pin PLCC, 100-Pin PQFP/TQFP (1)	52, 64, 76	C, I (1)	-10	10	100
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-12 (2)	12	90.9
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C, I	-15 (2)	15	76.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP (1), 160-Pin PQFP	68, 84, 100	C	-7	7.5	125
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP (1), 160-Pin PQFP	68, 84, 100	C, I (1)	-10(P)	10	100
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12 (2)	12	90.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP (1), 160-Pin PQFP	68, 84, 100	C, I	-15	15	76.9
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20 (2)	20	62.5
EPM7160S	160	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	64, 84, 104	C	-7	7.5	125
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP/TQFP (1), 160-Pin PQFP	64, 84, 104	C, I (1)	-10(P)	10	100
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12 (2)	12	90.9
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP/TQFP (1), 160-Pin PQFP	64, 84, 104	C, I	-15	15	76.9
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20 (2)	20	62.5
EPM7192S	192	160-Pin PQFP	124	C	-7	7.5	125
EPM7192S	192	160-Pin PQFP	124	C	-10	10	100
EPM7192E	192	160-Pin PQFP/PGA	124	C	-12(P)	12	90.9
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA (2)	124	C, I (1)	-15	15	76.9
EPM7192E	192	160-Pin PQFP/PGA	124	C, I	-20 (2)	20	62.5
EPM7256S	256	160-Pin PQFP, 208-Pin RQFP	132, 164	C	-7	7.5	125
EPM7256S	256	160-Pin PQFP, 208-Pin RQFP	132, 164	C	-10	10	100
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA (2), 208-Pin RQFP	132, 164	C	-12(P)	12	90.9
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA (2), 208-Pin RQFP	132, 164	C, I (1)	-15	15	76.9
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C, I	-20 (2)	20	62.5

Notes:
(2)Not available in MAX 7000S devices.
(1)Available in MAX 7000S devices only.

Data I/O Programming Support

Data I/O provides programming hardware support for select Altera devices. Algorithms are supplied via Data I/O's Keep Current Express - Bulletin Board Service (KCE-BBS). Programming support for Configuration EPROM, MAX 9000, and MAX 7000 devices is shown below. All information is subject to change. Data I/O customers with a current maintenance agreement can obtain qualified algorithms electronically from the KCE-BBS.

The following Configuration EPROM devices are supported by the 2900 version 5.3, the 3900 version 5.3, and UniSite version 5.3.

- EPC1213P-8
- EPC1213L-20
- EPC1064P-8
- EPC1064L-20
- EPC1064T-20
- EPC1064VL
- EPC1064VT
- EPC1P-8
- EPC1LC-20

The following MAX 9000 and MAX 7000 devices are supported by the 3900 version 5.3 and UniSite version 5.3.

MAX 9000 Devices

- EPM9320LC84
- EPM9320GC280
- EPM9320RC208
- EPM9400RC208
- EPM9400RC240
- EPM9480RC208
- EPM9480RC240
- EPM9560GC280
- EPM9560RC240
- EPM9560WC208
- EPM9560RC304

MAX 7000 Devices

- EPM7032L-44
- EPM7032Q-44
- EPM7032T-44
- EPM7032VL-44
- EPM7032VT-44
- EPM7064L-44
- EPM7064L-68
- EPM7064L-84
- EPM7064Q-100
- EPM7096L-68 (EPROM)
- EPM7096L-84 (EPROM)
- EPM7096Q-100 (EPROM)
- EPM7096L-68 (EEPROM)
- EPM7096L-84 (EEPROM)
- EPM7096Q-100 (EEPROM)
- EPM7128L-84
- EPM7128Q-100
- EPM7128Q-160
- EPM7128EL-84
- EPM7128EQ-100
- EPM7128EQ-160
- EPM7160L-84
- EPM7160Q-160
- EPM7160EL-84
- EPM7160EQ-100
- EPM7160EQ-160
- EPM7192G-160
- EPM7192Q-160
- EPM7192EG-160
- EPM7192EQ-160
- EPM7256G-192
- EPM7256W-208
- EPM7256M-208
- EPM7256EG-192
- EPM7256EG-160
- EPM7256ER-208

Current Software Versions

The latest versions of Altera software products are shown below:

- MAX+PLUS II version 7.1
  (PC, Sun SPARCstation, HP 9000 Series 700, and IBMRISC System/6000 platforms)

Programming Hardware Compatibility

The following tables contain the latest programming hardware information. To ensure correct programming, you should always use the software version shown in "Current Software Versions" on page 32. PLM- prefix adapters can be used only with the Master Programming Unit (MPU).

Programming with the BitBlaster & ByteBlaster

Device	Package	Hardware
FLEX 10K	All packages	PL-BITBLASTER PL-BYTEBLASTER
FLEX 8000	All packages	PL-BITBLASTER PL-BYTEBLASTER
MAX 9000	All packages	PL-BITBLASTER PL-BYTEBLASTER
MAX 7000S	All packages	PL-BITBLASTER PL-BYTEBLASTER

Software Utilities

eau000.exe Overview of electronic utilities
eau003.exe EP310 to EP330 JEDEC File converter
eau005.exe JEDPACK JEDEC File compactor
eau007.exe JEDSUM JEDEC checksum generator
eau017.exe LEF2AHDL converts A+PLUS LEF files to AHDL
eau018.exe PLD2EQN PAL/GAL/PLA file converter
eau019.exe ABEL2MAX file converter
eau020.exe PASM2TDF PALASM file converter
eau022.exe PLA2PDS PLA to PALASM file converter

Utilities are available from the Altera BBS via modem at (408) 954-0104 and the Altera FTP site at **ftp.altera.com**.

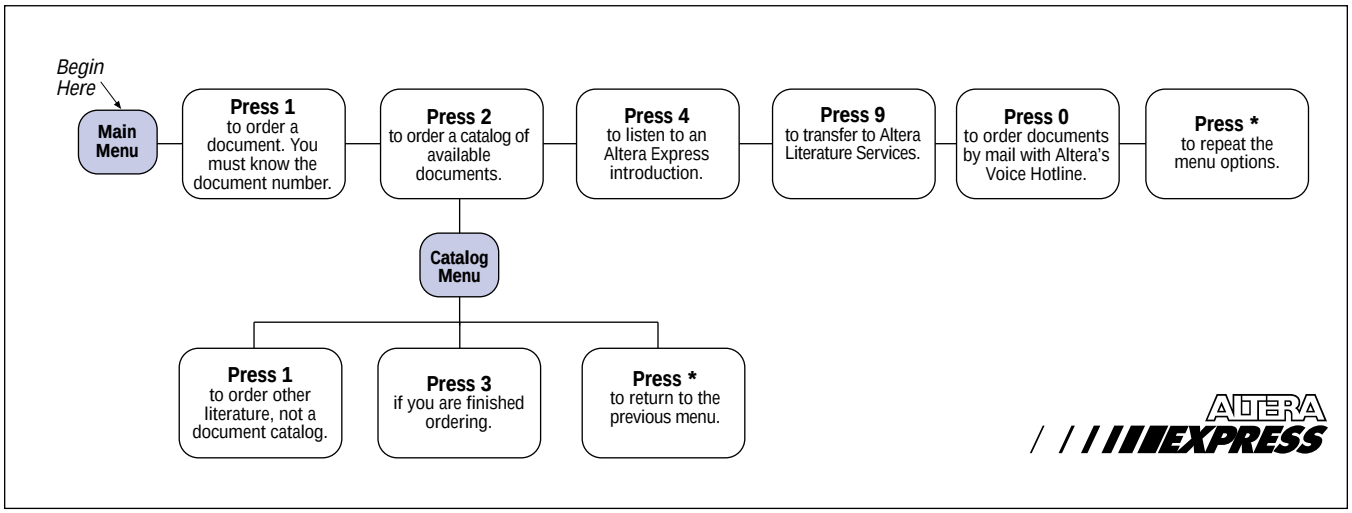
Programming Adapters

Device	Package	Adapter
EPC1064, EPC1064V, EPC1213 (all FLEX 8000 devices), *Note (1)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 (all FLEX 10K and FLEX 8000 devices), *Note (1)*	DIP J-lead	PLMJ1213 PLMJ1213
EPM9320	PGA J-lead (84-pin) RQFP (208-pin)	PLMG9000-280 PLMJ9320-84 PLMR9000-208
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	PGA RQFP (208-pin) RQFP (240-pin) RQFP (304-pin)	PLMG9000-280 PLMR9000-208 PLMR9000-240 PLMR9000-304
MAX 7000S (no carriers)	PQFP (100-pin)	PLMQ7000-100NC
EPM7032, EPM7032V	J-lead PQFP TQFP	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7064	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128S, EPM7160S (no carriers)	PQFP (160-pin)	PLMQ7128/160-160NC
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160, EPM7160E	J-lead PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7192S, EPM7256S (no carriers)	PQFP (160-pin)	PLMQ7192/256-160NC
EPM7192, EPM7192E	PGA PQFP	PLMG7192-160 PLMQ7192/7256-160
EPM7256S (no carriers)	RQFP (208-pin)	PLMQ7256-208NC
EPM7256E	PGA MQFP, RQFP PQFP	PLMG7256-192 PLMR7256-208 PLMQ7192/7256-160
MAX 5000 devices	All packages	*Note (2)*
Classic devices	All packages	*Note (2)*
EPS448	All packages	*Note (2)*

Notes:
(1) The hardware products for these devices are included with the FLEX Download Cable.
(2) Refer to the Altera ***1996 Data Book*** for device adapter information. Altera offers an adapter exchange program for 0.8-micron EPM5032, EPM5064, and EPM5130 programming adapters. See "Product Transitions" on page 6 of this newsletter for more information.

How to Request Altera Publications

Altera publications are available through Altera Express, a 24-hour, 7-day-a-week, automated fax service. In the U.S. and Canada, call (800) 5-ALTERA; international callers can retrieve information by calling (408) 894-7850 from a fax phone. See the following figure. Documents can also be obtained from Altera Literature Services at (888) 3-ALTERA or the Altera world-wide web site at **http://www.altera.com**.



How to Access Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera:

Altera Contact Information

Information Type	Access	U.S. & Canada	All Other Locations
Literature, *(1)*	Altera Express	(800) 5-ALTERA	(408) 894-7850
	Altera Literature Services	(888) 3-ALTERA lit_req@altera.com	(408) 894-7144 *(2)* lit_req@altera.com
	World-Wide Web	http://www.altera.com	http://www.altera.com
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 894-7000
	Fax	(408) 954-8186	(408) 954-8186
Technical Support	Telephone Hotline (8 a.m. to 5 p.m. Pacific Time)	(800) 800-EPLD (408) 894-7000	(408) 894-7000 *(2)*
	Fax	(408) 954-0348	(408) 954-0348 *(2)*
	Bulletin Board Service	(408) 954-0104	(408) 954-0104
	Electronic Mail	sos@altera.com	sos@altera.com
	FTP Site	ftp.altera.com	ftp.altera.com
	CompuServe	go altera	go altera
General Product Information	Telephone	(408) 894-7104	(408) 894-7104 *(2)*
	World-Wide Web	http://www.altera.com	http://www.altera.com

Notes:

(1) Literature Services does not distribute MAX+PLUS II software manuals. Contact Altera Customer Service or your local distributor for a copy.

(2) You can also contact your local Altera sales office or sales representative. See the Altera ***1996 Data Book*** for a list of sales offices and representatives.

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		Not Useful				Very Useful
1.	Devices & Tools	1	2	3	4	5
2.	New Altera Publications	1	2	3	4	5
3.	Questions & Answers	1	2	3	4	5
4.	Technical "How To" Articles	1	2	3	4	5
5.	Information on Altera's	1	2	3	4	5
	EDA Partners & Interface Support	1	2	3	4	5
6.	Customer Applications	1	2	3	4	5
7.	Software Utilities & Current Software versions	1	2	3	4	5
8.	Altera News	1	2	3	4	5

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