The Altera Advantage News & Views

Newsletter for Altera Customers ◆ Third Quarter ◆ August 1997

Altera Ships the New, Low-Cost FLEX 6000 Family

Altera recently began shipping the new, low-cost FLEX® 6000 programmable logic device family, which offers die size and cost that are directly comparable to those of gate arrays. See Figure 1. As a result of technological advances and architecture enhancements, the FLEX 6000 family combines the traditional PLD benefits of fast time-to-market and flexibility with exceptionally low cost for high-volume applications.

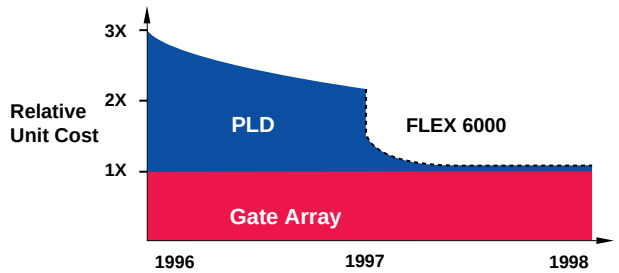
Gate array development often requires hidden costs that are commonly overlooked, including non-recurring engineering (NRE) costs, the cost of a lengthy design cycle, and the cost of market opportunities that are missed due to slow time-to-market. In contrast, FLEX 6000 devices can cost less than comparable ASIC devices when these hidden costs are added into the unit cost of gate arrays. For example, a 10,000-gate EPF6010 device in a 144-pin TQFP package is expected to cost just $6.00 for quantities of 50,000 by mid-1998.

System-Level Features

The FLEX 6000 device family contains a number of powerful system-level features to boost your design efficiency:

- Devices are fully compliant with the peripheral component interconnect (PCI) standard.
- Built-in JTAG boundary-scan test (BST) circuitry is available without consuming any device resources.

Figure 1. FLEX 6000 & Gate Array Pricing



- The MultiVolt™ I/O interface supports 5.0-V, 3.3-V, and 2.5-V mixed-voltage systems.
- Power consumption is less than 10 mA in standby mode.
- In-circuit reconfigurability (ICR) is available via an external Configuration EPROM or intelligent controller.

OptiFLEX Architecture Redefines Programmable Logic Efficiency

The competitive pricing of the FLEX 6000 device family is made possible by Altera's new OptiFLEX™ architecture. Every feature in the OptiFLEX architecture is targeted at producing maximum performance and utilization in the smallest possible die area. The FLEX 6000 architecture is shown in Figure 2.

Through an innovative feature called interleaved logic array blocks (LABs), each logic element (LE) can drive two local interconnects, optimizing global row and column resource utilization within the FLEX device. FLEX 6000 logic arrays are routed through Altera's patented FastTrack™ Interconnect, a series of fast, continuous row and column channels that run the entire length and width of the device. Each FastTrack row and column feeds multiple I/O elements (IOEs), which provide programmable slew-rate and individual tri-state output enable control for each pin.

The FLEX 6000 family also supports FastFLEX™ I/O. This innovative feature provides a direct path from the LE to the I/O pin for fast clock-to-output timing. FLEX 6000 devices offer the benefits of dedicated peripheral registers with the smallest possible die size.

continued on page 3

Contents

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Altera Ships the New, Low-Cost FLEX 6000 Family continued from page 1

µPitch Bond Pad Technology

With the µPitch™ bond pad feature, FLEX 6000 devices contain a bond pad pitch of just 3.2 mils (81 microns) to achieve maximum die size reduction. Therefore, a 16,000-gate FLEX 6000 device in a 240-pin package will be only 6% larger than a gate array with the same pin count, as shown in Figure 3.

FLEX 6000 Family Members

The FLEX 6000 device family offers from 5,000 to 24,000 usable gates of logic and is manufactured on a 0.5-micron, triple-layer metal SRAM process. Later in 1997, manufacturing will move to a 0.35-micron triple-layer metal process. Table 1 outlines the FLEX 6000 family.

Low Cost without Sacrificing Performance

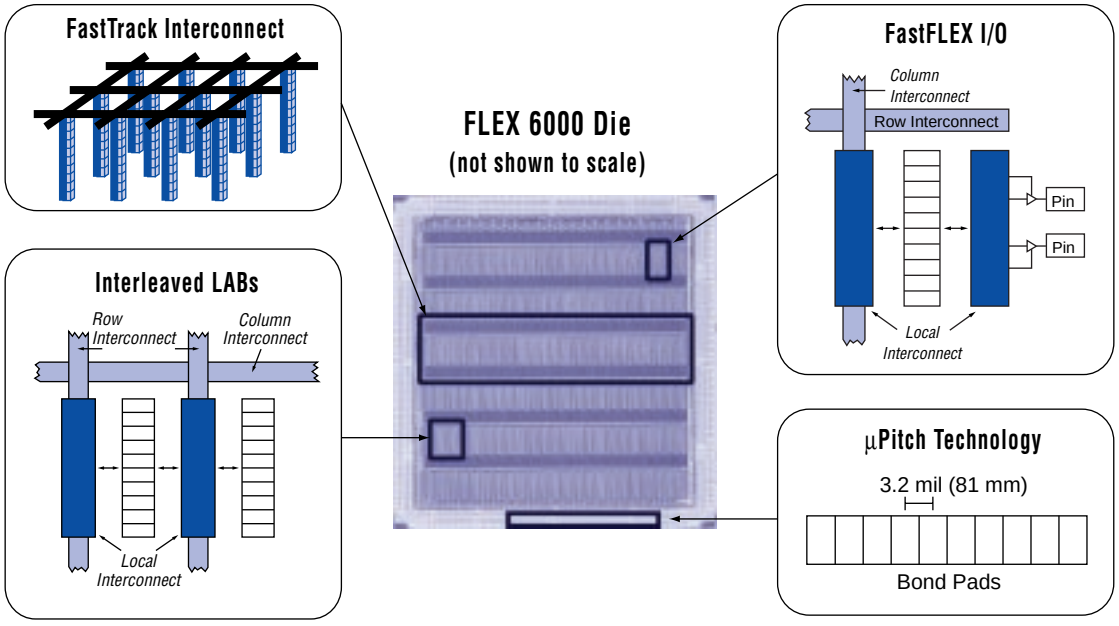
The FLEX 6000 device family achieves die size efficiency without sacrificing utilization or performance. For example, the stringent timing requirements of PCI compliance are achieved through FastFLEX I/O, without dedicated I/O element registers. In a FLEX 6000 device, a 16-bit loadable counter runs at 135 MHz, more than double the speed of competing field programmable gate arrays, which typically run at 60 MHz or slower. The performance of the FLEX 6000 device family is shown in Table 2.

continued on page 4

Table 1. FLEX 6000 Family Features

Feature	EPF6010	EPF6016	EPF6016A	EPF6024A
Process geometry	0.5 µ	0.5 µ	0.35 µ	0.35 µ
Supply voltage	5.0 V	5.0 V	3.3 V	3.3 V
Pin migration	Yes	Yes	Yes	Yes
Gate count	5,000 to 10,000	8,000 to 16,000	8,000 to 16,000	12,000 to 24,000
Logic elements	800	1,320	1,320	1,960
User I/O pins (maximum)	160	197	197	215
Package options	144-pin TQFP 208-pin PQFP	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin BGA	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin BGA	– 208-pin PQFP 240-pin PQFP 256-pin BGA

Figure 2. OptiFLEX Architecture



Altera Ships the New, Low-Cost FLEX 6000 Family continued from page 3

Availability, Packaging & Pricing

The 16,000-gate EPF6016 is available now. The first 0.35-micron, 3.3-V family member, the 24,000-gate EPF6024A, will be available in January 1998. The rest of the FLEX 6000 family is expected to be available in the first half of 1998. Contact your local Altera sales representative for availability of specific packages. Examples of mid-1998 projected pricing for quantities of 50,000 units are shown in Table 3.

Conclusion

Altera's FLEX 6000 device family provides designers with an ideal programmable alternative to gate arrays for high-volume production. Using the efficient OptiFLEX architecture, the FLEX 6000 family delivers the flexibility and time-to-market of programmable logic at prices that are competitive with gate arrays. For further details, refer to the *FLEX 6000 Programmable Logic Device Family Data Sheet* and *AN 87* (*Configuring FLEX 6000 Devices),* or contact your local Altera representative.

Figure 3. Relative Die Size Comparison

Devices shown are not actual size.

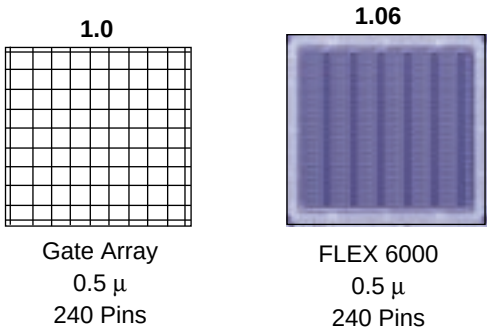


Table 2. FLEX 6000 Performance

Benchmark	LEs Used	-2 Speed Grade	-3 Speed Grade
16-bit loadable counter	16	135 MHz	99 MHz
16-bit accumulator	16	135 MHz	99 MHz
24-bit accumulator	24	99 MHz	72 MHz
16-to-1 multiplexer	10	5.5 ns	7.0 ns
16 x 16 multiplier, 4-stage pipeline	560	64 MSPS	50 MSPS
8-bit, 16-tap parallel finite impulse response (FIR) filter	599	78 MSPS	61 MSPS
8-bit, 512-point fast Fourier transform (FFT)	1,162	155 µS 41 MHz	139 µS 34 MHz
16450 universal asynchronous receiver/transmitter (UART)	478	23 MHz	18 MHz
PCI bus target with one wait state	398	33 MHz	25 MHz

Table 3. FLEX 6000 Volume Price Projections *Note (1)*

Device	Process	Projected Pricing 50,000 Units
EPF6010	0.5 micron	$6.00
EPF6016	0.5 micron	$7.50
EPF6016A	0.35 micron	$7.00
EPF6024A	0.35 micron	$10.00

Note:
(1) Prices are in U.S. dollars for OEM direct orders.

Get ES Site License Authorization Codes via the Web

Beginning with MAX+PLUS® II version 8.1—scheduled to ship in September 1997—you can obtain a MAX+PLUS II ES Site License authorization code via the world-wide web. Simply go to Altera's web site at **http://www.altera.com/es** and fill out the registration form. Your authorization code will be e-mailed to you within minutes. Using the Internet is a fast and easy way for you to get started with the MAX+PLUS II software.

Devices & TOOLS

FLEX 10K

Altera Increases FLEX 10K Performance

In August, Altera announced plans to increase FLEX® 10K performance by introducing new, faster -2 speed grade devices. These performance increases will allow Altera to continue to lead in high-density programmable logic performance. Contact your local Altera sales representative for more details regarding the new -2 speed grade devices.

FLEX 10K Pricing & Availability

On June 30, Altera reduced the prices of FLEX 10K devices by up to 49%. This price cut is a direct result of advances in process technology and reduced die size and cost. The price cuts in the high-density FLEX 10K family have been among the most aggressive in the industry, making the cost of these devices competitive with gate arrays. Since its introduction in 1995, the 100-unit list price of the 50,000-gate FLEX 10K/FLEX 10KA device has dropped from $995 to $99. FLEX 10K devices are available in a variety of quad flat pack (QFP), ball-grid array (BGA), and pin-grid array (PGA) packages. Sample 100-unit pricing is shown below:

FLEX 10K Price Reductions *Note (1)*

Device	Old 100-Unit Price	New 100-Unit Price	Percent Reduction
EPF10K100GC503-4	$595.00	$445.00	25%
EPF10K70RC240-4	$261.00	$195.00	25%
EPF10K50VRC240-4	$195.00	$99.00	49%
EPF10K50RC240-4	$195.00	$145.00	26%
EPF10K40RC208-4	$117.00	$92.00	21%
EPF10K30RC208-4	$87.50	$70.00	20%
EPF10K20TC144-4	$43.50	$34.00	22%
EPF10K10LC84-4	$22.00	$19.00	14%

Note:
(1) Prices are in U.S. dollars and are suggested resale.

EPF10K100A Coming Soon

Altera plans to ship the 100,000-gate EPF10K100A in November 1997. Initially, this device will be offered in 240-pin power quad flat pack (RQFP)packages. In the first quarter of 1998, Altera expects to provide devices in and 356-pin and 600-pin ball-grid array (BGA) packages.

Built on a 0.35-mm, quad-layer-metal (QLM) process, the EPF10K100A will be pin-compatible with current FLEX 10K devices in the 240-pin RQFP and 356-pin BGA packages. For instance, you will be able to migrate from the current 3.3-V, triple-layer-metal (TLM) EPF10K50V to a device of higher density without changing your board layout.

MAX 9000

MAX 9000A Update

The MAX® 9000A family, manufactured on a 0.5-micron, triple-layer-metal process, will offer speeds as fast as 7.5 ns. The family is pin-compatible with the MAX 9000 family and will offer you reduced power consumption. The family also supports Altera's MultiVolt I/O interface, making MAX 9000A devices ideal for mixed-voltage systems. The following table shows MAX 9000A device availability.

MAX 9000A Device Availability

Device	Fastest t_{PD} (ns)	Availability	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	356-Pin BGA
EPM9320A	10	October 1997	✓	✓		✓
EPM9320A	7.5	Q1 1998	✓	✓		✓
EPM9400A	10	Q1 1998	✓	✓	✓	
EPM9480A	10	Q1 1998		✓	✓	
EPM9560A	10	September 1997		✓	✓	✓

MAX 7000

MAX 7000S Pricing & Availability

On June 30, Altera reduced the prices of MAX 7000S devices by up to 49%. This price cut is a direct result of advances in process technology and reduced die size and costs. The latest price reductions for the MAX 7000S family are the result of continuing process

continued on page 6

Devices & Tools
continued from page 5

improvements and increased production volumes. Examples of the new 100-unit pricing are shown below:

***MAX 7000S Price Reductions** (1)*

Device	Old 100-Unit Price	New 100-Unit Price	Percent Reduction
EPM7256SRC208-15	$68.50	$51.00	26%
EPM7192SQC160-15	$42.00	$31.00	26%
EPM7128SLC84-15	$18.75	$11.25	40%
EPM7064SLC44-10	$9.70	$5.00	48%

Note:
(1) Prices are in U.S. dollars and are suggested resale.

Faster MAX 7000S Speed Grades

The MAX 7000S family is now faster than ever with new 6-ns and 7.5-ns speed grade devices. The following table shows speed grades and availability.

MAX 7000S Device Availability

Device	Package	Speed Grade	Availability
EPM7064S	44-pin PLCC	-6, -7, -10	Now
	44-pin TQFP	-6, -7, -10	Now
	100-pin TQFP	-6, -7, -10	Now
EPM7128S	84-pin PLCC	-7, -10, -15	Now
	100-pin TQFP	-7, -10, -15	Now
	100-pin PQFP	-7, -10, -15	Now
	160-pin PQFP	-7, -10, -15	Now
EPM7192S	160-pin PQFP	-7 -10, -15	October 1997 Now
EPM7256S	208-pin RQFP	-7, -10, -15	Now

MAX 7000S Supports ATE

Altera plans to begin shipping MAX 7000S devices that support automated test equipment (ATE) beginning in September 1997. Products that support ATE have an "F" as the last character of the ordering code, e.g., EPM7128SQC100-7F.

Contact your local Altera sales representative for information on availability and lead times for MAX 7000S devices that support ATE.

Conventional MAX 7000S Device Programming

You can now program MAX 7000S devices using Altera's Master Programming Unit (MPU), the MAX+PLUS II software, and the appropriate programming adapter. The ordering codes for these adapters are shown below:

MAX 7000S Devices that Support Socketed Programming

Devices	Ordering Code
All MAX 7000S devices in 100-pin PQFP packages	PLMQ7000-100NC
All MAX 7000S devices in 100-pin TQFP packages	PLMT7000-100NC
EPM7128S and EPM7160S devices in 160-pin PQFP packages	PLMQ7128/160-160NC
EPM7192S devices in 160-pin PQFP packages	PLMQ7192/256-160NC

Third-party programmers such as programmers from Data I/O and BP Microsystems also support socketed programming of MAX 7000S devices.

MAX 7000 Product Transitions

Altera is migrating existing MAX 7000 devices from a 0.65-micron process to a 0.5-micron process. Evaluation packets containing device samples and documentation are available from your local Altera sales representative. The following table outlines the process migration schedule.

***MAX 7000 Migration Schedule,** Note (1)*

Device	Reference (2)	Date	Process
EPM7256S EPM7256E	PCN9703 ADV9708	September 1, 1997	0.5-micron
EPM7192S EPM7192E	PCN9703 ADV9708	November 1, 1997	0.5-micron
EPM7128S	PCN9703 ADV9708	Complete	0.5-micron
EPM7128E	PCN9703 ADV9708	October 1, 1997	0.5-micron
EPM7064S EPM7064	PCN9703 ADV9708	September 1, 1997	0.5-micron

Notes:
(1) This process transition will not result in any changes to data sheet parameters or ordering codes.
(2) Altera provides advisories and process change notices. Go to the Altera world-wide web site for these reference documents.

MAX 5000 & Classic

Product Transitions

Altera is migrating existing MAX 5000 and Classic™ devices from a 0.8-micron process to a 0.65-micron process. Evaluation packets containing device samples and documentation are available from your local Altera sales representative. Table 1 outlines the process migration schedule.

New Altera programming adapters are required to program the 0.65-micron MAX 5000 devices (0.65-micron Classic devices do not require new adapters). Altera will exchange existing EPM5032, EPM5064, and EPM5130 programming adapters for new adapters *for free*. These new adapters are backwards-compatible and support all existing die revisions. Table 2 lists the existing MAX 5000 adapters that can be exchanged for new adapters. Contact your local Altera representative for more information.

Table 1. Product Migration Schedule

Description *(1)*	Reference *(2)*	Device	Date
MAX 5000 devices fabricated on a 0.65-micron process *Note (3)*	PCN 9407 ADV 9515 ADV 9606	EPM5032	Complete
		EPM5064	October 1, 1997
		EPM5128	Complete
		EPM5130	September 1, 1997
		EPM5192	Complete
Classic devices fabricated on a 0.65-micron process	PCN 9510 ADV 9607 ADV 9621	EP6*xx*	Complete
		EP9*xx*	Complete
		EP18*xx*	Complete

Notes:
(1) Data sheet parameters or ordering codes will not change.
(2) Go to the Altera world-wide web site for advisories and process change notices.
(3) Devices manufactured on the 0.65-micron process must be programmed with new programming adapters.

Table 2. MAX 5000 Replacement Adapters

Existing Adapter	New Adapter
PLEJ5064	PLMJ5064A
PLMJ5064	PLMJ5064A
PLEG5130	PLMG5130A
PLEJ5130	PLMJ5130A
PLMJ5130	PLMJ5130A
PLEQ5130	PLMQ5130A
PLMQ5130	PLMQ5130A

MAX+PLUS II

Improvement in High-Density Compilation Times

MAX+PLUS II version 8.0 significantly reduces the compilation times required for FLEX devices.

For designs that target FLEX 8000 devices and FLEX 10K devices with up to 50,000-gates, MAX+PLUS II version 8.0 provides compilation times that are 2 times faster than the previous version of the MAX+PLUS II software for both PCs and UNIX workstations. For designs that target large FLEX 10K devices (up to 250,000 gates), compilation is 3 times faster. See the table below. Watch for additional new product announcements with MAX+PLUS II version 8.1.

MAX+PLUS II Compilation Improvements

Density	Median Compilation Time in MAX+PLUS II Version 7.2 (minutes)	Median Compilation Time in MAX+PLUS II Version 8.0 (minutes)	Improvement Factor
< 3,000 logic elements (LEs)	21.24	8.41	2.5
8,000 to 9,000 LEs	78	33	2.4
9,000 to 10,000 LEs	183.75	39	4.7

MAX+PLUS II Version 8.1 to Ship in September 1997

MAX+PLUS II version 8.1 provides a host of new features in a continuing effort to provide value to our customers. This latest release of MAX+PLUS II significantly improves the timing-driven compilation capability to support designers who want to create high-density designs.

Additional features in this version include:

- HP-UX 10.10 support
- Packed register support for the FLEX 6000 family
- Internal global support for the FLEX 10K family

Altera's software maintenance program keeps you up-to-date with the latest features and gives you access to the newest devices. For more information on how to purchase a software maintenance agreement, contact your local Altera representative.

Discontinued Devices

In recent months, Altera has announced that various products will be discontinued (see the table below). Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's world-wide web site at **http://www.altera.com**. Rochester Electronics, an after-market supplier, offers support for many discontinued Altera products. Contact Rochester Electronics at (508) 462-9332 for more information.

Discontinued Device Ordering Codes

Device Family	Device	Last Order Date	Last Shipment Date	Reference
FLASHlogic	EPX880 and EPX8160 (all packages, temperature grades, and speed grades)	6/30/97	6/30/98	PDN 9625
	EPX740 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
MAX 5000	EPM5032SC-15	6/30/97	12/31/97	PDN 9624
	EPM5016 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
Classic	EP220, EP224, EP312, EP324 (all packages, temperatures, and speed grades)	3/31/97	9/30/97	PDN 9516
Function-Specific	EPS448, EPS464 (all commercial and industrial temperature grades; military devices have earlier last order and last shipment dates)	3/31/97	9/30/97	PDN 9516

New Altera Publications

New Altera publications are available from Altera Literature Services. Individual documents are available on the Altera world-wide web site. Document part numbers are shown in italics.

- **FLEX 6000 Programmable Logic Device Family Data Sheet** *A-DS-F6000-02*
  Describes the FLEX 6000 device architecture, features, operating conditions, and pin-outs.
- **AN 87 (Configuring FLEX 6000 Devices)** *A-AN-087-01*
  Describes how to use passive serial, passive serial asynchronous, or Configuration EPROM modes to configure FLEX 6000 devices.
- **Jam Programming & Test Language Specification** *A-SP-JAM-01*
  Provides an overview and technical information for the Jam language.
- **AN 88 (Using the Jam Language for ISP via an Embedded Processor)** *A-AN-088-01*
  Discusses how to use the Jam language to achieve the benefits of in-system programmability (ISP) with embedded processors.
- **In-System Programmability Handbook** *M-HB-ISP-01*
  Contains all current technical literature on the in-system programmability feature available in Altera MAX 9000 and MAX 7000S families.
- **Microperipheral MegaCore Function Data Book** *A-DB-MEGA-02*
  This revised version provides information on the a8259 programmable interrupt controller, as well as information on existing Altera microperipheral MegaCore functions.
- **FLEX 10K Embedded Programmable Logic Family Data Sheet Supplement** *A-DSS-F10K-2.4*
  Summarizes device capacitance and PCI timing specifications for FLEX 10K devices.
- **crc MegaCore Function Parameterized CRC Generator/ Checker Data Sheet** *A-DS-CRC-01*
  Describes parameter and port values of the fully-parameterized Altera crc MegaCore function.
- **Altera Digital Library CD-ROM** *P-CD-ADL-02*
  This revised version provides an electronic version of all current Altera technical literature.
- **TB 22: FLEX 10K Devices: The Density Leader** *M-TB-022-01*
- **TB 23: FLEX 10K Power Consumption** *M-TB-023-02*
- **TB 24: The Advantages of LPM** *M-TB-024-01*
- **TB 25: Using the OpenCore Evaluation Feature** *M-TB-025-01*
- **TB 26: FLEX 10K & pci_a: The Complete PCI Solution** *M-TB-026-01*
- **TB 27: Evaluating FLEX 6000 Performance** *M-TB-027-01*
- **TB 28: Advantages of Altera ISP-Based CPLDs** *M-TB-028-01*
- **SB 17: Early/Late Gate Synchronizer Megafunction** *A-SB-017-01*
- **SB 24: USB Function Controller Megafunction** *A-SB-024-01*
- **SB 28: USB Host Controller Megafunction** *A-SB-028-01*

Technical ARTICLES

Implementing an Encoder Using LPM Functions

As devices grow in density, designs will use more pre-built functions, such as functions from the library of parameterized modules (LPM). This article describes how to create an encoder using LPM functions. One implementation is written in VHDL, the other is written in the Altera Hardware Description Language (AHDL™). In both implementations, serial data enters a shift register. When the shift register is full, the counter will be at 7 and the coding of the 8-bit word will take place. Then, the 8-bit word is shifted out serially on the `datax` port as more data enters the shift register (the `datax` port provides the coded output). The data stream is constant, therefore, no handshaking is required.

The MAX+PLUS II VHDL example references the `lpm` library in the statements shown in blue text. A Generic Map Statement describes the parameters of the LPM function.

The AHDL example uses Include Statements (shown in blue text) to import the contents of the Include File containing the Function Prototypes for the LPM functions. An Instance Declaration (shown in red text) implements an instance of the function.

VHDL Encoder

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
LIBRARY lpm;
USE lpm.lpm_components.ALL;

ENTITY coder IS
     PORT (
       datain, clk : IN STD_LOGIC;
       datax       : OUT STD_LOGIC);
END coder;

ARCHITECTURE en OF coder IS
     SIGNAL q : std_logic_vector(7 DOWNTO 0);
     SIGNAL datacode :
       std_logic_vector(7 DOWNTO 0);
     SIGNAL eq :
       std_logic_vector(15 DOWNTO 0);

BEGIN
     shift : lpm_shiftreg
       GENERIC MAP (LPM_WIDTH => 8,
          LPM_DIRECTION => "RIGHT")
       PORT MAP (data => datacode,
          clock => clk,
          shiftin => datain,
          q => q,
          load => eq(7),
          shiftout => datax);
     count : lpm_counter
       GENERIC MAP (LPM_WIDTH => 3)
       PORT MAP (clock => clk, eq => eq);
     PROCESS BEGIN datacode <=  ((datain xor
       q(7)) & q(7) & not q(6 DOWNTO 5) &
       (q(4) xor q(3)) & q(3) & not
       q(2 DOWNTO 1));
     END PROCESS;
END en;
```

AHDL Encoder

```
INCLUDE "lpm_shiftreg.inc";
INCLUDE "lpm_counter.inc";

SUBDESIGN 'encoder'
     (clk, datain : INPUT;
     datax        : OUTPUT;)

VARIABLE
     shift : lpm_shiftreg WITH
       (LPM_WIDTH = 8,
       LPM_DIRECTION = "RIGHT");
     count : lpm_counter WITH
       (LPM_WIDTH = 3);

BEGIN
-- Connect the ports on the 8-bit shifter
     shift.clock = clk;
     shift.shiftin = datain;
     shift.load = count.eq7;
     shift.data[] = ((datain $ shift.q7),
       shift.q7, !shift.q[6..5],
       (shift.q4 $ shift.q3), shift.q3,
       !shift.q[2..1]);
     datax = shift.shiftout;

-- Connect the counter
     count.clock = clk;
END;
```

Configuring FLEX 6000 Devices

You can use an EPC1 Configuration EPROM or a microprocessor to configure FLEX 6000 devices using the following configuration schemes:

- Configuration EPROM
- Passive serial (PS)
- Passive serial asynchronous (PSA)

The Configuration EPROM and passive serial configuration schemes are similar to the Configuration EPROM and passive serial configuration schemes used to configure FLEX 8000 and FLEX 10K devices. This article focuses on the PSA scheme, a new configuration method that is supported only by FLEX 6000 devices.

Configuration EPROM & PS Configuration

The built-in clock in the EPC1 Configuration EPROM device controls configuration of FLEX 6000 devices. One Configuration EPROM device is large enough to configure any FLEX 6000 device, and you can configure multiple FLEX 6000 devices with one or more EPC1 Configuration EPROM devices. Programming support for the EPC1 Configuration EPROM is available via the Altera Master Programming Unit (MPU) and third-party programmers.

In PS mode, FLEX 6000 devices are controlled and clocked with one of the following configurations:

- BitBlaster download cable
- ByteBlaster download cable
- Microcontroller or other intelligent interface

The BitBlaster or ByteBlaster download cable generates a low-to-high transition on the nCONFIG pin to initiate configuration. The programming hardware then places the configuration data on the DATA pin of the FLEX 6000 device one bit at a time. The data is clocked into the FLEX 6000 device until nCONFIG goes high. The programming hardware is used in FLEX configuration mode, not in multi-device JTAG configuration or programming mode.

You can configure multiple FLEX 6000 devices with programming hardware by connecting the nCEO pin of a device to the nCE pin of the subsequent device. The other configuration pins are connected to all FLEX 6000 devices in the chain. All FLEX 6000 device CONF_DONE pins must be tied together, so that all FLEX 6000 devices initialize and enter user mode at the same time.

PSA Configuration

In PSA mode, configuration is controlled by a microprocessor. Configuration begins with the microprocessor driving nCONFIG high. The microprocessor then asserts the nCS and CS inputs to the FLEX 6000 device; these inputs must remain asserted until configuration and initialization are complete. The microprocessor places a configuration bit on the DATA input of the FLEX 6000 device and pulses nWS low on the FLEX 6000 device.

On the rising edge of nWS, the FLEX 6000 device latches the data and drives RDYnBSY low to indicate that it is processing the bit of data. While the bit of data is being processed, the microprocessor can perform other system functions.

The microprocessor can monitor CONF_DONE and INIT_DONE to ensure successful configuration. If the microprocessor has sent all configuration data and CONF_DONE does not become asserted, the FLEX 6000 device must be reconfigured.

If an error is detected during configuration, the FLEX 6000 device drives nSTATUS low to alert the microprocessor. The microprocessor can then pulse nCONFIG low to restart the configuration. Alternatively, if the *Auto-Restart Configuration on Frame Error* option is turned on in the MAX+PLUS II software, the FLEX 6000 device releases nSTATUS after a reset time-out period. After nSTATUS is released, the microprocessor can reconfigure the FLEX 6000 device.

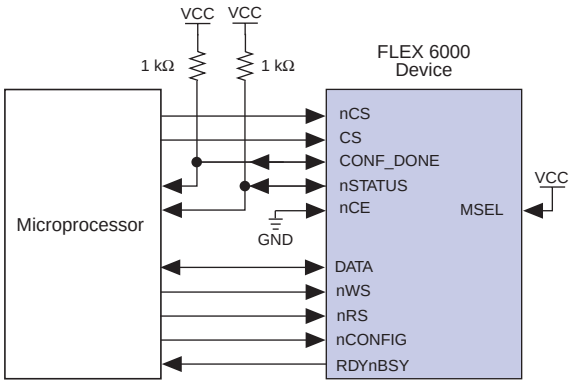
The FLEX 6000 device can initialize itself in PSA mode. Therefore, CONF_DONE is asserted and the device initializes before all data is sent. The microprocessor can stop sending configuration data when CONF_DONE is asserted.

Figure 1 shows the PSA configuration circuit and Figure 2 shows the state of the device during configuration, initialization, and user modes. Arrows show which signal transitions are dependent on other transitions.

PSA mode can be used to configure multiple FLEX 6000 devices. Multi-device PSA configuration is similar to single-device PSA configuration, except that the FLEX 6000 devices are cascaded. After the first FLEX 6000 device is configured nCEO is asserted,

which asserts nCE on the second device, causing it to begin configuration. All FLEX 6000 device CONF_DONE pins are tied together, so that all FLEX 6000 devices initialize and enter user mode simultaneously. Additionally, if any device detects an error, the entire chain will stop configuration because the nSTATUS lines are tied together. For additional information on FLEX 6000 devices, refer to *AN 87 (Configuring FLEX 6000 Devices)* and the *FLEX 6000 Programmable Logic Device Family Data Sheet*.

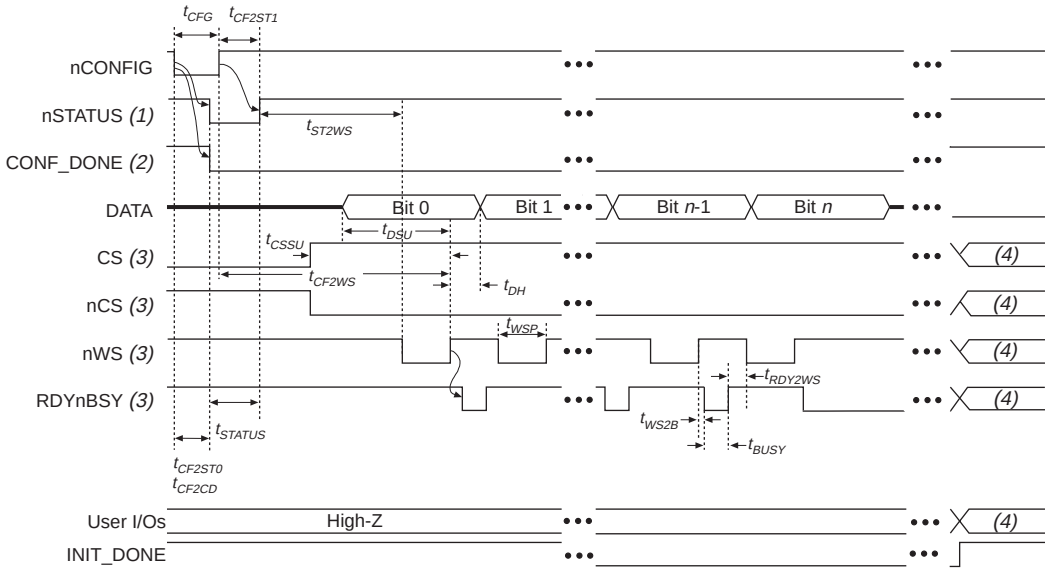
Figure 1. FLEX 6000 PSA Configuration



PSA Timing Parameters

Symbol	Parameter	Min	Max	Units
t_{CFG}	nCONFIG low pulse width	2		µs
t_{STATUS}	nCONFIG low pulse width	2.5		µs
t_{CF2ST1}	nCONFIG high to nSTATUS high		4	µs
t_{ST2WS}	nSTATUS high to first rising edge on nWS		1	µs
t_{CF2WS}	nCONFIG high to first rising edge on nWS	5		µs
t_{DSU}	Data setup time before rising edge on nWS	50		ns
t_{DH}	Data hold time after rising edge on nWS	0		ns
t_{CSSU}	Chip select setup time before rising edge on nWS	50		ns
t_{WSP}	nWS low pulse width	50		ns
t_{WS2B}	nWS rising edge to RDYnBSY low		50	ns
t_{BUSY}	RDYnBSY low pulse width		200	ns
t_{RDY2WS}	RDYnBSY rising edge to nWS falling edge	50		ns
t_{CF2CD}	nCONFIG low to CONF_DONE high		1	µs
t_{CF2ST0}	nCONFIG low to nSTATUS low		1	µs

Figure 2. Timing Waveform



Notes:

(1) Upon power-up, nSTATUS is held low for five microseconds.
(2) Upon power-up, CONF_DONE is low.
(3) After configuration, the state of CS, nCS, nWS, and RDYnBSY depends on the design programmed into the FLEX 6000 device.
(4) Device I/O pins are in user mode.

Introducing the Open-Standard Jam Programming & Test Language

A coalition of leading programmable logic device (PLD) manufacturers, programming equipment makers, and test equipment manufacturers recently announced a new programming language, called Jam™, that is compatible with all in-system programmability (ISP)-capable PLDs. The Jam language is planned to be submitted as an industry-standard language to the Joint Electronic Devices Engineering Council (JEDEC).

Altera and Cypress Semiconductor support the Jam language as a method of simplifying ISP. Also endorsing the Jam language and its standardization are programming equipment vendors BP Microsystems and Data I/O Corporation, as well as test equipment manufacturers Asset InterTech Corporation, GenRad Corporation, Gopel Electronic, JTAG Technologies, and Teradyne Corporation.

Jam Addresses the ISP Dilemma

Currently, in-system programming is plagued by proprietary file formats, vendor-specific programming algorithms, large file sizes, and long programming times. The result is a confusing array of options, and poor return on investment for design and manufacturing engineers trying to implement ISP using PLDs. The Jam language addresses each of these issues by providing a software-level standard for ISP. The Jam standard is vendor-independent, produces small file sizes, and reduces programming times.

While created by Altera, the Jam language will be freely licensed to all interested parties. Brian Moyer, chairman of this JEDEC 23.1 subcommittee, said the Jam language will be considered at the next JEDEC meeting.

The Importance of ISP

In-system programmability is important to designers who use PLDs because it offers distinct time-to-market advantages throughout the product life-cycle. For example, with ISP, design revisions in the prototyping stage can be compiled and programmed into a device within minutes. In production, ISP simplifies the manufacturing flow by allowing devices to be programmed during board testing with automated test equipment (ATE), minimizing coplanarity in quad flat pack (QFP) packages and reducing the need to store programmed devices in inventory. In addition, systems using ISP-capable devices can be easily upgraded in the field by downloading new configurations via modem or other data links. There are three standard ISP programming methods:

- Download cable
- ATE
- Embedded processor

The download cable method has been the most popular with designers and is expected to remain so in the near future.

What Is the Jam Language?

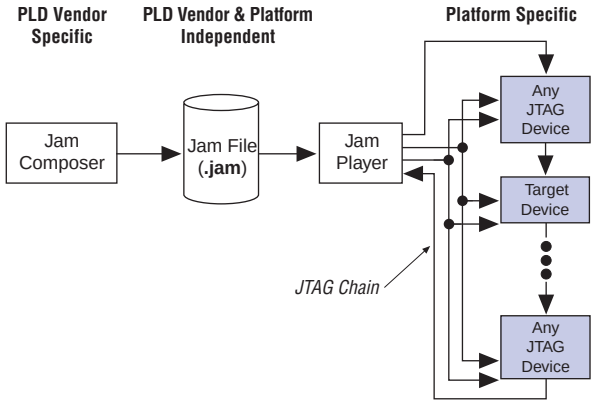
The Jam language allows the creation of a single file that specifies both the data to be programmed into a device and the algorithm required to accomplish programming. The language supports all ISP methods as well as standard programmers, which are used to program devices in bulk. The Jam language consists of two parts, the Jam Composer and the Jam Player. The Jam Composer writes files that contain the user data and programming algorithm for the device. The Jam Player interprets the Jam file and manages the JTAG port to program devices. The Jam instruction set includes JTAG-based and algorithmic instructions. These elements create a universal language and tools that address all PLDs and all programming methodologies. See Figure 1.

In addition, the Jam language addresses the issues associated with current ISP programming solutions, including smaller file sizes, faster programming times, and the ability to work with existing and future devices manufactured on different processes.

Smaller File Sizes

Currently, two file formats are used for ISP: ATE "bed of nails" vectors and ATE JTAG instructions. ATE vectors are a simple, low-level design representation ideal for testing. ATE JTAG instructions are ASCII-based files that are generally created by silicon vendors. However, both methods create large files, making them impractical for some design flows using ISP. For example, file size is critical for ISP via an embedded processor, which must manage both the design data and programming algorithm. At the same time, fully expanded ISP vectors are impractical in an ATE environment. For instance, the fully expanded code required to program a 128-macrocell device typically exceeds 20 Mbytes in size. In contrast, a Jam file for the same 128-macrocell device would be about

Figure 1. Flow Using the Jam Language



8 Kbytes. This file, created using compression ratios of up to 50:1, is comparable in size to the Programmer Object File (**.pof**) generated by Altera's MAX+PLUS II software.

Faster Programming Times

The longer it takes system manufacturers to program a device, the more expensive testing becomes. Current ISP methods require that silicon vendors provide a programming pulse time that is long enough to guarantee that every device has been adequately programmed, which is a challenging requirement because the programming pulse is an exponential function of the oxide thickness in EEPROM, FLASH, and EPROM processes. Therefore, programming pulses are specified up to 2 orders of magnitude longer than any given device may require.

The Jam language allows the required programming pulse width to be determined real-time by reading it from each device. Devices that require a short pulse can be programmed quickly, while ensuring that devices requiring a longer pulse will meet all requirements. On average this technique reduces programming times by approximately a factor of 10.

Conclusion

In-system programmability is an increasingly important feature for systems designers and manufacturers seeking to shorten time-to-market. While several methods of programming and re-programming are now in use, they have drawbacks in terms of file size and programming times. The Jam language addresses these concerns and, as an open standard, would benefit all silicon vendors, manufacturers, and programmers.

Frequently Asked Jam Language Questions

With the release of MAX+PLUS II version 8.0 in June 1997, Altera began supporting a new open-standard programming and test language called Jam. The Jam language is designed for devices that support in-system programmability (ISP). This article answers some common questions about the Jam language.

What is the Jam Language?

The Jam language is an interpreted language optimized for programming devices via the standard IEEE 1149.1 TAP controller (i.e., the JTAG interface). This interpreted language supports both new and existing ISP-capable devices, has a small interpreter code and file size, provides faster programming times, is silicon vendor- and platform-independent, and is an open standard that can be freely licensed.

Who would use the Jam Language?

The Jam language could be used by any designer programming a JTAG-compliant ISP-capable device. Whether the device is programmed with a proprietary download cable, embedded processor, or automated test equipment (ATE), the Jam language provides an efficient and quick solution.

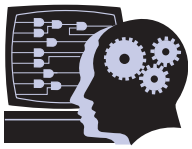
Why use the Jam Language?

Many of the existing programming vector formats used with ISP-capable devices are large and difficult to work with. In many instances, the size of these existing vector format files is measured in Mbytes because they do not support data compression and algorithmic instructions. The small size of Jam files eliminates this problem.

How do I get the Jam Language?

Contact your local Altera sales representative to receive a Jam Developers Kit and an authorization code for enabling Jam support within MAX+PLUS II version 8.0. You can also download the kit via the Internet at **http://www.altera.com/jam**.

Customer Training Brings You Up to Speed



Altera's Customer Training Department has revised and expanded its course offering. Classes are created specifically to meet different experience levels, provide realistic design examples and labs, and offer sound, realistic advice on hardware design techniques and software settings. These one-day sessions give you knowledge that might otherwise require months of trial and error work.

Introductory courses are ideal for designers beginning to use Altera devices. You will learn about the architecture and features of Altera device families, how to access these features with the MAX+PLUS II software, and how to analyze design results. Discussions include basic recommendations for design layout and software settings.

For experienced Altera users interested in gaining higher speed and utilization, advanced courses focus on fitting and performance for specific architectures. These classes contain more labs than the introductory courses. Faster paced and more challenging, the advanced labs require knowledge of the MAX+PLUS II software as well as a basic understanding of Altera device family architectures.

Valuable for both beginners and experienced users, *Designing with MAX+PLUS II* explores the features of the MAX+PLUS II software, including design entry with the Text Editor and Graphic Editor, Floorplan Editor, Timing Analyzer, and Simulator as well as synthesis and fitting. New users can discover what the MAX+PLUS□II software has to offer, and experienced users can learn about software options that they may not have used before.

Altera also offers VHDL and AHDL courses for all experience levels. These classes cover basic syntax and program structure, inferring and instantiating elements, and creating an overall design with the languages. Instructors emphasize the common problems of coding, particularly in the VHDL course.

A summary of available courses is shown below. You can also find more detailed information and a registration form on Altera's world-wide web site at **http://www.altera.com**.

- *Introduction to Altera's MAX Device Families*
- *Introduction to Altera's FLEX Device Families*
- *Advanced Design Techniques for Altera's MAX Device Families*
- *Advanced Design Techniques for Altera's FLEX Device Families*
- *Designing with MAX+PLUS II*
- *Designing with MAX+PLUS II using AHDL*
- *Designing with MAX+PLUS II using VHDL*

The Advantages of the LPM

As designers seek to take full advantage of the capacity and performance of high-density PLDs, such as Altera's FLEX 10K family, design methodology has evolved. Instead of using traditional schematic-based design techniques, designers are turning to modern design techniques that use hardware description languages (HDLs), megafunctions, and the library of parameterized modules (LPM). LPM functions offer many advantages, especially when designing with FLEX devices.

Why LPM?

The LPM allows you to create architecture-independent designs, while still maintaining silicon efficiency. Instead of spending time replicating standard logic functions, using LPM functions enables you to focus on adding value to your design. Using the LPM also frees you from deciding on a target architecture until late in the design flow. Design entry and simulation are architecture-independent; a device is targeted during logic synthesis or fitting. As part of the EDIF standard, the LPM is supported by a wide range of EDA tools. For additional information about the LPM or to download synthesizable or simulatable models of LPM functions, you can refer to the world-wide web at **http://www.edif.org**.

Currently, the standard contains 25 LPM functions. Each function is parameterized, i.e., you can use parameters to customize a module to fit your design needs. For example, the `LPM_PIPELINE` parameter can be used with the LPM multiplier, `lpm_mult`, to specify the number of pipeline stages to be used. Altera, a member of the EIA's LPM committee, has the broadest software support for the LPM of any PLD vendor, as shown in Table 1.

A Parameterized Multiplier Example

Multipliers are basic building blocks that are used in a wide variety of applications, from digital modulation to image compression. Multiplier performance is critical because it often limits overall system performance. Table 2 compares unsigned multiplier performance for FLEX devices.

Using the LPM function `lpm_mult` and the MAX+PLUS II tools, you can create a multiplier of any size in minutes. For maximum performance, `lpm_mult` has a pre-defined parameter, `LPM_PIPELINE`, that allows you to automatically pipeline a multiplier. By modifying `LPM_PIPELINE`, you can easily optimize the speed and efficiency of your multiplier application.

Table 1. LPM Modules

LPM Module	Supported by Altera
lpm_abs	✓
lpm_add_sub	✓
lpm_and	✓
lpm_bipad	
lpm_bustri	✓
lpm_clshift	✓
lpm_compare	✓
lpm_constant	✓
lpm_counter	✓
lpm_decode	✓
lpm_ff	✓
lpm_fsm	
lpm_inpad	
lpm_inv	✓
lpm_latch	✓
lpm_mult	✓
lpm_mux	✓
lpm_or	✓
lpm_outpad	
lpm_ram_dq	✓
lpm_ram_io	✓
lpm_rom	✓
lpm_shiftreg	✓
lpm_ttable	
lpm_xor	✓

Table 2. Multiplier Comparison

Logic	FLEX 10K -3 Speed Grade (MHz) *(1)*	FLEX 8000 -2 Speed Grade (MHz) *(1)*	FLEX 6000 -2 Speed Grade (MHz) *(1)*
8 × 8 multiplier pipelined	131	132	114
8 × 8 multiplier non-pipelined	37	44	38
12 × 12 multiplier pipelined	80	81	78
12 × 12 multiplier non-pipelined	21	22	22
16 × 16 multiplier pipelined	53	69	59
16 × 16 multiplier non-pipelined	19	21	20
32 × 32 multiplier pipelined	28	*Note (2)*	*Note (2)*

Notes:
(1) Source: Altera Applications.
(2) The 32 × 32 multiplier is too large to fit in FLEX 8000 and FLEX 6000 devices.

Nova Engineering Introduces Megafunction Development System

AMPP partner Nova Engineering introduced the Constellation FLEX 10K Hardware Development System as a megafunction companion. The system is ideal for real-time hardware verification, rapid prototype development, and reconfigurable computers/accelerators.

Constellation is a PLD-based, hardware development system with a modular architecture that can be easily molded into any prototype configuration. This system delivers the flexibility and ease of use necessary for rapid prototype development. It is a low-cost, off-the-shelf product that provides support for a wide range of Altera's FLEX 10K devices, including 3.3-V and 5.0-V devices. The FLEX 10K development board can operate in a standalone configuration or can be expanded to include additional PLDs and analog subsystems. Modular interconnects provide "plug-and-play" access to high-speed A/D and D/A converters, creating a base development system for communication, signal processing, data acquisition, control, and graphics products. For more information, go to Nova Engineering's web site at **http://www.nova-eng.com**.

Questions & ANSWERS

Q *What problems may occur if I use Iomega software and hardware on my system with MAX+PLUS II version 7.1?*

A MAX+PLUS II version 7.1 installation may fail if you have Iomega software and hardware installed on your system. If you remove the Iomega software and hardware, the MAX+PLUS II software will install correctly.

While you can reinstall the Iomega software and hardware after MAX+PLUS II version 7.1 installation, you should never use the MAX+PLUS II software guard and the Iomega Zip drive simultaneously. If the MAX+PLUS II software guard is connected to the Iomega Zip drive, the software guard will be destroyed.

Q *How do I define a hexadecimal number using MAX+PLUS II VHDL?*

A The following example shows how to define a hexadecimal number using MAX+PLUS II VHDL:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;

ENTITY hex IS
  PORT(
    D : OUT STD_LOGIC_VECTOR (7 DOWNTO 0)
  );
END hex;

ARCHITECTURE a OF hex IS

BEGIN
-- The following line will convert the
-- hexadecimal value to a STD_LOGIC_VECTOR in
-- VHDL 1993.
   D <= x"FC";

-- The following line will convert the
-- hexadecimal value to a STD_LOGIC_VECTOR in
-- VHDL 1987.
   D(7 DOWNTO 0) <=TO_STD_LOGIC_VECTOR
     (x"FC");

END a;
```

Q *Can the DATA0 pin be used as an I/O pin in user mode for FLEX 10K designs?*

A No, the DATA0 pin cannot be used as an I/O pin in user mode for FLEX 10K designs. To avoid conflicts between configuration and user mode, the FLEX 10K DATA0 pin is a dedicated configuration pin.

You can use the DATA1, DATA2, DATA3, DATA4, DATA5, and DATA7 pins as I/O pins in user mode because these pins are not used in all configuration modes.

Q *Can I drive the I/O pins on an Altera device before power-up?*

Applying power to the inputs of most devices before power-up can cause latch up. However, you can apply power to the inputs of FLEX 10KA devices before power-up (except for EPF10K130V and EPF10K50V devices).

Q *Can I use an Intel-format Hexadecimal File (**.hex**) to program an EPC1 Configuration EPROM device?*

You should not program EPC1 Configuration EPROM devices with Hex Files. You must use a Programmer Object File (**.pof**) to program EPC1 Configuration EPROM devices, regardless of whether you are using Altera or third-party programming hardware.

Q *Can I program my revision C EPC1 Configuration EPROM using Data I/O programmers version 5.3?*

A If you program revision C EPC1 Configuration EPROMs using Data I/O programmers version 5.3, you will receive device ID errors. This problem is corrected in Data I/O programming software version 5.4, which is available from the following sources:

- Data I/O FTP site (**ftp.data-io.com**)
- Data I/O Bulletin Board Service (BBS) at (206) 882-3211

Revision C EPC1 devices have date codes "*y*C*xxxx*" marked on the top of the device, where *y* is any letter and *x* is any number. For example, if the date code is AC9707, the device is a revision C device.

Q *How can I provide licenses for multiple applications using the same license file?*

A The following guidelines explain how to license multiple applications using the same license file.

1. Ensure that the host ID specified in each license file is the same.
2. If the version of **lmgrd** is different between applications, use the latest version. However, if an application uses **lmgrd** pre-version 3.0, the application must be licensed separately with its own copy of **lmgrd**.

After these requirements are met, use the following format for the combined license file:

```
SERVER <host name> <host ID> <TCP/IP port number>
DAEMON <daemon application #1> <path/daemon file name>
DAEMON <daemon application #2> <path/daemon file name>
DAEMON <daemon application #3> <path/daemon file name>
FEATURE <feature name> <daemon> <version> <expiration date>
        <authentication code>
```

The single SERVER line gives the TCP/IP port number used by all applications when accessing licensing information. Specifying multiple license files to the LM_LICENSE_FILE environment variable using the : operator indicates that separate TCP/IP ports should be used for communication.

The individual DAEMON lines, required by all applications being licensed, can be listed in any order. **lmgrd** will start daemons in the order in which they are listed.

You can list FEATURE lines in any order after the DAEMON lines. After the application daemon is started, the FEATURE lines are read.

Q *How do I obtain the checksum for a device in a JTAG chain?*

A If the **Multi-Device JTAG Chain** command is turned on (JTAG menu) and you are programming devices in a JTAG chain, the checksum will not appear in the MAX+PLUS II Programmer because each device has an individual checksum (there is no checksum for the entire JTAG chain).

However, you can view the checksum of individual devices in the JTAG Chain by turning off the **Multi-Device JTAG Chain** command and selecting each programming file individually.

Q *How do I instruct the MAX+PLUS II Compiler to generate a timing Simulator Netlist File (**.snf**) for a device that supports a mixed-voltage interface with the MultiVolt feature?*

A In MAX+PLUS II version 8.0 and higher, perform the following steps in the Compiler:

1. Choose **Global Project Device Options** (Assign menu).
2. Turn on the *Low Voltage I/O* option.
3. Choose **OK**.

You cannot perform this action in MAX+PLUS II version 7.22 and lower. To obtain the correct timing parameters using these MAX+PLUS II software versions, refer to the appropriate device family data sheet. Substitute t_{OD2} for t_{OD1} to get the proper delay.

Q *How is a "blind interrogation" of the devices in a JTAG chain accomplished?*

A The IEEE 1149.1-1990 specification provides an optional IDCODE instruction mode that permits blind interrogation of the devices in a JTAG chain.

Upon power-up, any device that supports IDCODE will automatically load the IDCODE instruction into the instruction register. Any device that does not support IDCODE will automatically load the BYPASS instruction into the instruction register.

After power-up, the blind interrogation is accomplished by shifting data from the data register. Any device that supports IDCODE will shift out the 32-bit ID value with a "1" in the least significant bit (LSB) and any device that does not will shift out a "0" in the BYPASS register. To determine if a device supports IDCODE, simply check whether the first bit shifted out is a "1" or "0."

For additional information refer to *AN 39 (JTAG Boundary-Scan Testing in Altera Devices)*.

Q *Can I program a MAX 7000S device with a MAX□7000E Programmer Object File (**.pof**)?*

A Yes, you can program a MAX 7000S device with a MAX 7000E POF. The MAX 7000S device features are a superset of the MAX 7000E device features. Therefore, if you program a MAX 7000S device with a MAX 7000E POF, the MAX+PLUS II software will automatically disable the superset features on the MAX 7000S device.

This programming (often called cross-programming) is supported by the MAX+PLUS II software, as well as by third-party programmers such as programmers from Data I/O (**http://www.data-io.com**) and BP Microsystems (**http://www.bpmicro.com**).

Altera VIEWPOINT

PLD Pricing Roadmap Shows Steeper Reductions

Cliff Tong
Senior Director,
Product Marketing

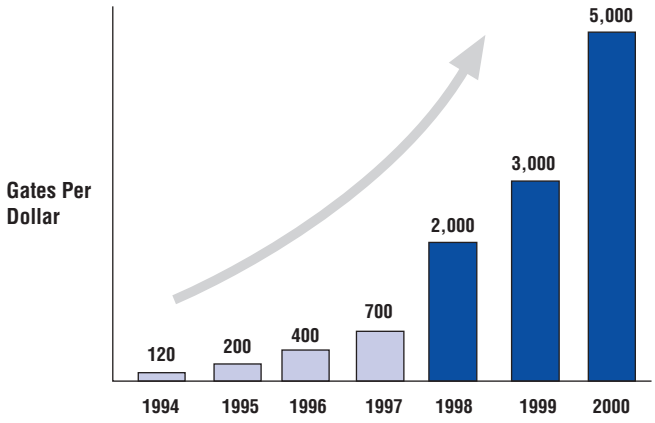
Altera expects to target PLD process technology at 0.18-micron by the year 2000.

The value of using high-density programmable logic in high volume will increase from the current level of about 700 gates per dollar to about 5,000 gates per dollar by the year 2000.

While ASIC and PLD suppliers provide a variety of information and tools to help designers determine performance and integration density, it is sometimes difficult for designers to obtain volume price projections. This difficulty is somewhat ironic, as device price is a significant factor in the up-front decision process of the system designer. In fact, several recent surveys of both programmable logic and ASIC users have shown that device price has commonly been identified as the most critical factor influencing device selection.

As the PLD price leader, Altera is more focused than ever on providing designers with the necessary insight on pricing, as well as the technical attributes of both existing and future products. Over the next three years, Altera anticipates an acceleration in cost reduction that will lead to price cuts of as much as 50% annually. The value of using high-density programmable logic in high volume is expected to increase from the current level of about 700 gates per dollar to about 5,000 gates per dollar by the year 2000 (see Figure 1). These price reductions, combined with the traditional time-to-market and risk reduction benefits of PLDs, will serve to further increase the use of high-density PLDs in volume applications where gate arrays were once used exclusively.

Figure 1. Altera Value Pricing Trend



Process Technology Advances Lead Die Size Reductions

Altera has been among the industry leaders in developing advanced process technologies. Since 1992, Altera's SRAM process geometry has exhibited an average linear shrink of nearly 20% per year, compared to an industry average of 11%. Altera has already begun 0.25-micron process development and plans to release devices using this process in the first half of 1998. Altera also plans to launch a project this year with one of its wafer manufacturing partners, Taiwan Semiconductor Manufacturing Corporation (TSMC), to develop a 0.18-micron SRAM process geometry for production in late 1999.

Further die size reductions may be obtained with the addition of metal layers in the circuit design. The continuous interconnect structure of Altera PLDs optimally leverages multilayer metal layout (see Figure 2). Current Altera devices are fabricated on a three-layer metal process, and Altera plans to ship devices using a four-layer metal process later this year. Five-layer metal process development is also underway for 1998.

Advanced Device Packaging Technology

As PLD process geometries continue to shrink, device packaging will take on added importance. Because device packaging is expected to become an increasing percentage of the total device cost, reducing package cost will become one of Altera's key objectives. Altera is working with packaging and assembly partners to develop lower-cost, production-worthy packages. Altera is

also researching a variety of advanced packaging, including new types of ball-grid array and flip-chip packages.

In ASIC designs, bond pad limitations are often the pacing item for die size and per-unit cost. Until recently, the amount of core logic has been the primary factor for determining PLD die size and cost. With the acceleration of process technologies, Altera PLDs are becoming "pad limited," where die size is no longer constrained by the total number of gates, but by bond-pad pitch. Altera is at the technology forefront of programmable logic suppliers by offering a bonding pad pitch of 81 µ for the recently introduced FLEX 6000 devices, and is aggressively developing an advanced bonding pad pitch of 55 µ for next-generation, 0.25-µ process devices.

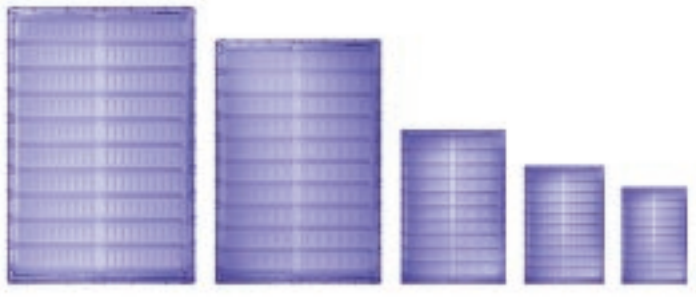
Other Technological Improvements

In addition to process geometry and advanced packaging, Altera will evaluate other technological improvements to lower device costs. Ongoing improvements in the use of circuit redundancy can greatly enhance product yield, leading to a lower per unit cost. Additional refinement of the continuous interconnect structure will further enhance device performance and die size, while maintaining routability. Continued investment in advanced synthesis and placement and routing algorithms will allow further gains in device resource usage.

Price Projections

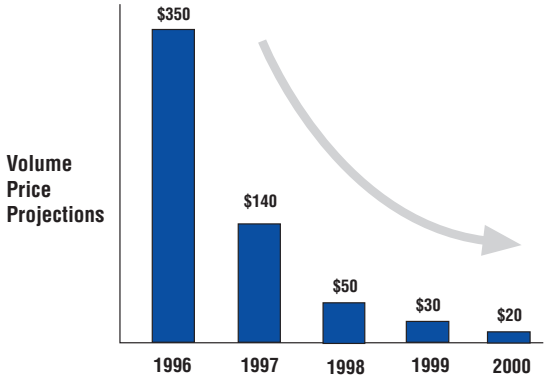
Device pricing is a critical factor in the system design process. During the next three years, Altera expects both FLEX and MAX family prices to decrease greatly. FLEX device pricing is expected to fall as much as 50% annually; MAX device pricing per macrocell is projected to fall by up to 37% annually. For example, the projected volume price for Altera's 100,000-gate EPF10K100 device is $140 at the end of 1997; by the end of 1998, it is expected to drop to $50; and by the end of the year 2000, pricing for this device is projected to be $20 (i.e., 5,000 gates per dollar). See Figure 3.

Figure 2. EPF10K50 Die Size Comparison



Note:
(1) This value indicates a normalized die size. Die shown are not actual size.

Figure 3. Projected Price Evolution for 100,000-Gate PLDs (EPF10K100)

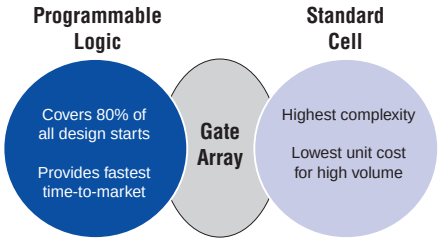


Conclusion

Dramatic feature size reductions are expected to decrease cost and increase device density and performance.

Price reductions are often larger than anticipated by the PLD market. In the future, Altera will use advanced process technologies to further reduce die size and costs, which permits even lower prices as well as dramatic increases in device density, performance, and functionality. Advanced packaging, proprietary circuit redundancy, and improved development tools accelerate the increasing value of the programmable logic solution. The combination of flexibility and faster time-to-market gives PLD users an increasingly attractive alternative to traditional gate-array solutions for high-volume applications (See Figure 4).

Figure 4. The Gate Array "Squeeze"



Customer Application

Bailey Controls Uses Megafunctions to Solve the PCI Challenge

"New and faster processors started hitting the market every 11 months or so, and we just didn't have the engineering bandwidth to create a new design and develop a new product every year."
—Bill Mohat, Senior Design Engineer, Bailey Controls

Bailey Controls, part of the international Elsag Bailey Process Automation N.V. group, needed a PCI bus to create a new industrial controls product that enabled processor upgrading without imposing costly product redesign burdens. They found the solution by working with Eureka Technology, an independent megafunction developer specializing in architecture-independent PCI megafunction solutions.

The Challenge

The engineers at Bailey Controls were caught in a difficult situation: they needed the ability to easily upgrade the microprocessors in their industrial control products but did not have the resources to completely redesign their single-board system. For years, Bailey Controls designed products based on Motorola 68000 family of microprocessors and proprietary ASICs. "Up to a certain point, our typical product life cycle was five to eight years using a specific processor," said Bill Mohat, a senior design engineer. "But new and faster processors started hitting the market every 11 months or so, and we just didn't have the engineering bandwidth to create a new design and develop a new product every year."

Managers and engineers decided they needed to develop an entirely new product line. Designing in the ability to upgrade without obsoleting the entire printed circuit board (PCB) would require uncoupling all custom elements from the microprocessor, including proprietary networks and I/O channels. At the same time, the Bailey Controls staff decided to use off-the-shelf hardware as much as possible and remain with the Motorola 68000 family. On top of these requirements, they faced limited engineering resources.

To meet the basic criteria, the design needed a bus that was both processor and clock-rate independent. The peripheral component interconnect (PCI) bus—a common, but complex bus technology—fit the criteria, but was unfamiliar to Bailey engineers. Finally, Bailey staff settled on a PCI-to-68030 bridge that would enable them to create a modular system enabling easy upgrades.

Bailey engineers looked at a number of alternatives for implementing the PCI interface. However, general-purpose devices failed to provide the necessary flexibility. In addition, they studied hardware solutions developed by other divisions in their parent company Elsag Bailey Process Automation, but found these solutions to be too demanding of engineering resources to meet the specific needs of the project.

The Megafunction Solution

An Altera field applications engineer (FAE) had worked with Bailey on programmable logic solutions and was familiar with the companies participating in the Altera Megafunction Partners

Eureka Technology

AMPP℠ ALTERA MEGAFUNCTION PARTNERS PROGRAM

Program (AMPP℠), an alliance of independent developers. The FAE suggested Bailey work with Eureka Technology of Los Altos, California, a company that specializes in PCI and PowerPC bus controller megafunctions.

"We wanted as generic an interface as possible and no one else had it," said Mohat. "Eureka took a PCI bus interface and de-multiplexed it. They had about a dozen or so registers inside the megafunction instead of the 200 we had found in standard products. And, they had the software and hardware to get this project up off the ground with a minimum of trouble. We talked to Simon Lau (Eureka President) and asked for some changes. We wanted multiple base address registers and the interrupt set up in a certain way. In a day or two we had a megafunction—containing all of our requirements—that could be dropped into an Altera device to turn it into a PCI interface."

As with most new products, there were final questions to answer before the new system was ready for production. "Our PowerPC processor is very abusive of the PCI bus and when there were back-to-back transfers to different boards, Eureka's megafunction mistakenly forwarded the wrong data byte," said Mohat. "We made one phone call to Simon and three hours later we had the new code via e-mail. One day later we had the new design running." The entire relationship with Eureka was conducted through e-mail and over the telephone. Figure 1 shows the prototyping and end-product hardware developed by Bailey using Eureka's PCI megafunction.

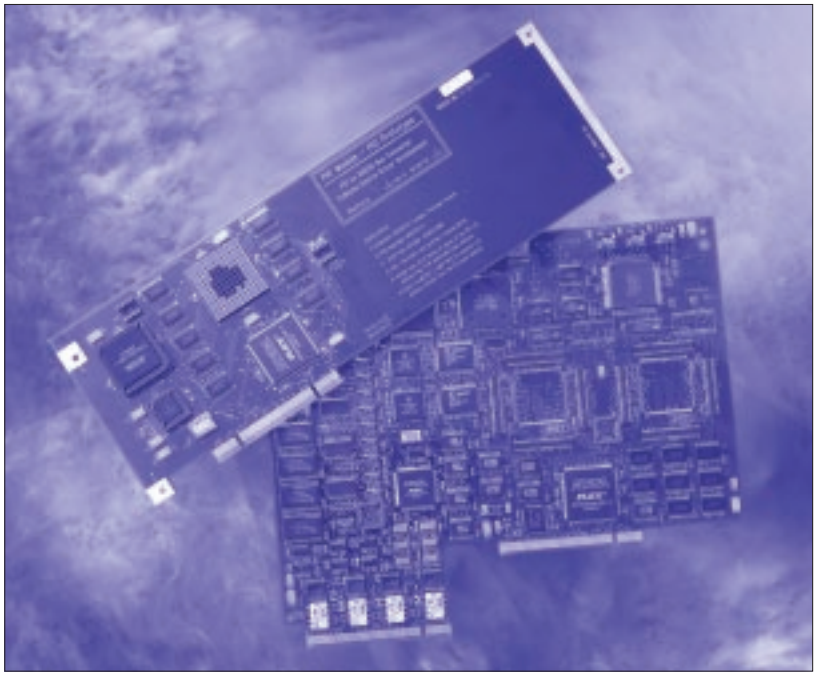
Looking Forward

Mohat knows that megafunctions will be vital to future Bailey products.

"Megafunctions are the way designs are going to be created over the next few years," he said. "As more and more people start selling larger pieces of intellectual property—either in the form of megafunctions, or VHDL or Verilog HDL source code—designers will buy more pieces and integrate them. We simply don't have the time or resources to do it all anymore."

The first pass with Eureka's PCI megafunction was so easy and successful that Bailey went back to Eureka directly for the next generation product—which was just as easy to use and as successful. The PCI megafunction not only saved Bailey valuable engineering time, but also cost less than designing the solution in-house, according to Mohat. "It appears easier to grab an ASSP at $25 per piece," he said. "But unless you've worked with a PCI bus, you don't understand how fiendishly complex it is, and standard products don't eliminate all that complexity. It's far cheaper to use megafunctions when all the costs are considered."

"Megafunctions are the way designs are going to be created over the next few years," Mohat said. "As more and more people start selling larger pieces of intellectual property—either in the form of megafunctions, or VHDL or Verilog HDL source code—designers will buy more pieces and integrate them."



Altera's Failure Analysis Service

Altera offers a Failure Analysis Service, which is designed to perform detailed analysis on suspected failing devices. The main goal of Altera's Failure Analysis Service is to resolve these problems quickly. Altera recognizes that timely failure analysis is critical to meet the time-to-market needs of today's designers.

Altera's Failure Analysis Service not only includes device examination, but also helps you troubleshoot device-related issues. Resolving an issue quickly, without requiring devices to be sent to Altera for analysis, helps you use Altera® devices in your systems with greater ease. For more difficult issues, Altera will analyze the device to determine the cause of the failure. Altera will then inform you of the cause of the failure, as well as suggest ways to prevent the failure from occurring in the future.

Failure Analysis Capabilities

Altera uses state-of-the-art equipment for failure analysis. Depending on the type of failure reported, Altera can perform any number of tests to resolve the issues, including full functional and timing tests, C-mode scanning acoustic microscopy (C-SAM), scanning electron microscopy, emission microscopy, x-ray, and liquid crystal testing. See Figures 1, 2, and 3.

Using Altera's Failure Analysis Services

To use Altera's failure analysis services, first contact your Altera Failure Analysis Specialist (FAS), who has been trained on failure analysis techniques and can initiate a failure analysis. If you are unsure how to contact your FAS, contact Altera Applications or your local Altera sales office. The FAS will review the failure in detail, and may even be able to resolve the issue immediately.

If the FAS cannot resolve the issue immediately and device analysis is warranted, the FAS will issue an Evaluation Return Materials Authorization (ERMA) and send you a Failure Analysis Kit. The ERMA number authorizes you to send devices directly to Altera for failure analysis. If you would like credit for the devices, a credit request form is included in the Failure Analysis Kit.

Failure Analysis Kit

You can use the Failure Analysis Kit to quickly and safely return devices to Altera for analysis. The Failure Analysis Kit (see Figure 4) contains the following items:

- A pre-addressed, pre-paid Federal Express package for you to send failing devices to Altera

Figure 1. Device with Delamination

The C-SAM test non-destructively checks for device delamination. Delamination (separation of the die from the molding compound) can be caused by improper solder reflow techniques or by improper handling of moisture-sensitive devices. This figure shows a device with delamination. For more information, refer to AN 81 (Reflow Soldering Guidelines for Surface-Mount Devices).

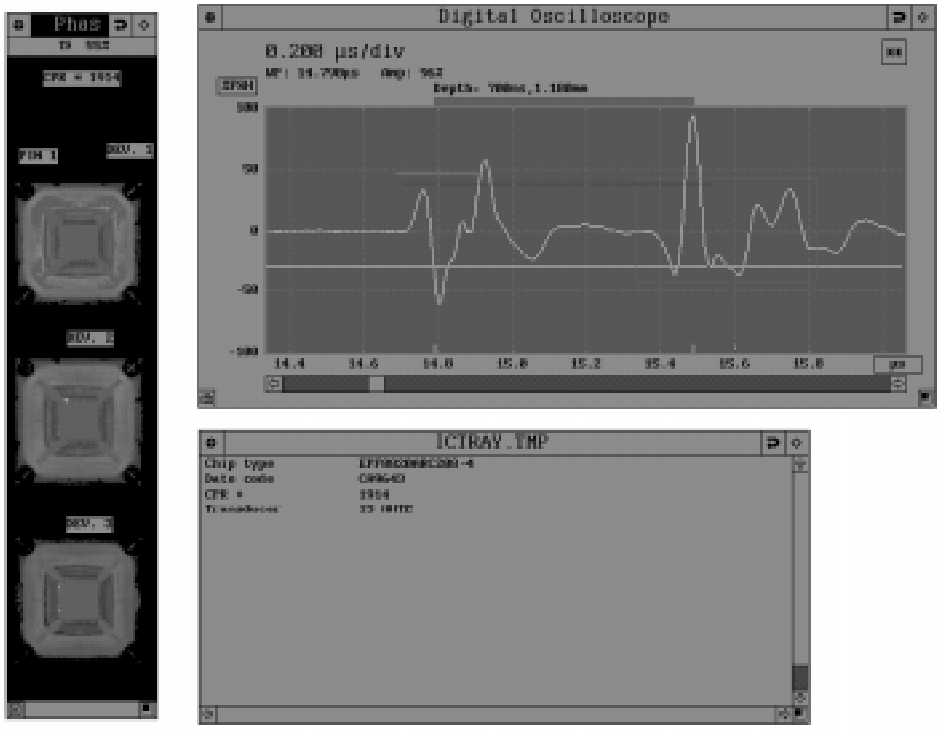


Figure 2. Emmission Microscope Shows Leakage on Pins 19 & 20

Emission microscopy can isolate the specific location of the failure. In this test, the device is loaded with test vectors to "exercise" the device. An emission microscope can detect excessive current, pinpointing damaged circuitry. This figure shows the results of an emission microscope test; high current leakage is normally shown in red, but for this publication, the location is shown with arrows.

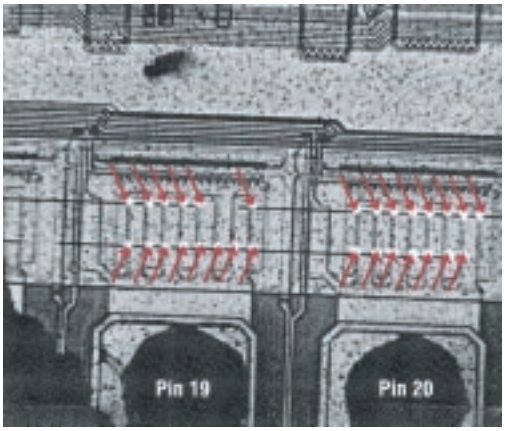
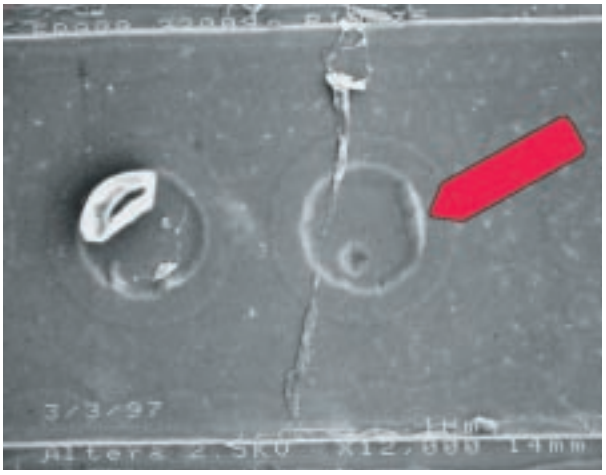


Figure 3. SEM Test Shows Spiking

Altera can also use a scanning electron microscope (SEM) to analyze a device. In this figure, the SEM test found spiking under metal caused by electrical overstress.



- Appropriate device packaging to protect the device during shipment
- Instructions and a questionnaire to obtain more detailed information regarding the failure (a completed form is required for processing)
- A 3.5-inch diskette to send back the design, programming, and simulation files (the diskette also includes a soft copy of all questionnaires)
- Credit request form (must be completely filled out to receive credit for up to five devices)

Failure Analysis Results

Altera will fax you a confirmation upon receipt of the FedEx package. The initial analysis is typically performed within three working days of receipt of the devices at Altera. The initial production test results are faxed directly to you.

If further testing is required, the FAS will keep you informed of the progress of the failure analysis until the issue is closed with a final report. The final reports are written by the FAS and all the results are reviewed with you to ensure the issue is resolved to your satisfaction.

Altera provides this new Failure Analysis Service as part of its commitment to quality and customer service. Approximately half of all devices sent to Altera for failure analysis are good devices. Thus, sending devices to Altera without first fully checking the setup pattern can delay the resolution of an issue. For questions or comments regarding Altera's Failure Analysis Services, please contact your FAS or Altera at **fas@altera.com**.

Figure 4. Failure Analysis Kit Contents

The Advantages of EABs for PCI Applications

The FLEX 10K embedded array blocks (EABs) provide significant advantages for numerous applications. For example, peripheral component interconnect (PCI) designs gain important benefits if an on-device first-in first-out (FIFO) function is implemented in FLEX 10K EABs using a PCI megafunction.

The Importance of FIFOs

Without a pre-built FIFO function, you must choose one of three alternatives, each of which has drawbacks:

- Operate the local side interface at the same speed as the PCI bus
- Add an external FIFO on a second device
- Implement an internal FIFO by using logic as RAM

In many applications, it may not be technically possible to operate the local side interface at the same speed as the PCI bus. Even if it is possible, the overall cost may be too high, as a higher operating frequency means faster, more expensive devices, and a more complicated printed circuit board (PCB) design.

Using an external FIFO function on a separate device leads to higher costs, increased power consumption, and increased PCB space.

Two problems can result from converting logic into RAM to implement an internal FIFO function. If you are implementing the FIFO function in an FPGA, for example, the unpredictable timing of these devices makes it almost impossible to convert logic to RAM and still meet the rigorous PCI timing requirements. Also, by using logic as RAM, less logic is available for other features, such as integrating local side functionality into the PLD.

In contrast, Altera's FLEX 10K devices impose no such tradeoff; neither speed nor area is lost when an on-device FIFO function is implemented in the FLEX 10K EABs.

Maximum PCI Bus Speed

Including a FIFO with a PCI interface allows the PCI bus to operate at its maximum speed. Without a FIFO to buffer data, the PCI bus and the local side would have to operate at the same speed, i.e., the speed of the local side. The FIFO provided with the `pci_a` MegaCore™ function, for example, allows the PCI bus to operate at its maximum operating data rate of 33 MHz, even when the local side cannot transfer data at the same rate.

You can also use the EAB architecture in FLEX 10K devices to implement larger on-device FIFO buffers if needed. Larger FIFO buffers support larger PCI bus burst transfers and therefore higher bus throughput. For example, Altera's next generation PCI functions will allow designers to include an on-device FIFO as large as 1,024 bytes (using 4 EABs) in an EPF10K30 device and still have all of the EPF10K30 logic elements (LEs) available for logic.

Conclusion

Using the FLEX 10K EABs to implement an on-device FIFO function for a PCI design offers you distinct advantages. With an on-device FIFO, the PCI bus can operate at its maximum speed, without concern for the speed of the local side. The complete PCI design, including the FIFO, can be accommodated on a single device. Valuable logic is conserved for user-defined needs. Altera's FLEX 10K EAB architecture and the PCI megafunctions offered by Altera and the Altera Megafunction Partners Program (AMPP) provide the winning combination. For further information about Altera's PCI solution, refer to the *PCI Master/Target MegaCore Function with DMA Data Sheet* or contact your local Altera sales representative.

The Altera Power Play Scores Big at DAC

At the June Design Automation Conference (DAC) in Anaheim, Altera showcased the "Power Play" solution, which combines cutting-edge high-density devices with advanced megafunctions and powerful design tools. Over 1,000 designers visited Altera's booth, which featured hands-on demonstrations from Altera and ACCESS™ partners.

Altera Target Applications

Target Applications provides solutions to designers' application-specific needs. Target Applications leverages MegaCore functions and functions from the Altera Megafunction Partners Program (AMPP) to provide integrated solutions that deliver significant time-to-market benefits. The complete Target Applications solution includes the megafunctions and documentation that are critical to get these functions working in-system. Altera Target Applications focuses on the following areas:

- FLEX DSP
  - DSP building blocks
  - DSP imaging functions
  - DSP wireless and broadband communications
- Bus interfaces
  - PCI
  - Universal serial bus (USB)
- Communications
  - Data communications and telecommunications
  - Asynchronous transfer mode (ATM)

Several new bus interface functions have been developed recently, including:

- AMPP partner Sapien Technology has produced a USB function and a USB node controller
- New AMPP and MegaCore PCI functions

Future bus interface applications will include functions supporting the I2C, CANbus, and FireWire (IEEE 1394) interfaces. A summary of the current bus interface functions is shown in the table below.

Bus Interface Functions

Function	Source
PCI Master/Target Interface	Altera MegaCore Function
PCI Target Interface	Eureka Technology
PCI Master/Target Interface	Eureka Technology
PCI Target Interface	PLD Applications
PCI Master/Target Interface	PLD Applications
USB Node Controller	Sapien Technology
USB Function Controller	Sapien Technology

Altera at DSP World Expo

Altera will be participating in the International Conference on Signal Processing and Technology (ICSPAT) and DSP World Expo September 14 through 17 in San Diego. Altera engineers will present two papers, *Pipelined Adaptive Filters in Altera PLDs* and *DSP Processor Core for FLEX 10K,* and will co-present *PLD-Based FFTs* and *A PLD-Based Solution for Cable Modem* with AMPP partner Integrated Silicon Systems. These papers will be presented in the FPGAs in DSP session.

Altera will also be showcasing the FLEX DSP solution on the DSP World Expo floor. Stop by booth 115 for the latest demonstration of Altera's DSP solution.

Altera Has Moved

In July 1997, Altera moved to new corporate headquarters. You can now contact Altera at:

Altera Corporation
101 Innovation Drive
San Jose, CA 95134
Telephone: (408) 544-7000
http://www.altera.com

MAX 7000 Beats Kasparov

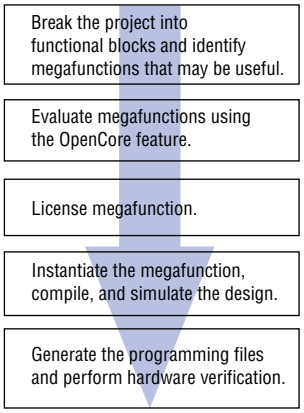
In May 1997, the reigning world chess champion was bested by a computer. IBM's chess-playing computer Deep Blue defeated Garry Kasparov, the reigning Grand Master, 3.5 to 2.5. This computing triumph was also a victory for the MAX 7000 family; Altera MAX□7000 devices were used in the construction of Deep Blue. Kasparov put up a valiant struggle against Deep Blue and MAX 7000, but in the end Deep Blue, powered by MAX 7000 devices, was victorious.

Test-Drive Megafunctions with the OpenCore Feature

The unique, no-risk OpenCore™ evaluation feature offered by Altera allows you to test-drive MegaCore functions before you purchase them. Altera's MegaCore functions are reusable, synthesizable megafunctions that are optimized for Altera programmable logic devices (PLDs). Simply download a MegaCore function from the Altera world-wide web site at **http://www.altera.com** free of charge. Then, you can instantiate the megafunction in a MAX+PLUS II file, and simulate and verify your design. Once your design is completed, you can license the MegaCore function and obtain an authorization code. With the fully licensed version you can use the MAX+PLUS II software to generate programming files, EDIF netlist files, and VHDL and Verilog HDL output files for simulation in third-party EDA tools.

In addition to the Altera MegaCore functions, the OpenCore feature allows you to test-drive the megafunctions offered by the partners in the Altera Megafunctions Partners Program (AMPP). Contact the AMPP partners directly to obtain the encrypted AMPP megafunction file and an OpenCore evaluation authorization code. The OpenCore feature allows you to compile the megafunction and determine the megafunction's size and speed. Once your design is completed, you can license the megafunction from the AMPP partner and obtain an authorization code to generate programming files and other output files. Figure 1 shows the design flow when using either an Altera MegaCore function or an AMPP megafunction.

Figure 1. Design Flow for an Altera MegaCore Function or AMPP Megafunction



In Every ISSUE

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for selected Altera devices. Algorithms are supplied via Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Microsystems' BBS. Programming support for Configuration EPROM, MAX 9000, and MAX 7000 devices is shown in the table below. All information is subject to change.

Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPM7032	✓	✓
EPM7064	✓	✓
EPM7096	✓	✓
EPM7128E	✓	✓
EPM7128S	✓	✓
EPM7160E	✓	✓
EPM7192E	✓	✓
EPM7192S	✓	✓
EPM7256E	✓	✓
EPM7256S	✓	✓
EPM9320	✓	*Note (3)*
EPM9400	✓	*Note (3)*
EPM9480	✓	*Note (3)*
EPM9560	✓	*Note (3)*

Notes to tables:

(1) These devices are supported by Data I/O 2900 version 5.5, 3900 version 5.5, and UniSite version 5.5 programmers.

(2) These devices are supported by BP Microsystems programmers version 3.25.

(3) BP Microsystems plans to support MAX 9000 devices in the future. Contact your local Altera representative or BP Microsystems for more information.

Altera Programming Hardware Support

The following tables contain the latest programming hardware information for Altera devices. For correct programming, use the software version shown in "Current Software Versions" below. PLM-prefix adapters can be used only with the Master Programming Unit (MPU). See Table 1.

Table 1. Altera Programming Adapters (Part 1 of 2) *Note (1)*

Device	Package	Adapter
EPC1064, EPC1064V, EPC1213 (all FLEX 8000 devices)	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 (FLEX 10K and FLEX 8000 devices)	DIP J-lead	PLMJ1213 PLMJ1213
MAX 9000A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC PLMR9000-240NC
EPM9320	PGA J-lead (84-pin) RQFP (208-pin)	PLMG9000-280 PLMJ9320-84 PLMR9000-208
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	PGA RQFP (208-pin) RQFP (240-pin) RQFP (304-pin)	PLMG9000-280 PLMR9000-208 PLMR9000-240 PLMR9000-304
MAX 7000S *(2)*	PQFP (100-pin) TQFP (100-pin)	PLMQ7000-100NC PLMT7000-100NC
EPM7032, EPM7032V	J-lead PQFP TQFP	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7064S	J-lead TQFP	PLMJ7000-44 PLMT7000-44

Current Software Versions

The latest versions of Altera software products are shown below:

- MAX+PLUS II version 8.0
  (PC, Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 platforms)

Table 1. Altera Programming Adapters (Part 2 of 2) *Note (1)*

Device	Package	Adapter
EPM7064	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128S, EPM7160S *(2)*	PQFP (160-pin)	PLMQ7128/160-160NC
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160, EPM7160E	J-lead PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7192S *(2)*	PQFP (160-pin)	PLMQ7192/256-160NC
EPM7192, EPM7192E	PGA PQFP	PLMG7192-160 PLMQ7192/7256-160
EPM7256S *(2)*	RQFP (208-pin)	PLMQ7256-208NC
EPM7256E	PGA MQFP, RQFP PQFP	PLMG7256-192 PLMR7256-208 PLMQ7192/7256-160

Table 2 provides programming information for the BitBaster™ serial and ByteBlaster™ parallel port download cables.

Table 2. Programming with the BitBlaster & ByteBlaster

Device	Package	Hardware
FLEX 10K	All packages	PL-BITBLASTER PL-BYTEBLASTER
FLEX 8000	All packages	PL-BITBLASTER PL-BYTEBLASTER
FLEX 6000	All packages	PL-BITBLASTER PL-BYTEBLASTER
MAX 9000	All packages	PL-BITBLASTER PL-BYTEBLASTER
MAX 7000S	All packages	PL-BITBLASTER PL-BYTEBLASTER

Notes to tables:

(1) Refer to the Altera ***1996 Data Book*** for device adapter information for MAX 5000 and Classic devices. Altera offers an adapter exchange program for 0.8-micron EPM5032, EPM5064, and EPM5130 programming adapters. See "Product Transitions" on page 7 of this newsletter for more information.

(2) These devices are not shipped in carriers.

Altera Device Selection Guide

All current information for the Altera FLEX 10K, FLEX 8000, MAX 9000, and MAX 7000 devices is listed here. Information on other Altera products is located in the Altera ***1996 Data Book***. Contact Altera or your local sales office for current product availability.

FLEX 10K Devices

DEVICE *(1)*	GATES	PIN/PACKAGE OPTIONS	I/O PINS	TEMP.	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin QFP	59, 107, 134	C	-3, -4	720	576	6,144
EPF10K10A		144-Pin TQFP, 208-Pin QFP	107, 134	I	-4			
EPF10K20	20,000	144-Pin TQFP, 208-Pin QFP, 240-Pin QFP	107, 147, 189	C	-3, -4	1,344	1,152	12,228
EPF10K30	30,000	144-Pin TQFP *(2)*, 208-Pin QFP, 240-Pin QFP, 356-Pin BGA	107, 147, 189, 246	C	-3, -4	1,968	1,728	12,228
EPF10K30A		240-Pin QFP	189	I	-4			
EPF10K40	40,000	208-Pin QFP, 240-Pin QFP	147, 189	C	-3, -4	2,576	2,304	16,384
EPF10K50	50,000	240-Pin QFP, 356-Pin BGA, 403-Pin PGA *(3)*	189, 274, 310	C	-3, -4	3,184	2,880	20,480
EPF10K50V		240-Pin QFP	189	I	-4			
EPF10K50A								
EPF10K70	70,000	240-Pin QFP, 503-Pin PGA	189, 358	C	-3, -4	4,096	3,744	18,432
EPF10K100	100,000	240-Pin QFP *(2)*, 356-Pin BGA *(2)*, 503-Pin PGA, 600-Pin BGA *(2)*	189, 274, 406, 406	C	-3, -4	5,392	4,992	24,576
EPF10K100A								
EPF10K130V	130,000	600-Pin BGA, 599-Pin PGA	470	C	-3, -4	7,120	6,656	32,768
EPF10K130A								
EPF10K250A	250,000	600-Pin BGA, 599-Pin PGA	470	C	-3, -4	12,624	12,160	40,960

Notes:
(1) Not all devices are currently available. Contact Altera for FLEX 10KA device availability.
(2) Available in FLEX 10KA devices only.
(3) Not available in FLEX 10KA devices.

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS *(1)*	TEMP.	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C	A-2	282	208
		84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-3		
		84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-4		
EPF8282AV *(2)*	2,500	100-Pin TQFP	78	C	A-4	282	208
EPF8452A	4,000	160-Pin PQFP	120	C	A-2	452	336
		84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA / PQFP	68, 120	C, I	A-3		
		84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA / PQFP	68, 120	C, I	A-4		
EPF8636A	6,000	208-Pin PQFP	136	C	A-2	636	504
		84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	C	A-3		
		84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	C, I	A-4		
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	112, 120, 152	C	A-2	820	672
		144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	C	A-3		
		144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	C, I	A-4		
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C	A-2	1,188	1,008
		208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-3		
		208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-4		
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-2	1,500	1,296
		240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C, I	A-3		
		240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-4		

Notes:
(1) Four I/O pins are dedicated inputs.
(2) A "V" indicates a 3.3-V voltage supply.

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS *(1)*	TEMP.	SPEED GRADE	FLIPFLOPS	LOGIC ELEMENTS
EPF6010	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin QFP	81, 117, 160	C	-2	800	800
		100-Pin TQFP, 144-Pin TQFP, 208-Pin QFP	81, 117, 160	C, I *(3)*	-3	800	800
EPF6016	16,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin QFP, 240-Pin PQFP, 256-Pin BGA	81, 117, 171, 199, 204	C	-2	1,320	1,320
		100-Pin TQFP, 144-Pin TQFP, 208-Pin QFP, 240-Pin PQFP, 256-Pin BGA	81, 117, 171, 199, 204	C, I *(3)*	-3	1,320	1,320
EPF6016A *(2)*	16,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin QFP, 240-Pin PQFP, 256-Pin BGA	81, 117, 171, 199, 204	C	-2	1,320	1,320
		100-Pin TQFP, 144-Pin TQFP, 208-Pin QFP, 240-Pin PQFP, 256-Pin BGA	81, 117, 171, 199, 204	C, I *(3)*	-3	1,320	1,320
EPF6024A *(2)*	24,000	208-Pin QFP, 240-Pin PQFP, 256-Pin BGA	171, 199, 215	C	-2	1,960	1,960
		208-Pin QFP, 240-Pin PQFP, 256-Pin BGA	171, 199, 215	C, I *(3)*	-3	1,960	1,960

Notes:
(1) Four I/O pins are dedicated inputs.
(2) An "A" indicates a 3.3-V voltage supply.
(3) The faster commercial temperature speed grade devices are de-rated to operate over the industrial temperature range.

MAX 9000 Devices

DEVICE	MACRO-CELLS	PIN/PACKAGE OPTIONS	I/O PINS *(1)*	TEMP.	SPEED GRADE
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	C	-15
	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	C, I	-20
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	C	-7, -10
	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	C, I	-15
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-15, -20
EPM9400A	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-10, -12
	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C, I	-15
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C	-15, -20
EPM9480A	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C	-10, -12
	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C, I	-15
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C	-15
	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C,I	-20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C	-10, -12
	560	208-Pin RQFP, 240-Pin RQFP, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	C,I	-15

Note:
(1) Four I/O pins are dedicated inputs.

MAX 7000 Devices *(Part 1 of 2)*

DEVICE	MACRO-CELLS	PIN/PACKAGE OPTIONS	I/O PINS	TEMP.	SPEED GRADE	t_{PD} (ns)	f_{CNT} (MHz)
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-5	5	178.6
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-6	6	150
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-7	7.5	125
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C, I *(1)*	-10	10	100
EPM7032	32	44-Pin PLCC/TQFP	36	C, I	-12 *(2)*	12	90.9
EPM7032	32	44-Pin PLCC/TQFP	36	C, I	-15 *(2)*	15	76.9
EPM7032V *(2)*	32	44-Pin PLCC/TQFP	36	C	-12	12	90.9
EPM7032V *(2)*	32	44-Pin PLCC/TQFP	36	C	-15	15	76.9
EPM7032V *(2)*	32	44-Pin PLCC/TQFP	36	C, I	-20	20	62.5
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC *(2)*, 84-Pin PLCC, 100-Pin PQFP *(2)*/TQFP *(1)*	36, 52, 68	C	-6	6	150
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC *(2)*, 84-Pin PLCC, 100-Pin PQFP *(2)*/TQFP *(1)*	36, 52, 68	C	-7	7.5	125
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC *(2)*, 84-Pin PLCC, 100-Pin PQFP *(2)*/TQFP *(1)*	36, 52, 68	C, I *(1)*	-10	10	100
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-12 *(2)*	12	90.9
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C, I	-15 *(2)*	15	76.9

continued on page 30

Altera Device Selection Guide, continued from page 29

MAX 7000 Devices (Part 2 of 2)

DEVICE	MACRO-CELLS	PIN/PACKAGE OPTIONS	I/O PINS	TEMP.	SPEED GRADE	t_{PD} (ns)	f_{CNT} (MHz)
EPM7096	96	68-Pin PLCC *(2)*, 84-Pin PLCC, 100-Pin PQFP/TQFP *(1)*	52, 64, 76	C	-7	7.5	125
EPM7096	96	68-Pin PLCC *(2)*, 84-Pin PLCC, 100-Pin PQFP/TQFP *(1)*	52, 64, 76	C, I *(1)*	-10	10	100
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-12 *(2)*	12	90.9
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C, I	-15 *(2)*	15	76.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP *(1)*, 160-Pin PQFP	68, 84, 100	C	-7	7.5	125
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP *(1)*, 160-Pin PQFP	68, 84, 100	C, I *(1)*	-10(P)	10	100
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12 *(2)*	12	90.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP *(1)*, 160-Pin PQFP	68, 84, 100	C, I	-15	15	76.9
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20 *(2)*	20	62.5
EPM7160S	160	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	64, 84, 104	C	-7	7.5	125
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP/TQFP *(1)*, 160-Pin PQFP	64, 84, 104	C, I *(1)*	-10(P)	10	100
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12 *(2)*	12	90.9
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP/TQFP *(1)*, 160-Pin PQFP	64, 84, 104	C, I	-15	15	76.9
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20 *(2)*	20	62.5
EPM7192S	192	160-Pin PQFP	124	C	-7	7.5	125
EPM7192S	192	160-Pin PQFP	124	C	-10	10	100
EPM7192E	192	160-Pin PQFP/PGA	124	C	-12(P)	12	90.9
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA *(2)*	124	C, I *(1)*	-15	15	76.9
EPM7192E	192	160-Pin PQFP/PGA	124	C, I	-20 *(2)*	20	62.5
EPM7256S	256	208-Pin RQFP	132, 164	C	-7	7.5	125
EPM7256S	256	208-Pin RQFP	132, 164	C	-10	10	100
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA *(2)*, 208-Pin RQFP	132, 164	C	-12(P)	12	90.9
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA *(2)*, 208-Pin RQFP	132, 164	C, I *(1)*	-15	15	76.9
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C, I	-20 *(2)*	20	62.5

Notes:
(1) Available in MAX 7000S devices only.
(2) Not available in MAX 7000S devices.

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	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline (8 a.m. to 5 p.m. Pacific Time)	(800) 800-EPLD (408) 544-7000	(408) 544-7000 *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	sos@altera.com	sos@altera.com
	FTP Site	ftp.altera.com	ftp.altera.com
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Notes:
(1) For MAX+PLUS II software manuals, contact Altera Customer Service or your local distributor.
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