The Altera Advantage News & Views

Newsletter for Altera Customers ◆ Second Quarter ◆ May 1998

Altera Unveils FLEX 10KE Devices

Altera recently unveiled enhanced versions of FLEX® 10K embedded programmable logic devices—FLEX 10KE devices. Fabricated on a 0.25-µm, five-layer-metal process with a 2.5-V core, FLEX 10KE devices meet the demands of system designers for increased functionality and faster performance at a low cost.

The FLEX 10KE devices, which include EPF10K100B devices, has added enhancements that extend Altera's leadership in embedded architectures to new levels of performance and silicon efficiency. Combined with the inherent time-to-market benefits of programmable logic, the enhanced FLEX 10KE devices will accelerate the movement of high-speed designs from masked gate arrays to programmable logic.

Enhanced Features

The "E" in FLEX 10KE devices stands for "enhanced" features. FLEX 10KE devices contain many powerful system-level features that boost design performance and device utilization, including:

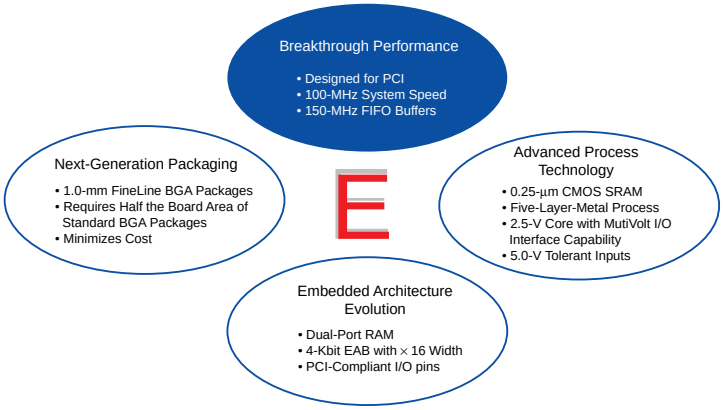
- Embedded array blocks (EABs) with double the amount of RAM (4 Kbits)
- Dual-port RAM capability with 150 MHz first-on first-out (FIFO) performance
- Pin-selectable I/O clamping diodes, which provide 3.3-V PCI compliance and 5.0-V tolerance in the same device
- 1.0-mm FineLine BGA™ packaging option, utilizing almost half the board area of traditional ball-grid array (BGA) packages
- Low power consumption
- MultiVolt™ I/O operation, supporting 2.5-V, 3.3-V, and 5.0-V mixed-voltage systems

Figure 1 summarizes the enhanced FLEX 10KE features.

Innovative Embedded Architecture

Altera pioneered the embedded programmable logic architecture in 1995 by combining EABs with logic array blocks (LABs). This new architecture provided a dramatic increase in the performance and density of the industry's first embedded PLDs—FLEX 10K devices. FLEX 10KE devices maintain this unique embedded architecture, while adding significant enhancements to the original family. FLEX 10KE devices are pin- and function-compatible with existing FLEX 10K and FLEX 10KA devices.

Figure 1. Enhanced FLEX 10KE Features



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Dual-Port RAM

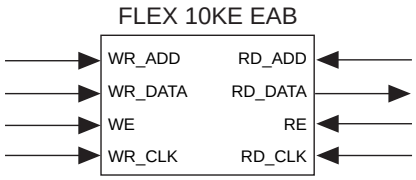
Each FLEX 10KE EAB has dual-port RAM capability, 4 Kbits of memory, and up to 16 bits of width. These enhancements provide a new level of performance and efficiency for implementing megafunctions such as high-speed memories, first-in first-out (FIFO) buffers, and specialized logic functions. The EABs also support dual-port applications and other large memory block requirements. Figure 2 shows the FLEX 10KE dual-port RAM block.

Advanced Process Technology

FLEX 10KE devices are based on an advanced 0.25-µm, five-layer-metal process consisting of a continuous transistor-free metal interconnect that optimizes the use of multiple process metal layers. This architecture allows the "stacking" of metal layers. This "metal-friendly" architecture also supports die sizes that are half the size of comparable field programmable gate arrays (FPGAs). FPGAs use transistor-heavy interconnects, which cannot be "stacked" and cannot optimize the use of multiple process metal layers. Therefore, FPGAs have significant die size increases, and they sacrifice both cost-effectiveness and performance.

Figure 3 shows how the smaller process geometry and metal efficiency of FLEX 10KE devices results in a die size that is smaller than a comparable FLEX 10KA device and less than half the size of a comparable FPGA.

Figure 2. FLEX 10KE Dual-Port RAM Block



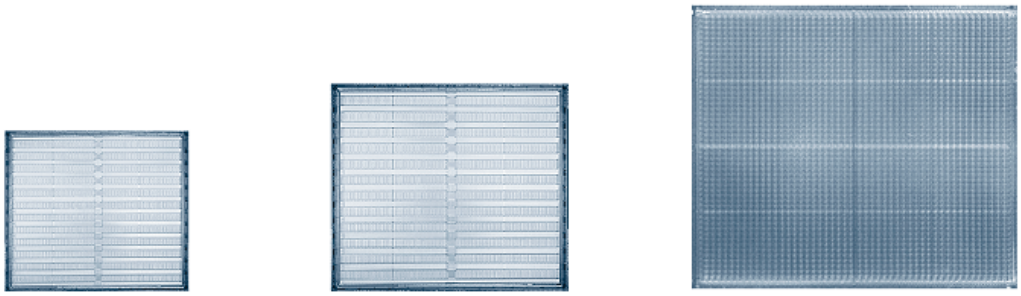
Breakthrough Performance

FLEX 10KE devices provide significant performance improvements. With the 0.25-µm, five-layer-metal process and an enhanced EAB structure, these devices provide a higher level of system bandwidth for today's demanding performance requirements. For example, FLEX 10KE devices can support up to 150-MHz FIFO buffer performance, with 6.5-ns access time for a 256 × 16 memory block. Table 1 shows the FLEX 10KE-1 FIFO performance.

Table 1. FLEX 10KE FIFO Speed

FIFO Size (d × w)	FLEX 10KE-1 (MHz)	FLEX 10KA-1 (MHz)
16 × 32	150	128
32 × 32	125	81
64 × 32	115	81
128 × 32	100	78
256 × 32	98	76

Figure 3. FLEX 10KE Die Comparison



Altera
EPF10K100E
Relative Die Size = 0.6
0.25 µ
4,992 Logic Cells
12 EABs

Altera
EPF10K100A
Relative Die Size = 1.0
0.35 µ
4,992 Logic Cells
12 EABs

Comparable
FPGA
Relative Die Size = 1.91
0.35 µ
4,608 Logic Cells
0 EABs

3.3-V PCI Compliance

All FLEX 10KE devices support the PCI Special Interest Group (PCI-SIG) ***PCI Local Bus Specification, Revision 2.1***. The devices will offer 100-MHz system speed and support 66-MHz PCI performance for advanced communication applications, such as 100-Mbit and 1-Gbit Ethernet connections.

In addition, FLEX 10KE devices have pull-up I/O clamping diodes on every I/O, dedicated input, and dedicated clock pin to allow simultaneous PCI compliance and 5.0-V tolerance on the same device. These diodes clamp the signal to the V_{CCIO} value and are required for 3.3-V PCI compliance. They are controlled on a pin-by-pin basis via a user-selectable option in the Altera® MAX+PLUS® II software, which will allow a device to bridge between a 3.3-V PCI bus and a 5.0-V local-side device.

Lower Power Consumption & MultiVolt I/O Interface

FLEX 10KE devices have a core supply voltage of 2.5 V, which reduces power consumption significantly. FLEX 10KE devices also offer the MultiVolt I/O interface, which enables core operation at 2.5 V, but allows the I/O pins to be compatible with 2.5-V, 3.3-V, or 5.0-V devices.

Innovative FineLine BGA Packaging

FLEX 10KE devices will be available in FineLine BGA packages, which are 1.0-mm BGA packages that offer higher lead counts and smaller package sizes. The innovative FineLine BGA packages have pin counts ranging from 100 to 672 pins and require less than half the board area of standard 1.27-mm BGA packages. For more details on FineLine BGA packages, see "Next-Generation BGA Packaging" on page 12.

FLEX 10KE devices will also be offered in thin quad flat pack (TQFP), plastic quad flat pack (PQFP), and power quad flat pack (RQFP) packages. See Table 1.

Device Availability

The first FLEX 10KE device, the 100,000-gate EPF10K100B device, is scheduled to be released in June 1998. This device is a process migration of the existing EPF10K100A device architecture and will provide higher performance and lower cost. For more information on the availability of EPF10K100B devices, contact Altera Applications at (800) 800-EPLD or your local sales representative.

The 50,000-gate EPF10K50E device will be introduced in the fourth quarter of 1998. Other FLEX 10KE devices are scheduled to be released in early 1999. Table 3 on page 9 shows FLEX 10KE device availability.

Table 2. FLEX 10KE Device Features

Features	EPF10K30E	EPF10K50E	EPF10K100E	EPF10K100B	EPF10K130E	EPF10K200E	EPF10K250E
Gates (logic & RAM)	30,000	50,000	100,000	100,000	130,000	200,000	250,000
Usable gates	22,000 to 119,000	36,000 to 199,000	62,000 to 257,000	62,000 to 158,000	82,000 to 342,000	123,000 to 513,000	149,000 to 474,000
Logic elements	1,728	2,880	4,992	4,992	6,656	9,984	12,160
EABs	6	10	12	12	16	24	20
Total RAM bits	24,576	40,960	49,152	24,576	65,536	98,304	81,920
Package Options	144-pin TQFP 208-pin PQFP 256-pin BGA 484-pin BGA	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin BGA 484-pin BGA	208-pin PQFP 240-pin PQFP 256-pin BGA 356-pin BGA 484-pin BGA	208-pin PQFP 240-pin PQFP 256-pin BGA	240-pin PQFP 484-pin BGA 672-pin BGA	240-pin RQFP 599-pin PGA 600-pin BGA 672-pin BGA	240-pin RQFP 599-pin PGA 672-pin BGA

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Devices & TOOLS

FLEX Update

FLEX 10K Devices Available in 600-Pin BGA Packages

Altera is now shipping EPF10K100A and EPF10K130V devices in 600-pin ball-grid array (BGA) packages. This package supports 400 or more I/O pins, which allows you to take advantage of FLEX® 10K performance and density for applications that require a high number of I/O pins. Contact your local Altera® sales representative or Altera Applications at (800) 800-EPLD for more information about these new package offerings.

EPF10K30A Devices Available

EPF10K30A devices provide ultra-high system performance (e.g., 126 MHz for an 8-bit, 16-tap FIR filter) that addresses design engineers' performance needs. EPF10K30A devices are available in 144-pin thin quad flat pack (TQFP), 208-pin plastic quad flat pack (PQFP), and 240-pin PQFP packages. Devices in 356-pin BGA packages are scheduled for release in July 1998.

0.25-µm EPF10K100B Device Available in June 1998

Initial shipments of EPF10K100B devices will be available in June 1998. Built on a 0.25-µm, 5-layer-metal process, EPF10K100B devices offer high performance at a low cost. With a 2.5-V core, EPF10K100B devices use less power than comparable 3.3-V field-programmable gate arrays (FPGAs). Additionally, the MultiVolt™ feature enables EPF10K100B devices to interface with 2.5-V, 3.3-V, or 5.0-V devices. EPF10K100B devices will be available in 240-pin PQFP, 208-pin PQFP, and 256-pin BGA packages.

More FLEX 6000 Devices Coming Soon

Altera plans to ship EPF6016A devices in June 1998 and EPF6010A devices in July 1998. Both devices are manufactured on a 0.35-µm, triple-layer-metal process and offer a 3.3-V supply voltage. The EPF6016A device offers 16,000 usable gates, and the EPF6010A device will offer 10,000 usable gates. For more details, contact your local sales representative or Altera Applications at (800) 800-EPLD.

FLEX 6000 Family Offers 3.3-V & 5.0-V Devices

Altera is now shipping 3.3-V EPF6024A and 5.0-V EPF6016 devices, which deliver higher performance at prices directly competitive with gate arrays. These FLEX 6000 devices combine fast time-to-market and flexibility with exceptionally low cost for high-volume applications. See Table 1.

Table 1. EPF6016 & EPF6024A Device Features

Feature	EPF6016	EPF6024A
Process geometry	0.5 µ	0.35 µ
Supply voltage	5.0 V	3.3 V
Pin migration	Yes	Yes
Gate count	8,000 to 16,000	12,000 to 24,000
Logic elements	1,320	1,960
User I/O pin (maximum)	204	218
Package options	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin BGA	144-pin TQFP 208-pin PQFP 240-pin PQFP 256-pin BGA

FLEX 6000 Device Availability

Table 2 shows FLEX 6000 device availability.

Table 2. FLEX 6000 Device Availability

Device	Availability	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin BGA
EPF6010A	July 1998	✓	✓			
EPF6016	Now		✓	✓	✓	✓
EPF6016A	June 1998	✓	✓	✓		
EPF6024A	Now		✓	✓	✓	✓

Configuration EPROM Update

Announcing the EPC2 Device

Altera plans to introduce the EPC2 device—Altera's first reprogrammable Configuration EPROM—in October 1998. A single EPC2 device will be able to configure any FLEX device up to 130,000 gates and will be programmable in-system using the IEEE Std. 1149.1 Joint Action Test Group (JTAG) boundary-scan test (BST) ports. Altera plans to offer the EPC2 device in 20-pin PLCC and 32-pin TQFP packages. The EPC2 device will be pin-compatible with all existing Altera Configuration EPROMs in the same package. The EPC2 will operate at 3.3 V or 5.0 V.

MAX Update

MAX 9000A Device Availability

With propagation delays as fast as 10 ns, MAX® 9000A devices offer a significant performance enhancement and cost reduction over existing MAX 9000 devices. Production quantities of high-performance EPM9320A and EPM9560A devices are available today. Table 1 summarizes MAX 9000A device availability.

Table 1. MAX 9000A Device Availability

Device	t_{PD} (ns)	Availability	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	356-Pin BGA
EPM9320A	10	Now	✓	✓		✓
EPM9560A	10	Now		✓	✓	✓

Industrial-Temperature MAX 9000A Devices Now Available

Altera now offers industrial-temperature -10 speed grade EPM9560 devices in 240-pin power quad flat pack (RQFP) packages. In addition, -10 speed grade EPM9560A devices in 208-pin RQFP packages, and EPM9320A devices in 84-pin PLCC and 208-pin PLCC packages, will be available in May 1998.

EPM7128A Devices Now Available

Based on Altera's industry-leading MAX architecture, EPM7128A devices support MultiVolt I/O pins, pin-compatibility with 5.0-V MAX 7000S devices, and propagation delays as fast as 5.0 ns. Altera currently offers -7 and -10 speed grade EPM7128A devices in 84-pin PLCC, 100-pin TQFP, and 144-pin TQFP packages.

In addition, Altera plans to ship EPM7256A devices in June 1998. The EPM7064A device will begin shipping in the third quarter of 1998. All three devices will be supported by MAX+PLUS II version 9.0.

MAX 7000S Device Availability

MAX 7000S devices are the fastest product-term-based PLDs, with speed grades as fast as 5 ns. These devices offer features such as ISP, IEEE Std. 1149.1 JTAG BST circuitry in devices with 128 or more macrocells, and an open-drain output option. Table 2 describes MAX 7000S package options, speed grades, and availability.

Table 2. MAX 7000S Device Availability

Device	Package	Speed Grade	Availability
EPM7032S	44-pin PLCC	-7, -10	Now
	44-pin TQFP	-7, -10	Now
EPM7064S	44-pin PLCC	-5, -6, -7, -10	Now
	44-pin TQFP	-5, -6, -7, -10	Now
	84-pin PLCC	-6, -7, -10	Now
	100-pin TQFP	-6, -7, -10	Now
EPM7128S	84-pin PLCC	-6, -7, -10, -15	Now
	100-pin TQFP	-6, -7, -10, -15	Now
	100-pin PQFP	-6, -7, -10, -15	Now
	160-pin PQFP	-6, -7, -10, -15	Now
EPM7160S	84-pin PLCC	-6, -7, -10	Now
	100-pin TQFP	-6, -7, -10	Now
	160-pin PQFP	-6, -7, -10	Now
EPM7192S	160-pin PQFP	-7, -10, -15	Now
EPM7256S	208-pin RQFP	-7, -10, -15	Now

MAX 7000 Product Transitions

Altera is migrating MAX 7000 devices from a 0.65-µm process to a 0.5-µm process. Table 3 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notification page on the Altera web site at **http://www.altera.com**.

Table 3. MAX 7000 Process Migration Schedule *Note (1)*

Device	Reference *Note (2)*	Date	Process
EPM7032	PCN9703 ADV9803	August 1998	0.5-µm
EPM7064 EPM7064S	PCN9703 ADV9708	Complete	0.5-µm
EPM7128E EPM7128S	PCN9703 ADV9708	Complete	0.5-µm
EPM7160E	PCN9703 ADV9803	October 1998	0.5-µm
EPM7192E EPM7192S	ADV9708 ADV9708	Complete	0.5-µm
EPM7256S EPM7256E	PCN9703 ADV9708	Complete	0.5-µm

Notes:
(1) This process transition will not result in any changes to data sheet parameters or ordering codes.
(2) Go to the Altera web site at **http://www.altera.com** for advisories and process change notices.

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Devices & Tools, continued from page 7

Tools Update

Network Licensing for PCs Available in July 1998

With the release of MAX+PLUS® II version 9.0 in July 1998, floating-node licenses will be available for both PC (ordering code: PLS-NET/PC) and UNIX platforms (ordering code: PLS-WS/*xx*). A floating-node license for PC platforms can be served from a UNIX or Windows NT-based license server. The license file utilizes either the UNIX server host ID or the network interface card (NIC) ID for Windows NT servers.

All floating-node design sites will have the list price of $6,995 per node. Additionally, software maintenance for both PC and UNIX floating-node licenses will be covered by a new maintenance product (ordering code: PLAESW-FLOAT, list price: $1,695 per node). Altera will also continue to sell fixed-node PC design sites that are based on MAX+PLUS II software guards (i.e., PLS-MAGNUM and PLS-BASE).

Altera will offer the new floating-node license for PCs at a special promotional price for customers with valid maintenance agreements on existing fixed-node design sites. This special promotional price of $1,495 per node will be available from July 1, 1998 to September 30, 1998. For more information on this promotion, ask your local Altera sales representative about the PLS-PROMO design site.

Version-Controlled Licensing for MAX+PLUS II Version 9.1

Starting with MAX+PLUS II version 9.1, Altera will introduce version-controlled licensing, which will require you to have a valid maintenance agreement to utilize the features of each new release. Altera will send a new license file to maintained customers before MAX+PLUS II version 9.1 is released. You will also be able to generate a license file via the Altera® web site at **http://www.altera.com**.

Discontinued Support for SunOS 4 Operating System

Beginning with MAX+PLUS II version 9.1, scheduled for release in October 1998, Altera will no longer provide MAX+PLUS II support for the SunOS 4.*x* operating system.

The SunOS 4 system has not been updated for several years, does not run on the new UltraSPARC machine, and cannot support MAX+PLUS II integrated features such as Verilog HDL synthesis and MegaWizard™ Plug-Ins. The UNIX operating systems that will be supported by MAX+PLUS II version 9.1 and higher are Solaris 2.5+, HP-UX 10.20+, and IBM AIX 4.1+.

How to Obtain MegaCore Functions

To provide you with the most up-to-date functions, you can now download Altera MegaCore™ functions via the Altera web site at **http://www.altera.com/html/products/megacore.html**. The Altera web site has the most up-to-date function files, and allows you to begin designing with Altera MegaCore functions immediately.

Because MegaCore functions can be downloaded from the web, Altera will stop distributing the functions on the ***MAX+PLUS II CD-ROM,*** starting with MAX+PLUS II version 8.3.

Authorization Codes for Microperipheral MegaCore Library

Altera now provides individual authorization codes for each of the seven MegaCore functions in the entire Microperipheral MegaCore Library (ordering code: PLSM-MICROLIB). The functions are:

- `a8237` Programmable DMA Controller
- `a8251` Programmable Communications Interface
- `a8255` Programmable Peripheral Interface Adapter
- `a8259` Programmable Interrupt Controller
- `a6402` Universal Asynchronous Receiver/Transmitter
- `a16450` Universal Asynchronous Receiver/Transmitter
- `a6850` Asynchronous Communications Interface Adapter

Previously, Altera provided a single authorization code for the entire library. You now have license these functions individually (list price: $1,995 each) or license the entire Micropheripheral MegaCore Library (list price: $7,995). If you purchased the Microperipheral MegaCore Library and do not have seven individual authorization codes, please contact Altera Customer Service at (800) SOS-EPLD.

This library of functions is available on the Altera web site at **http://www.altera.com/html/products/megacore.html.** You should always go to the web site to get the most current Microperipheral MegaCore library. Do not use the MegaCore files from old ***MAX+PLUS II Software*** CD-ROMs.

Altera Introduces ByteBlasterMV Download Cable

Altera introduces the ByteBlasterMV™ parallel port download cable (ordering code: PL-BYTEBLASTERMV),

which supports both 3.3-V and 5.0-V in-system programmability (ISP)-capable devices.

The ByteBlasterMV download cable can interface with a standard 25-pin PC parallel port, and uses the same 10-pin circuit board connector as the ByteBlaster™ and BitBlaster™ download cables. The download cable is fully compatible with existing circuit boards. The ByteBlasterMV download cable allows PC users to program MAX® 9000, MAX 7000S, and MAX 7000A devices in-system, and configure FLEX® 10K, FLEX 8000, and FLEX 6000 devices in-circuit via a standard parallel port.

For more information, refer to the *ByteBlasterMV Parallel Port Download Cable Data Sheet* on the Altera web site at **http://www.altera.com**, or contact your local Altera sales representative.

New PCI Target MegaCore Function

Altera introduces a new PCI target interface MegaCore function (ordering code: PLSM-PCIT1, list price: $4,995), which targets for FLEX 10K and FLEX 6000 devices. For more information about this MegaCore function, contact your local sales representative.

Discontinued Devices Update

Altera has announced that various products will be discontinued (see the table below). Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's world-wide web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (508) 462-9332 or go to their web site at **http://www.rocelec.com**.

Discontinued Device Ordering Codes

Device Family	Device	Last Order Date	Last Shipment Date	Reference
FLASHlogic	EPX880 and EPX8160 (all packages, temperature grades, and speed grades)	6/30/97	6/30/98	PDN9625
	EPFX740 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN9516

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MAX+PLUS II Software Support

Software support for FLEX 10KE devices will be included in the MAX+PLUS II software, version 9.0 in July 1998. For more details, contact Altera Applications at (800) 800-EPLD.

Conclusion

With enhanced features such as dual-port RAM, FineLine BGA packaging, and a 2.5-V core with MultiVolt I/O capability, FLEX 10KE devices provide increased performance and efficiency at low cost. For more information about FLEX 10KE devices, contact Altera Applications at (800) 800-EPLD or your local sales representative.

Table 3. FLEX 10KE Availability

Device	Availability
EPF10K30E	First Half of 1999
EPF10K50E	Q4 1998
EPF10K100E	First Half of 1999
EPF10K100B	June 1998
EPF10K130E	First Half of 1999
EPF10K200E	First Half of 1999
EPF10K250E	First Half of 1999

Technical ARTICLES

Selecting the Right UART Megafunction

The universal asynchronous receiver/transmitter (UART) is a key module for low-cost serial communication between the central processing units of a microprocessor or microcontroller. UART protocols can now be implemented in programmable logic devices (PLDs) and are available in the Altera® Microperipheral MegaCore™ Function library or from Altera Megafunction Partners Program (AMPP℠) partners.

About UARTs

The basic UART protocol consists of transmitting and receiving serial information through one data line and one status line in both directions. Each data packet contains various numbers of information bits, stop bits, and parity bits. UARTs are generally used with RS-232 hardware, which converts 5-V to –12-V signals and 0-V to +12-V signals, and vice versa.

Many UARTs have a processor interface which instructs the UART by filling registers with commands and settings. UARTs also have various buffer sizes for received data. When a character is received by a UART, it is transferred to the buffer and an interrupt is sent to the central processing unit (CPU), which reads the stored data and makes space for the next packet.

UART megafunctions are usually listed under different acronyms by chipset and microcontrollers to address different combination requirements. Some of these acronyms are:

- ACIA (Asynchronous Communications Interface Adapter)
- DAR (Dual Asynchronous Receiver Transmitter)
- DUART (Dual Universal Asynchronous Receiver Transmitter)
- MUART (Multifunction Universal Asynchronous Receiver Transmitter),
- SIO (Serial Input Output)
- USART (Universal Synchronous/Asynchronous Receiver/Transmitter)

The Musical Instrument Digital Interface (MIDI) and the Infrared Data Association (IrDa) communications interfaces can also incorporate UART functionality.

Benefits of UARTs in Programmable Logic

Implementing UART megafunctions in PLDs offers you several key benefits compared to an application-specific standard product (ASSP):

- Higher data rates
- Lower system cost
- Faster time-to-market

Higher Data Rates

From a performance standpoint, programmable logic offers the highest data rates. For example, CAST Inc., an AMPP partner, has a c16550 megafunction that allows you to easily achieve transmission rates of 1.5 Mbps. At the system level, a UART megafunction implemented in a PLD can reduce the number of instruction cycles for the system CPU, and therefore increases the overall performance.

Lower System Cost

A microcontroller typically has 3 or 4 different types of peripheral UARTs with set parameters. Few designs use the whole capability of these UARTs; however, many designs require specific features that are not included with the standard product. For example, your design may require an c16550 UART megafunction with a deep first-in first-out (FIFO) buffer, but no baud-rate generation.

If you are designing with a chipset solution, you must pay for an under-utilized baud rate feature and add memory for the FIFO buffer to your board, increasing your overall system cost. These additional production costs are eliminated when you implement a user-parameterizable UART megafunction in a PLD. By using reprogrammable UART megafunctions, you can easily make changes to your prototype design after implementation.

Faster Time-to-Market

Programmable logic is the most flexible solution when implementing UART megafunctions and greatly contributes to decreasing time-to-market. For example,

CAST Inc. offers a large number of UART megafunctions with standard protocols such as C16450, C16550, C6850, and C8251 megafunctions, as well as a user-customized C_UART megafunction. In addition, CAST also provides VHDL simulation test-bench with each UART megafunction to guarantee the protocol's functionality.

Key UART Megafunction Parameters

When starting a digital design that requires a UART megafunction, you must decide:

- How many UARTs does the system require?
- What is the bus type of the back end (Intel, Motorola, or other specific bus)?
- What are the baud rate generator requirements? Which frequency?
- What are the number of information bits per character?
- What are the number of stop bits?
- Which type of parity checking should be used?
- What is the direction of the UART function (transmitter, receiver, or both)?
- Does the UART require a fixed or programmable protocol?
- What is the FIFO buffer depth?

Checklist for Selecting the Right UART Megafunction

The following checklist will help you select the right UART megafunction for your design needs. Complete the information on this checklist and then contact Altera Applications at (800) 800-EPLD for further assistance.

Functionality Needed (check all that apply):
- ❑ 16450 function
- ❑ 16550 function
- ❑ 6402 function
- ❑ 6850 function
- ❑ 8251 function
- ❑ C_UART function
- ❑ MIDI function
- ❑ Other (specify): _____

Custom Core (check all that apply):
- ❑ Asynchronous
- ❑ Synchronous
- ❑ HDLC
- ❑ All

Protocol:
- ❑ Fixed
- ❑ Programmable

Number of Bits:
- ❑ 5
- ❑ 6
- ❑ 7
- ❑ 8
- ❑ Other (specify): _____

Number of STOP Bits:
- ❑ 1
- ❑ 2
- ❑ Other (specify): _____

Parity:
- ❑ Odd
- ❑ Even
- ❑ All
- ❑ No parity

FIFO Depth:
- ❑ Reception at _____ depth
- ❑ Transmission at _____ depth

Other Solutions

UART megafunctions are available from the Altera Microperipheral MegaCore library or from AMPP partners such as CAST, Inc. and Fastman, Inc. You can preview the megafunctions before licensing via the OpenCore™ feature available with the MAX+PLUS II software. This pre-purchase evaluation system allows you to instantiate and simulate the UART megafunctions but not generate programming files.

Conclusion

For more information about the UART megafunctions offered through these Altera programs, contact Altera Applications at (800) 800-EPLD or your local sales representative or go to the Altera web site at **http://www.altera.com**.

Next-Generation BGA Packaging

The 1.0-mm pitch plastic ball-grid array (BGA) package, called the FineLine BGA™ package, is Altera's latest innovative space-saving package. This package minimizes printed circuit board (PCB) size and meets the challenges of high-density programmable logic devices (PLDs). Currently, the 1.0-mm FineLine BGA package provides the most board space efficiency of any other package, requiring less than half the board space of conventional 1.27-mm BGA packages and even less board space when compared to conventional quad flat pack (QFP) packages.

Features

FineLine BGA packages have the following features:

- Pin count ranging from 100 to 672 leads
- Easy prototyping
- Compatible with solder reflow processes

Table 1 shows the planned FineLine BGA packages.

Packaging Efficiency

FineLine BGA packages offer more board space savings and higher lead density compared to conventional QFP and 1.27-mm BGA packages. Table 2 compares the packaging efficiency of the 1.0-mm FineLine BGA to plastic quad flat pack (PQFP), thin quad flat pack (TQFP), and 1.27-mm BGA packages.

As Table 2 shows, the 144-lead TQFP package uses almost the same amount of area as the 672-lead FineLine BGA package, while the 356-lead conventional BGA package requires almost twice the area of the 672-lead FineLine BGA package.

On average, the 1.0-mm FineLine BGA packages use less than half the board space of 1.27-mm BGA packages. In addition to lower package costs, the board space savings significantly minimizes manufacturing costs. See Figure 1.

Conclusion

With the 1.0-mm FineLine BGA package, Altera continues its cutting-edge leadership in providing more advanced and flexible packages. FLEX® 10KE, FLEX 10KA, FLEX 6000, and MAX® 7000A devices will be available in 1.0-mm FineLine BGA packages. These FineLine BGA packages also meet the specifications in the industry-standard *JEDEC Publication No. 95*. For detailed information on the FineLine BGA package, contact Altera Applications at (800) 800-EPLD or your local sales representative.

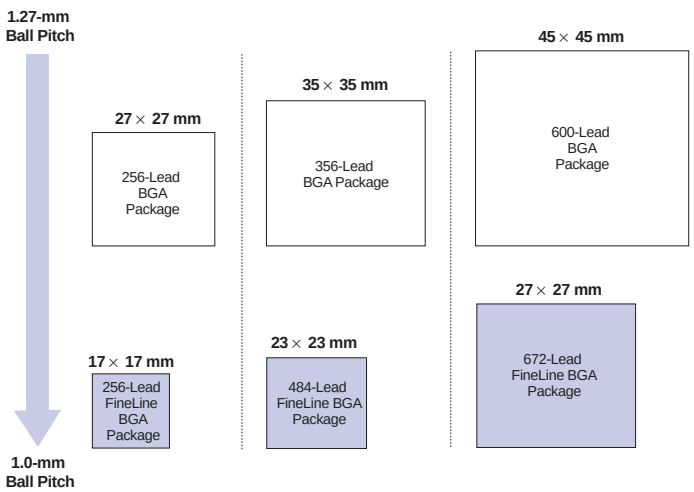
Table 1. FineLine BGA Package Types

Lead Count	Package Size (mm)
100	11 × 11
256	17 × 17
484	23 × 23
672	27 × 27

Table 2. Package Type Comparison

Package	TQFP	PQFP	1.27-mm BGA	FineLine BGA
Package Size (mm)	22 × 22	28 × 28	35 × 35	27 × 27
Board Area (in^2)	0.8	1.5	1.9	1.1
Lead Count	144	208	356	672
Lead Density (leads/in^2)	200	140	180	600

Figure 1. FineLine BGA vs. 1.27-mm BGA Package Comparisons



FIFO Solutions for FLEX Devices

Altera offers multiple first-in first-out (FIFO) buffer design solutions for FLEX® devices. A FIFO buffer is used to buffer data transferred from one subsystem to another in a design. For instance, FIFO buffers are used to hold data driving from multiple sources to a shared bus. When the bus is busy, data is stored in the FIFO buffer; when the bus is free, the FIFO buffer sends the data to the bus.

For most FIFO buffers, FLEX 10K embedded array blocks (EABs) provide high performance, large size, and no logic-vs.-memory tradeoffs. FIFO buffers implemented in logic elements (LEs) can also provide a good solution, depending upon your FIFO needs.

When using FIFO buffers, you must consider various system requirements. For example, you must consider whether a FIFO buffer needs to be read from and written to simultaneously. Some FIFO buffers require separate read and write clocks, while others have the same clock for reading and writing. Altera offers FIFO solutions to meet all these requirements.

Interleaved-Memory FIFO

The interleaved-memory FIFO buffer is well-suited for relatively deep buffers that have one read/write clock. For this FIFO buffer, two EABs are used for each 8 bits of width. You can implement a FIFO buffer of up to 512 words deep without using additional EABs.

Each EAB can be read or written on a given clock cycle. By using two EABs, you can implement simultaneous reads and writes. Data is pre-fetched from the non-written EAB, which prevents conflicts that occur during simultaneous reads and writes to the same EAB. This FIFO buffer can achieve 80-MHz performance in a FLEX 10KA device.

Cycle-Shared FIFO

The cycle-shared FIFO buffer is well-suited for designs that require many EABs in addition to the FIFO buffer, because it uses fewer EABs than the interleaved-memory FIFO buffer. This FIFO buffer has one read/write clock, and its EABs are time-domain multiplexed with a doubled clock. That is, an EAB is read and written on subsequent doubled clock cycles. For example, a cycle-shared FIFO buffer with 33-MHz throughput can be implemented with a 66-MHz clock and will achieve 40-MHz performance in a FLEX 10KA device.

Arbitrated FIFO

In some FIFO applications, simultaneous read and write is not required. For instance, an asynchronous transfer mode (ATM) design may have FIFO buffers where an entire 53-byte cell is read or written in one burst. The ATM design may have multiple FIFO buffers, where one port writes a cell to one FIFO buffer while another port reads a cell from a different FIFO buffer. An application that does not require simultaneous reads and writes can use an arbitrated FIFO buffer. An arbitrated FIFO buffer uses an EAB to store the buffered data. A parameter allows you to prioritize reading or writing. The arbitrated FIFO buffer uses one read/write clock, running over 80 MHz in a FLEX 10KA device.

Synchronous LE-Based FIFO

Sometimes more FIFO buffers are required than are available in the EABs of a target device. Alternatively, a FIFO buffer may be required in a FLEX 6000 design. In either case, a synchronous LE-based FIFO buffer provides a cost-effective solution; it creates shift registers to store data in the FIFO buffer. This FIFO buffer is ideal for multiple shallow, wide FIFO buffers with one read/write clock. The synchronous LE-based FIFO buffer is good for high-speed applications, and can achieve over 100-MHz performance.

Asynchronous LE-Based FIFO

For applications that require distinct read and write clocks, the asynchronous LE-based FIFO buffer offers an ideal solution. A FIFO buffer may buffer data coming from a 33-MHz PCI bus to a 50-MHz back end. These FIFO buffers are referred to as "asynchronous," "two-clock," or "bisynchronous." The asynchronous LE-based FIFO buffer is created by using a bank of registers to store data. The write counter is decoded to determine which registers to write to and a multiplexer is used to determine which registers to read.

A memory structure created from registers and multiplexers can be read and written simultaneously, because the reading multiplexer is independent of the write decoders. This structure can be written and read with different clocks. The FIFO buffer control circuitry prevents any metastable disturbances in the system.

continued on page 15

Design Tips

Altera Applications

Creating an Efficient State Machine

This article is the second of a four-part series that discusses practical design tips from Altera Applications. This article shows you how to create an efficient state machine when using VHDL. Upcoming issues of *News & Views* will feature the following topics:

- Using arithmetic operators in MAX+PLUS® II VHDL
- Importance of hierarchical instantiation

By using the design techniques discussed in this article, you will learn to distinguish between efficient and inefficient state machines, which can help you maximize your design's overall performance.

If you use inefficient state machines, your design may not achieve your performance requirements. To ensure that your design achieves the performance needed, Altera Applications recommends that you follow these state machine coding guidelines:

- Remove all arithmetic functions and data paths from the state machine.
- Only use state machine control logic inside If Statements.
- Do not use control variables or signals on the right-hand side of <= signal assignments, except for state assignments.

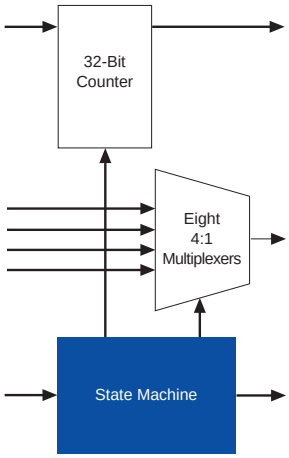
Figure 1 illustrates a state machine that directly controls a counter and eight 4:1 multiplexers.

The following MAX+PLUS II VHDL examples show two different ways to create the state machine shown in Figure 1. Example 1 shows an inefficient way to create this state machine, while Example 2 presents a more efficient method.

Example 1: Inefficient Coding Method

```
.
.
.
ELSIF (clk'EVENT AND clk = '1') THEN
     muxout <= muxa;
     CASE state IS
       WHEN s0 =>
```

Figure 1. Sample State Machine




```
    IF (sm_in(4) = '1' AND sm_in (2) =
    '1') THEN
           state <= s6;
           muxout <=  muxc;
           count <= count - '1';
        ELSIF (sm_in(1) = '1') THEN
           state <= s5;
           count <= count + '1';
        ELSE
           state <=  s2;
           muxout <= muxb;
        END IF;
      WHEN s1 =>
.
.
.
```

In Example 1, all multiplexer output signals are controlled within the If Statement, which can create extra logic for the multiplexer control signals. The counter is also incremented and decremented within the If Statement, which can cause two counters to be inferred.

Example 2: Efficient Coding Method

```
.
.
.
ELSIF (clk'EVENT AND clk = '1') THEN
     muxsel <= "00";
     count_en <= "0";
     count_ud <= "0"; – – "1" = count up,
     – – "0" = count down
     CASE state IS
      WHEN s0 =>
         IF (sm_in(4) = '1' AND sm_in
      (2) = '1') THEN
            state <= s6;
            muxsel <= "10";
            count_en <= "1";
         ELSIF (sm_in(1) = '1') THEN
            state <=  s5;
            count_en <= "1";
            count_ud <= "1";
            ELSE
               state <= s2;
               muxsel <= "01";
            END IF;
.
.
.
```

In contrast, Example 2 has control signals inside the If Statement, but the counter and multiplier are declared outside the If Statement. This style is more efficient because it allows the state machine to control only the counter and multiplexer, without creating extra logic. The counter and multiplexer are declared as separate structures, not inferred in the state machine. Separating the counter and multiplexer from the state machine gives more efficient results.

For more information on creating an efficient state machine, contact Altera Applications at (800) 800-EPLD.

Coming Soon: AMPP Catalog, Version 3

The ***AMPP Catalog*** version 3 will be available in June 1998 from Altera Literature Services. This catalog describes the Altera Megafunction Partners Program (AMPP), and includes megafunction descriptions and profiles of each AMPP℠ partner.

Contact Altera Literature Services at (888) 3-ALTERA or your Altera sales representative for a copy. The ***AMPP Catalog*** is also available on the Altera web site at **http://www.altera.com**.

FIFO Solutions for FLEX 10K Devices, continued from page 13

This FIFO buffer is ideal for applications with independent read and write clocks, and it can be combined with other FIFO buffers to create larger FIFO buffers with independent read and write clocks. It can achieve 60-MHz performance in a FLEX 10KA device.

Combination Functions

Altera also offers combination FIFO solutions for certain designs. For instance, a 256 × 16 asynchronous FIFO buffer can be built using a small asynchronous LE-based FIFO buffer with an EAB-based FIFO buffer. This type of FIFO buffer combines EAB size and performance to store data while using LEs to buffer clock rates.

The cycle-shared FIFO buffer is available in `csfifo` in provided in the MAX+PLUS II software. Other functions will be included in future MAX+PLUS II releases. All functions are parameterizable, so you simply need to set the parameters for your system requirements and create custom logic for your design.

Conclusion

FLEX devices, combined with FIFO functions, provide good solutions for designs with FIFO requirements. These solutions meet a wide variety of FIFO requirements and offer high performance and large size at low costs.

For more information on Altera FIFO buffer solutions, contact Altera Applications at (800) 800-EPLD or your local Field Applications Engineer.

Questions & ANSWERS

Q *Can I configure an EPF10K100B or any FLEX® 10KE device with a FLEX 10K or FLEX 10KA configuration file?*

A No, you cannot use a FLEX 10K or FLEX 10KA configuration file to configure EPF10K100B or FLEX 10KE devices, because these devices have different features. For example, the EPF10K100B device has a pin-by-pin switchable PCI clamp feature that is not available in EPF10K100A devices. Additionally, the FLEX 10KE device enhanced RAM structure differs from that of FLEX 10K or FLEX 10KA devices.

Q *How can I check for setup/hold time violation messages when performing a VITAL simulation on a MAX+PLUS® II VHDL output file?*

A By default, the VITAL simulator does not return setup/hold time violation messages when you are performing a VITAL simulation on a MAX+PLUS II output file. To show setup/hold time violation messages, perform the following steps:

1. Edit the VHDL/VITAL file **atl_vtl.vhd** (in **/usr/maxplus2/vhdl93/vital/v3_0** for UNIX workstations or <*drive letter*>**\maxplus2\vhdl93\vital\v3_0** for PCs) and change the Constant Definition to a True Statement so that it matches the following line:

   ```
   CONSTANT DefTimingMsgOn : BOOLEAN : = TRUE
   ```

2. Reanalyze the modified **alt_vtl.vhd** library file. The VITAL simulator now returns setup/hold violation messages.

Q *What is the maximum input leakage current for FLEX 10K or MAX® 7000A devices with a V_I up to 5.0 V?*

A Although the *FLEX 10K Embedded Programmable Logic Family Data Sheet* (***1998 Data Book***) states that the maximum input leakage current is 10 µA when $V_I = V_{CC}$ or GND, this specification is actually valid when V_I = GND up to the maximum recommended input voltage, which is 5.0 V.

Q *How can I use the MAX+PLUS II sequential group (or bus) naming feature to name an input or output pin?*

A The sequential group (or bus) naming feature can be used only to name an input pin or internal node, not an output pin. If you are using this feature to name an output pin, the MAX+PLUS II software will give the following error message:

"`Illegal assignment-- a[12..9], b[2..0] on pin` <*number*>"

For example, you can name an array of input pins as `a[12..9]`, `b[2..0]`.

To name output pins:

1. You must break the group into two output buses: `a[12..9]` on one output pin and `b[2..0]` on a separate output pin.

or

2. You must use a `WIRE` primitive to rename the bus with a single bus name of matching width: `c[7..0]`.

Q *How can I obtain in-system programmability (ISP) support for programming Altera® devices with embedded processors or in-circuit testers?*

A If you are using Altera ISP in an embedded processor or in-circuit tester environment, register to join the Altera ISP Support Program. With this program, Altera Application Engineers offer extensive support for your ISP implementations.

When you join the program, Altera will send you an authorization code via e-mail that enables Serial Vector Format (**.svf**) File and Jam™ Composer support in your MAX+PLUS II software. Altera recommends that you upgrade your MAX+PLUS II software to the latest version to ensure support for the SVF File and Jam Composer.

To inquire about the Altera ISP Support Program, send e-mail to **ispembed@altera.com** if you are using embedded processors, or to **ispate@altera.com** if you are using in-circuit testers.

Q *How do I perform in-system programming with "F" suffix MAX 7000 devices?*

A In-system programming can be performed with either an adaptive or constant algorithm. Because some in-circuit test (ICT) platforms have difficulties supporting an adaptive algorithm, Altera offers devices tested with a constant algorithm. MAX 7000 devices tested to the constant algorithm are marked with an "F" suffix in the ordering code.

MAX 7000 devices can also be programmed in systems that use adaptive algorithms, such as systems that use BitBlaster™ serial download cable, ByteBlaster™ parallel download cable, ByteBlasterMV™ parallel download cable, and embedded processors.

Q *What is the minimum bus transaction length for the* `a16450` *universal asynchronous receiver/transmitter (UART) MegaCore™ function?*

A The minimum bus transaction length for the `a16450` UART MegaCore function is a single-cycle read and write.

By default, the `a16450` MegaCore function uses the following settings:

- the `a[]` and `cs` input signals are registered
- the `dout[]` output signal is registered

If you use these default settings, the `a16450` MegaCore function uses two clock cycles to perform a read or write. In the first cycle, valid `a[]` and `cs` input signals need to be asserted to enable input registers. On the first clock edge, `a[]` and `cs` input signals are written into the registers. For a write in the second cycle, you must assert `wr` to write data to the second clock edge. For a read in the second cycle, you must assert `rd` for valid data to appear at the `dout[]` signal after the second clock edge.

If you change the parameters that control the registering of the input and output signals, you can eliminate the input registers on `a[]` and `cs` signals, and/or the output register on the `dout[]` signal. Eliminating these input and output registers allow you to perform single-cycle reads and writes.

Q *Where can I find information regarding moisture sensitivity and related handling recommendations for Altera devices?*

A There are three sources of information for moisture sensitivity and related handling recommendations for Altera devices:

- JEDEC moisture ratings for Altera devices can be found on the Altera Customer Notifications page on the Altera web site at **http://www.altera.com**.
- Drypack and handling guidelines are given in *Application Note 71 (Guidelines for Handling J-Lead & QFP Devices)*, which can be found in the ***1998 Data Book*** or on the Altera web site.
- Reflow recommendations for surface-mount devices are located in *Application Note 81 (Reflow Soldering Guidelines for Surface-Mount Devices)*, which can be found in the ***1998 Data Book*** or on the Altera web site.

Q *Do I have to use a special system power-up sequence when using FLEX 10KE (including EPF10K100B), FLEX 10KA (including EPF10K50V and EPF10K130V), or FLEX 6000 devices?*

A You do not have to use a special power-up sequence when using FLEX 10KE, FLEX 10KA, or 3.3-V FLEX 6000 devices. They can tolerate any power-up sequence.

The MultiVolt I/O interface allows a device to bridge between systems operating at different voltages. For example, 5.0-V input signals may drive a FLEX 10KE, FLEX 10KA, or a 3.3-V FLEX 6000 device before a 3.3-V V_{CC} is applied to the device, and you can drive signals into them before power-up.

Q *Why do I receive the following error message: "Initialization failed. Check licensing server name and port number in the license file?"*

A You may receive this network licensing error message when trying to run MAX+PLUS II PLS-WEB version 8.2. This error message occurs if you are using a network license file that was generated for PLS-WEB version 8.1. You can obtain a new license file to run PLS-WEB version 8.2 from the Altera web site at **http://www.altera.com**.

This error message can also occur if your **license.dat** file contains carriage returns. Make sure that the `feature` line is contained on one line with no carriage returns.

Q *Can I drive 5.0-V MAX device input pins before* V_{CCINT} *is powered up?*

A Altera does not recommend driving 5.0-V MAX device input signals before V_{CCINT} is powered up. Applying V_{CCINT} before driving the inputs correctly biases the device substrate. This process ensures that these input signals do not overshoot or undershoot the specified limit of acceptable logic levels, which also prevents the device from latching up.

Customer Application

NEC Creates the Simple Node Using Altera Devices

"The key issues were understanding customer needs and reflecting them in the product, and time to market," said Yusuke Nishimura.

With demands for faster and better communication, the volume of traffic on corporate and public networks is increasing rapidly. To cope with the demand, networking engineers are seeking to create a new type of network, one that can distinguish between voice and data signals and transmit them efficiently over existing systems of leased lines, ISDN lines, and public networks. A new system should also run on any future system. This was the challenge that motivated engineers at NEC Shizuoka, a design center of NEC Corporation, to design the Simple Node.

An Integrated Node with Hybrid Multiplexing

"One of the reasons we selected Altera devices is the quality of the design tool. The MAX+PLUS II software is very easy to use."

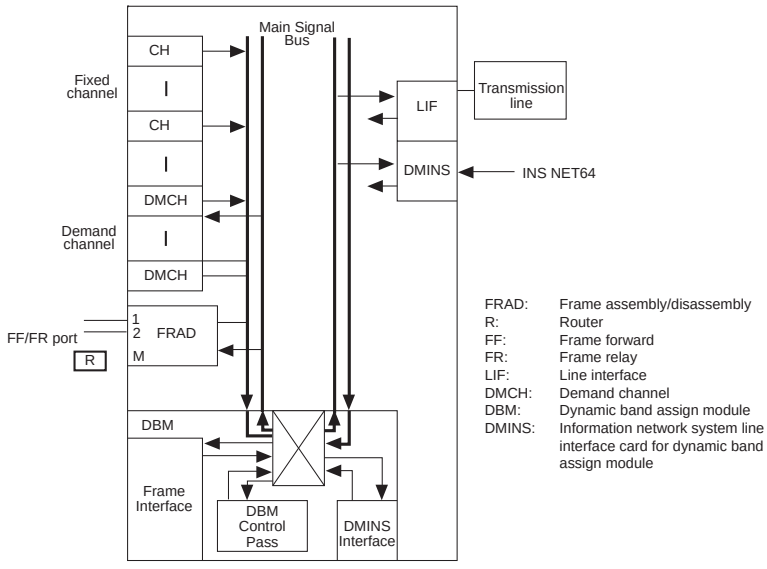
The Simple Node is an integrated node that uses hybrid multiplexing to combine the functions of a time-division multiplexer (TDM) with a private branch exchange (PBX). Hybrid multiplexing optimizes both the bandwidth and band-pass use of circuits so that voice and data signals with differing speeds and time delays are both transmitted efficiently, reducing communication costs.

The Simple Node processes low-speed, short-time-delay voice data signals, as well as low-speed, longer-time-delay host-terminal data signals and high-speed, burst inter-LAN data signals. It assigns optimum bandwidth and band-pass to these different types of signals, and outputs the data to the transmission line. With the Simple Node, circuit switching and time-division multiplexing is accomplished in one compact system.

The NEC designers used Altera® FLEX® 8000 and MAX® 7000 devices for the Simple Node boards. Their decision to use Altera devices was based on their desire to satisfy customer needs and to bring the product to market quickly. "The key issues were understanding customer needs and reflecting them in the product, and time-to-market," said Yusuke Nishimura, assistant manager of the transmission engineering department of NEC Shizuoka. The flexibility of Altera PLDs and the ease of use of the MAX+PLUS® II software allowed them to set the specifications and design the boards simultaneously, adding new features and modifying the designs as necessary. "One of the reasons we selected Altera devices is the quality of the design tool. The MAX+PLUS II software is very easy to use," said Yusuke Nishimura.

Figure 1 shows the Simple Node block diagram. The Dynamic Band Assign Module (DBM) is the product's innovative feature, where the hybrid multiplexing takes place. Figure 2 shows the DBM block diagram. The DBM controls bandwidth and assigns both fixed and variable band-pass. The DBM boards are shown in Figure 3 on page 20.

Figure 1. Simple Node Block Diagram



The Simple Node contains the following Altera devices:

- Two EPF8820AQC160-4 devices for the line interface (LIF) that connects the DBM and the frame relay.
- One EPM7160ELC84-15 device for the alarm that monitors the hardware and transmission interrupt and the frame-to-frame transfer.
- Two EPF8452AQC160-4 devices and six EPF8820AQC160-4 devices for the time slot assign that allots the signal to a board.
- Two EPM7128ELC84-10 devices for the DBM control pass that sets the control path through the band-assign modules.
- One EPF8452AQC160-4 device for the demand watchdog that monitors demand from the low-speed channel.

The Simple Node

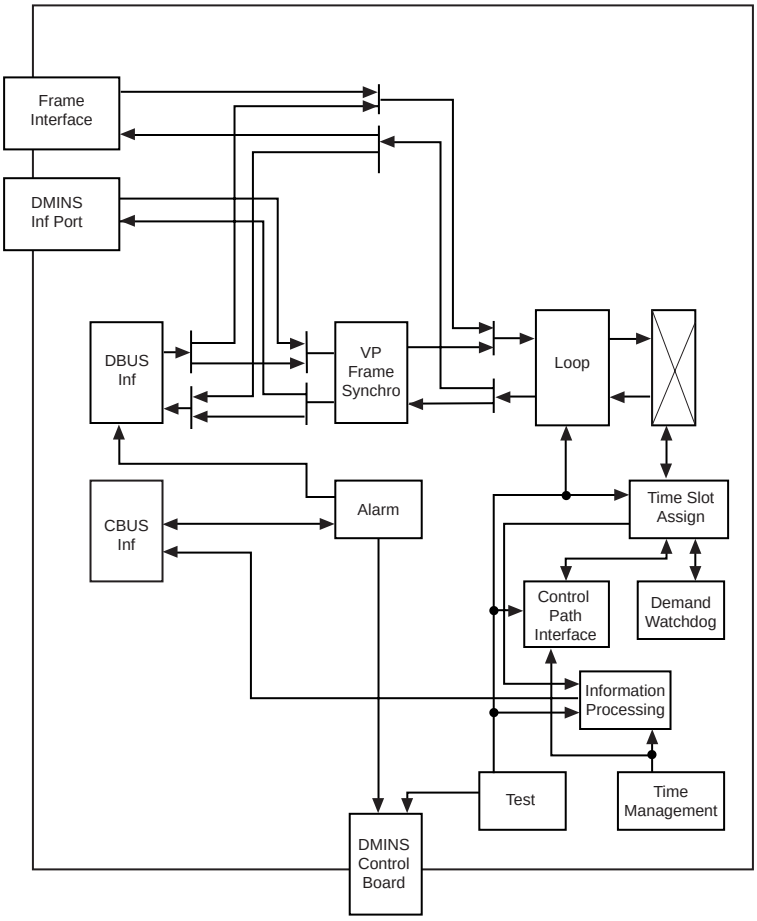
The Simple Node functions by the fixed channel interface and demand channel interface connecting to the DBM through the main signal bus. Low-speed, short-time-delay data are passed from the fixed channel interface to the DBM, which multiplexes the data as a fixed bandwidth (see Figure 4 on page 20) and outputs it on the transmission line through the Line Interface (LIF).
Connection calls carrying voice data are passed from the demand channel interface to the DBM. The DBM confirms the changes needed in bandwidth assignment, changes to the required bandwidth in the demand band-pass (see Figures 4 and 5 on page 20), and then outputs the data to the transmission line through the line interface using high-quality voice compression that complies with ITU-T G.728/G729.

Low-speed, longer-time-delay data signals and high-speed, burst data signals are passed from the Frame Forward/Frame Relay port to the Frame Assembly/Disassembly (FRAD), which performs logic multiplexing on them. The data from the FRAD is output to the time-division multiplexer (TDM), which multiplexes the data as a frame relay bandwidth (see Figures 4 and 5) and outputs it through the line interface to the transmission line. In networks based on traditional TDMs, the bandwidth is fixed and therefore is occupied even when it is not being used. The bandwidth sharing for the frame relay band-pass and the demand band-pass provided by the FRAD allows bandwidth flexibility and improves circuit efficiency.

continued on page 20

Contact Information:
NEC Corporation
Corp. Communications
System Division
33-7 Tokuei Bldg.
5 Chome
Shiba Minato-ku, Tokyo
Japan
Phone: (81) 3 3340 9480

Figure 2. Dynamic Band Assign Module Block Diagram



Customer Application, continued from page 19

Figure 3. Three PCBs Comprising the DBM

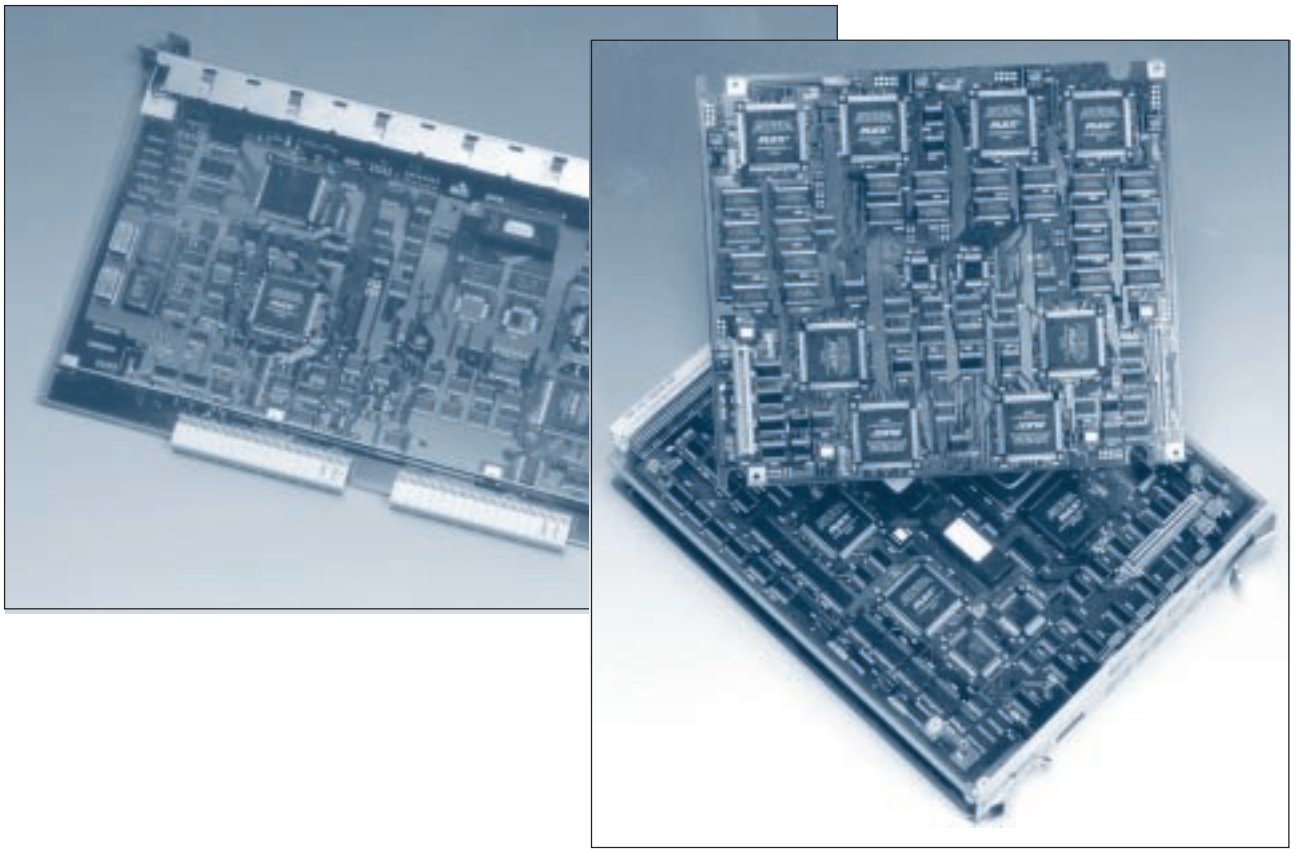


Figure 4. Transmission Band for Dynamic Variable Bandwidth

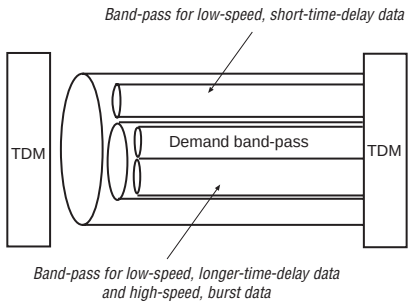
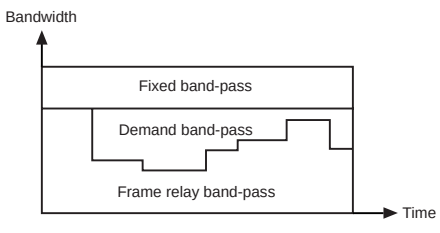


Figure 5. Band-Pass Assignment



Conclusion

With Altera devices and the MAX+PLUS II software, NEC transmission engineers were in full control of the design schedule for the Simple Node integrated node. They were able to incorporate changes into the specifications, integrate new features into the design, and still bring this innovative product to market on time.

Benchmarks for Measuring Design Performance

When selecting programmable logic devices (PLDs), most designers compare density, price, and performance to decide which devices meet their design requirements. Designers can generally compare density and price by looking at a price list or contacting a sales representative. Comparing performance, however, is a more challenging process. To determine performance, you must consider numerous factors such as signal routing, logic complexity, type of memory interface, and fan-out. With so many factors involved in determining performance, it is difficult to predict performance accurately.

To develop general guidelines for selecting PLDs and determining design performance, Altera® Applications recently completed multiple experiments that use several independent benchmarks. By evaluating the results from these experiments, you can estimate a design's performance before implementation. Likewise, it will allow you to compare performance in Altera devices with other manufacturers' PLDs under identical conditions. This article summarizes the five main benchmarks to be used in upcoming experiments.

Typical Applications

The typical applications benchmark measures design performance using large designs that are commonly found in high-density applications such as bus interface, digital signal processing (DSP) functions, and control circuitry. All designs used for this benchmark were created in VHDL or Verilog HDL by independent consultants and compiled with timing-driven compilation. Because no manual optimization design techniques were used in this benchmark, the results show the worst-case performance for designs of similar type.

Logic & Routing Analysis

The logic and routing analysis benchmark analyzes routing and logic utilization by using varying routing distances and logic complexities to determine performance. Although this benchmark is not as effective in predicting real design performance of a particular design, it is helpful in determining the performance differences between different PLD architectures.

Pre-Optimized Functions

The optimized functions benchmark measures design performance using large, pre-optimized functions that were chosen because they are commonly implemented in PLDs. The following functions were used:

- Finite impulse response (FIR) filter (8-bit 16-tap)
- 16 × 16 multiplier
- Master/target peripheral component interconnect (PCI) function
- Viterbi decoder

Because these designs were pre-optimized by each PLD vendor, the results eliminate performance variability associated with design methodology and design tool efficiency. Consequently, the benchmark results are an excellent tool for comparing the silicon performance of comparable PLDs from different vendors. Additionally, these benchmarks show the best-case performance for designs of similar structure and size in the devices analyzed.

Memory

The memory benchmark measures design performances of RAM implemented in PLDs. Different RAM sizes (i.e., width and depth) and structures (i.e., single port and dual port) were tested. This benchmark measured the maximum interface performance to the RAM.

I/O Performance

The I/O performance benchmark analyzes input setup and hold times, and output clock-to-output times. This benchmark is important in determining whether a device will meet critical system design parameters.

Conclusion

In order to help designers with the system performance estimation process, Altera will present the results through a series of technical documents that can be downloaded from the Altera web site at **http://www.altera.com**. For more information about benchmarks for measuring design performance, contact Altera Applications at (800) 800-EPLD.

FLEX 6000 Devices Compete Sucessfully with ASICs

FLEX® 6000 devices combine the traditional programmable logic device (PLD) benefits of fast time-to-market and flexibility with exceptionally low cost for high-volume applications. Since FLEX 6000 devices were introduced in June 1997, these devices have successfully been used as logical alternatives to application-specific integrated circuits (ASICs).

Cornet, Inc. is one such company that has switched successfully to FLEX 6000 devices. Cornet is a high-speed switch manufacturing leader, providing solutions for air traffic control systems, data centers, LAN/WAN management, and applications requiring high-speed data handling.

FLEX 6000 Devices Used for Prototyping

Before FLEX 6000 devices were introduced, Cornet used PLDs for prototyping and ASICs for high-volume production.

With the help of a local distributor, Wyle Electronics, Inc., Cornet started using FLEX 6000 devices for their new switch product and several corresponding special function cards. Cornet also used a FLEX 6000 device to upgrade the functionality of their older switch products, allowing existing customers to add features as their needs grow.

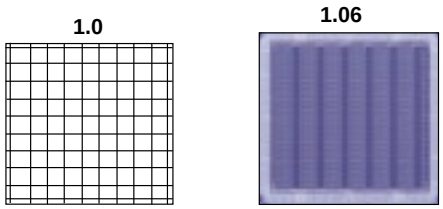
FLEX 6000 Devices Provide Flexibility

Because FLEX 6000 devices are reprogrammable, they provide more flexibility than ASICs. According to Jim Crews, a Cornet Sr. Engineer, "The EPF6016 device met our design criteria so well, we were able to design the EPF6016TC144-3 device into 10 different boards on one of our port switches. If we had used an ASIC, we would have had 10 different devices; but with Altera, we only needed to purchase one and we got the added benefit of reprogrammability."

Cost-Competitive FLEX 6000 Devices

Cornet quickly discovered that by using cost-competitive FLEX 6000 devices for production, they could still reduce usage cost during prototyping and obtain the added benefits of fast time-to-market and flexibility during high-volume production. FLEX 6000 devices are cost-competitive with gate arrays because their die sizes are similar. See Figure 1.

Figure 1. Relative Die Size Comparison



Although Cornet was satisfied with using ASICs for high-volume production, they decided to switch to FLEX 6000 devices because they were directly cost competitive with ASICs. Even though their ASIC vendor quotes very aggressive prices for ASICs, Cornet still considered FLEX 6000 devices the more logical solution.

As Nat Kumar, the president of Cornet, stated, "I appreciate the benefits of reprogrammability but I need to keep my costs low. I gave [Altera] a very aggressive price comparable to that of an ASIC. To my surprise, they came back and met my price!" Altera was able to offer a low-cost solution with the added benefits of reprogrammability.

Cornet plans to purchase thousands of FLEX 6000 devices over the next several months. Annual usage will increase over the next few years as Cornet expands product offerings and redesigns older products. This type of response confirms that the FLEX 6000 family is a viable alterative to ASICs for high-volume production.

Conclusion

Because FLEX 6000 devices offer comparable cost and density to ASICs plus the benefits of reprogrammability, they are being used for both prototyping and high-volume production. FLEX 6000 devices continue to be the ideal reprogrammable alternative to ASICs.

For more details about Cornet, Inc. and their high-speed switching solutions, go to the Cornet web site at **http://www.cornet.com**. For more information on FLEX 6000 devices, contact Altera Applications at (800) 800-EPLD or go to the Altera web site at **http://www.altera.com**.

New Jam Language Hardware Support

A growing number of programming hardware vendors support the Jam™ Programming and Test Language, an industry-standard interpreted language. The Jam language is vendor- and platform-independent and is optimized for in-system programmability (ISP)-capable devices via the IEEE Std. 1149.1 (JTAG) interface.

The most recent vendors to announce Jam language hardware support are Hi-Lo System Research (also known as Tribal Microsystems in the United States) and Xeltek Corporation. This article describes each vendor's universal programmer and support for the Jam language.

Hi-Lo System Research: ALL-11 Universal Programmer

The ALL-11 universal programmer is the sixth-generation universal programmer product from Hi-Lo System Research. The ALL-11 programmer supports over 39 Altera® MAX® 9000A and MAX 7000S devices. The programmer consists of a universal base and exchangeable pack options. These packs range from general purpose to multiple sockets for multi-device programming.

The ALL-11 programmer offers the following features:

- Supports Jam Files (**.jam**) created by the MAX+PLUS® II software
- Supports devices instantly as they become available from programmable logic device (PLD) manufacturers
- Supports 8- to 300-pin devices
- Pin drivers are fully programmable
- High-speed CPU and expandable memory buffer (from 1 Mbit to 128 Mbytes)
- High-speed serial port interface (up to 115 kbyte baud)
- USB port interface (optional)
- Windows 95 or MS-DOS user interface
- Free software updates via bulletin board service (BBS) and the web site

Xeltek Corporation: Superpro III Universal Programmer

Xeltek recently introduced the Superpro III universal programmer, a low-cost programmer that supports more than 4,000 devices. The Superpro III offers the following features:

- Supports Jam Files created by the MAX+PLUS II software
- Supports devices instantly as they become available from PLD manufacturers
- 48 universal pin drivers
- Dual-range switching power supply adapter (90 V/240 V)
- Optional 100-pin expansion module
- Optional universal socket or multi-device adapters for various device packages
- Printer port interface
- Windows 95 or MS-DOS user interface
- Parallel port
- Large variety of socket adapters available for most device packages

Table 1 shows Altera ISP-capable devices that are currently supported by the Superpro III programmer.

Table 1. ISP-Capable Devices Supported by Superpro III

Family	Device
MAX 9000	EPM9400 EPM9320
MAX 7000S	EPM7032S EPM7160S EPM7128S EPM7256S EPM7064S

Conclusion

In addition to full support for Altera devices, the ALL-11 and Superpro III programmers support vendors' devices that can be programmed with Jam Files.

For more information on hardware support for the Jam language from Hi-Lo, Xeltek, or other third-party programmer vendors, go to the Jam web site at **http://www.jamisp.com**.

EDA Tools Supported through the ACCESS Program

The Altera® Commitment to Cooperative Engineering Solutions (ACCESS℠) program is an alliance between Altera and EDA vendors that provides direct support for Altera programmable logic devices (PLDs) or integration with Altera's MAX+PLUS® II development software.

In an ongoing effort to simplify a seamlesss design flow between the MAX+PLUS II software and other EDA tools, Altera has developed the MAX+PLUS II ACCESS Key Guidelines, which provide complete instructions on how to create, compile, and simulate your design with tools from leading EDA vendors such as Cadence, Exemplar Logic, Mentor Graphics, Synplicity, Synopsys, and Viewlogic, and the MAX+PLUS II software. The guidelines can be found at:

- Altera web site at **http://www.altera.com**
- ***MAX+PLUS II CD-ROM*** (version 8.2 and higher)

The guidelines are organized by vendor, tool, and functionality to make it easy for you to find the information you need quickly. The MAX+PLUS II ACCESS Key Guidelines are part of Altera's ongoing plan to give designers state-of-the-art tools that enhance productivity for even the highest-density devices.

In addition to the guidelines, Altera recently introduced the first of several new technical briefs that demonstrate the ease with which designers can interface their existing tools with the MAX+PLUS II software. These technical briefs provide steps for setting up the EDA environment and generating the necessary files for a simple design to target Altera devices. Available EDA technical briefs include:

- *Technical Brief 39 (Using the Synopsys Design Compiler & FPGA Compiler to Synthesize Designs for MAX+PLUS II Software)*
- *Technical Brief 42 (Using the Synopsys FPGA Express Software to Synthesize Designs for MAX+PLUS II Software)*
- *Technical Brief 44 (Using the Synplicity Synplify Software to Synthesize Designs for MAX+PLUS II Software)*
- *Technical Brief 45 (Importing Synthesized Files from the EDA Software into the MAX+PLUS II Software)*

You can obtain these documents from the following sources:

- Altera Literature Services at (888) 3-ALTERA
- Altera web site at **http://www.altera.com**
- Your local Altera sales representative

New Altera European Technical Center

On March 16, 1998, Altera announced the establishment of its first European Technical Center. The role of the center is to:

- Provide locally based technical support to Altera® European hardware and software customers
- Execute research and development activities focused on device design and the development of MegaCore™ megafunctions and MegaWizard™ Plug-Ins

The European Technical Center will be housed in Altera's current facility outside of London, and is already equipped with WAN and videoconferencing, enabling the staff to stay in constant contact with Altera personnel worldwide. The center will employ as many as 50 engineers in the next two years.

The addition of a research and development center in the United Kingdom to existing research and development operations in Penang, Malaysia, and Altera headquarters in San Jose, California, advances Altera's fulfillment to ongoing research and development worldwide.

For more information about the new Altera European Technical Center, go to the Altera web site at **http://www.altera.com**.

New AMPP Megafunctions

For your digital signal processing (DSP), telecommunications, and bus interface design needs, Altera has introduced three new Altera Megafunction Partners Program (AMPP) partners and several new megafunctions. These megafunctions, targeted for specific Altera device architectures, allow you to focus on proprietary sections of your overall design. All megafunctions are optimized by the AMPP partner and then verified by Altera.

You can evaluate the megafunctions prior to purchasing a license by using the OpenCore™ evaluation feature of the Altera MAX+PLUS® II software. The OpenCore feature allows you to compile the megafunctions and determine the megafunction's size and speed. To generate programming files, you must license the function.

HammerCores

HammerCores, a new AMPP partner, currently offers the following high-performance, user-parameterizable megafunctions for DSP applications:

- Reed-Solomon Encoder/Decoder
- Cordic Cordpol Function
- Ultra-Fast Reed-Solomon Coder
- LMS and Zero-Forcing Equalizers
- Embedded Processor FlexCore

All HammerCores megafunctions are available for OpenCore evaluation on the HammerCores web site at **http://www.hammercores.com**.

Simple Silicon

Simple Silicon provides leading-edge digital connectivity solutions for networking, consumer electronics, computing, audio, video, and mass storage devices. Simple Silicon provides proven expertise in IEEE Std. 1394 physical and link layer controllers, and offers the following megafunctions:

- Si-Link: IEEE Std. 1394 Link Layer Controller
- Si-Phy: IEEE Std. 1394 Physical Layer Controller
- Si-Hub: USB Hub Controller
- Si-Function: USB Function Controller
- Si-Enable USB-86: USB Host Controller

All functional emulation and verification of Simple Silicon megafunctions is performed using Altera FLEX® 10K devices. For pricing and information on prototyping boards, contact Simple Silicon directly at:

Simple Silicon, Inc.
10430 South De Anza Blvd, Suite 195
Cupertino, CA 95014. USA
Phone: (408) 873-2260
Fax: (408) 873-2261
E-mail: **info@simplesi.com**
http://www.simplesi.com

NComm, Inc.

NComm, Inc. enters the AMPP program with 15 years of experience in designing programmable logic for telecommunications applications. NComm has already implemented Altera MegaWizard™ Plug-Ins, and has developed a parameterized tone generation megafunction called ToneGen.

An encrypted evaluation copy of the ToneGen megafunction, enabled by the OpenCore feature, is available by contacting NComm at:

NComm, Inc.
401 Main Street, Suite 204
Salem, NH 03079
Telephone: (603) 893-6186
Fax: (603) 893-6534
E-mail: **info@ncomm.com**
http://www.ncomm.com

Conclusion

Up-to-date information on the AMPP program, including partner profiles and megafunction descriptions, are available in the new ***AMPP Catalog*** version 3 or on Altera's web site at **http://www.altera.com**.

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on Altera's world-wide web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- ***AMPP Catalog*** (A-CAT-AMPP-03)
- *FLEX 10KE Embedded Programmable Logic Family Data Sheet* (A-DS-F10KE-01)
- *FLEX 10K Embedded Programmable Logic Family Data Sheet Supplement* (A-DSS-F10K-03.1)
- *ByteBlasterMV Parallel Port Download Cable Data Sheet* (A-DS-BYTBLMV-01)
- *Technical Brief 39: Using the Synopsys Design Compiler & FPGA Compiler to Synthesize Designs for MAX+PLUS II Software (M-TB-039-01)*
- *Technical Brief 40: Advantages of MAX+PLUS II Fitting* (M-TB-040-01)
- *Technical Brief 41: Power Measurements: FLEX 10KA vs. XC4000 Devices* (M-TB-041-01)
- *Technical Brief 42: Using the Synopsys FPGA Express Software to Synthesize Designs for MAX+PLUS II Software (M-TB-042-01)*
- *Technical Brief 44: Using the Synplicity Synplify Software to Synthesize Designs for MAX+PLUS II Software (M-TB-044-01)*
- *Technical Brief 45: Importing Synthesized Files from the EDA Software into the MAX+PLUS II Software (M-TB-045-01)*

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for selected Altera devices. Algorithms are supplied via Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Microsystems' BBS. Programming support for Configuration EPROM, MAX® 9000A, and MAX 7000 devices is shown in the table below. All information is subject to change.

Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPC1441	✓	✓
EPM7032	✓	✓
EPM7032S	✓, *(3)*	✓, *(3)*
EPM7064	✓	✓
EPM7064S	✓	✓
EPM7096	✓	✓
EPM7128E	✓	✓
EPM7128S	✓	✓
EPM7128A	✓, *(3)*	✓, *(3)*
EPM7160E	✓	✓
EPM7192E	✓	✓
EPM7192S	✓	✓
EPM7256E	✓	✓
EPM7256S	✓	✓
EPM9320	✓	✓
EPM9320A	✓	✓
EPM9400	✓	✓
EPM9480	✓	✓
EPM9560	✓	✓
EPM9560A	✓	✓

Notes:

(1) These devices are supported by Data I/O 3900 version 5.7 and UniSite version 5.7 programmers.

(2) These devices are supported by BP Microsystems programmers version 3.31.

(3) This device will be supported by Data I/O 3900 version 5.8 and BP Microsystems programmers version 3.36 in July 1998. Earlier programming support may be available sooner than the scheduled release date.

Current Software Version

The latest version of Altera software product are shown below:

- MAX+PLUS® II version 8.3 (PC, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 platforms)

Programming Hardware Support

Table 1 contains the latest programming hardware information for Altera devices. For correct programming, use the software version shown in "Current Software Version" on page 26.

Table 1. Altera Programming Adapters (Part 1 of 2) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)*, EPC1064V *(2)*, EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)*, EPC1213, *(2)*	DIP J-lead	PLMJ1213 PLMJ1213
EPM9320A	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9320-84 PLMR9000-208NC *(4)* PLMR9000-240NC *(4)*
EPM9320	PGA J-lead (84-pin) RQFP (208-pin)	PLMG9000-280 PLMJ9320-84 PLMR9000-208
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(4)* PLMR9000-240NC *(4)*
EPM9560	PGA (280-pin) RQFP (208-pin) RQFP (240-pin) RQFP (304-pin)	PLMG9000-280 PLMR9000-208 PLMR9000-240 PLMR9000-304
EPM7032S	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7032, EPM7032V	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7064S	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC *(4)*
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-4 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) TQFP (144-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(4)* PLMT7000-100NC *(4)* PLMT 7000-144NC PLMQ7128/160-160NC
EPM7128A	J-lead (84-pin) TQFP (100-pin) TQFP (144-pin)	PLMJ7000-84 PLMT7000-100NC *(4)* PLMT 7000-144NC

Table 1. Altera Programming Adapters (Part 2 of 2) *Note (1)*

Device	Package	Adapter
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(4)* PLMQ7128/7160-160NC *(4)*
EPM7160E	J-lead PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7192S *(4)*	PQFP (160-pin)	PLMQ7192/256-160NC
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7256S *(4)*	RQFP (208-pin)	PLMQ7256-208NC
EPM7256E	PQFP (160-pin) PGA (192-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208
EPM7256A	PQFP (208-pin) TQFP (144-pin)	PLMR7256-208 PLMT7000-144NC

Notes:
(1) Refer to the Altera ***1998 Data Book*** for device adapter information on MAX 5000 and Classic devices. Altera offers an adapter exchange program for 0.8-micron EPM5032, EPM5064, and EPM5130 programming adapters.
(2) FLEX 8000 Configuration EPROM.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 Configuration EPROM.
(4) These devices are not shipped in carriers.

Table 2 shows provides programming and configuration compatibility information for the BitBlaster™ serial port, ByteBlaster™ parallel port, and the ByteBlasterMV™ parallel port download cables.

Table 2. BitBlaster & ByteBlaster Cable Compatibility

Device	BitBlaster	ByteBlaster	ByteBlasterMV
FLEX 10K	✓	✓	✓
FLEX 10KA	✓	✓	✓
FLEX 10KE			✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A			✓

Altera Device Selection Guide

All current information for the Altera FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, and MAX 7000 devices is listed here. Information on other Altera devices is located in the Altera ***1998 Data Book***. For the most up-to-date information about Altera products, go to the Altera web site at **http://www.altera.com**. Contact Altera or your local sales office for current product availability.

FLEX 10K Devices

DEVICE[1]	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	66[2], 102, 134, 150[2]	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin PQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191[2], 246, 246[2]	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-pin BGA[1], 484-pin BGA[1]	102, 147, 176[2], 220[2]	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1]	189, 274, 310[2]	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 189, 191[2], 256[2]	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-pin BGA	189, 274, 371[2], 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	147, 189, 191[2]	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 484-pin BGA[1]	147, 189, 191[2], 340[2]	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 484-Pin BGA[1], 672-Pin BGA[1]	186, 371[2], 426[2]	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	240-Pin RQFP, 599-Pin PGA, 672-pin BGA[1]	182, 470, 470[2]	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960
EPF10K250E	250,000	240-Pin RQFP, 599-Pin PGA, 672-Pin BGA[1]	179, 470, 470[2]	2.5 V	-1, -2, -3	12,160	81,920

Notes:
(1) This package is the space-saving FineLine BGA package.
(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	5.0 V	-2, -3, -4	282	208
EPF8282AV	2,500	100-Pin TQFP	78	3.3 V	-3, -4	282	208
EPF8452A	4,000	160-Pin PQFP	120	5.0 V	-2	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	5.0 V	-3, -4	452	336
EPF8636A	6,000	208-Pin PQFP	136	5.0 V	-2	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	5.0 V	-3, -4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	112, 120, 152	5.0 V	-2	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	5.0 V	-3, -4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	5.0 V	-2, -3, -4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	5.0 V	-2, -3, -4	1,500	1,296

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	81, 117	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 117, 171, 218[2]	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218[2]	3.3 V	-1, -2, -3	1,960	1,960

Notes:
(1) This package is the space-saving FineLine BGA package.
(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10, -15
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480A	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-10, -15
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10, -15
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032A	32	44-Pin PLCC/TQFP	36	3.3 V	-5, -7, -10
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-6, -7, -10
EPM7032	32	44-Pin PLCC/TQFP/PQFP	36	5.0 V	-6, -7, -10, -12, -15
EPM7032V	32	44-Pin PLCC/TQFP	36	3.3 V	-12, -15, -20
EPM7064A	64	44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin BGA[1]	38, 68, 68	3.3 V	-5, -7, -10
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin PQFP/TQFP	36, 52, 68	5.0 V	-5, -6, -7, -10
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	5.0 V	-6, -7, -10, -12, -15
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	5.0 V	-7, -10, -12, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-5, -6, -7, -10
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-7, -10, -12, -15, -20
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 104	5.0 V	-10, -12, -15, -20
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7192E	192	160-Pin PQFP/PGA	124	5.0 V	-12, -15, -20
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 164, 164	3.3 V	-6, -7, -10
EPM7256S	256	208-Pin RQFP/PQFP	132, 164	5.0 V	-7, -10, -15
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	5.0 V	-12, -15, -20
EPM7384A	384	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -15
EPM7512A	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -15
EPM71024A	1,024	208-Pin PQFP, 256-Pin BGA[1]	176, 212	3.3 V	-7, -10, -15

Note:
(1) This package is a space-saving FineLine BGA package.

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Notes:
(1) The ***MAX+PLUS II Getting Started*** Manual is available from the Altera web site. To obtain other MAX+PLUS II software manuals, contact Altera Customer Service or your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

New Toll-Free Number for Renewing Software Maintenance

Software maintenance ensures that you always receive the most up-to-date version of the MAX+PLUS II software. You should renew your software maintenance each year to continue to get the latest software. When your maintenance is about to expire, Altera will mail you a notification with a renewal quote.

To make it easier for you to renew your software maintenance agreement, Altera now has a dedicated support line for North American customers. To renew your maintenance, simply call (888) 800-0631; this number is highlighted on all maintenance quotes for North American customers. Customers outside North America should continue to work with their existing sales representative.

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