The Altera Advantage News & Views

Newsletter for Altera Customers ◆ Third Quarter ◆ August 1998

Raphael: Embedded PLD Family for System-Level Integration

The new Raphael™ programmable logic device (PLD) family, based on the revolutionary MultiCore™ architecture, meets system-level design challenges by offering complete system integration on a single device.

Ranging from 100,000 to over 1 million gates and manufactured using a 6-layer-metal process, the 0.25-µm, 2.5-V Raphael devices will extend Altera's leadership in embedded architectures to new levels of efficiency and performance. Raphael devices give designers the ultimate in design flexibility so they can efficiently address much larger designs in a broader range of applications.

System-Level Features

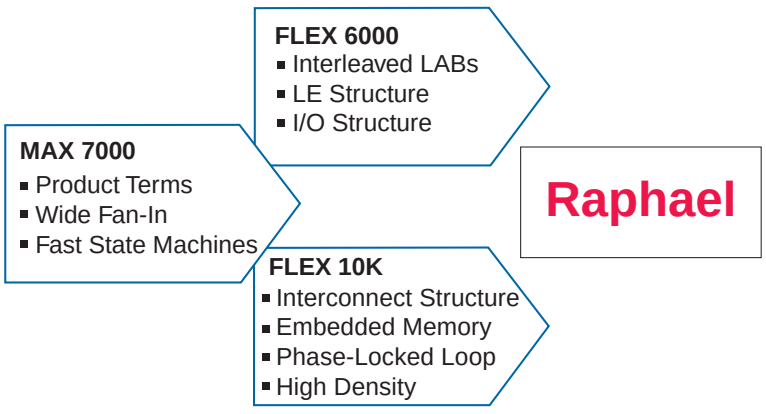
Raphael devices contain powerful system-level features that offer design flexibility and high-performance system-on-a-chip functionality, including:

- MultiCore embedded architecture with embedded product terms, high-speed dual-port RAM, and content-addressable memory (CAM)
- Enhanced 4-level FastTrack Interconnect™ routing structure, which features the new MegaLAB™ interconnect
- Support for existing and emerging I/O standards including low-voltage transistor-to-transistor logic (LVTTL), low-voltage complementary metal-oxide semiconductor (LVCMOS), stub-series terminated logic (SSTL-3), Gunning transceiver logic (GTL/GTL+), and low-voltage differential signaling (LVDS)
- Enhanced phase-locked loop (PLL) supporting 1×, 2×, and 4× clock multiplication
- System performance of over 125 MHz, as well as 64-bit, 66-MHz peripheral component interconnect (PCI) compliance
- 1.0-mm FineLine BGA™ packaging that uses only half the board area of traditional ball-grid array (BGA) packages

Embedded Architecture Breakthrough

Raphael devices provide a single-chip solution for complex system design, saving board space and simplifying system design implementation. The Raphael MultiCore architecture combines and enhances the strengths of the FLEX® 6000, MAX® 7000, and FLEX 10K architectures, as shown in Figure 1, and permits designers to integrate an entire system into a single device.

Figure 1. Raphael Incorporates LUTs, Product Terms, & Embedded Memory



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Raphael: Embedded PLD Family for System-Level Integration, continued from page 1

Altera pioneered embedded PLD architecture in 1995 with the introduction of the FLEX 10K family. The Raphael device's revolutionary MultiCore embedded architecture takes the embedded concept to a new level with an innovative combination of three different types of PLD structures: look-up tables (LUTs), like those found in FLEX devices; product-term arrays, like those found in MAX devices; and enhanced embedded memory blocks, like those found in FLEX□10KE devices. Together, these structures make the integration of complex functions such as megafunctions an easy and efficient process.

The key to the Raphael architecture is the embedded system block (ESB). The ESB offers embedded product-term capability with fast 3.9-ns performance. Many system designs today are implemented with multiple FLEX and MAX devices. However, where designs with multiple devices suffer from on-device/off-device delays that decrease system performance, Raphael devices integrate product-term and LUT capability to offer vastly improved system speeds. Figure 2 shows an example of the system speed improvements that can be achieved with Raphael devices.

The Raphael ESB can be configured as product-term logic, dual-port RAM, read-only memory (ROM), or CAM. This system-level memory integration efficiently supports the various memory requirements of a system-level design, such as cache RAM, dual-port first-in first-out (FIFO) buffers, or ROM.

CAM accelerates search applications such as databases, lists, and patterns, and high-speed communication applications. Unlike RAM, which looks up data at a specific address, CAM looks up data in the memory and outputs the address. With speeds of over 125 MHz, Raphael CAM is faster than traditional CAM.

The Raphael ESBs are located in the new MegaLAB structure, as shown in Figure 3 on page 4. Each MegaLAB consists of one ESB and 16 logic array blocks (LABs) composed of 10 logic elements (LEs). The MegaLABs are connected internally via the MegaLAB interconnect, which adds a fourth hierarchical level to the continuous metal FastTrack Interconnect routing structure, increasing both performance and efficiency.

Low-Voltage I/O Support

The trend toward system integration, higher performance requirements, and lower supply voltages makes it imperative for devices to support multiple low-voltage I/O standards. Raphael devices offer

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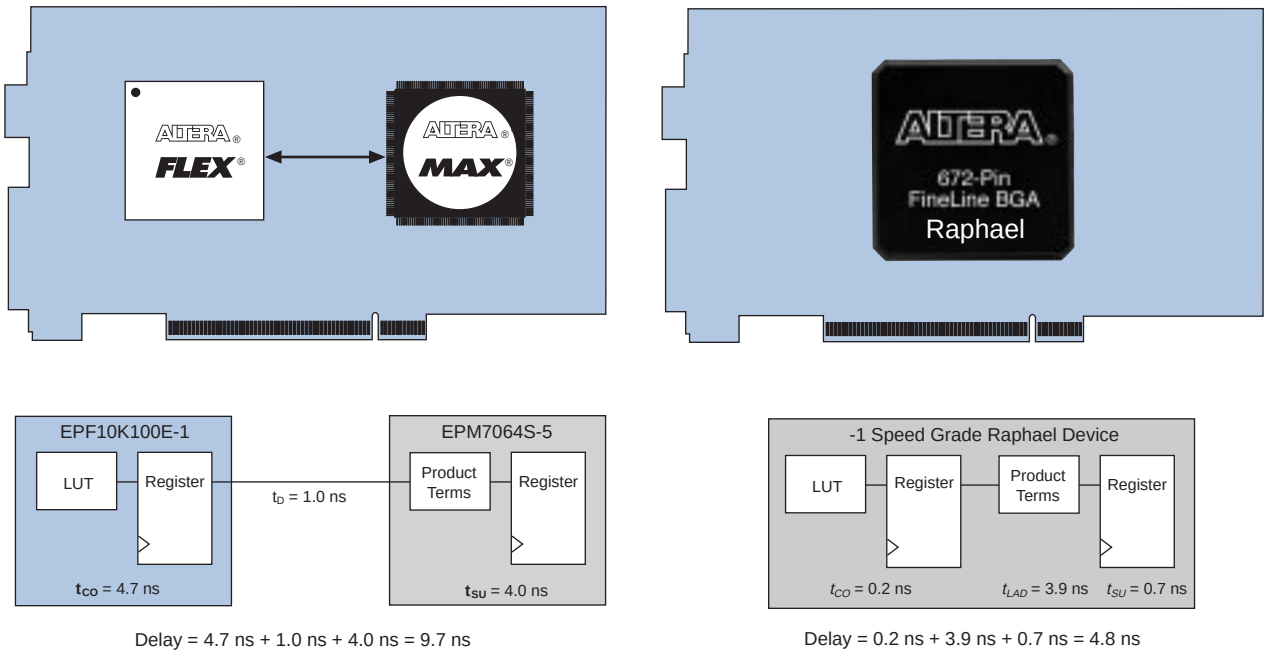
Figure 2. Integrated Product-Term Performance Capability Improves System Speeds



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selectable I/O support for the new LVTTL, LVCMOS, SSTL-3, GTL/GTL+, and LVDS standards, allowing high-speed interfacing between SDRAMs, processors, and system backplanes. Raphael devices also support the Altera MultiVolt™ I/O interface for 3.3-V, 2.5-V, and 1.8-V mixed voltage systems.

Raphael Family Members

The Raphael device family ranges from 100,000 to over 1 million usable gates of logic and will be introduced on a 0.25-µm, six-layer-metal SRAM process, with plans to migrate to a 0.18-micron, six-layer-metal process and then to a 0.15-micron, seven-layer-metal process. Table 1 outlines the Raphael family.

Availability and Packaging

The first Raphael family member, the 400,000-gate R400, is planned to ship in Q1 1999. It is expected to be available in 208-pin quad flat pack (QFP), 240-pin QFP packaging, and 599-pin pin-grid array (PGA), as well as the new 1.0-mm pitch FineLine BGA™ packaging.

Conclusion

Altera's Raphael device family has the density, performance, and system-level features to take PLDs into the next generation of flexible, system-on-a-chip design. These new and complex devices require an advanced software tool—Altera is developing software to meet this challenge. Using the revolutionary Raphael architecture and Altera's next-generation software, designers can find the ideal programmable logic solution for system-on-a-chip applications.

For further details, visit the Altera world-wide web site at **http://www.altera.com** or contact your local representative.

Figure 3. Raphael MegaLAB

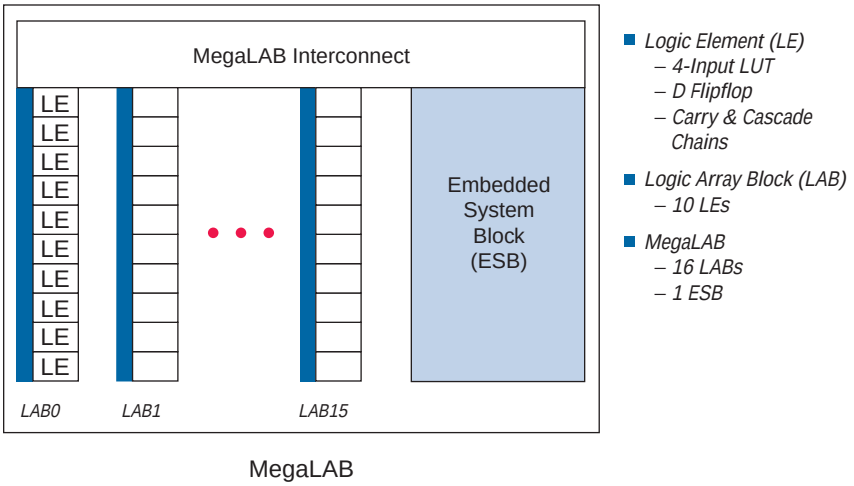

Table 1. Raphael Family Features

Feature	R100	R160	R200	R300	R400	R500	R1000
Maximum gates	263,000	404,000	526,000	728,000	1,052,000	1,294,000	2,670,000
Typical gates	53,000 to 106,000	82,000 to 163,000	106,000 to 211,000	147,000 to 293,000	213,000 to 423,000	262,000 to 520,000	541,000 to 1,073,000
LEs	4,160	6,400	8,320	11,520	16,640	20,480	42,240
Maximum RAM bits	53,248	81,920	106,496	147,456	212,992	262,144	540,672
Maximum macrocells	416	640	832	1,152	1,664	2,048	4,224
Maximum I/O pins	250	320	320	420	500	620	780
Packages, *Note (1)*	FineLine BGA 144-pin TQFP 208-pin QFP 240-pin QFP	FineLine BGA 144-pin TQFP 208-pin QFP 240-pin QFP	FineLine BGA 208-pin QFP 240-pin QFP	FineLine BGA 208-pin QFP 240-pin QFP	FineLine BGA 208-pin QFP 240-pin QFP 599-pin PGA	FineLine BGA	FineLine BGA

Note:
(1) TQFP: thin quad flat pack, QFP: quad flat pack, BGA: ball-grid array, PGA: pin-grid array.

Devices & TOOLS

FLEX Update

Design for FLEX 10KE Today

The Altera® MAX+PLUS® II version 9.01 software delivers advanced support for FLEX® 10KE devices, complete with full pin-out information. Designers can design, simulate, and lay out their boards today to take advantage of the high-performance, low-power, and dual-port RAM capability of FLEX 10KE devices. Table 1 lists the FLEX 10KE devices supported by the MAX+PLUS II version 9.01 software.

Table 1. FLEX 10KE Devices Supported by MAX+PLUS II Version 9.01 Software

Device	Package
EPF10K30E	144-Pin TQFP 208-Pin PQFP 256-Pin FineLine BGA 484-Pin FineLine BGA
EPF10K50E	144-Pin TQFP 208-Pin PQFP 240-Pin PQFP 256-Pin FineLine BGA 484-Pin FineLine BGA
EPF10K100B	208-Pin PQFP 240-Pin PQFP
EPF10K100E	208-Pin PQFP 240-Pin PQFP 356-Pin BGA 484-Pin FineLine BGA
EPF10K130E	240-Pin PQFP 484-Pin FineLine BGA 672-Pin FineLine BGA
EPF10K200E	599-Pin PGA 600-Pin BGA 672-Pin FineLine BGA

Table 2 shows FLEX 10KE device availability.

Table 2. FLEX 10KE Availability

Device	Availability
EPF10K30E	Q1 1999
EPF10K50E	October 1998
EPF10K100E	Q1 1999
EPF10K100B	Now
EPF10K130E	Q1 1999
EPF10K200E	Q4 1998
EPF10K250E	Second Half of 1999

250,000-Gate EPF10K250A Devices Shipping

Altera is currently shipping the industry's highest density device, the 250,000-gate EPF10K250A. This device is offered in 599-pin pin-grid array (PGA) and 600-pin ball-grid array (BGA) packages. With 12,160 logic elements (LEs) and 40,960 memory bits, this device is ideal for application-specific integrated circuit (ASIC) prototyping and allows system integration on a single chip.

2.5-V EPF10K100B Device Available

The EPF10K100B device is built on a 0.25-µm, 5-layer-metal process, offering high performance and low power consumption. The EPF10K100B device's 0.25-µm process provides nearly an 84% performance advantage and a 66% power savings over competing 0.35-µm, 3.3-V devices. The MultiVolt™ feature enables these devices to interface with 2.5-V, 3.3-V, or 5.0-V devices. The EPF10K100B devices in 240-pin plastic quad flat pack (PQFP) are available today. The 256-pin FineLine BGA™ package with a 17mm^2 footprint will be available in September 1998.

Entire 3.3-V FLEX 10KA Family Available

With high-performance, low-cost, embedded memory, and space-saving package offerings, the EPF10K10A device is a cost-effective solution for today's high-volume programmable logic device (PLD) designs. The smallest FLEX 10KA device, the feature-rich EPF10K10A is an ideal solution for your production design needs.

With the availability of the EPF10K250A and EPF10K10A devices, all of the 3.3-V FLEX 10KA devices have now been introduced.

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EPF6010A & EPF6016A Devices Available

Altera is now shipping 3.3-V EPF6010A and EPF6016A devices, which deliver high performance at prices that are competitive with gate arrays. These devices, along with the EPF6024A device (already shipping), are offered in 3 speed grades, including a new high-performance -1 speed grade. Support for these new -1 speed grades is available in the MAX+PLUS II version 9.01 software. Table 3 shows the features offered in the FLEX 6000 devices.

Table 3. FLEX 6000 Device Features

Feature	EPF6010A	EPF6016	EPF6016A	EPF6024A
Process	0.35 µm	0.5 µm	0.35 µm	0.35 µm
Supply Voltage	3.3 V	5.0 V	3.3 V	3.3 V
Logic Elements	880	1,320	1,320	1,960
Usable Gates	5,000 to 10,000	8,000 to 16,000	8,000 to 16,000	12,000 to 24,000
User I/O Pins (Maximum)	139	204	171	218

New FLEX 6000 Devices Coming Soon

FLEX 6000 devices in 100-pin and 256-pin FineLine BGA packages are planned for the fourth quarter of 1998. These area-efficient packages require less than half the board size of traditional ball-grid array (BGA) packages. Software support is planned for the MAX+PLUS II version 9.1 software, scheduled for release in Q4 1998. Table 4 shows FLEX 6000 package availability.

Configuration EPROM Update

EPC2 Device Available in October

The EPC2 device, the first reprogrammable Configuration EPROM from Altera, is scheduled for introduction in October 1998. This device, which will be offered in 20-pin plastic J-lead chip carrier (PLCC) and 32-pin thin quad flat pack (TQFP) packages, will be pin-compatible with all existing Altera Configuration EPROMs in the same packages. A single EPC2 device, which can configure any FLEX device up to 130,000 gates, can be programmed in-system using the industry-standard IEEE Std. 1149.1 Joint Test Action Group (JTAG) test ports. The EPC2 will operate at 3.3 V or 5.0 V.

MAX Update

MAX 9000A Device Availability

With propagation delays of 10 ns, MAX 9000A devices offer customers significant performance enhancements as well as cost reductions over MAX 9000 devices. Packages for the EPM9320A and EPM9560A devices are currently available in production quantities. Table 1 summarizes both commercial- and industrial-temperature grade MAX 9000A device availability.

Table 1. MAX 9000A Device Availability *Note (1)*

Device	t_{PD}	84-Pin PLCC	208-Pin PLCC	240-Pin RQFP	356-Pin BGA
EPM9320A	10 ns	C, I	C, I		C
EPM9560A	10 ns		C, I	C, I	C

Note:
(1) A "C" designates commercial and an "I" designates industrial temperature grade availability.

Table 4. FLEX 6000 Package Availability

Device	Availability	100-Pin TQFP	100-Pin BGA *(1)*	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin BGA	256-Pin BGA *(1)*
EPF6010A	Now	✓	✓	✓				✓
EPF6016	Now			✓	✓	✓	✓	
EPF6016A	Now	✓	✓	✓	✓			✓
EPF6024A	Now			✓	✓	✓	✓	✓

Note:
(1) FineLine BGA packages will be available in Q4 1998.

MAX 7000 & MAX 9000 Product Transitions

Altera is moving the MAX 7000 and MAX 9000 devices from a 0.65-µm process to a 0.5-µm process. Table 2 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notification page on the Altera web site at **http://www.altera.com**.

Table 2. MAX 7000 & MAX 9000 Migration Schedule *Note (1)*

Device	Reference *(2)*	Availability	Process
EPM7032	PCN9703 ADV9803	August 1998	0.5-micron
EPM7064 EPM7064S	PCN9703 ADV9708	Now	0.5-micron
EPM7128E EPM7128S	PCN9703 ADV9708	Now	0.5-micron
EPM7160E	PCN9703 ADV9803	October 1998	0.5-micron
EPM7192E EPM7192S	PCN9703 ADV9708	Now	0.5-micron
EPM7256S EPM7256E	PCN9703 ADV9708	Now	0.5-micron
EPM9320	PCN9703 ADV9803	September 1998	0.5-micron
EPM9560	PCN9703 ADV9803	September 1998	0.5-micron

Notes:
(1) The transition process will not result in any changes to data sheet parameters or ordering codes.
(2) Advisories and process change notices are available from Altera's web site.

Altera In-Circuit Tester Support

The MAX 7000S family offers complete in-circuit tester support. The most efficient way for customers to use in-circuit testers for in-system programming is to order fixed programming algorithm devices. These devices are denoted with an "F" at the end of the ordering code. For example, an EPM7128STC100-10 device for use with in-circuit testers has the ordering code EPM7128STC100-10F. To order "F" devices, contact your local Altera sales representative.

MAX 7000AE Devices

The new MAX 7000AE devices will provide the speed and functionality of MAX 7000A devices, plus enhanced in-system programmability (ISP) features. The MAX 7000AE devices will be offered in densities ranging from 32 to 512 macrocells and with propagation delays as fast as 5 ns, continuing the MAX 7000 family's industry leadership in density and performance.

The MAX 7000AE enhanced features are summarized in Table 3.

Table 3. MAX 7000AE Enhanced Features

Feature	Enhancement
New ISP programming algorithm	Improves programming by a factor of 2 to 10 times.
ISP_Done bit	Ensures complete programming.
Pull-up resistor on I/O pins	I/O pins pull high while programming in-system.

The first MAX 7000AE device, the EPM7064AE, will be available in September 1998. Table 4 shows Altera's MAX 7000A devices. The EPM7128A and EPM7256A, without the enhanced feature set, are currently available.

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Table 4. MAX 7000A Devices

Feature	EPM7032AE	EPM7064AE	EPM7128A	EPM7256A	EPM7384AE	EPM7512AE
Macrocells	32	64	128	256	384	512
Maximum User I/O Pins	36	68	100	164	212	212
Minimum t_{PD} (ns)	5.0	5.0	6.0	7.5	7.5	7.5
Packages	44-pin PLCC 44-pin TQFP	44-pin PLCC 44-pin TQFP 84-pin PLCC 100-pin TQFP 256-pin BGA	84-pin PLCC 100-pin TQFP 100-pin BGA 144-pin TQFP	100-pin TQFP 144-pin TQFP 208-pin PQFP 256-pin BGA	144-pin TQFP 208-pin PQFP 256-pin BGA	144-pin TQFP 208-pin PQFP 256-pin BGA
Projected Availability	Q1 1999	September 1998	Now	Now	Q1 1999	November 1998

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MAX 7000A Availability

Two 3.3-V MAX 7000A devices, the EPM7128A and EPM7256A, are currently shipping. Each MAX 7000A device supports ISP, MultiVolt I/O pins, and propagation delays as fast as 5.0 ns. MAX□7000A devices also provide pin-compatibility with the industry-standard MAX 7000 devices. Table 5 shows MAX 7000A device availability.

Table 5. MAX 7000A Device Availability

Device	Package	Speed Grade	Availability
EPM7032AE	44-pin PLCC	-5, -7, -10	Q1 1999
	44-pin TQFP	-5, -7, -10	
EPM7064AE	44-pin PLCC	-5, -7, -10	September 1998
	44-pin TQFP	-5, -7, -10	
	84-pin PLCC	-5, -7, -10	
	100-pin TQFP	-5, -7, -10	
EPM7128A	84-pin PLCC	-6, -7, -10, -12	Now
	100-pin TQFP	-6, -7, -10, -12	
	100-pin PQFP	-6, -7, -10, -12	
	160-pin PQFP	-6, -7, -10, -12	
	256-pin BGA	-6, -7, -10, -12	
EPM7256A	100-pin TQFP	-7, -10, -12	Now
	144-pin TQFP	-7, -10, -12	
	208-pin PQFP	-7, -10, -12	
	256-pin BGA	-7, -10, -12	
EPM7384AE	144-pin TQFP	-7, -10, -12	Q1 1999
	208-pin PQFP	-7, -10, -12	
	256-pin BGA	-7, -10, -12	
EPM7512AE	144-pin TQFP	-7, -10, -12	November 1998
	208-pin PQFP	-7, -10, -15	
	256-pin BGA	-7, -10, -12	

MAX 7000S Devices

All MAX 7000S devices are now available. These devices offer features such as speed grades up to 5 ns, ISP, IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells, and an open-drain output option. Table 6 shows the available packages and speed grades.

Table 6. MAX 7000S Device Features

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-6, -7, -10
	44-pin TQFP	-6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

Discontinued Devices Update

Altera has no new announcements regarding discontinued devices. Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

Tools Update

New Features Available in MAX+PLUS II Version 9.01

Altera is now shipping the MAX+PLUS II version 9.01 software. This version provides compilation and simulation support for all Altera FLEX 10KE devices, as well as enhancements that can significantly increase your design productivity, including:

- Improved place-and-route algorithms that increase average registered design performance by 5%.
- Improved quality of results for Altera VHDL and Verilog HDL synthesis that is now comparable to the quality of results for Altera Hardware Description Language (AHDL) synthesis.
- Jam™ Byte Code, a compiled representation of a JBC File (**.jbc**), which is available in MAX+PLUS II version 9.01, speeds up in-system programming times by 25%. For more information on Jam Byte Code, see "Introducing Jam Byte Code" on page 20.
- Support for the new FineLine BGA packages.

PC Network Licensing in MAX+PLUS II Version 9.01

The MAX+PLUS II version 9.01 software provides floating-node licenses for PC networks. Customers can order this new product using the PLS-NET/PC ordering code. This product is full-featured and supports all Altera device families. Floating-node licenses for PC platforms can be implemented on UNIX- (Solaris 2.5+, HP-UX 10.20+, and IBM AIX 4.1+) or Windows NT-based license servers. The license will be based on either the UNIX server HOST ID or the Network Interface Card (NIC) ID for Windows NT servers. For a limited time, customers with fixed-node versions of MAX+PLUS II on active maintenance can purchase floating-node design sites at a significant discount. Contact your local Altera sales representative and ask about the PLS-PROMO discount. This offer is valid through Q3 1998.

Version-Controlled Licensing in MAX+PLUS II Version 9.1

The MAX+PLUS II version 9.1 software (scheduled for release in October 1998) will feature GLOBEtrotter's FLEXlm, a leading license management program. FLEXlm integration allows easy and flexible network licensing and ensures full Year 2000 compliance for the MAX+PLUS II software.

This new license management program also changes the software licensing structure in a number of ways:

- Licensing for fixed-node, PC-based systems still requires software guards, but a license file is used instead of an authorization code. When you upgrade to MAX+PLUS II version 9.1, you must obtain a new license file to use the software.
- To minimize any inconvenience, Altera will ensure that a new license is sent to all customers who have a valid software maintenance agreement before the release of the MAX+PLUS II version 9.1 software. Additionally, after October 1, 1998, MAX+PLUS II version 9.1 users will be able to generate a license file on the Altera web site at **http://www.altera.com**.
- Starting with MAX+PLUS II version 9.1 software, only customers with a valid maintenance agreement will be able to use the features of each new release. Customers without a maintenance agreement can continue to use their existing version of MAX+PLUS II software. A new license file must be generated each time the maintenance contract is renewed (generally once a year).

Technical ARTICLES

FLEX 10KE EAB Provides Advanced Features

Altera® FLEX® 10KE devices contain advanced system-level features, including enhanced embedded array blocks (EABs), that increase performance and resource utilization. The FLEX 10KE EAB is a flexible block of RAM with registers on the input and output ports. The EAB is also suitable for functions such as multipliers, vector scalars, and error correction circuits when programmed with a read-only pattern. These functions can be combined in applications such as digital filters and microcontrollers.

Logic functions are implemented by programming the EAB with a read-only pattern during configuration, thereby creating a large look-up table (LUT). With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of EABs. The large capacity of EABs enables designers to implement complex functions in one logic level without the routing delays associated with linked logic elements (LEs) or field-programmable gate array (FPGA) RAM blocks. For example, a single EAB can implement a 5×4 multiplier with nine inputs and nine outputs. Parameterized functions such as library of parameterized module (LPM) functions can take advantage of the EAB automatically.

The FLEX 10KE EAB provides advantages over FPGAs, which implement on-board RAM as arrays of small, distributed RAM blocks. These small FPGA RAM blocks must be connected together to make usable-sized RAM blocks. The RAM blocks are connected together using multiplexers implemented with more logic blocks. These extra multiplexers cause extra delays, which slow down the RAM block. FPGA RAM blocks are also prone to routing problems because small blocks of RAM must be connected together to make larger blocks. In contrast, EABs can be used to implement large, dedicated blocks of RAM that eliminate these timing and routing concerns.

Dual-Port Mode

The FLEX 10KE enhanced EAB adds dual-port capability to the existing EAB structure. The dual-port structure is ideal for first-in first-out (FIFO) buffers with one or two clocks. The FLEX 10KE EAB can act in dual-port or single-port mode. When in dual-port mode, separate clocks may be used for EAB read and write sections, which allows the EAB to be written and read at different rates. It also has separate synchronous clock enable signals for the EAB read and write sections, which allows independent control of these sections. See Figure 1 on page 11.

Single-Port Mode

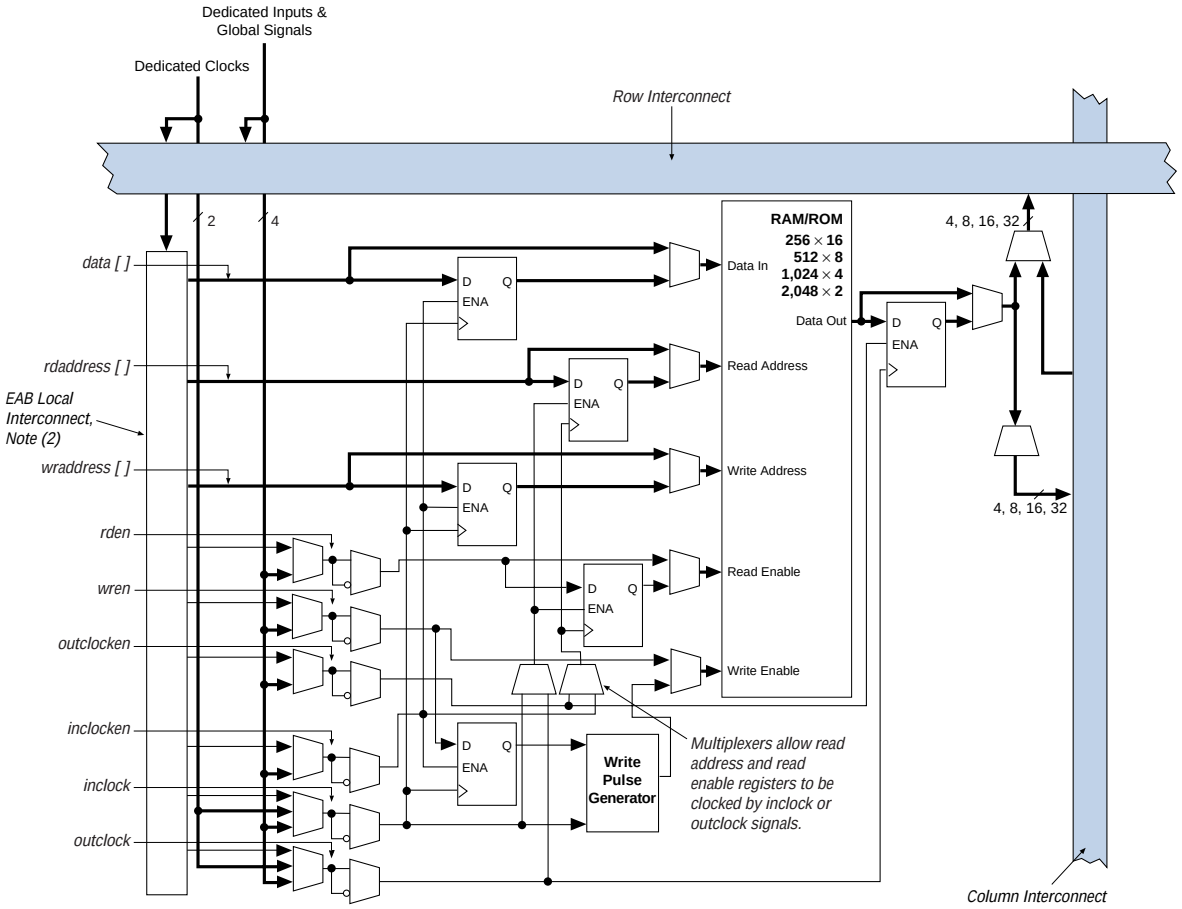
The FLEX 10KE EAB can also be used in single-port mode. This mode is also used for backward compatibility with FLEX 10K designs. For an example of a FLEX 10KE device in single-port mode, see Figure 2 on page 12.

Synchronous RAM

EABs can be used to implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (`WE`) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the `WE` signal. In contrast, the EAB's synchronous RAM generates its own `WE` signal and is self-timed with respect to the input or write clock. A circuit using the EAB's self-timed RAM must only meet the setup and hold time specifications of the global clock. When used as RAM, each EAB can be configured in any of the following sizes: 256 × 16, 512 × 8, 1,024 × 4, or 2,048 × 2.

Larger blocks of RAM are created by combining multiple EABs. For example, two 256 × 16 RAM blocks can be combined to form a 256 × 32 block; two 512 × 8 RAM blocks can be combined to form a 512 × 16 block. See Figure 3 on page 12.

Figure 1. FLEX 10KE Device in Dual-Port RAM Mode *Notes (1), (3)*



Notes:

(1) All registers can be asynchronously cleared by EAB local interconnect signals, global signals, or the chip-wide reset.

(2) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels. EPF10K100E, EPF10K130E, EPF10K200E, and EPF10K250E devices have 104 EAB local interconnect channels.

(3) The EPF10K100B device does not offer dual-port RAM mode.

If necessary, all EABs in a device can be cascaded to form a single RAM block. EABs can be cascaded to form RAM blocks of up to 2,048 words without impacting timing. Altera's MAX+PLUS® II software automatically combines EABs to meet a designer's RAM specifications.

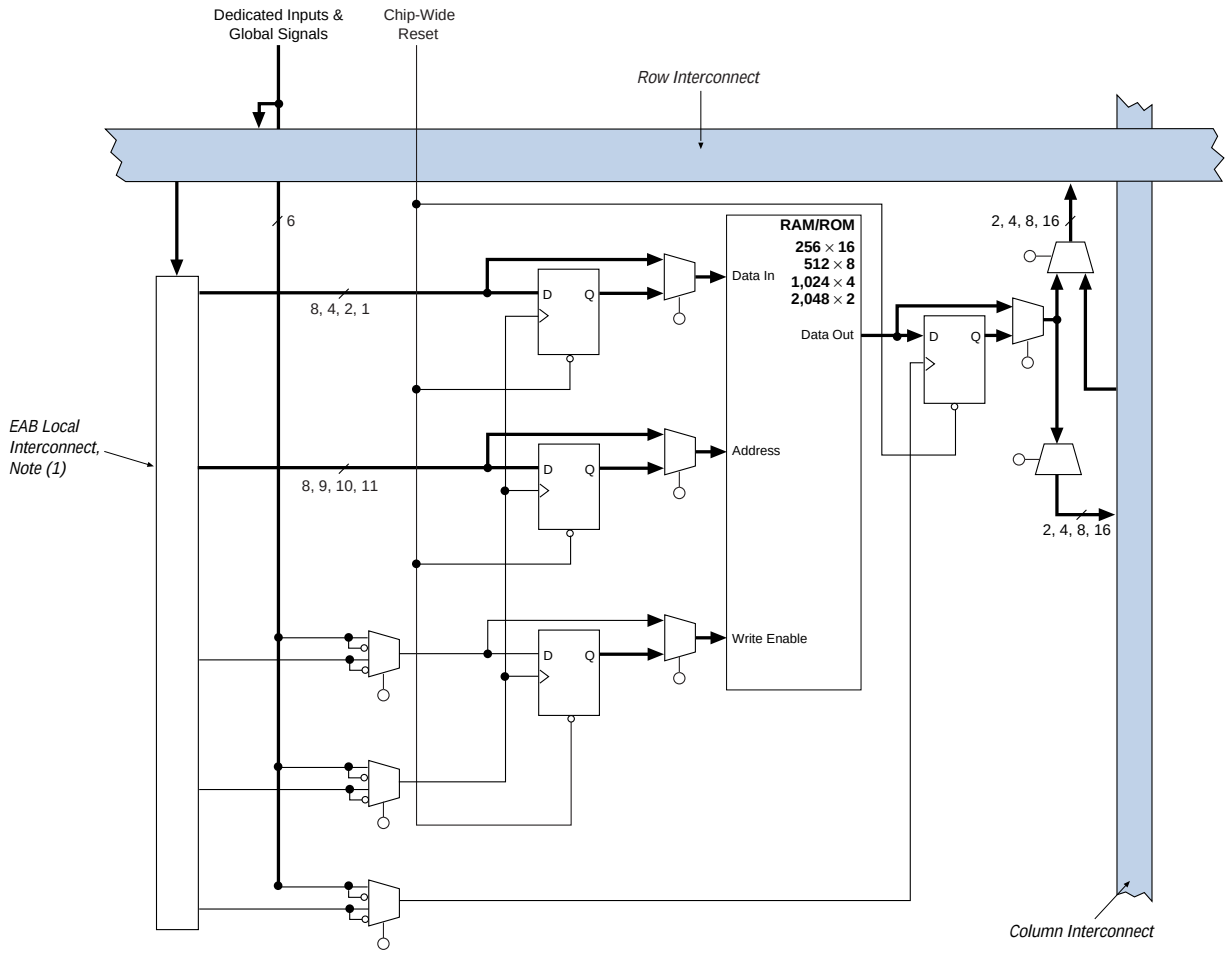
EABs provide flexible options for driving and controlling clock signals. Different clocks and clock enables can be used for reading and writing to the EAB. Registers can be independently inserted on the data input, EAB output, write address, WE signals, read address, and read enable (RE) signals. The global signals and the EAB local interconnect can drive WE, RE, and clock enable signals. The global signals, dedicated clock pins, and EAB local interconnect can drive the EAB clock signals. Because the LEs drive the EAB local interconnect, the LEs can control WE, RE, clear, clock, and clock enable signals.

An EAB is fed by a row interconnect and can drive out to row and column interconnects. Each EAB output can drive up to two row channels and up to two column channels; the unused row channel can be driven by other LEs. This feature increases the routing resources available for EAB outputs. The column interconnect, which is adjacent to the EAB, has twice as many channels as other columns in the device. See Figures 2 and 3 on page 12.

continued on page 12

FLEX 10KE EAB Provides Advanced Features, continued from page 11

Figure 2. FLEX 10KE Device in Single-Port RAM Mode



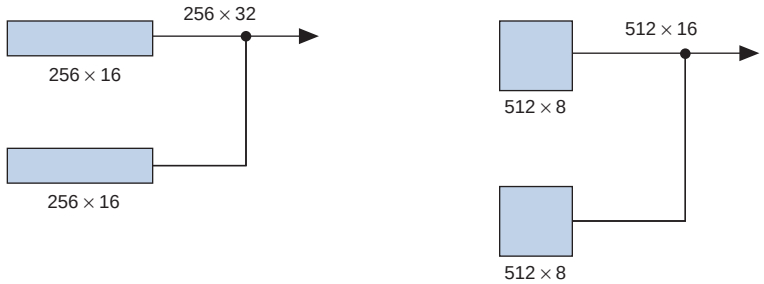
Notes:

(1) EPF10K30E and EPF10K50E devices have 88 EAB local interconnect channels. EPF10K100E, EPF10K100B, EPF10K130E, EPF10K200E, and EPF10K250E devices have 104 EAB local interconnect channels.

For more information on FLEX 10KE devices, refer to the *FLEX 10KE Embedded Programmable Logic Family Data Sheet*, or contact Altera Applications.

The *Design Tips from Altera Applications* series will resume next quarter.

Figure 3. Examples of Combining EABs



Guidelines for Using ISP

As time-to-market pressures increase, design engineers require advanced system-level products to ensure problem-free development and manufacturing. Programmable logic devices (PLDs) with in-system programmability (ISP) can help accelerate development time, simplify the manufacturing flow, reduce inventory costs, and improve printed circuit board (PCB) testing capabilities. Altera® MAX®9000 (including MAX 9000A), MAX 7000S, and MAX 7000A devices can be programmed and reprogrammed using ISP via the IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface. This interface allows devices to be programmed and the PCB to be functionally tested in a single manufacturing step, saving testing time and assembly costs. This article describes some of the guidelines you should follow when using ISP.

Device Operating Conditions

Each Altera device has several parametric ratings, or operating conditions, that are required for proper operation. Even if these conditions are violated in user mode, the device usually operates correctly. However, these conditions should not be exceeded during in-system programming. Violating any of the operating conditions during in-system programming can result in programming failures or incorrectly programmed devices. Go to the appropriate family data sheet in the ***1998 Data Book*** for the specifications.

TCK Signal

Most in-system programming failures are caused by a noisy TCK signal. Noisy transitions on rising or falling edges can cause incorrect clocking of the IEEE Std. 1149.1 Test Access Port (TAP) controller. Incorrect clocking can cause the state machine to transition to an unknown state, leading to in-system programming failures.

Further, because the TCK signal must drive all IEEE Std. 1149.1 devices in the chain in parallel, the signal will have a high fan-out. Like any other high-fan-out user-mode clock, you must manage a clock tree to maintain signal integrity. Typical errors that result from clock integrity problems are invalid ID messages, blank-check errors, or verification errors.

MultiVolt Devices

For the JTAG circuitry to operate correctly during in-system programming or boundary-scan testing, all devices in a JTAG chain must be in the same state. Therefore, in systems with multiple power supply voltages, the JTAG circuitry must be held in the test-logic-reset state until all devices in the chain are completely powered up. This procedure is particularly important because systems with multiple power supplies cannot power all voltage levels simultaneously.

Altera devices with the MultiVolt™ feature can use two power supply voltages (V_{CCINT} and V_{CCIO}). V_{CCINT} provides power to the JTAG circuitry; V_{CCIO} provides power to output drivers for all pins, including TDO. Therefore, when these devices use two power supply voltages, the JTAG circuitry must be held in the test-logic-reset state until both power supplies are turned on. The easiest way to ensure this is to pull TCK low and TMS high.

Using "F" vs. Non-"F" Devices

MAX devices are either fixed-algorithm ("F"), or require branching algorithms (non-"F"). Most in-circuit tester file formats (e.g., Serial Vector Format Files (**.svf**), Hewlett-Packard Pattern Capture Format Files (**.pcf**), DTS, and ASC) are "fixed" or deterministic, which means they can only support one fixed algorithm without branching. The MAX+PLUS II software version 8.2 and higher generates SVF files for "F" devices. Because the algorithms in SVF files are constant, you can always use these SVF files to program future "F" devices.

Altera does not recommend programming non-"F" devices via most in-circuit testers. Some testers support the Jam™ Programming and Test Language and can program non-"F" devices. Non-"F" devices require branching based on three variables read from the device: programming pulse time, erase pulse time, and manufacturer silicon ID. These three variables are programmed into all Altera non-"F" devices. Using only "F" devices eliminates potential problems if these variables change.

Conclusion

The information provided in this article is based on development experiences and customer issues resolved by Altera. Refer to *Application Note 100 (In-System Programmability Guidelines)* for complete details. For more information on resolving in-system programming problems, contact the ISP Support Program at **ISPembed@altera.com** or **ISPATE@altera.com**.

Implementing FIFO Solutions for Altera Devices with the New FIFO MegaWizard Plug-In

Altera now offers first-in first-out (FIFO) buffer solutions with a new MegaWizard™ Plug-In for FIFO buffers. This feature provides fast, flexible, and easy-to-implement FIFO solutions by automatically selecting the appropriate megafunction based upon FIFO design requirements. This feature is available beginning with MAX+PLUS® II version 9.01 software.

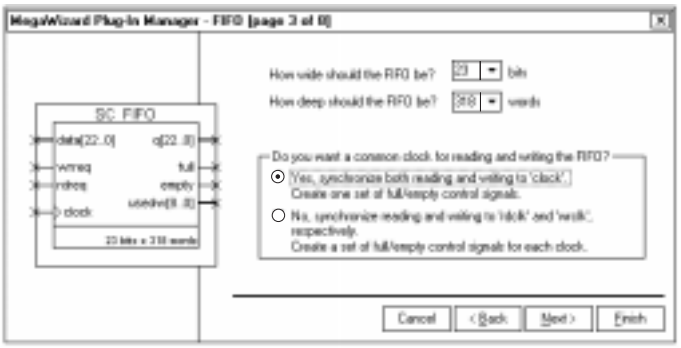
The FIFO MegaWizard solution implements two new megafunctions, the single-clock FIFO (`scfifo`) and the double-clock FIFO (`dcfifo`). The `SCFIFO` is used for synchronous FIFO designs implemented in all FLEX 10K device family embedded array blocks (EABs), including the new FLEX 10KE dual-port RAM. The `dcfifo` is implemented for asynchronous FIFO designs (designs requiring separate read and write clocks) in the FLEX 10KE dual-port EAB. Both FIFOs can be implemented as logic element- (LE) based FIFOs in all FLEX devices.

With the FIFO MegaWizard plug-in, FIFO width and depth dimensions, output control signals, and read access can easily be chosen or modified for a wide range of FIFO solutions.

Synchronous FIFO Designs

Using the FIFO MegaWizard plug-in, synchronous FIFO designs are implemented by selecting the option to assign a common clock for both reading and writing to the FIFO function. Simultaneous reads and writes are possible with the synchronous FIFO function. Figure 1 shows the MegaWizard Plug-In Manager with the option for a synchronous FIFO design selected.

Figure 1. Selecting a Synchronous FIFO



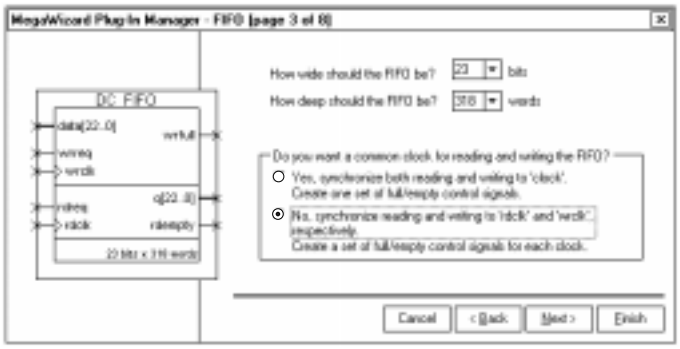
The synchronous FIFO function is ideal for implementation in FLEX 10KE devices, taking full advantage of the EABs' dual-port architecture, 16-bit width, and 4,096-bit memory per EAB.

With the FLEX 10K, FLEX 10KA, and the EPF10K100B devices, the MegaWizard plug-in-generated megafunction is efficiently implemented in EABs as an interleaved FIFO function, allowing simultaneous reads and writes to be performed.

Asynchronous FIFO Designs

With the MegaWizard feature, asynchronous FIFO designs are implemented by selecting the option to assign separate clocks for reading and writing to the FIFO function. Figure 2 shows the MegaWizard Plug-In Manager with the option for an asynchronous FIFO design selected.

Figure 2. Selecting an Asynchronous FIFO



As with the synchronous FIFO function, the asynchronous FIFO function takes full advantage of the FLEX 10KE device's dual-port architecture.

For more information on the MegaWizard Plug-In Manager, FLEX 10KE dual-port EAB, and `scfifo` and `dcfifo` functions, contact Altera Applications at (800) 800-EPLD or consult MAX+PLUS II Help (version 9.01 or higher). For more information about FIFO solutions for FLEX devices, refer to Altera's May 1998 *News & Views* on the Altera web site, or contact Altera Applications.

Contributed Article

ASSET InterTech Provides Low-Cost Test & ISP Support

by Dave Bonnett
Product Marketing Manager
ASSET InterTech, Inc.

For several years, end equipment manufacturers have heard about in-system programmability (ISP) as an exciting and effective way to help meet the increasingly difficult cost and time-to-market requirements of their industries. The emergence of ISP as the programming methodology of choice for programmable logic devices (PLDs) has not been accidental. The PLD industry has expended significant effort to provide both the devices and the tools to support ISP. Now, the de facto adoption of the boundary-scan (IEEE Std. 1149.1) Test Access Port (TAP) as the serial interface for ISP combines companies that are the experts in devices capable of ISP with companies that are the experts in boundary-scan tests (BSTs). With the ASSET suite of tools, the promises of ISP can be realized today.

ASSET's ISP Leadership

ASSET has long been an active leader in the standardization process for ISP. In addition to helping Altera with its efforts to standardize the Jam™ Programming and Test Language through JEDEC, ASSET has been responsible for maintaining the serial vector format (SVF) specification. Many on the staff at ASSET worked on the development of SVF as a standard format that would allow vectors to be transferred among different BST systems. ASSET has enhanced SVF by adding instructions and capabilities that allow it to be used effectively in the ISP process.

A Valuable ASSET

The ASSET® product family, which runs on PC or VXI platforms, allows users to quickly and easily test and perform in-system programming during any phase of a product's life, including design, manufacturing, and in-field maintenance. ASSET's ISP capabilities are available in two different products. ScanProgrammer™ is an interactive programming product that is used during design verification. ISPExtender brings the full power of ISP to ASSET's existing manufacturing test solutions.

While the ASSET system has been used for some time to perform ISP with SVF files, ScanProgrammer automates and simplifies the process. ScanProgrammer adds the ability to use the Jam language to ASSET's existing support for ISP using SVF. ScanProgrammer can be used to program devices during the manufacturing/assembly test process. ScanProgrammer can also load programmable devices during burn-in testing. In addition, it can be used later in a system's life cycle to load updated software into PLDs after the system has been shipped and installed in the field.

ISPExtender adds support for the Jam language to ASSET's ScanDriver™, allowing Jam files to be used in either a stand-alone programming station or ISP that is integrated into the manufacturing flow. ScanDriver/ISPExtender is controlled from a manufacturing test user interface so that it will fit seamlessly into any manufacturing process.

The Future of ISP

Although the need for ISP has gained significant momentum in recent years, the increased use of new, more delicate and finer-pitch packages like ball-grid array packages, chip scale packages, and others will certainly accelerate the use of ISP in the years ahead. The tools—like ASSET—used to reduce PLD programming costs and cut a system's time-to-market, are available today for the designers seeking a competitive advantage.

Contact Information:
ASSET InterTech, Inc.
2201 N. Central Expressway
Suite 105
Richardson, TX 75080
http://www.asset-intertech.com

Questions & ANSWERS

Q *What are the extra balls that are not part of the ball grid on some ball-grid array (BGA) packages, and will they affect the reflow process?*

A The extra solder balls provide ground for the V_{SS} plane that is connected to the package. The extra balls are called high-temperature balls because they have a different tin/lead (Sn/Pb) composition than the regular BGA solder balls and melt at a higher temperature. These high-temperature balls have a 90/10 ratio of Sn/Pb and melt at 240° to 245° C. Device pin leads have a 63/37 ratio of Sn/Pb.

The maximum temperature a package can reach before it damages the solder or the device is 220° C. Therefore, the high-temperature balls will not disturb the reflow process because they melt at a temperature well above the maximum package temperature. If the high-temperature balls do melt, it is an indication that the reflow temperature is too high.

Q *How do I combine multiple Timing Analyzer outputs into one file when running the MAX+PLUS® II software from the command line?*

A You can use either the `type` command (from a DOS or command prompt) or the `cat` command (from a UNIX prompt) to combine multiple Timing Analyzer Output Files (**.tao**) into a single file. For example:

DOS: `type <`*filename*`>.tao > <`*result name*`>.txt`

UNIX: `cat <`*filename*`>.tao > <`*result name*`>.txt`

You can also use these commands in a batch or script file. A sample DOS batch file is shown below:

```
maxplus2 -c chiptrip -ta_reg chiptrip
type chiptrip.tao >> results.txt
```

The example above compiles the project **chiptrip** and creates a **chiptrip.tao** file for registered performance. The batch file then adds the TAO file information to a file named **results.txt**. This process can be repeated for different compilations and timing analyses to save all TAO file information to the same **results.txt** file.

Q *Can I configure an EPF6016A device with an EPF6016 configuration file?*

A The EPF6016A and EPF6016 devices are not configuration file-compatible; you cannot configure an EPF6016A device with an EPF6016 configuration file, or vice versa. To migrate an EPF6016 design to the EPF6016A device, change the device assignment to the EPF6016A device and recompile it. Using the **Smart Recompile** command (Processing menu) will allow the MAX+PLUS II Compiler to skip over the Logic Synthesizer and Fitter, speeding the recompilation.

After recompilation, Altera recommends re-running timing analysis and simulation to verify correct design operation with the faster EPF6016A device.

Q *Why does my FLEX® 8000 device fail during in-circuit reconfiguration (ICR) when using the Active Serial (AS) configuration mode?*

A You may require stabilization on `DCLK`. Prior to the start of configuration, FLEX 8000 devices in AS mode tri-state `DCLK`, which becomes active after `nSTATUS` is released by the FLEX 8000 device and pulled high to V_{CC}. `DCLK` is tri-stated and floating for a period of time between `nSTATUS` being released and `DCLK` starting to toggle.

If `nSTATUS` is connected to the count enable of the serial Configuration EPROM device, the EPROM counter can be enabled by pulling `nSTATUS` high to V_{CC}. Then, the configuration EPROM can be ready to send out data if rising edges on the `DCLK` input are seen. A floating `DCLK` can potentially send erroneous rising edges to the configuration EPROM, thereby clocking the EPROM counter before the FLEX 8000 device is ready to accept data correctly. This situation may cause configuration to fail.

One solution is to add a 2.2-KΩ pull-down resistor to `DCLK`. While `DCLK` is tri-stated at the start of ICR, the pull-down resistor prevents the EPROM device from recognizing spurious rising edges on its clock input until the FLEX 8000 device actively toggles `DCLK`.

For more details on FLEX 8000 device configuration, refer to the following documents:

- *Application Note 33 (Configuring FLEX 8000 Devices)*
- *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*

Q *What is the minimum time that a clear signal must be held active on a FLEX device to make sure that a reset is actually performed?*

A To ensure that a reset is performed, you must hold the clear signal active for a length of time that is at least as long as the delay from the input pin to the clear port on the flipflop. You can find the delay by using the Timing Analyzer (Delay Matrix) in the MAX+PLUS II software. Select the input pin to which the clear signal is assigned as the timing analysis source and the clear port of the flipflop as the timing analysis destination.

Q *Does the MAX+PLUS II software show the effect of using a 3.3-V V_{CCIO} with a FLEX 10KE device (including EPF10K100B)?*

A The MAX+PLUS II software shows the effect of using MultiVolt™ I/O for all devices that support this feature. On 5.0-V and 3.3-V devices, using MultiVolt I/O will slow I/O output performance slightly, because the V_{CCIO} level is lowered. However, on 2.5-V FLEX 10KE devices, V_{CCIO} can be driven to 3.3 V. When driving V_{CCIO} at 3.3 V, the I/O output performance is faster than when V_{CCIO} is 2.5 V.

To model the effect of MultiVolt I/O on any device that supports this feature, turn on the *MultiVolt I/O* option in the **Global Project Device Options** dialog box (Assign menu).

Q *Where can I find information on how to use the MAX+PLUS II software with third-party EDA tools?*

A For information on using the MAX+PLUS II software with other EDA tools, go to the MAX+PLUS II ACCESS℠ Key Guidelines on Altera's web site or on the ***MAX+PLUS II Software CD-ROM*** version 8.2 or higher. However, you should always refer to the web for the most up-to-date information. These guidelines replace the software interface guides that were available for MAX+PLUS II version 8.1 and earlier. For version 9.01, these guidelines should automatically be installed together with the MAX+PLUS II software.

Q *Are MAX® 7000, MAX 7000E, MAX 7000S, and MAX 7000A device Programmer Object Files (**.pof**) compatible?*

A Typically, you can program a newer device type with an older programming file, but not vice versa. The following programming files are compatible:

- You can program a MAX 7000E device with a MAX 7000 POF.
- You can program a MAX 7000S device with a MAX 7000E or MAX 7000 POF. The MAX 7000S device features are a superset of the MAX 7000E device features. Therefore, if you program a MAX 7000S device with a MAX 7000E POF, the MAX+PLUS II software will automatically disable the superset features on the MAX 7000S device. This programming (often called cross-programming) is supported by the MAX+PLUS II software, as well as by third-party programmers such as programmers from Data I/O (**http://www.data-io.com**) and BP Microsystems (**http://www.bpmicro.com**).
- You can program a MAX 7000A device with a MAX 7000, MAX 7000E, or MAX 7000S POF.

Q *Can I toggle nCS and CS while configuring one or more FLEX devices in the Passive Parallel Asynchronous (PPA) or Passive Serial Asynchronous (PSA) modes?*

A You can toggle nCS and CS during configuration if your design meets the specifications listed in the table below.

Table 1. FLEX Device Family

Parameter	Definition	FLEX 6000	FLEX 8000	FLEX 10K
t_{CSSU}	Chip select setup time before rising edge on nWS (minimum)	50 ns	50 ns	50 ns
t_{WSP}	nWS low pulse width (minimum)	50 ns	500 ns	200 ns
t_{CSH}	Chip select hold time after rising edge on nWS (minimum)	5 ns	10 ns	10 ns, *(1)* 15 ns, *(2)*

Notes:
(1) This specification applies to EPF10K10, EPF10K20, EPF10K30, EPF10K40, EPF10K50, and all FLEX 10KA and FLEX 10KE devices.
(2) This specification applies to EPF10K70 and EPF10K100 devices only.

Altera
VIEWPOINT

Next-Generation Tool Requirements

Robert K. Beachler
Sr. Director, Development Tools Marketing

The era of multi-million-gate programmable logic design is fast approaching. Are you ready? Altera has already set the stage by designing Raphael™ devices, the latest Altera® programmable logic device (PLD) family that will offer single-chip densities measured in millions of gates. The ramifications of devices of this size are substantial: designers must modify their methodology to create designs successfully. Additionally, programmable logic designers will need new techniques to meet the demand of shrinking development cycles. This article describes some of the ways the design process must change to accommodate multi-million-gate devices.

Megafunctions: Pre-Tested Functional Blocks

In the era of multi-million-gate design, the use of megafunctions will increase dramatically. No other single factor can improve designer productivity as much as using megafunctions. Altera has pioneered the use of megafunctions in programmable logic, and has developed key technology innovations that will accelerate multi-million-gate design. Altera is the only company to offer the OpenCore™ capability, allowing engineers to "test drive" encrypted functions from Altera and its Altera Megafunction Partners Program (AMPP℠) partnership. MegaWizard™ Plug-Ins provide powerful parameterization capability to ease the integration of megafunctions into diverse design requirements. Improvement in these capabilities and increasing function availability will be part of the multi-million-gate design methodology.

Design Collaboration

With today's rapid development cycles, it is unlikely that a single individual will undertake designs of this size. Multi-person design teams must be assigned to a single PLD, much like application-specific integrated circuits (ASICs) are designed today. To support large design teams, next-generation tools will require workgroup-computing capability, complete with heterogeneous network support and design modification tracking.

Advanced Software

To support multi-million-gate designs, industrial-strength databases will be required to support the Mbytes of data needed to represent the design. As design size grows, design iteration time must be kept to a minimum. Exciting new technologies will allow engineers to make small design changes and see results in minutes. Without such advanced software, a design compiled from scratch would take hours.

Today, an engineer can order and receive a dual-processor Pentium II-based PC in less than 10 days, but very few software applications are written to take advantage of this tremendous computing power. Next-generation software will maximize the potential of two- and four-processor machines. Load-sharing facilities will take advantage of under-used CPUs across a network, helping to keep compilation times low.

Tool Integration

There is a thriving business in third-party development tools for programmable logic. For next-generation PLD development tools, the integration with these third-party tools will grow even closer. Users will be hard-pressed to tell where one tool ends, and the next one begins.

Internet Support

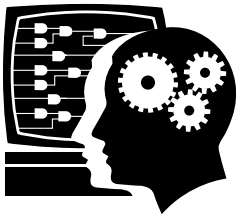
When the MAX+PLUS® II software was designed in the early 1990s, the Internet was not as widespread or popular as it is today. Looking forward, it is clear that

the Internet will become a critical component of the support infrastructure for system designers. Using the Internet to its full advantage will allow engineers to stay abreast of the latest software releases, device information, and solutions to the toughest design problems.

Right Around the Corner

The multi-million-gate design era is almost upon us. New tools, embracing the latest advances in computing hardware and software technology, will be necessary to realize the full potential of the latest silicon. Be prepared for an exciting new chapter in programmable logic design.

Customer Training Brings You Up to Speed



Altera's Customer Training Department has revised and expanded its course offerings. Classes are created specifically to meet different experience levels, provide realistic design examples and labs, and offer sound advice on hardware design techniques and software settings. These one-day sessions give you knowledge that might otherwise require months of trial and error work.

Introductory courses are ideal for designers who are beginning to use Altera devices. These courses introduce the architecture and features of Altera device families, as well as how to access these features and analyze design results with the MAX+PLUS® II software. Discussions include basic recommendations for design layout and software settings.

For experienced Altera users interested in gaining higher speed and utilization, advanced courses focus on fitting and performance for specific architectures. These classes contain more labs than the introductory courses. The advanced courses are faster paced, more challenging, and require knowledge of the MAX+PLUS□II software as well as a basic understanding of Altera device family architectures.

Altera also offers VHDL and AHDL courses for designers at any experience level. These classes cover basic syntax and design structure, inferring and instantiating elements, and creating an overall design with the languages. Instructors emphasize the common problems of coding, particularly in the VHDL course.

A list of available courses is shown below. You can also find more detailed information and a registration form on the Altera world-wide web site at **http://www.altera.com**.

- *Introduction to Altera's MAX Device Families*
- *Introduction to Altera's FLEX Device Families*
- *Advanced Design Techniques for Altera's MAX Device Families*
- *Advanced Design Techniques for Altera's FLEX Device Families*
- *Designing with MAX+PLUS II*
- *Designing with MAX+PLUS II Using AHDL*
- *Designing with MAX+PLUS II Using VHDL*

Introducing Jam Byte Code

The Jam™ programming and test language, a software-level standard for in-system programmability (ISP), provides a solution to problems that have plagued in-system programming, such as ease of use, fast programming times, and small file sizes. To address issues that have arisen since its first implementation—file sizes too large for DOS-based PC programming and for embedded processors with little cache—Altera developed Jam Byte Code. Jam Byte Code is a binary-based programming file format that produces smaller file sizes and faster programming times than the original ASCII-based Jam File. Jam Byte Code accomplishes these improvements through reduced overhead parsing and added compression algorithms and is available in MAX+PLUS II version 9.01 (complete online documentation will be available in version 9.1).

Jam Byte Code Files

Jam Byte Code is a binary file format analogous to the existing ASCII Jam format. Like ASCII Jam files, Jam Byte Code files comply with the *Jam Programming and Test Language Specification* and use defined variables. Jam Byte Code is also vendor- and platform-independent, and programs devices via the IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface.

Jam Byte Code files consist of two software components: the Jam Byte Code Compiler and the Jam Byte Code Interpreter. The Jam Byte Code Compiler writes the Jam Byte Code File (**.jbc**) required to program a design into a specified device. The Jam Byte Code Interpreter interprets the JBC File and programs the target device. Together, these elements create a universal language and tool that addresses all programmable logic devices (PLDs) and all programming methodologies.

Jam Byte Code Compiler

The Jam Byte Code Compiler version 1.0 uses literal or compressed data. Literal JBCs produce faster programming times but are slightly larger than the original ASCII Jam File (**.jam**). See Table 1. Compressed JBC Files are up to 50% smaller than the original Jam Files. Version 1.1 of the compiler will allow designers to choose between data compression for small file sizes or literal data for programming speed.

Starting with version 9.01, the MAX+PLUS® II software will generate JBC Files directly. Designers will simply specify a JBC File using the **Generate Jam or SVF File** command (File menu) in the MAX+PLUS II Programmer or Compiler. In version 9.01, designers will also use the Jam Byte Code Compiler to convert existing ASCII Jam Files into JBC File format. Further, because the Byte Code Compiler is fully architecture-independent, it can convert any vendor's Jam File into JBC format.

Table 1. Programming Times

Device	Jam File Format, *Note (1)*		Improvement
	ASCII (Seconds)	Byte Code (Seconds)	
EPM7064S	35	10	71%
EPM7128S	39	13	66%
EPM7256S	55	21	61%
EPM9320	108	35	67%
EPM9560	115	36	68%

Note:
(1) Programming times were gathered using a 200 MHz Pentium processor with a download cable and 32-bit DOS Jam Byte Code Interpreter.

Jam Byte Code Interpreter

JBCs are applied to ISP-capable devices through the Jam Byte Code Interpreter (JBI). The JBI is similar to the ASCII Jam Interpreter, using identical interface routines and porting steps. The only difference is that the JBI is roughly 30% smaller than the ASCII interpreter. The C source code for the JBI is available via the Jam web site at **http://www.jamisp.com**. Figure 1 on page 22 shows a block diagram of how JBC Files are applied to ISP-capable devices.

For existing projects, designers must apply ASCII Jam files to ISP-capable devices through the ASCII Jam Interpreter. Table 2 describes which Jam Interpreter to use with each file format.

Compatibility

Altera recommends using Jam Byte Code for all projects because it generates smaller file sizes and

Table 2. Jam Player Support

File Format	ASCII Jam Player version 1.1	Jam Byte Code Player version 1.0
Jam	✓	
JBC		✓

continued on page 22

Altera
NEWS

SameFrame Pin-outs for FineLine BGA Packaging

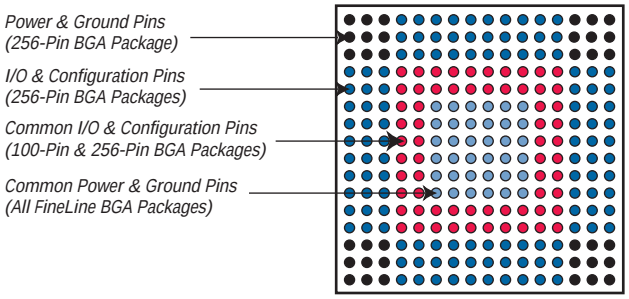
SameFrame™ pin-outs refer to the unique arrangement of solder balls on the new 1.0-mm pitch FineLine BGA™ packaging recently introduced by Altera. With SameFrame pin-outs, the balls are arranged so that FineLine BGA packages with lower ball counts form a subset of packages with higher ball counts. The SameFrame pin-out feature offers a unique level of flexibility, allowing designers to use the same printed circuit board (PCB) layout for packages with varying pin counts and for devices with different densities.

With SameFrame pin-outs, Altera has enhanced the concept of device migration, taking it from vertical to diagonal migration. Vertical migration enables designers to use the same PCB layout with devices of different densities within a common package. The SameFrame pin-out diagonal migration capability means that the same board layout can accommodate changes in both the device density and package size, bringing designers flexibility, cost savings, and faster time-to-market.

Matching Pin-outs

Figure 1 shows an example of the SameFrame pin-out for 100-pin and 256-pin FineLine BGA packages. In this simplified example, the common power and ground pins are located in the center of the packaging so that they are compatible in both the smaller 100-pin package and in the larger 256-pin package. A ring of common I/O and configuration pins surrounds the common power and ground pins, making these pins compatible in both packages. The additional power and ground pins of the larger 256-pin package are located in the four corners of the package, and the additional I/O and configuration pins are located on the four outer edges. In this way, designers can place the 100-pin package in precisely the same PCB location as the larger 256-pin package, and can be sure that the pin-outs match.

Figure 1. 100-Pin & 256-Pin BGA Pin-Out Example



SameFrame Pin-out Device Support

The SameFrame pin-out feature is supported by FLEX®□10KA, FLEX 10KE, FLEX 6000A, and MAX®□7000A devices, as shown in Table 1.

Table 1. SameFrame Pin-Out Device Support *Note (1)*

Device	100-Pin FineLine BGA	256-Pin FineLine BGA	484-Pin FineLine BGA	672-Pin FineLine BGA
EPF10K10A		✓		
EPF10K30A		✓	✓	
EPF10K50V			✓	
EPF10K30E		✓	✓	
EPF10K50E		✓	✓	
EPF10K100A			✓	
EPF10K100B		✓		
EPF10K100E		✓	✓	
EPF10K130E			✓	✓
EPF10K200E				✓
EPF10K250E				✓
EPF6010A	✓	✓		
EPF6016A	✓	✓		
EPF6024A		✓		
EPM7064A	✓			
EPM7128A	✓	✓		
EPM7256A	✓	✓		
EPM7384A		✓		
EPM7512A		✓		

Note:
(1) Devices shown in the same color support SameFrame pin-out migration capability.

continued on page 22

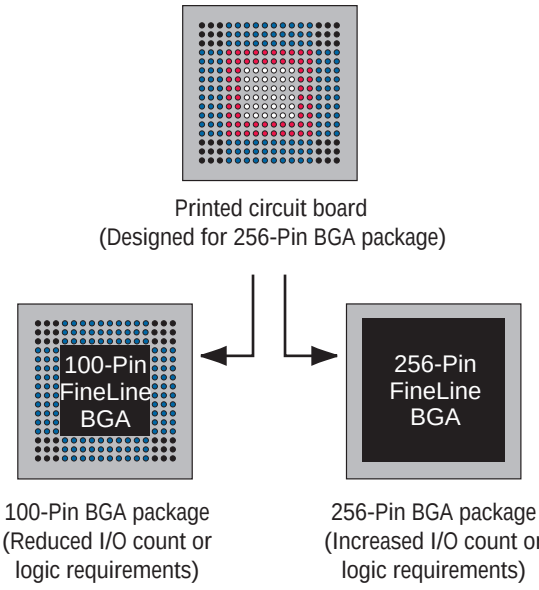
Designing for SameFrame Pin-outs

To take advantage of the SameFrame pin-outs capability of Altera devices, designers should follow two basic steps:

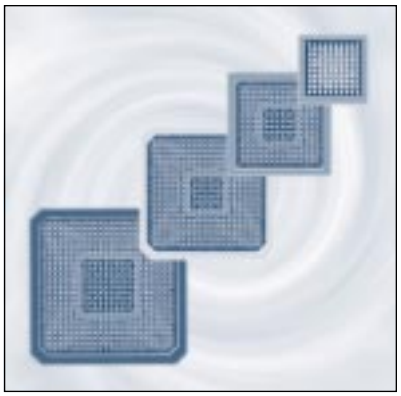
1. When creating your design, estimate the maximum pin count that is needed for your current design and any future design revisions.
2. Lay out the PCB for the package that fits this maximum pin count first, so that packages with a smaller ball count can become potential drop-in replacements.

Figure 2 illustrates a board design for a 256-pin FineLine BGA package that can accommodate either a 100-pin or 256-pin package.

Figure 2. SameFrame Pin-out Flexibility



When designing for SameFrame pin-outs, you should also consider the variance in I/O count between your current and target design. Your board design should avoid using I/O pins that will not be available in a device or package that might be used in the future.



The MAX+PLUS® II version 9.1 software simplifies the task of using only available I/O pins. Designers can select which devices they may use for future migration and the MAX+PLUS II software compiles the design using only I/O pins that are common to the different packages. Thus, by following a few simple steps, SameFrame pin-outs assure easy migration between devices.

The Altera Pin-out Advantage

The SameFrame pin-outs, combined with FineLine BGA packaging, add a new dimension of flexibility to Altera's cutting-edge devices. The SameFrame pin-out feature offers unprecedented design migration across densities and pin counts. Previously, vertical migration enabled designers to change the density of the device they wished to use and still keep the same printed circuit board, but only if they maintained the same package and pin-out. Now, with the diagonal migration capability of the SameFrame pin-outs, the device density and package size can change without creating a need for a new board layout. Because the PCB layout can be completed before the final selection of a device, the product can be brought to market in a shorter time. Costs can be cut by moving from a higher to a lower density device or from a higher to a lower pin-count package. Altera's SameFrame pin-outs offer flexibility, fast time-to-market, and cost savings.

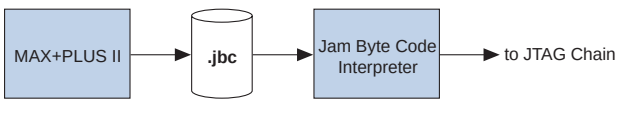
For more information on the SameFrame pin-outs, contact Altera Applications at (800) 800-EPLD or your local sales representative. For details on the FineLine BGA packaging, see "Next-Generation BGA Packaging" in the May 1998 issue of *News & Views* on Altera's web site.

Introducing Byte Code Jam, continued from page 20

faster programming times. However, Altera will continue to support ASCII Jam so that designers can program existing projects into ISP-capable devices.

For more information on Jam Byte Code and the Jam programming and test language, refer *to Application Note 88 (Using the Jam Language for ISP via an Embedded Processor)* and the *Jam Programming & Test Language Specification*.

Figure 1. JBC File Path



ACAP: Outsourcing Design & Development

When Splash Technology, Inc. of Torrance, CA wanted to increase their development capacity to supplement their peripheral component interconnect (PCI) business, they decided to look outside the company for help. The design, involving Altera® EPF10K30 programmable logic devices (PLDs), had already been completed. However, due to scheduling constraints, internal Splash resources were not available to work on the PLD simulation portion. After viewing the Altera Consultants Alliance Program (ACAP℠) listing on the Altera's web site, Splash Technology found the expertise they needed in the System Design Group (SDG) of San Diego, CA.

SDG is one of several ACAP consultants who have been successful in leveraging their expertise to meet the design requirements of Altera customers. In its short life span of nine months, the ACAP program has been able to provide customers with a new resource to accelerate their design cycle times and increase time-to-market productivity. Motorola, Hughes Network Systems, Ericsson, and Hewlett Packard are among the Altera customers that have used the expertise and design engineering services of ACAP consultants.

Today's increasing PLD densities encourage more complex designs, but complex designs usually require more expertise and design time. As device densities and system speeds increase, designs become more complex. At the same time, competitive time-to-market pressures require faster design cycles.

ACAP provides a viable solution for customers to outsource their designs and offer an alternative product development path. Before Altera certifies and recommends ACAP consultants, they receive advanced training in Altera device architec–tures and software, and are equipped with state-of-the-art design tools. Certified ACAP consultants are currently working in North America, Europe, and Asia. The qualifications of ACAP consultants and their areas of expertise are available on the Altera world-wide web site at **http://www.altera.com**. Below is a list of current ACAP consultants:

Western U.S.

- Advanced Logical Design, Inc., Saratoga, CA
- Bright Design Services, Seattle, WA
- Great River Technology, Inc., Albuquerque, NM
- HNA Engineering, Inc., Santa Clara, CA
- Innovative Configuration, Inc., Aptos, CA
- Northwest Logic Design, Beaverton, OR
- Norton Engineering Consultants, Oakland, CA
- PM Systems, San Jose, CA
- Seitz and Associates, Inc., Beaverton, OR
- Software and Systems Engineering, Inc., Tucson, AZ
- System Design Group, San Diego, CA
- Wipro Limited, Santa Clara, CA

Central U.S.

- ASIC Designs, Inc., Naperville, IL
- Design Analysis Associates, Inc., Logan, UT
- DNA Enterprises, Inc., Richardson, TX
- Eberwein & Associates, Inc., Houston, TX

Eastern U.S. & Canada

- Applied Microelectronics, Inc., Halifax, Nova Scotia, Canada
- Bolton Engineering, Inc., Melrose, MA
- Courtenay Johnson, Ontario, Canada
- DMC Manufacturing, Inc., Pennsauken, NJ
- Mettrix Technology Corporation, Hopewell Junction, NY
- Moore Labs, Hudson, MA
- Nova Electronic Design and Analysis, Corp., Ashburn, VA
- Plandscapes, Inc., Stow, MA
- Princeton Technology Group, East Windsor, NJ
- Sam Lowenstein & Associates, Vienna, VA
- Szabo Electronic Systems, Watertown, MA

Europe

- BARCO SILEX, Louvain-la-Neuve, Belgium
- Frontec ASIC Design Center, Solna, Sweden
- Ingenieurbüro für IC-Technologie, Wertheim, Germany
- Locke's Digital Developments Ltd., Dorsett, England
- ProDrive B.V., Eindhoven, The Netherlands

Asia

- Gid'el Ltd., Israel
- Wipro Limited, India

To inquire or comment about the ACAP program, please send email to **acap-info@altera.com**. To find out more about becoming an ACAP member, please send email to **acap@altera.com**.

Achieving Cost Efficiency

Altera's aim is to provide customers with programmable logic devices (PLDs) that offer the best performance, the highest density, and the lowest price. To satisfy today's design requirements, devices must offer an advanced feature set, backed by efficient design tools, widely available intellectual property, and reliable customer support and service. Nonetheless, component price remains a key factor in device selection.

FLEX 10K Architecture Maximizes Performance & Minimizes Costs

To offer the lowest prices, Altera strives to reduce its manufacturing costs. Die size and yield are factors that directly affect these costs. Because wafer prices are fixed, increasing the number of dice on a wafer lowers the cost per die. Reducing die size, however, is not enough. An increase in the number of dice per wafer is only cost-effective if these dice are usable. A small die size must be combined with high yield for maximum cost reduction. With the innovative FLEX 10K architecture, Altera is able to increase density and improve performance while minimizing die size and maximizing yield.

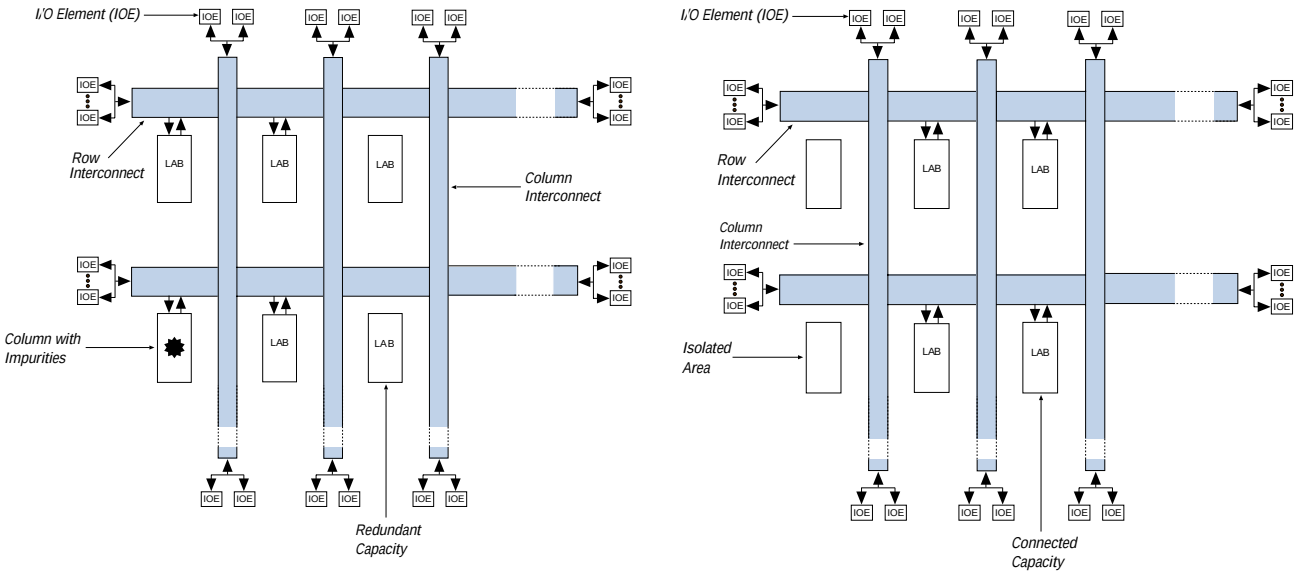
Reducing Die Size

Two features of the FLEX 10K architecture are crucial in reducing die size and increasing yield. One is the continuous hierarchical routing structure. This structure, which consists of device-wide metal lines, offers fast, predictable performance and fast compilation times. It is also a "metal friendly" structure that can be stacked to take advantage of extra metal process layers. When the 0.5-mm, 3-layer-metal process FLEX 10K devices were migrated to FLEX 10KA devices and manufactured on a 0.35-mm, 4-layer-metal process, die size was reduced significantly, not merely because of the horizontal "shrink", but also because of the added layer of metal.

Increasing Yield

The feature of the FLEX 10K device architecture that dramatically increases yield is redundancy. Redundant circuits, commonly employed in memory devices, are provided on FLEX 10K devices so that, when an impurity is found on a die, the defective area can be bypassed and a redundant circuit used in its place. Figure 1 shows how an affected die is transformed into

Figure 1. FLEX 10K Redundancy Allows Impurities to be Bypassed



a good die. The redundant circuitry can only be brought into use, however, because of the continuous interconnect structure of the FLEX 10K architecture. Together, these two features maximize yield.

Conclusion

The cost of a semiconductor is dependent on the number of dice per wafer and the die yield. By combining a continuous interconnect structure with redundancy to decrease die size and increase yield, Altera has been able to reduce device costs dramatically. These and other engineering innovations ensure that Altera's customers enjoy optimal performance and the lowest prices.

Altera continues to push down the prices of its programmable logic devices to allow customers to use programmable logic in production.

Altera at DAC 1998

The crowds around the Altera® booth at the recent Design Automation Conference (DAC) in San Francisco showed the growing popularity of Altera's solution for programmable logic designs. The Altera solution focuses on improving productivity and reducing product development cycles. Over 1,200 engineers and managers viewed Altera's presentation or participated in software and hardware demonstrations. The soccer balls used as promotional giveaways proved to be quite popular throughout the conference.

The Altera booth offered numerous demonstrations using Altera devices and tools from Altera's electronic design automation (EDA) partners. Design engineers operated the new MegaWizard™ Plug-Ins that provide user customization for megafunctions. Also featured was the first public demonstration of the Jam™ language programming devices from Altera, Cypress, Lattice, Vantis, and Xilinx all on a single board. Altera also distributed the latest ***AMPP Catalog***, which summarizes the current 85 Altera Megafunction Partners Program (AMPP℠) functions and provides a corporate profile of each AMPP partner. For a copy of the ***AMPP Catalog***, contact Altera Literature Services; up-to-date AMPP information is also available on the Altera world-wide web site at **http://www.altera.com**.

1998 ICSPAT/DSP World

The International Conference on Signal Processing Applications & Technology will be held September 13 to 16, 1998, at the Toronto Convention Center, in Toronto, Canada. Be sure to stop by and visit Altera at booth #807 to get details on the latest digital signal processing (DSP) developments at Altera. Altera® representatives will be distributing papers and will provide a three-hour product demonstration on September 13th, highlighting Reed-Solomon, Viterbi decoder, and filter solutions.

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on the Altera world-wide web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- ***Altera Digital Library CD-ROM****, version 4* (P-CD-ADL-04)
- *PCI Master/Target MegaCore Function with DMA Data Sheet (A-DS-PCI1-02)*
- *pci_b PCI Master/Target MegaCore Function Data Sheet* (A-DS-PCIB-01)
- *pcit1 PCI Target MegaCore Function Data Sheet* (A-DS-PCIT1-01.01)
- *FLEX 10KE Embedded Programmable Logic Family Data Sheet* (A-DS-F10KE-01)
- *AN 96: Performance Measurements of Typical Applications* (A-AN-096-01)
- *AN 97: Comparing Performance of High-Density PLDs* (A-AN-097-01)
- *AN 98: Comparing Performance of Common Megafunctions* (A-AN-098-01)
- *AN 99: Comparing Performance of Dual-Port Memory Functions* (A-AN-099-01)
- *AN 100: In-System Programmability Guidelines* (A-AN-100-01)
- *SB 37: 64-Bit PCI Bus Target Megafunction* (A-SB-037-01)
- *TB 48: Passing Hierarchical Timing Constraints from Synopsys Tools to MAX+PLUS II Version 9.0* (M-TB-048-01)

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for Altera devices. Algorithms are available from either Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Microsystems' BBS or with the MAX+PLUS® II software releases. Programming support for Configuration EPROM, MAX® 9000, and MAX 7000 devices is shown in the table below. All information is subject to change.

Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPC1441	✓	✓
EPM7032	✓	✓
EPM7032S	✓	✓
EPM7064	✓	✓
EPM7064S	✓	✓
EPM7096	✓	✓
EPM7128E	✓	✓
EPM7128S	✓	✓
EPM7128A	✓	✓
EPM7160E	✓	✓
EPM7192E	✓	✓
EPM7192S	✓	✓
EPM7256E	✓	✓
EPM7256S	✓	✓
EPM9320	✓	✓
EPM9320A	✓	✓
EPM9400	✓	✓
EPM9480	✓	✓
EPM9560	✓	✓
EPM9560A	✓	✓

Notes:
(1) These devices are supported by Data I/O 3900 version 5.8 and UniSite version 5.8 programmers.
(2) These devices are supported by BP Microsystems programmers version 3.34.

Current Software Version

The latest version of Altera® software is shown below:

- MAX+PLUS II version 9.01 (PC, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 platforms)

Programming Hardware Support

The following tables contain the latest programming hardware information for Altera devices. For correct programming, use the software version shown in "Current Software Version" on the previous page. See Table 1.

Table 1. Altera Programming Adapters (Part 1 of 2) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)*, EPC1064V *(2)* EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)*, EPC1213, *(2)*	DIP J-lead	PLMJ1213 PLMJ1213
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(4)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(4)* PLMR9000-240NC *(4)*
EPM7032, EPM7032V	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S, EPM7032AE	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7064S, EPM7064AE	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(4)*
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A	J-lead (84-pin) TQFP (100-pin) TQFP (144-pin)	PLMJ7000-84 PLMT7000-100NC *(4)* PLMT 7000-144NC *(4)*

Table 1. Altera Programming Adapters†(Part 2 of 2) *Note (1)*

Device	Package	Adapter
EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(4)* PLMT7000-100NC *(4)* PLMQ7128/160-160NC *(4)*
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(4)* PLMQ7128/7160-160NC *(4)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/256-160NC *(4)*
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A EPM7256S	PQFP (208-pin) RQFP (208-pin)	PLMR7256-208NC *(4)* PLMT7000-208NC *(4)*
EPM7384AE	TQFP (144-pin) PQFP (208-pin)	PLMT7000-144NC *(4)* PLMR7256-208NC *(4)*
EPM7512AE	TQFP (144-pin) PQFP (208-pin)	PLMT7000-144NC *(4)* PLMR7256-208NC *(4)*

Notes:
(1) Refer to the Altera ***1998 Data Book*** for device adapter information for MAX 5000 and Classic devices. Altera offers an adapter exchange program for 0.8-micron EPM5032, EPM5064, and EPM5130 programming adapters.
(2) FLEX 8000 Configuration EPROM.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 Configuration EPROM.
(4) These devices are not shipped in carriers.

Table 2 provides programming and configuration compatibility information for the BitBlaster™ serial port, ByteBlaster™ parallel port, and the ByteBlasterMV™ parallel port download cables.

Table 2. BitBlaster & ByteBlaster Cable Compatibility

Device	BitBlaster	ByteBlaster	ByteBlasterMV
FLEX 10K	✓	✓	✓
FLEX 10KA			✓
FLEX 10KE			✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓ *(1)*	✓ *(1)*	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A			✓

Note:
(1) This download cable is available for EPF6016 devices only.

Altera Device Selection Guide

All current information for the Altera FLEX 10K, FLEX 8000, FLEX 6000, MAX 9000, and MAX 7000 devices is listed here. Information on other Altera products is located in the Altera ***1998 Data Book***. For the most up-to-date information about Altera products, go to the Altera world-wide web site at **http://www.altera.com**. Contact Altera or your local sales office for current product availability.

FLEX 10K Devices

DEVICE[1]	GATES	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin PQFP	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-pin BGA[1], 484-pin BGA[1]	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1]	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-pin BGA	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 356-pin BGA, 484-pin BGA[1]	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 484-Pin BGA[1], 672-Pin BGA[1]	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-pin BGA[1]	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	3.3 V	-1, -2, -3	12,160	40,960
EPF10K250E	250,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[1]	2.5 V	-1, -2, -3	12,160	81,920

Note:
(1) This package is a space-saving FineLine BGA™ package.

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	5.0 V	-2, -3, -4	282	208
EPF8282AV	2,500	100-Pin TQFP	78	3.3 V	-3, -4	282	208
EPF8452A	4,000	160-Pin PQFP	120	5.0 V	-2	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	5.0 V	-3, -4	452	336
EPF8636A	6,000	208-Pin PQFP	136	5.0 V	-2	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	5.0 V	-3, -4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	112, 120, 152	5.0 V	-2	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	5.0 V	-3, -4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	5.0 V	-2, -3, -4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	5.0 V	-2, -3, -4	1,500	1,296

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	71, 81[2], 102, 139[2]	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 81[2], 117, 171, 171[2]	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218[2]	3.3 V	-1, -2, -3	1,960	1,960

Notes:
(1) This package is a space-saving FineLine BGA package.
(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-5, -7, -10
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-6, -7, -10
EPM7032	32	44-Pin PLCC/TQFP/PQFP	36	5.0 V	-6, -7, -10, -12, -15
EPM7032V	32	44-Pin PLCC/TQFP	36	3.3 V	-12, -15, -20
EPM7064AE	64	44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin BGA[1]	38, 68, 68	3.3 V	-5, -7, -10
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin PQFP/TQFP	36, 52, 68	5.0 V	-5, -6, -7, -10
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	5.0 V	-6, -7, -10, -12, -15
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	5.0 V	-7, -10, -12, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-7, -10, -12, -15, -20
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-6, -7, -10
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 104	5.0 V	-10, -12, -15, -20
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7192E	192	160-Pin PQFP/PGA	124	5.0 V	-12, -15, -20
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256S	256	208-Pin RQFP/PQFP	164	5.0 V	-7, -10, -15
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	5.0 V	-12, -15, -20
EPM7384AE	384	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -12
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -12

Note:
(1) This package is a space-saving FineLine BGA package.

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