Quartus: Altera's Fourth-Generation Development Tool

QUARTUS

With Altera's new Quartus™ software, programmable logic development tools enter the multi-million-gate era. This powerful fourth-generation software meets the challenges of designing for one-million-plus-gate devices such as the new Altera® APEX™ 20K devices. The size and complexity of APEX devices require revolutionary software and a new, innovative design methodology—one that enhances productivity. To cope with shrinking design cycles, the Quartus software offers design features never before available in programmable logic device (PLD) development tools.

State-of-the-Art Features

The Quartus software offers state-of-the-art features to enhance design productivity:

■ *Workgroup computing*—Multiple designers can work on a single project with global file management and design revision control.
■ *Integrated logic analysis functionality*—The SignalTap™ logic analyzer megafunction within the software offers system-level verification of devices running at speed, which significantly reduces verification times.
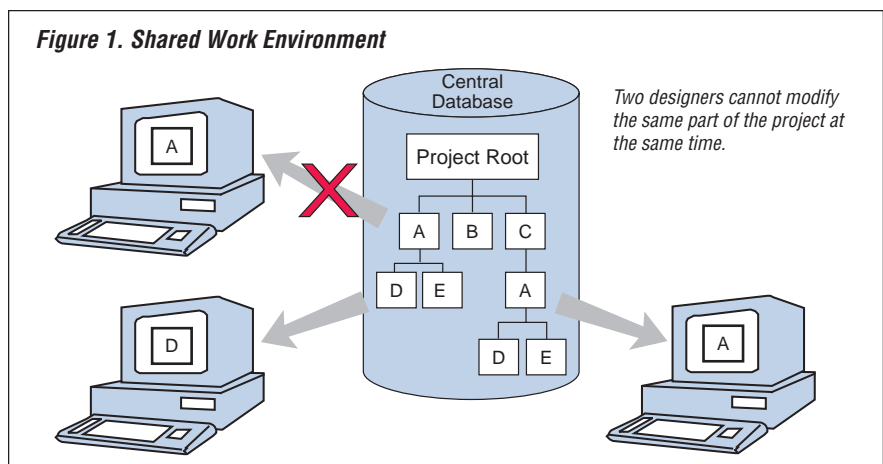■ *EDA tool integration*—The NativeLink™ interface connects the Quartus software seamlessly to and from other synthesis and design verification tools, also reducing verification times.
■ *Multi-processor support*—Computer-intensive functions are distributed to multiple processors locally, across networks, and across operating systems, reducing compilation times.
■ *Incremental recompilation*—The nSTEP™ Compiler permits fast iterations for small portions of a design, offering huge savings in compilation time.
■ *Intellectual property (IP) integration*—A block-based design orientation allows easy integration of megafunctions with OpenCore™ evaluation and MegaWizard™ Plug-In parameterization; blocks are placed to optimize timing.

Design Collaboration

Today's rapid development cycles often require several designers to work on a single product simultaneously. The Quartus software offers a centralized, object-oriented design database and global file management system (see Figure 1) that allow several computers to

Figure 1. Shared Work Environment

Central Database

Project Root

A B C

D E A

D E

Two designers cannot modify the same part of the project at the same time.

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access the same project across a network without interrupting the design cycle. The built-in revision control feature prevents more than one designer from working on any particular section of a project concurrently. The Quartus software also integrates with standard external source control software to manage each design revision.

Built-in Verification & Logic Analysis Solution

As design methodology shifts and designers use multi-million-gate devices, verification can create a bottleneck. The Quartus software includes the SignalTap logic analyzer (see Figure 2) that reduces verification time for system-level verification and simulation. This innovative logic analyzer lets designers perform hardware debugging in-system at system clock speeds.

To implement the logic analyzer, designers can specify the signals to monitor. Next, the designer compiles the project and the Quartus software inserts a logic analyzer into the design for verification purposes. After the device is configured, the designer can use the Quartus software and the logic analyzer in the device to perform system debugging.

Register transfer level-based simulation is integrated into the Quartus software. The Quartus software can accept VHDL, Verilog HDL and Tcl testbenches, and easily integrates with third-party simulators. Therefore, designers can choose the most efficient verification flow for their needs. With these enhancements to the verification process, a design can go into production much faster.

NativeLink Integration with EDA Tools

Altera has worked closely with EDA partners to develop a truly seamless interface between the Quartus software and major EDA tools, allowing tool developers access to the Quartus interface while it is still under development. The resulting NativeLink integration enables users to launch and control the Quartus software from other EDA tools, eliminating the need to learn a new design tool. More importantly, parameters can now be passed much more efficiently between EDA tools and the Quartus software. Designers can now locate errors in original hardware description language (HDL) source code instead of in an EDIF netlist.

Shortening the Design Cycle

Another revolutionary feature of the Quartus software is incremental compilation. Traditionally, designers needed to perform a full compilation of a design before they could examine the results. Full compilations are a time-consuming part of the design process, taking hours to complete for complex designs requiring multiple iterations. The Quartus nSTEP Compiler reduces the need for full compilations by allowing designers to recompile small portions of a design in minutes. Figure 3 on page 4 compares the compilation times for increasing numbers of gate changes. During this process, the nSTEP Compiler uses Altera's new CoreSyn™ synthesis capability to invoke the appropriate synthesis technology and determine the optimal mapping of a design to the device architecture. The Compiler analyzes the design and then partitions fuctions into the appropriate
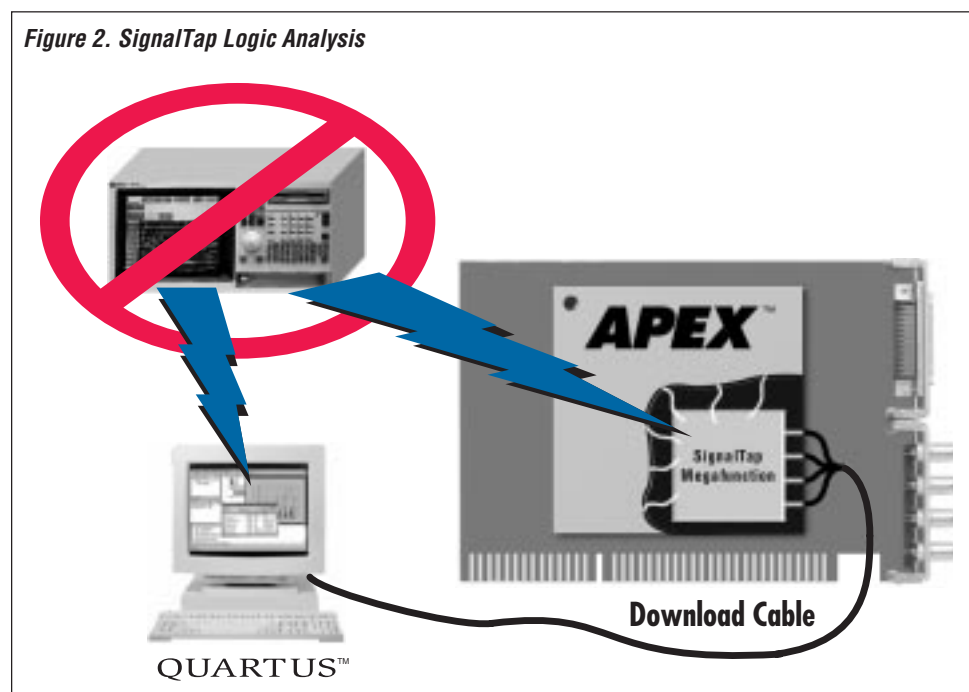
Figure 2. SignalTap Logic Analysis

QUARTUS™

Download Cable

type of look-up table (LUT)-based logic element, product-term-based macrocell, or embedded memory logic block within the APEX 20K architecture. Therefore, designers can compile, make changes, and recompile in a fraction of the time once needed.

Another feature that reduces compilation times is the support for multiprocessor computing. The Quartus software is optimized with multi-threading links to take advantage of multiple processors, which can be located on one computer or across a network and run on homogeneous (e.g., Solaris 2.5) or heterogeneous (e.g., Windows NT 4.0 and Solaris 2.5) operating systems. The fitting of each row in a device can be designed on a different processor. Utilizing multiple processors harnesses a great deal of computing power and considerably reduces compilation times.

Enhanced Support for IP

The Quartus software supports state-of-the-art system-level methodology with block-level editing and enhanced support for megafunctions. Using high-level definitions of functional blocks and reusable functions gives designers more time to focus on behavioral verification.

Utilizing megafunctions that are tested and optimized for a particular architecture also helps to reduce design

time. Altera offers MegaCore™ and Altera Megafunction Partners Program (AMPP℠) megafunctions, both of which can be evaluated risk-free with the OpenCore™ feature. The Quartus software expands Altera's support for megafunctions by enabling file-specific assignments and giving greater control over synthesis. Designers can maintain assignments for each instance of a MegaCore or AMPP megafunction in a design rather than for each function.

Web-Enabled Design Tool

The Quartus software is "web-aware," with the latest Internet browser technology built in. From within the software, designers have direct access over the Internet to the Altera Technical Support (Atlas℠) Solutions database to find immediate solutions for common design problems. For more specific issues, designers can submit service requests on-line directly to Altera Applications, attaching their design files to the request so that the Altera engineer assigned to the issue can accurately duplicate the design environment and find a solution.

Many basic support issues are handled automatically by the Quartus software. Notifications of software patches, new device support, and on-line help updates will be sent out when they are available. Registered designers can even choose to let the Quartus software update their registered design sites automatically.
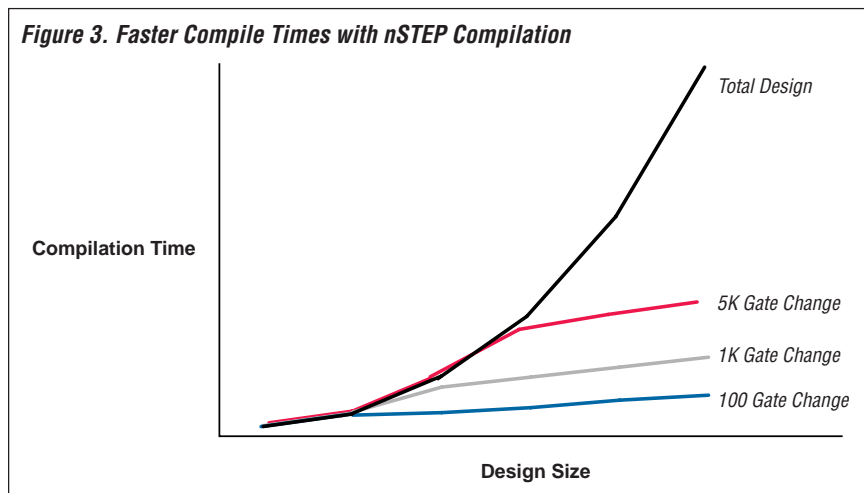
Conclusion

Altera's Quartus software is the development tool for the multi-million-gate era. Its powerful, innovative features allow designers to realize the full potential of the latest devices while shortening design time and increasing productivity. By using the revolutionary APEX 20K devices together with the unmatched Quartus software, design teams can find the ideal solution for the multi-million-gate design challenge.

Figure 3. Faster Compile Times with nSTEP Compilation

Devices & TOOLS

FLEX Update

EPF10K50E Devices Now Available

EPF10K50E devices are the first "enhanced" devices from the FLEX® 10KE family, featuring dual-port RAM with independent read/write ports. EPF10K50E devices are manufactured on a fully optimized 0.25-µm, 5-layer-metal SRAM process. With a 2.5-V core, the devices use 66% less power versus comparable 3.3-V field-programmable gate arrays (FPGAs). EPF10K50E devices also offer high performance, with a 16-tap, 8-bit finite impulse response (FIR) filter performance of 140 MHz. This is 84% faster than competing 3.3-V devices. Additionally, the MultiVolt™ I/O feature enables EPF10K50E devices to interface with 2.5-V, 3.3-V, or 5.0-V devices. EPF10K50E devices are available in 144-pin thin quad flat pack (TQFP), 208-pin plastic quad flat pack (PQFP), 240-pin PQFP, 256-pin FineLine BGA™, and 484-pin FineLine BGA packages.

Fast EPF10K50E Devices with 8.5-ns t_{DRR} Available Today

The EPF10K50E devices perform much faster than initially specified. The t_{DRR} specification, which measures register to register delay, is 8.5 ns for the fastest -1 speed grade. Updated timing models will be provided in the MAX+PLUS® II version 9.1 software. The -2 and -3 speed grade devices also have improved performance of 10.0 ns and 13.5 ns respectively.

PLL Feature in FLEX 10KE Devices

FLEX 10KE devices with phase-locked loops (PLLs) will offer the ClockLock™ and ClockBoost™ options to reduce clock delay and skew, and to perform clock multiplication. The PLL option will be offered in -1 and -2 speed grade FLEX 10KE devices for all device densities and packages (except the 599-pin pin-grid array (PGA) package used for prototyping). Devices with PLLs will have a "-X" suffix (e.g., EPF10K200EBC600-1X). The first FLEX 10KE devices with PLLs, the EPF10K200E devices, will be available in January 1999. Software support for the PLL circuitry is planned for the MAX+PLUS II version 9.2 software, which is expected to be released in January 1999.

FineLine BGA Packages for FLEX 10K Devices Now Available

Altera® is now shipping EPF10K100B devices in 256-pin FineLine BGA packages and EPF10K30A devices in 484-pin FineLine BGA packages. Altera's small die sizes allow the use of state-of-the-art FineLine BGA packaging to help designers reduce costly board space. The 256-pin FineLine BGA package uses only 17×17 mm^2 of board space—the same amount of space consumed by a 100-pin TQFP package. Altera will offer FineLine BGA packages for all FLEX 10KE devices as well for the EPF10K10A, EPF10K50V, and EPF10K100A devices.

Table 1 shows the expected availability of FLEX 10KE devices.

Table 1. FLEX 10KE Introduction Schedule			
Device	Package	Speed Grade	Availability
EPF10K30E	144-pin TQFP	-1, -2, -3	Q2 1999
	208-pin PQFP	-1, -2, -3	Q2 1999
	256-pin FineLine BGA	-1, -2, -3	Q2 1999
	484-pin FineLine BGA	-1, -2, -3	Q2 1999
EPF10K50E	144-pin TQFP	-1, -2, -3	Now
	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FineLine BGA	-1, -2, -3	December 1998
	484-pin FineLine BGA	-1, -2, -3	December 1998
EPF10K100B	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FineLine BGA	-1, -2, -3	November 1998
EPF10K100E	208-pin PQFP	-1, -2, -3	Q2 1999
	240-pin PQFP	-1, -2, -3	March 1999
	256-pin FineLine BGA	-1, -2, -3	Q2 1999
	356-pin BGA	-1, -2, -3	Q2 1999
	484-pin FineLine BGA	-1, -2, -3	Q2 1999
EPF10K130E	240-pin PQFP	-1, -2, -3	March 1999
	484-pin FineLine BGA	-1, -2, -3	Q2 1999
	672-pin FineLine BGA	-1, -2, -3	Q2 1999
EPF10K200E	599-pin PGA	-1, -2, -3	December 1998
	600-pin BGA	-1, -2, -3	December 1998
	672-pin FineLine BGA	-1, -2, -3	January 1999
EPF10K250E	599-pin PGA	-1, -2, -3	Q2 1999
	672-pin FineLine BGA	-1, -2, -3	Q2 1999

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Table 2 shows the expected availability of FLEX 10KA devices.

Notifications page on the Altera web site at **http://www.altera.com**.

Table 2. FLEX 10KA Introduction Schedule			
Device	**Package**	**Speed Grade**	**Availability**
EPF10K10A	100-pin TQFP	-1,-2,-3	Now
	144-pin TQFP	-1,-2,-3	Now
	208-pin PQFP	-1,-2,-3	Now
	256-pin FineLine BGA	-1,-2,-3	December 1998
EPF10K30A	144-pin TQFP	-1,-2,-3	Now
	208-pin PQFP	-1,-2,-3	Now
	240-pin PQFP	-1,-2,-3	Now
	256-pin FineLine BGA	-1,-2,-3	December 1998
	356-pin BGA	-1,-2,-3	November 1998
	484-pin FineLine BGA	-1,-2,-3	Now
EPF10K50V	240-pin PQFP	-1,-2,-3	November 1998
	240-pin RQFP, *(1)*	-1,-2,-3,-4	Now
	356-pin BGA	-1,-2,-3,-4	Now
	484-pin FineLine BGA	-1,-2,-3	Q1 1999
EPF10K100A	240-pin RQFP	-1,-2,-3	Now
	356-pin BGA	-1,-2,-3	Now
	484-pin FineLine BGA	-1,-2,-3	November 1998
	600-pin BGA	-1,-2,-3	Now
EPF10K130V	599-pin PGA	-2,-3,-4	Now
	600-pin BGA	-2,-3,-4	Now
EPF10K250A	599-pin PGA	-1,-2,-3	Now
	600-pin BGA	-1,-2,-3	Now

Note:
(1)   RQFP: power quad flat pack.

FLEX 10KA Product Transitions

Altera is moving EPF10K50V, EPF10K100A, EPF10K30A, and EPF10K10A devices from a 0.35-μm process to a 0.3-μm process. Table 3 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer

Table 3. FLEX 10KA Migration Schedule			
Device	**Transition Date**	**Reference**	**Process (μm)**
EPF10K50V	December 1998	PCN 9810	0.30
EPF10K100A	February 1999	PCN 9810	0.30
EPF10K30A	Q2 1999	PCN 9810	0.30
EPF10K10A	Q2 1999	PCN 9810	0.30

3.3-V FLEX 6000 Devices Shipping

All 3.3-V FLEX 6000 devices are now shipping. These devices deliver high performance at prices directly comparable to gate arrays. The EPF6010A, EPF6016A, and EPF6024A devices are offered in three speed grades, including a high-performance -1 speed grade. Software support for -1 speed grade devices is available in MAX+PLUS II version 9.01 and higher. Table 4 shows the features of the FLEX 6000 family.

Table 4. FLEX 6000 Device Features				
Feature	**EPF6010A**	**EPF6016**	**EPF6016A**	**EPF6024A**
Process Geometry	0.35 μm	0.5 μm	0.35 μm	0.35 μm
Supply Voltage	3.3 V	5.0 V	3.3 V	3.3 V
Logic Elements	880	1,320	1,320	1,960
Gate Count	5,000 – 10,000	8,000 – 16,000	8,000 – 16,000	12,000 – 24,000
Maximum User I/O Pins	139	204	171	218

FLEX 6000 devices in the FineLine BGA packages are expected to be available in the second quarter of 1999. These area-efficient packages require less than half the board space of traditional ball-grid array (BGA) packages. Table 5 shows FLEX 6000 device expected availability.

Table 5. FLEX 6000 Device Availability							
Device	**100-Pin TQFP**	**100-Pin FineLine BGA**	**144-Pin TQFP**	**208-Pin PQFP**	**240-Pin PQFP**	**256-Pin BGA**	**256-Pin FineLine BGA**
EPF6010A	✓	Q2 1999	✓				Q2 1999
EPF6016			✓	✓	✓	✓	
EPF6016A	✓	Q2 1999	✓	✓			Q2 1999
EPF6024A			✓	✓	✓	✓	Q2 1999

Configuration EPROM Family

EPC2 Reprogrammable Configuration EPROM Introduced

The EPC2, Altera's first reprogrammable Configuration EPROM, is now shipping. This device, which is offered in 20-pin plastic J-lead chip carrier (PLCC) and 32-pin TQFP packages, is pin-compatible with all existing Altera Configuration EPROMs in the same packages. A single EPC2 can configure any FLEX device with up to 130,000 gates and can be programmed in-system using IEEE Std. 1149.1 Joint Test Action Group (JTAG) test ports. The EPC2 operates at 3.3 V or 5.0 V.

Configuration EPROM Product Transitions

Altera is migrating EPC1213 and EPC1064 devices from a 0.8-μm process to a 0.65-μm process. Table 1 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com**.

Table 1. Configuration EPROM Migration Schedule

Device	Transition Date	Reference	Process (μm)
EPC1213	December 1998	PCN 9802, ADV 9812	0.65
EPC1064	December 1998	PCN 9802, ADV 9812	0.65

MAX Update

MAX 9000A Device Availability

With propagation delays as fast as 10 ns, MAX® 9000A devices offer significant performance enhancements. All packages of the EPM9320A and EPM9560A devices are available in production quantities. Table 1 summarizes the commercial- and industrial-temperature grade MAX 9000A devices currently available.

Table 1. MAX 9000A Device Availability   Note (1)

Device	t_PD	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	356-Pin BGA
EPM9320A	10 ns	C, I	C, I		C
EPM9560A	10 ns		C, I	C, I	C

Note:
(1) A "C" designates commercial- and " I" designates industrial-temperature device availability.

MAX 7000A Availability

Four 3.3-V MAX 7000A devices—the EPM7064AE, EPM7128A, EPM7256A, and EPM7512AE devices—are now shipping. MAX 7000A devices offer in-system programmability (ISP), MultiVolt I/O pins, pin-compatibility with existing industry-standard MAX 7000 devices, and propagation delays as fast as 5.0 ns. Table 2 shows MAX 7000A device expected availability.

Table 2. MAX 7000A Device Availability

Device	Package	Speed Grade	Availability
EPM7032AE	44-pin PLCC	-5, -7, -10	Q1 1999
	44-pin TQFP	-5, -7, -10	
EPM7064AE	44-pin PLCC	-5, -7, -10	Now
	44-pin TQFP	-5, -7, -10	
	84-pin PLCC	-5, -7, -10	
	100-pin TQFP	-5, -7, -10	
EPM7128A	84-pin PLCC	-6, -7, -10, -12	Now
	100-pin TQFP	-6, -7, -10, -12	
	100-pin BGA	-6, -7, -10, -12	
	144-pin TQFP	-6, -7, -10, -12	
	256-pin FineLine BGA	-6, -7, -10, -12	
EPM7128AE	84-pin PLCC	-5, -7, -10, -12	Q1 1999
	100-pin TQFP	-5, -7, -10, -12	
	100-pin BGA	-5, -7, -10, -12	
	144-pin TQFP	-5, -7, -10, -12	
	256-pin FineLine BGA	-5, -7, -10, -12	
EPM7256A	100-pin TQFP	-7, -10, -12	Now
	144-pin TQFP	-7, -10, -12	
	208-pin PQFP	-7, -10, -12	
	256-pin FineLine BGA	-7, -10, -12	
EPM7256AE	100-pin TQFP	-6, -7, -10, -12	Q2 1999
	100-pin FineLine BGA	-6, -7, -10, -12	
	144-pin TQFP	-6, -7, -10, -12	
	208-pin PQFP	-6, -7, -10, -12	
	256-pin FineLine BGA	-6, -7, -10, -12	
EPM7384AE	144-pin TQFP	-7, -10, -12	Q1 1999
	208-pin PQFP	-7, -10, -12	
	256-pin FineLine BGA	-7, -10, -12	
EPM7512AE	144-pin TQFP	-7, -10, -12	Now
	208-pin PQFP	-7, -10, -12	
	256-pin FineLine BGA	-7, -10, -12	

MAX 7000 & MAX 9000 Product Transitions

The migration of MAX 7000 and MAX 9000 devices from a 0.65-μm process to a 0.5-μm process has been completed. Table 3 on page 8 outlines the device

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migrations and lists the associated reference documentation. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com**.

Table 3. MAX 7000 & MAX 9000 Process Migrations Note (1)	
Device	**Reference Documentation**, *(2)*
EPM7032	PCN 9703
	ADV 9803
EPM7064	PCN 9703
EPM7064S	ADV 9708
EPM7128E	PCN 9703
EPM7128S	ADV 9708
EPM7160E	PCN 9703
	ADV 9803
EPM7192E	PCN 9703
EPM7192S	ADV 9708
EPM7256S	PCN 9703
EPM7256E	ADV 9708
EPM9320	PCN 9703
	ADV 9803
EPM9560	PCN 9703
	ADV 9803

Notes:
(1)   The process transition will not result in any changes to data sheet parameters or ordering codes.
(2)   Altera provides advisories and process change notices. Go to the Altera web site at **http://www.altera.com** for these reference documents.

MAX 7000S Family Update

All MAX 7000S devices are now available. These devices offer features such as -5 ns speed grades, ISP, an open-drain output option, and IEEE Std. 1149.1 boundary-scan test (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in commercial and industrial temperature grades. See Table 4.

Table 4. MAX 7000S Device Packages			
Device	**Package**	**Speed Grade**	
		Commercial	**Industrial**
EPM7032S	44-pin PLCC	-5, -6, -7, -10	-7
	44-pin TQFP	-5, -6, -7, -10	-7
EPM7064S	44-pin PLCC	-5, -6, -7, -10	-7
	44-pin TQFP	-5, -6, -7, -10	-7
	84-pin PLCC	-5, -6, -7, -10	-7
	100-pin TQFP	-5, -6, -7, -10	-7
EPM7128S	84-pin PLCC	-6, -7, -10, -15	-10
	100-pin TQFP	-6, -7, -10, -15	-10
	100-pin PQFP	-6, -7, -10, -15	-10
	160-pin PQFP	-6, -7, -10, -15	-10
EPM7160S	84-pin PLCC	-6, -7, -10	-10
	100-pin TQFP	-6, -7, -10	-10
	160-pin PQFP	-6, -7, -10	-10
EPM7192S	160-pin PQFP	-7, -10, -15	-10
EPM7256S	208-pin PQFP	-7, -10, -15	-10

Tools Update

Introducing the Altera Subscription Program

Altera now offers a new way for you to keep up with the latest upgrades and tool releases. With the Altera Subscription Program, you receive updates for all Altera software (including both the MAX+PLUS II and Quartus™ software) for 12 months.

Whether you are a new user of Altera software or have an existing subscription, you can receive all MAX+PLUS II and Quartus software releases and updates for $2,000 per year. To receive the same support under the old Altera maintenance program, you had to purchase a PLS-MAGNUM ($4,995) plus one year of software maintenance ($1,495). The new program provides a significant cost reduction and also includes updates for the Quartus software. At the end of your current 12 month subscription, you must purchase a renewal in order to receive uninterrupted support.

Benefits

The Altera Subscription Program provides the following benefits:

■   You receive both the MAX+PLUS II and Quartus software. MAX+PLUS II updates will be sent to you immediately upon release and the Quartus software will be sent to you when it is released in 1999.
■   You receive the full-featured development system. Altera will no longer offer base products and migration products. For $2,000, individual (fixed-node) users can use all MAX+PLUS II and Quartus products for a 12-month period.

■ Your ordering process is simplified. With the new program, you order one product and receive all development tools and updates for the duration of the subscription.

If you have a current software maintenance agreement, you must purchase a subscription to receive the Quartus software when it is available. You will also receive Quartus and MAX+PLUS II upgrades for the duration of your subscription.

Table 1 provides descriptions for the Altera Subscription Program options. For more information on the Altera Subscription Program, contact your local Altera sales office.

Table 1. Altera Subscription Program Product Line		
Product	**Description of Coverage**	**List Price**
FIXEDPC	PCs using software guards	$2,000
FLOATPC	Networked environment consisting of PC clients only	$2,200
FLOATNET	Networked environment consisting of PC, UNIX, or a combination of clients	$2,400
RENEWAL	Renew existing subscription program for additional 12 month period	$2,000
ADD-FLOATPC	Additional seats to add on to FLOAT-PC product	$1,700
ADD-FLOATNET	Additional seats to add on to FLOAT-NET product	$1,800

Quartus SignalTap Logic Analysis

The recently announced that the Quartus programmable logic development system contains a new capability called SignalTap™ logic analysis. SignalTap analysis reduces verification times because engineers can check internal chip signal values while the system is running at speed.

SignalTap logic analysis consists of the SignalTap megafunction, the interface software, and a communications cable. To use this new capability, simply select the signals that you wish to observe and set trigger points. The SignalTap megafunction is inserted transparently into your design and compiled. The SignalTap megafunction acts as an embedded logic analyzer, capturing data at specified trigger points and storing the data in the embedded memory of APEX™ 20K embedded system blocks. This data is

then sent to the IEEE Std. 1149.1 port of an APEX 20K device, uploaded through the communications cable, and displayed in the Quartus waveform editor.

New ES Site Licensing Methodology in MAX+PLUS II Version 9.1

The ES Site License provides you with an entry-level version of the MAX+PLUS II software. Traditionally, the ES Site License was enabled with an authorization code; when you purchased a copy of the MAX+PLUS II software, you could install unlimited copies of the ES Site License version of the MAX+PLUS II software. However, starting with MAX+PLUS II version 9.1, you must enable the ES Site License version using a license file. This license file is based on the hard disk serial number of your PC, and the license is valid for six months. The new licensing method ensures Year 2000-compliance for the ES Site License software.

To obtain a license file, go to the Altera web site at **http://www.altera.com**. Your license file will be sent to you via e-mail. If you wish to continue to use pre-9.1 versions of the MAX+PLUS II software, use your existing authorization code.

Year 2000 Compliance

The MAX+PLUS II version 9.1 software is Year 2000-compliant per DISC PD-2000-1, *A Definition of Year 2000 Conformity Requirements*, published by the British Standards Institute. If you have a current software maintenance agreement with Altera, you should have received the software update automatically.

Altera cannot guarantee that pre-9.1 versions of the MAX+PLUS II software are Year 2000-compliant, or that such versions will continue to function properly at Year 2000.

Altera's Year 2000 Readiness Disclosure and other information on the Altera Year 2000 Compliance Program can be found on the Altera web site at **http://www.altera.com/html/new/yr2k.html**.

MAX+PLUS II Version 9.1 Licensing

Altera has begun shipping the MAX+PLUS II version 9.1 software to all customers who have a current software maintenance agreement. This new version is Year 2000-compliant and features GLOBEtrotter's latest FLEXlm license management software. To use the MAX+PLUS II version 9.1

Technical
A R T I C L E S

PLLs in FLEX 10KE Devices

FLEX® 10KE devices include the ClockLock™ and ClockBoost™ features that were introduced with the first FLEX 10K devices. The ClockLock circuitry includes a phase-locked loop (PLL) to minimize clock skew and delay within a device, significantly increasing performance. The ClockBoost feature uses a PLL to implement internal clocks that operate at twice the frequency of the system clock. Designers can create new applications because of the faster clock speeds. These enhancements can provide significant breakthroughs in system performance and bandwidth.

PLL Functionality

FLEX 10KE devices use a PLL to minimize clock skew and delay. The PLL circuitry contains the following elements:

- *Phase comparator*—Monitors the difference between the incoming clock and delayed feedback clock and adjusts the voltage-controlled oscillator (VCO) according to the phase difference between the two clocks.
- *Locked clock*—Distributed to the device as an output signal from the VCO.
- *Delay element*—Models the clock delay to the register.
- *Frequency divider*—Used to create the multiplied clock output. A PLL with a divide-by-two frequency divider forces the output locked clock to be twice the frequency of the input clock. The phase comparator adjusts the VCO so that the feedback clock is the same as the input clock.

Figure 1 illustrates the functional block diagram of the PLL circuitry.

Faster System Performance

As programmable logic devices (PLDs) increase in density, clock skew and delay increase as well, which leads to a greater impact on performance. To avoid hold time issues, delay is added into the data path. This delay can increase setup times (t_{SU}) under worst-case conditions. The easy-to-use ClockLock feature reduces the clock skew and delay in PLDs, significantly improving performance. Figure 2 shows how the ClockLock feature eliminates clock skew and delay,

resulting in increased I/O performance. This performance increase helps designers meet the high-speed bus interface requirements of the future. Table 1 on page 11 shows the I/O performance for -1 speed grade EPF10K200E devices using the ClockLock feature.

Increased System Bandwidth & Reduced Area

The ClockBoost circuitry in FLEX 10KE devices provides clock multiplication. Popularly used in microprocessors, clock multiplier circuits allow an external clock frequency to be "multiplied" inside the device. The ClockBoost feature allows designers to run the internal logic twice as fast as the input clock frequency, doubling the datapath bandwidth. The ClockBoost feature is useful in memory (DRAM, SDRAM,

Figure 1. Phase-Locked Loops (PLLs)

A PLL maintains a phase delay between an input clock and an internal oscillator. Dividing the feedback signal can provide clock multiplication.
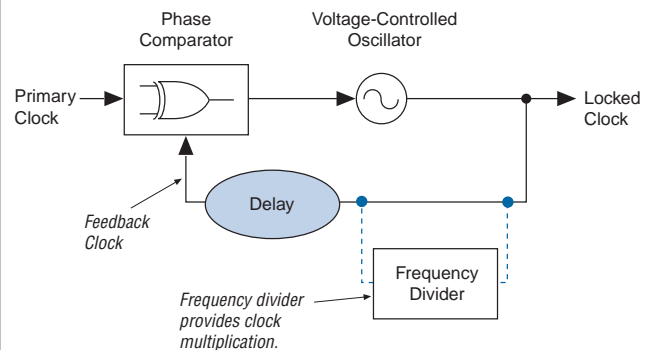

Figure 2. ClockLock Feature

The ClockLock feature improves clock-to-output times by 21% because clock delay and skew are eliminated.
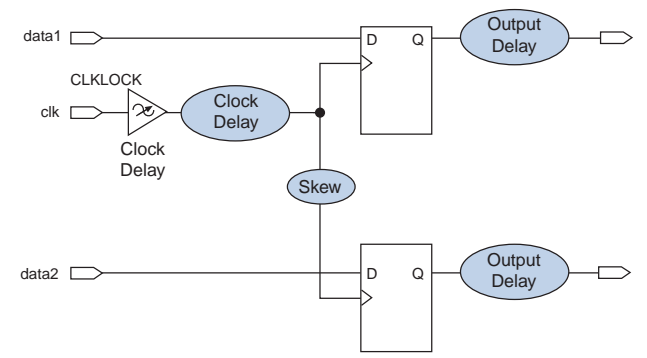
Table 1. EPF10K200E-1 Device I/O Performance

Parameter	Performance		Percentage Improvement
	Without the PLL	With the PLL	
t_{SU}	3.1 ns	2.1 ns	32%
t_{CO}	4.7 ns	3.7 ns	21%

asynchronous SRAM) controllers, time-domain multiplexing (TDM), 2× clock state machines, sampling asynchronous inputs, gated clock applications, digital signal processing (DSP) designs, data compression algorithms, and other applications where complex data manipulation is performed at very high speeds.

Using TDM, the ClockBoost feature allows the designer to enhance device area efficiency via resource sharing within the device. For example, a design that requires a 64-bit datapath function running at 50 MHz can be implemented with a 32-bit datapath function running internally at 100 MHz, achieving the same functionality with nearly half the logic resources and I/O require-ments. Figure 3 shows an example of a TDM design.

Software Support

The MAX+PLUS® II version 9.1 software supports both the ClockLock and ClockBoost features for FLEX 10KE devices. To enable the ClockLock or ClockBoost circuitry, designers use a MAX+PLUS II megafunction called CLKLOCK. The CLKLOCK function has parameters for input clock frequency and the clock doubling option. After design compilation, the designer can use the MAX+PLUS II software for

functional and timing simulation as well as timing analysis. Electronic design automation (EDA) support for the ClockLock and ClockBoost circuitry is available through Verilog HDL and VHDL models.

Availability

The EPF10K200E device (planned for release in January 1999) will be the first FLEX 10KE device to incorporate the ClockLock and ClockBoost options. Each FLEX 10KE device family member will be available with the optional ClockLock and ClockBoost features in 1999. Devices with the ClockLock feature have a "-X" suffix. The EPF10K200E ordering codes are: EPF10K200EFC672-1X, EPF10K200EFC672-2X, EPF10K200EBC600-1X, and EPF10K200EBC600-2X.

Figure 3. ClockBoost Feature

A clock multiplier increases the bandwidth of the data path without increasing the board-level clock speed.
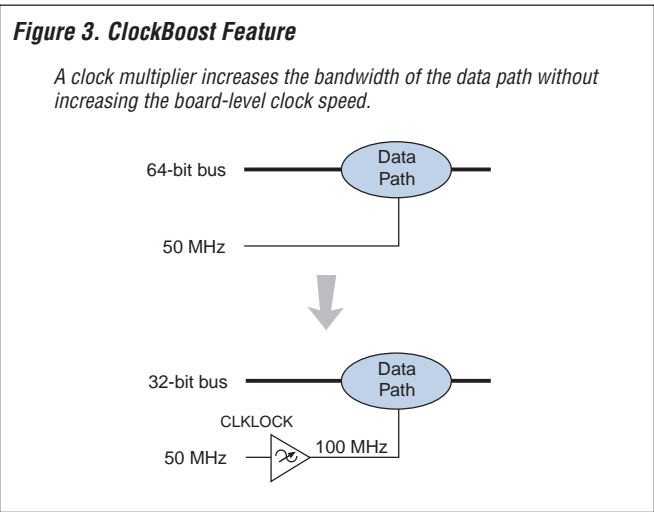
software, you will need to use a new license file for both PCs and UNIX workstations.

If you have a current software maintenance agreement, you should have received the license file required to enable the MAX+PLUS II version 9.1 software from Altera in November 1998. If you did not receive the file, you can obtain it from the web-based license generator on Altera's web site at **http://www.altera.com**. You must have a current software maintenance agreement to use the latest version of the MAX+PLUS II software.

Beginning with the MAX+PLUS II version 9.1 software, only users with a current software maintenance

agreement will be able to use the features of each new release. If you do not have a maintenance agreement, you can continue to use your existing version of MAX+PLUS II software.

When you obtain your new license file, it enables the MAX+PLUS II software for the length of time remaining in your maintenance agreement. Whenever you renew your maintenance contract, you must obtain and install a new license file.

For more information on the new licensing program, contact your local Altera representative.

Using Altera's 1.00-mm FineLine BGA Packages

Altera has taken a leadership position in programmable logic device (PLD) packaging with the recent introduction of 1.00-mm FineLine BGA™ packages. These packages optimize the area on a printed circuit board (PCB) while maintaining a very high pin count.

Overview

When using ball-grid array (BGA) packages, the challenge is to route all signals to the system board without increasing PCB complexity and cost. Because I/O connections are made through a matrix of solder balls across the bottom of the package, less room is available on the PCB for escape routing—the method used to route each signal from a package to another element on the PCB. This challenge is met through the use of a multi-layer PCB. Signals are routed from the inner balls of the BGA package to various elements on the PCB through vias (plated through-holes), which provide electrical connections between various PCB layers. To use 1.00-mm FineLine BGA packages, ensure that your PCB has enough room for vias and escape routing.

Vias

To see if enough space is available on your PCB for vias, you must determine:

- The size of surface land pads
- The size and layout of via capture pads

The surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and escape routing, which both occupy the area between the land pads. Altera recommends using a 17.72-mil surface land pad, which is the same size as the solder pad on the BGA package. Using similarly-sized pads minimizes the stress on the solder joints. Figure 1 shows how much space is available for vias and escape routing when using 17.72-mil surface land pads.

Vias are electrically connected to PCB layers through via capture pads, which also affect the amount of space available for vias and escape routing. Via capture pads can be laid out either in line with the surface land pads or in the diagonal (see Figure 2 on page 13).

The decision to place a via capture pad diagonally or in-line with the surface land pads is based on the following criteria:

- Diameter of the via capture pad
- Trace width and length
- Clearance between the via capture pad and the surface land pad

To determine whether enough room is available to place via capture pads in-line with the surface land pads, use the following formula:

$$a + c + d \leq 21.653 \text{ mils}$$

To determine if enough room is available to place via capture pads in the diagonal of the surface land pads, use the following formula:

$$a + c + d \leq 37.961 \text{ mils}$$

If your PCB guidelines do not conform to either equation, contact Altera® Applications for further assistance.

Figure 1. PCB Pad Layout

All dimensions are shown in mils. Millimeter measurements are shown in parentheses.

Surface Land Pads
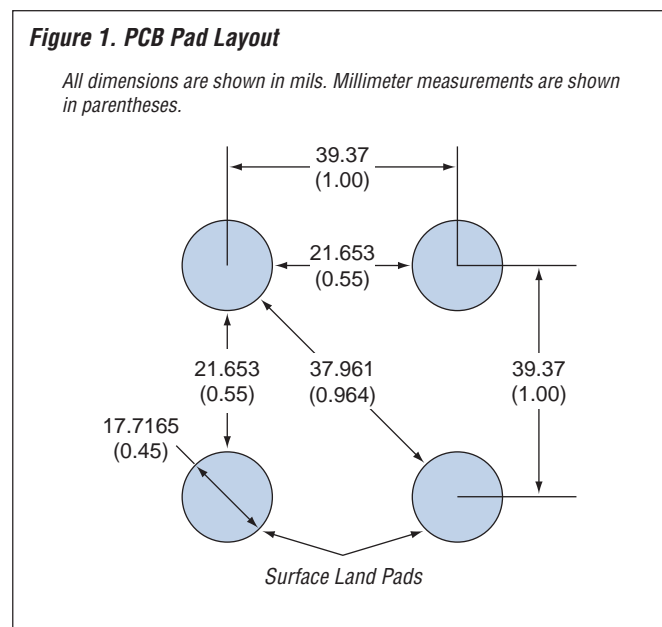
Escape Routing

To perform escape routing, you must determine the width of the trace and the minimum space required between traces. The minimum area for signal routing is the smallest area the signal must be routed through (i.e., the distance between two vias, or g in Figure 2). This area is calculated with the following formula:

g = 39.37 mils – d

The number of traces that can be routed through this area is based on the permitted line trace and space widths. For example, if the permitted line trace width is 4 mils and the space width is also 4 mils, the total area required is 12 mils (i.e., space + trace + space). If g is 12 mils or greater, it is possible to route one trace. If g is less than 12 mils, you may not be able to use the 1.00-mm FineLine BGA package. Each PCB vendor has its own specifications for via size, trace, and space

widths. Depending on these specifications, your escape routing can incorporate various number of traces between pads. Contact your PCB vendor for that company's specifications.

Table 1 shows how to determine the total number of traces that can be routed in area g. In general, the number of traces is inversely proportional to the number of PCB layers required to route the package.

For more information on FineLine BGA packages, see the *Using Altera's 1.00-mm FineLine BGA Packages White Paper* on the Altera web site.

Table 1. Number of Traces Routed through g

Number of Traces	Formula
1	$g \geq [2 \times f] + e$
2	$g \geq [3 \times f] + [2 \times e]$
3	$g \geq [5 \times f] + [3 \times e]$

Figure 2. Placement of Via Capture Pad

All dimensions are shown in mils. Millimeter measurements are shown in parentheses.

☐ Surface land pad
■ Via capture pad
▨ Vias
▨ Trace

a Trace length
b Trace width
c Clearance between via capture pad and surface land pad
d Via capture pad size
e Trace width
f Space width
g Area for escape routing (This area is on a different PCB layer than the surface land pads.)
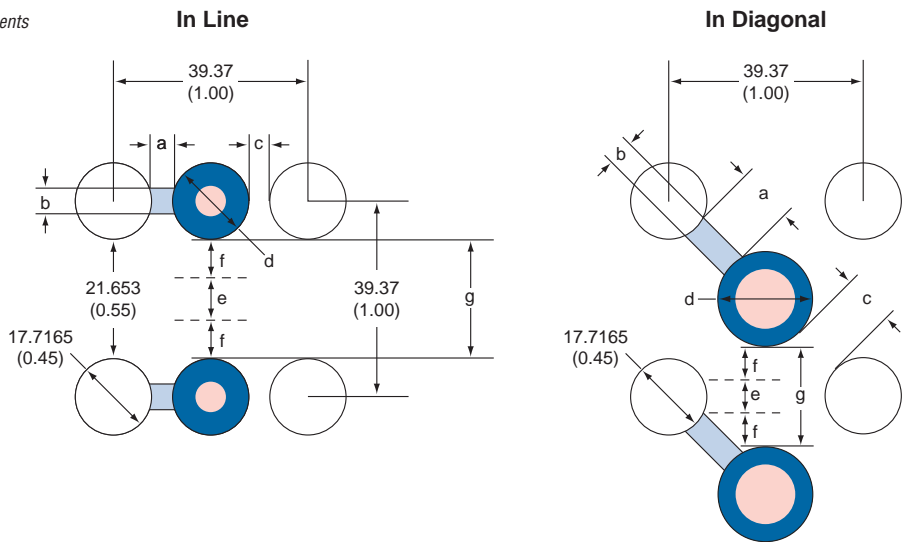
New Classes Offered by the Altera Technical Training Program

In today's competitive marketplace, it is necessary to use resources more effectively, increase productivity, accelerate product development, and get to market faster. As system requirements become more demanding and product life-cycles become shorter, companies realize that thorough training is essential to meet these goals. The Altera Technical Training Program provides you with the knowledge you need to maintain a competitive edge.

The following new classes are offered by the Altera Technical Training Program:

- Achieving High Performance & Optimal Utilization in FLEX® 10K Devices
- Achieving High Performance & Optimal Utilization in FLEX 6000 & FLEX 8000 Devices
- Optimizing Designs for MAX® 9000 Devices
- Optimizing Designs for MAX 7000 Devices

Using Parameterized Dual-Port RAM in FLEX 10KE Devices

Dual-port RAM provides added functionality to embedded array blocks (EABs) within Altera® FLEX® 10KE devices. Designers have the ability to use separate clocks for EAB read and write sections through dual-port RAM. This allows the EAB to be written and read at different rates. The `altdpram` megafunction, available with the MegaWizard™ Plug-In Manager in the MAX+PLUS® II software version 9.01 and higher, provides users with complete control over the FLEX 10KE EABs' dual-port RAM architecture.

Figure 1 shows the `altdpram` symbol.

Figure 1. altdpram Megafunction Symbol

```
FILE=
INDATA_ACLR="ON"
INDATA_REG="INCLOCK"
NUMWORDS=2"WIDTHAD"
OUTDATA_ACLR="ON"
OUTDATA_REG="UNREGISTERED"
RDADDRESS_ACLR="ON"
RDCONTROL_REG="OUTCLOCK"
USE_EAB=
WIDTH=
WIDTHAD=
WRADDRESS_ACLR="ON"
WRADDRESS_REG="INCLOCK"
WRCONTROL_ACLR="ON"
WRCONTROL_REG="INCLOCK"
```

```
              ALTDPRAM
    rdaddress[]
    rden              q[]
    outclock
    outclocken
    data[]
    wraddress[]
    wren
    inclock
    inclocken    aclr
```

The FLEX 10KE family's high-performance dual-port memory is ideal for implementing RAM functions, and has the following features:

- 16-bit depth and 4,096 bits per EAB (twice the RAM of other FLEX 10K devices)
- Choice of sizes for EAB configuration: 256×16, 512×8, $1,024 \times 4$, or $2,048 \times 2$
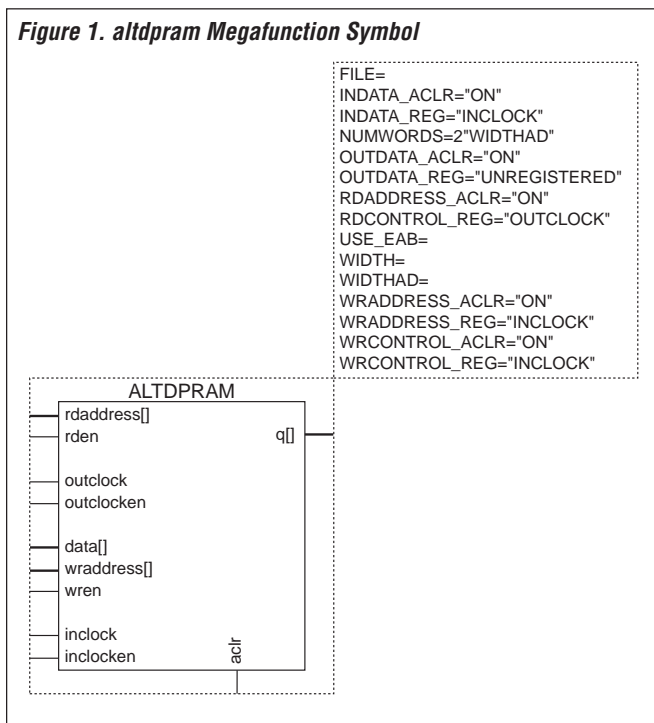- Independent read and write data ports
- Independent read and write addresses

- Enhanced register control
  - User-selectable registering of all EAB inputs
  - Independent input and output clocks
  - Ability to drive read and read enable registers with either the input or output clock
  - Independent clock enables on input and output registers
  - Asynchronous clear

In addition to control over the FLEX 10KE EAB architecture, the `altdpram` megafunction provides the following features:

- Ability to perform simultaneous reads and writes
- Parameterizable data and address bus widths or depths
- Automatic cascading of EABs for designs that require more width than one EAB can provide
- Ability to preload RAM contents with a Memory Initialization File (**.mif**) or Hexadecimal (Intel-Format) File (**.hex**)

Using Independent Input & Output Clocks

For RAM functions that require separate input and output clocks, the write address and write enable ports can be clocked by an input clock and the data output port can be clocked by an output clock. Either the input clock or the output clock can clock the read address and read enable ports, allowing the designer to configure the EAB in one of two modes.

Separate Read/Write Clock

In the separate read/write clock mode, the input clock acts as a write clock and the output clock acts as a read clock. The input clock and output clock drive the signal registers listed in Table 1.

Table 1. Signal Registers Driven by the Input & Output Clocks

Signal	Input Clock	Output Clock
Data Input	✓	
Write Address	✓	
Write Enable	✓	
Read Address		✓
Read Enable		✓
Data Output		✓

This configuration can be implemented using the Altera MegaWizard Plug-In Manager. Within the MegaWizard Plug-In Manager, specify the dual-port RAM megafunction, and on the third page of the Plug-In Manager, select the *Dual Clock: use separate 'read' and 'write' clocks* option (see Figure 2).

Separate Input/Output Clock

In the separate input/output clock mode, the input clock and output clock drive the signal registers listed in Table 2.

This configuration can also be implemented using the Altera MegaWizard Plug-In Manager. Specify the dual-port RAM megafunction, and on the third page of the Plug-In Manager, select the *Dual Clock: use separate 'input' and 'output' clocks* option.

For more information on instantiating parameterized megafunctions with the MegaWizard Plug-In Manager, see "Parameterizing Megafunctions with MegaWizard Plug-Ins" in the February 1998 issue of *News & Views*.

Using a Single Clock

For RAM functions with one clock signal and registered inputs and outputs, the `inclock` and `outclock` inputs are driven by the same clock signal. A single clock configuration can also be implemented using the Altera MegaWizard Plug-In Manager by selecting the dual-port RAM megafunction and selecting the *Single clock* option.

Table 2. Signal Registers Driven by the Input & Output Clocks

Signal	Input Clock	Output Clock
Data Input	✓	
Write Address	✓	
Write Enable	✓	
Read Address	✓	
Read Enable	✓	
Data Output		✓

Software Support

The MAX+PLUS II software (versions 9.01 and higher) supports the `altdpram` megafunction. The `altdpram` megafunction can be instantiated in both schematic and hardware description language (HDL) (Altera Hardware Description Language (AHDL), VHDL, and Verilog HDL) designs.

The `altdpram` megafunction is also supported by third-party tools in the design flow process. Additionally, the MAX+PLUS II software can generate output files for use in third-party simulators.

Additional information on the `altdpram` megafunction can be obtained by contacting Altera Applications at (800) 800-EPLD, referring to MAX+PLUS II Help, or going to the Altera web site at **http://www.altera.com**.

Figure 2. Implementing the altdpram Megafunction Using the MegaWizard Plug-In Manager
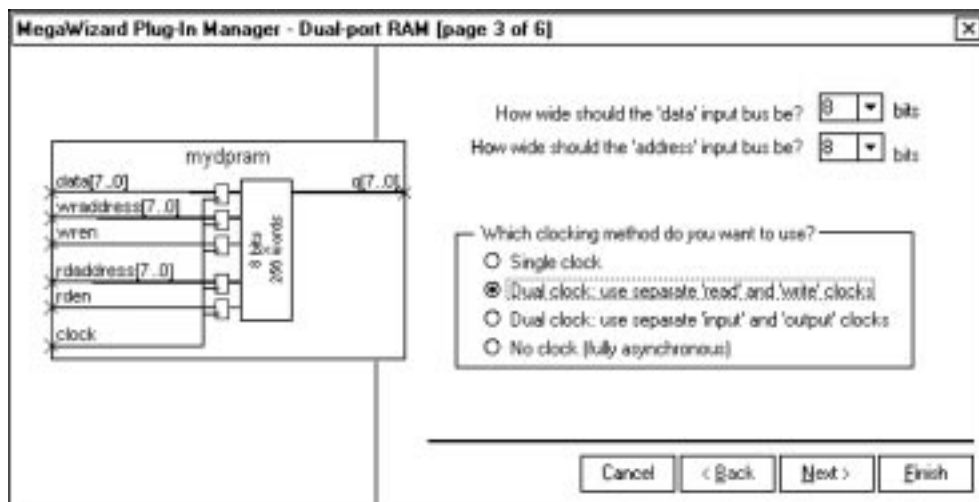
Customer
Application

Axis Systems Selects Altera Devices for New EDA Tool

"The Xcite-1000 addresses the design productivity gap between silicon capabilities and existing verification solutions." Mike Tsai, President & CEO, Axis Systems

Complete system integration on a single device offers products with high performance, capacity, and reliability. However, while this implementation is appealing, design verification is time-consuming, taking up to 70% of design time. Quite often, a company's verification team is larger than the design team. To remove this bottleneck, Axis Systems has introduced its first product, the Xcite-1000, a reconfig-urable computing (RCC) engine that establishes a new category of electronic design automation (EDA) tools. Altera® FLEX® 10K devices are an integral part of this product (see Figure 1).

Until now, no single tool has offered a complete solution for verifying the entire design process, from behavioral simulation to hardware and software verification. The verification tools used

currently—simulation, emulation, and acceleration—have not kept pace with developments in device size and complexity. Designers require a system that fits directly into existing verification and design flows, is faster than software simulation, and offers a better price-to-performance ratio than emulation and hardware acceleration technology. The Xcite-1000 logic verification system addresses this need. "Xcite-1000 addresses the design productivity gap between silicon capabilities and existing verification solutions," said Mike Tsai, Axis founder, president, and CEO.

Design Verification System Using RCC Technology

Axis Systems' Xcite-1000 is a fast, functional Verilog HDL simulator using RCC engine technology. Axis Systems' RCC engine has a massively parallel architecture based on a

Figure 1. Xcite-1000 RCC Architecture

Verilog HDL Design RTL, (1)

Always @posedge cfc
begin
nw_bas = interfac
if (bus_active)

Gate

inv inv1 (b, a);
and and2(c, b, a);
dffp mydff(q, d, clk);

Behavioral

initial
begin
  $monitor(...);
  $my_pfi(...);

Reconfigurable Computing Element

Axis RCC PCI Boards

EPF10K250   EPF10K250
EPF10K250   EPF10K250
EPF10K250   EPF10K250   EPF10K250   EPF10K250

Sun Ultra SPARC II

PCI Interface

SIMD Controller

PCI

Note:
(1)   RTL: Register transfer level.

single-instruction multiple-data (SIMD) algorithm. Computer-intensive tasks are mapped onto hundreds of thousands of reconfigurable computing elements, as shown in Figure 1 on page 16. Reconfigurable elements are custom processors designed for a single task. Communication between the processing elements is based on a systolic array structure by which data is transferred between nearest neighbors.

The Xcite-1000 includes a Verilog HDL software simulator, an RCC compiler, and an RCC hardware engine. For the custom processors used in the hardware engine, Axis Systems chose Altera EPF10K250A devices. The hardware fits inside a Sun workstation and connects directly to the peripheral component interconnect (PCI) backplane, as shown in Figure 2.

Figure 2. Xcite-1000 Boards Fit Inside A Sun Workstation

The number of PCI boards installed determines the capacity. For example, one board with four 599-pin pin-grid array (PGA) EPF10K250AGC599-3 devices can handle designs up to 250,000 gates. Eight boards can fit into a Sun workstation, creating the current total capacity of 2 million gates. By the end of this year, the Xcite-1000 board's capacity will be 4 million gates. The boards are shown in Figure 3.

The Xcite-1000 is the first commercially available functional verification system using RCC technology. Figure 4 on page 18 shows the Xcite-1000 design verification flow. It can accept designs described at the Verilog HDL behavioral level, the register transfer level (RTL), and the gate level. Instead of performing logic synthesis and

translating the higher-level constructs into logic gates, the RCC compiler maps each RTL statement onto the RCC elements and provides inter-active debugging at hardware speed with the built-in software simulator.

Altera Devices are the Perfect Fit

Axis Systems chose Altera devices for the Xcite-1000 because of their fast compile time and high device utilization. "Based on our RCC requirements of fast compile times with high device utilization, Altera's programmable device architecture was the perfect fit for our needs," said Steven Wang, the vice president of marketing for Axis Systems.

The fast compile times of the MAX+PLUS® II software are also key to the project. The two companies have signed an agreement enabling Axis to embed the MAX+PLUS II algorithm-optimization and place-and-route software in the RCC product line.

Altera has been working with Axis Systems since the company's inception and the partnership will continue as Axis adopts the latest high-capacity Altera devices. According to Steven Wang, "To protect our customers'

"Based on our RCC requirements of fast compile times with high device utilization, Altera's programmable device architecture was the perfect fit for our needs." Steven Wang, Marketing VP, Axis Systems
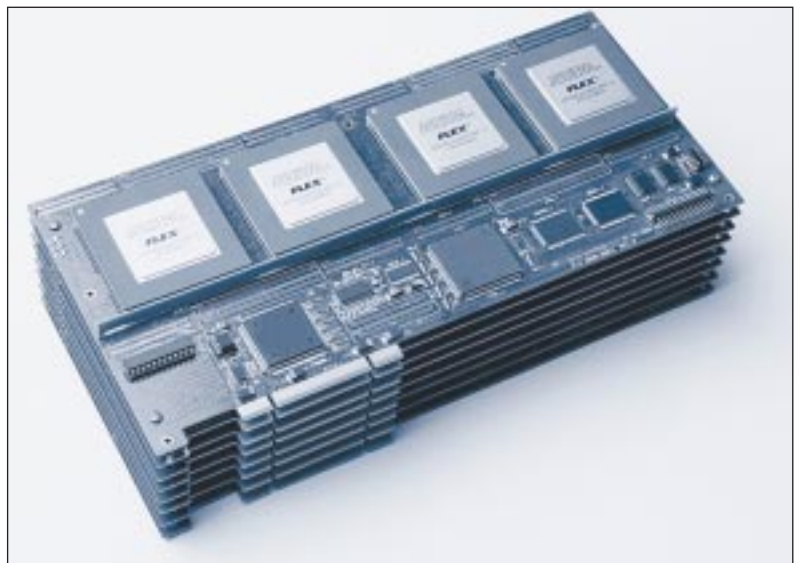
**Figure 3. Xcite-1000 Boards with Four EPF10K250A Devices Each**

Axis Systems Selects Altera Devices for New EDA Tool, continued from page 17

investment, we plan for Xcite-1000's performance and capacity to improve along with technology. When Altera ships higher-capacity devices, we will offer upgrades to our customers." The company is eagerly waiting for the 600-pin ball-grid array (BGA) EPF10K250ABC600-3 devices to become available later this year. They also intend to be among the first to use the revolutionary Altera APEX™ 20K device family and the Quartus™ software when the 400,000-gate EP20K400 devices ship early next year.

Conclusion

The 250,000-gate EPF10K250A devices offer the highest gate count of any programmable logic device on the market and the fast system performance required by today's designs. Using EPF10K250A devices in the Xcite-1000 logic verification system has enabled Axis Systems to not only bring their product to market quickly but also provide a new EDA tool that will enable others to speed their designs through the design and verification process and out to their customers.

Figure 4. Xcite-1000 Design Verification Flow
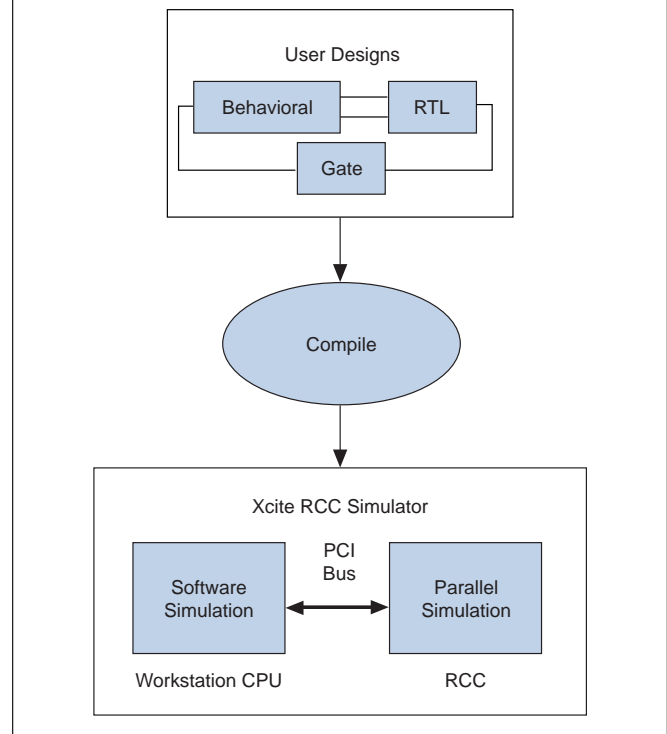
Lexra LX-4080P: The Processor on a PLD

As device densities approach a million gates and system-level designs become more common and more complex, reliable, reusable megafunctions are a vital tool for the design engineer. The Altera Megafunction Partners Program (AMPP℠) provides such megafunctions to users of Altera® programmable logic devices (PLDs). A valuable addition to the processor megafunctions offered by the program is the new LX-4080P function.

The LX-4080P megafunction, recently announced by Lexra, Inc., a new member of AMPP, is the programmable logic industry's first 32-bit R3000-class reduced instruction set computer (RISC) processor megafunction. Targeted for FLEX® 10KE devices, a major advantage of the LX-4080P is its small footprint. When implemented in an EPF10K200E device, it operates at 33 MHz and occupies less than half the device's logic capacity, so that approximately 100,000 gates of logic are still available for implementing other megafunctions or custom logic. This breakthrough gives designers the means to prototype, and even mass-produce, embedded processor designs using PLDs.

Until now, synthesizable 32-bit microprocessors overwhelmed the logic and memory capacity of programmable logic devices. Together, the LX-4080P megafunction and the FLEX 10KE family offer engineers a programmable logic solution for embedded system applications that use R3000-class microprocessors, such as data communications products, network protocol processors, cable modems, set-top boxes, and disk controllers. Engineers can quickly and easily verify the functionality of a 32-bit RISC system early in the design cycle, without the need for costly and complicated hardware emulators, thus reducing the time-to-market for their product.

A Next-Generation Megafunction

The LX-4080P is currently available for FLEX 10KE devices and next year will support the Altera APEX™ 20K devices. Designers will be able to implement the LX-4080P function through the MAX+PLUS® II development system and the next-generation Quartus™ development environment, in combination with the Lexra evaluation system. The

Questions

&ANSWERS

Q *Why is the maximum number of I/O pins available for the FLEX® 10KE devices less than the maximum number of I/O pins available for the equivalent FLEX 10K or FLEX 10KA devices?*

A FLEX 10KE devices generally have fewer I/O pins than the equivalent FLEX 10K or FLEX 10KA devices. For example, the EPF10K50E device has a maximum of 254 I/O pins while the EPF10K50 device has a maximum of 310 I/O pins. FLEX 10KE devices are pad-limited; therefore their smaller die size reduces the I/O pin count.

Q *To what voltage should I connect the EPC1, EPC2, or EPC1441 Configuration EPROM V_{CC} pin when configuring a FLEX device with different V_{CCIO} and V_{CCINT} voltages?*

A The EPC1, EPC2, or EPC1441 Configuration EPROM V_{CC} pin can be connected to either a 3.3-V or 5.0-V supply voltage, because all FLEX 10K and FLEX 6000 devices have 5.0-V tolerant inputs.

When the EPROM's V_{CC} pin is connected to 3.3 V, you should turn on the *Use Low-Voltage Configuration EPROM* option in the **Global Project Device Options** dialog box (Assign menu) before generating a programming file for the Configuration EPROM.

Q *Why do I receive the error message: "Error: Can't open VHDL 'STD.STANDARD'"?*

A This error occurs during compilation of VHDL designs if you delete all of the **.dls** files from your hard drive(s). The **.dls** files from the **maxplus2\vhdl93\std** or **maxplus2\vhdl87\std** library directories, which are required to use the library

packages within the **vhdl87** and **vhdl93** directories, were deleted as well. If these files are deleted, the MAX+PLUS® II software should be re-installed to replace them.

MAX+PLUS II Help states that when troubleshooting "unknown error" messages you should delete the **.dls** files in the current project directory and recompile. Be sure to delete **.dls** files within your project directory only, not within the **maxplus2\vhdl87** or **maxplus2\vhdl93** directories.

Q *When I run the Jam™ Player, it says that programming or configuration was successful but nothing happens. Why?*

A The Jam Player is not executed unless you initialize the specific programming/configuration variables for this function. If you do not initialize these variables, the Jam Player simply performs a syntax check on the Jam File.

The initialization statement for programming devices is:

```
jam -dDO_PROGRAM=1 jamfile.jam
```

The initialization statement for configuring devices is:

```
jam -dDO_CONFIGURE=1 jamfile.jam
```

The initialization statement for both programming and configuring devices is:

```
jam -dDO_PROGRAM=1 -dDO_CONFIGURE=1
jamfile.jam
```

You can type the initialization statements shown above at your system command line. For more information about the Jam language, initialization variables, and statements, refer to *Application Note 88 (Using the Jam Language for ISP using an Embedded Processor)*.

---

evaluation system consists of a printed circuit board (PCB) with the LX-4080P function implemented in an EPF10K200E device and a software development kit.

Included with the LX-4080P megafunction is a core database for use with the Altera MAX+PLUS II Design Kit, a simulation model, a comprehensive test environment with a regression test suite, and full user documentation.

LX-4080P & FLEX 10KE: A Rapid Prototyping & Production Solution

With the LX-4080P megafunction and FLEX 10KE devices, Lexra and Altera are providing users with a powerful combination of cutting-edge intellectual property and state-of-the-art devices. Engineers can easily implement the LX-4080P megafunction in FLEX 10KE devices to produce an embedded system application that uses an R3000-level microprocessor, and rapidly bring their product to market.

Contributed
A r t i c l e

GOEPEL electronics Integrates Jam Player into Boundary-Scan Test Software

by Renato Paelicke
Applications Engineer
and
Heiko Ehrenberg
Manager US Operations
GOEPEL electronics

The Jam™ programming and test language, a software-level standard for in-system programmability (ISP), provides an in-system programming solution that is easy to use and offers fast programming times. The Jam Player can easily be integrated into in-circuit testers and used to test and program ISP-capable devices. In this way, device programming can fit into the standard manufacturing flow, reducing time-to-market.

Recently, GOEPEL electronics, a leading manufacturer of IEEE Std. 1149.1-compliant boundary scan test systems, integrated the Jam Player into its SYSTEM CASCON (computer-aided, scan-based observation and node control) software version 3.2. SYSTEM CASCON is a leading, industry-approved boundary-scan test, verification, and programming software. SYSTEM CASCON, available either as a complete testing solution or in specialized development, test, and repair packages, can be combined with any of GOEPEL electronics' wide range of testing hardware to offer a comprehensive laboratory, production, or service testing system.

Easy-to-Use Jam Player Integration

The Jam Player is an integral part of SYSTEM CASCON packages, and Jam Files (**.jam**) are an accepted test file format, as illustrated in Figure 1.

In the SYSTEM CASCON software, the options for the Jam Player are set in the easy-to-use dialog box shown in Figure 2 on page 21.

The user simply browses to the appropriate Jam File, selects one or more

Figure 1. Features of the SYSTEM CASCON Software
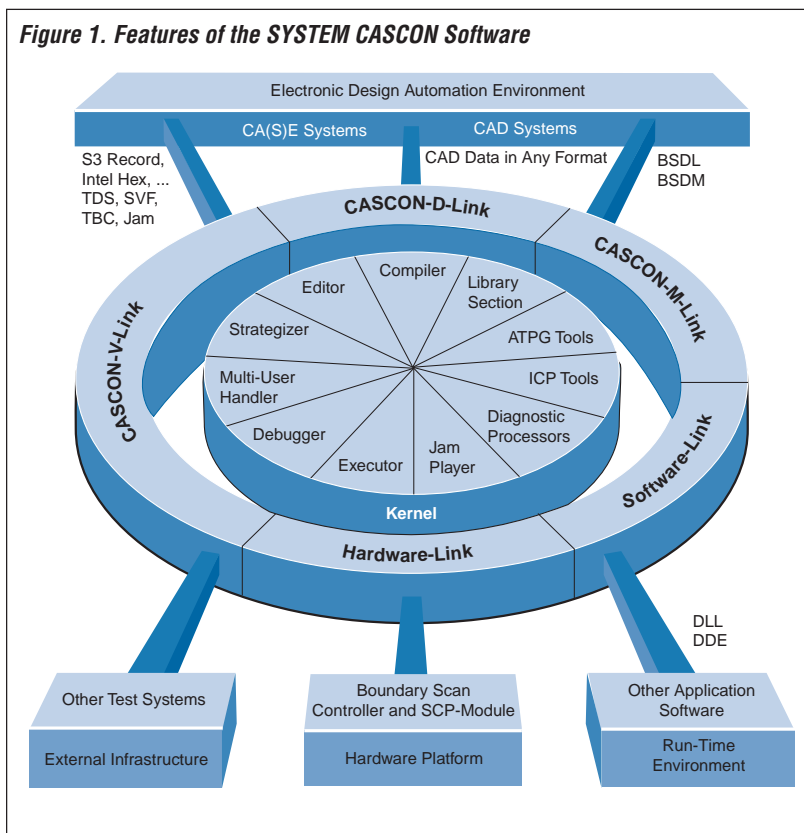
of the predefined values or actions, and defines initialization variables as a string list before choosing OK. The actions and messages generated by the Jam Player are shown in the SYSTEM CASCON test window.

Superior Programming Times Obtained Using the Jam Player

GOEPEL electronics recorded superior programming times in an experiment using the Jam Player to program three devices. The devices programmed were an Altera EPM7064SLC44-10 and EPM9560ARC304-15 device, and a Lattice Semiconductor ispLSI3256A70LM device. The test station was set up on a 200-MHz Pentium processor PC running the Windows NT operating system, and the devices were programmed on a Jam demonstration board. The programming times were obtained using three different controllers. For the low-performance test, GOEPEL electronics employed the parallel-port SCAN BOOSTER controller. For the high-performance tests, the CASCON GALAXY software package was used with a PC/AT-bus ASC 16 controller and a PCI-bus PSC 1149.1-A controller. The results are listed in Table 1. The Altera® MAX® devices recorded very fast programming times with both the low- and high-performance controllers.

SYSTEM CASCON & the Jam Player: A Superior Combination

Integrating the Jam Player into the SYSTEM CASCON software has enabled GOEPEL electronics to offer a fast, easy-to-use way to test and program ISP-capable devices using their boundary-scan testers. Together, these hardware and software tools help designers realize the possibilities of ISP and meet the difficult cost and time-to-market requirements of today's PLD industry.

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Figure 2. SYSTEM CASCON Jam Player Options Dialog Box
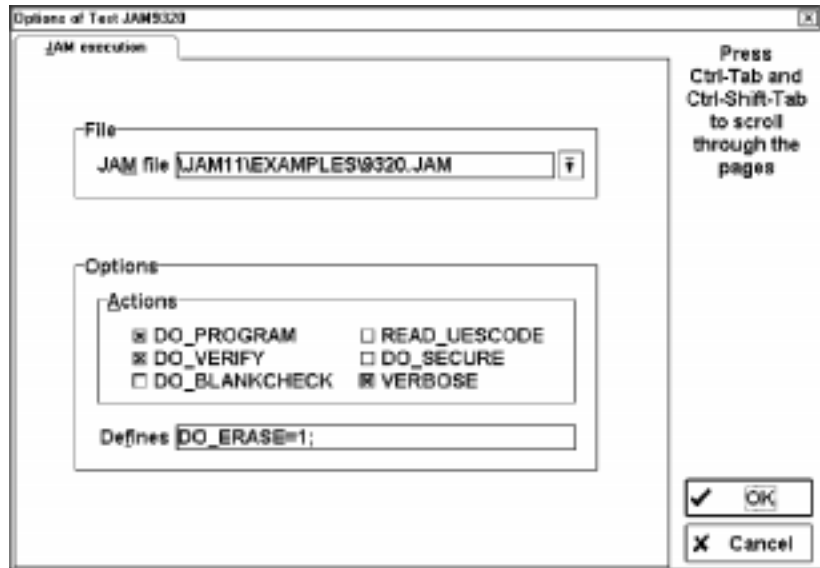
Table 1. Programming Times Using Jam Player & IEEE 1149.1 Controllers

Device	Jam File	ASC 16 PC/AT Bus (seconds), *(1)*	PSC 1149.1-A PCI Bus (seconds), *(1)*	SCAN BOOSTER Parallel Port (seconds), *(1)*
EPM7064SLC44-10	**7064s.jam**	2/16	2/13	3/20
EPM9560RC304-15	**9560.jam**	10/85	10/75	15/94
ispLSI3256A70LM	**3256a.jam**	52/95	52/93	67/122

Note:
(1) The first number is the programming time for the device only. The second number is the total time (the programming time plus verification time).

Design Tips
Altera Applications

Using Arithmetic Operators in MAX+PLUS II VHDL

This article is the third of a four-part series that discusses ways to achieve optimal logic cell utilization with VHDL in MAX+PLUS® II software. The next issue of News & Views will feature the fourth and final part of the series, the importance of hierarchical instantiation.

Designers constantly strive to improve the performance of their designs. One way to achieve this is through area efficiency; if you reduce logic and optimize your design by using arithmetic operators cautiously, you can eliminate extra adders.

Careful use of arithmetic operators is necessary because the MAX+PLUS II software does not automatically combine related adders into a single adder and add multiplexing logic to reduce area utilization. For example, whenever an addition statement is written in VHDL code, an adder is created. You should optimize your VHDL code to remove unnecessary instances of arithmetic functions before compiling in the MAX+PLUS II software. By carefully implementing and grouping arithmetic operators, you can optimize your design by reducing the number of adders and streamlining the critical path.

When two addition statements are implemented in VHDL code, two adders are created with one multiplexer on the input signals. This implementation results in additional logic (see Example 1).

Example 1

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY add_ex2 IS
   PORT
   (
      a, b: IN STD_LOGIC_VECTOR(15
         DOWNTO 0);
      c, d: IN STD_LOGIC_VECTOR(15
         DOWNTO 0);
      input : IN STD_LOGIC;
      sum: OUT STD_LOGIC_VECTOR(15
         DOWNTO 0)
   );
END add_ex2;
```

```
ARCHITECTURE behavior OF add_ex2 IS
BEGIN

   PROCESS (a,b,c,d,input)
      BEGIN
         IF input = '0' THEN
            sum <= a + b;
         ELSE
            sum <= c + d;
      END IF;
   END PROCESS;
END behavior;
```

Figure 1 shows a schematic representation of Example 1.

Figure 1. Schematic Representation of Code Creating Two Adders

The VHDL code in Example 2 creates two multiplexers and one adder on the input signals. This implementation uses less logic than Example 1.

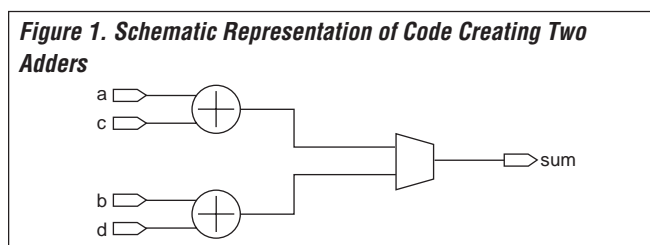### Example 2

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY add_ex1 IS
   PORT
   (
      a, b: IN STD_LOGIC_VECTOR(15
         DOWNTO 0);
      c, d: IN STD_LOGIC_VECTOR(15
         DOWNTO 0);
      input : IN STD_LOGIC;
      sum: OUT STD_LOGIC_VECTOR(15
         DOWNTO 0)
   );
END add_ex1;
```

```
ARCHITECTURE behavior OF add_ex1 IS
   SIGNAL a_in1 : STD_LOGIC_VECTOR(15
      DOWNTO 0);
   SIGNAL a_in2 : STD_LOGIC_VECTOR(15
      DOWNTO 0);

BEGIN

   PROCESS (a,b,c,d,input)
      BEGIN
         IF input = '0' THEN
            a_in1 <= a;
            a_in2 <= b;
         ELSE
            a_in1 <= c;
            a_in2 <= d;
         END IF;
      END PROCESS;
   sum <= a_in1 + a_in2;

END behavior;
```

Figure 2 shows a schematic representation of
Example 2.

Figure 2. Schematic Representation of Code Creating One Adder
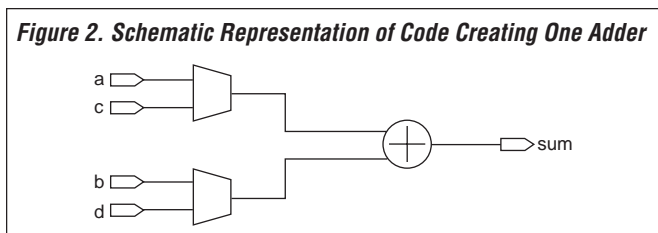
The ordering and grouping of arithmetic functions is
another important aspect of design optimization.
Careful grouping of arithmetic functions in VHDL can
affect the critical path through cascaded circuitry.
Example 3 shows two ways of implementing the same
arithmetic function.

Example 3

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY arithmetic IS
   PORT
   (
      a,b,c,d : IN STD_LOGIC_VECTOR(3
         DOWNTO 0);
      x,z: OUT STD_LOGIC_VECTOR(3 DOWNTO
         0)
   );
END arithmetic;
```

```
ARCHITECTURE behav OF arithmetic IS
BEGIN
   z <= (a + b) + (c + d);
      -- This code creates 2 parallel
      -- adders and another adder to
      -- add them together
   x <= a + b + c + d;
      -- This code creates 3 adders
      -- cascaded in series
END behav;
```

The two arithmetic functions have the same
functionality, but the first statement
(z <= (a + b) + (c + d);) creates two stages of
adders (see Figure 3). This grouping of arithmetic
functions creates better timing results and has one less
level of delay.

Figure 3. Two Stages of Adders
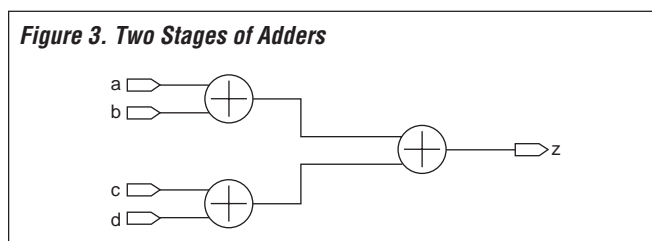
The second statement (x <= a + b + c + d;)
creates three stages of adders (see Figure 4). Because
the first statement creates two adders and the second
statement creates three adders, the z output will be
valid before the x output. Therefore, the first statement
results in a faster circuit.

Figure 4. Three Stages of Adders
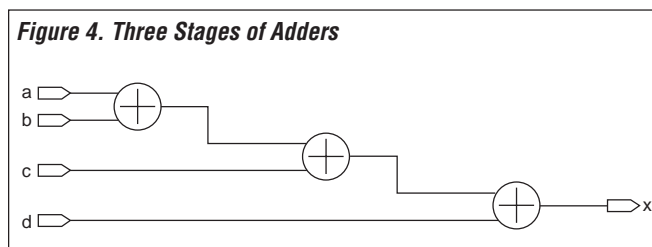
For more information on arithmetic operators with
MAX+PLUS II VHDL, see MAX+PLUS II Help.

Altera

N E W S

AMPP Partner HammerCores Delivers Fully Parameterized Reed-Solomon Encoder & Decoder

^{SM} Altera Megafunctions Partners Program (AMPP^{SM}) member HammerCores has delivered fully parameterized Reed-Solomon (RS) encoder and decoder functions optimized for Altera® programmable logic devices (PLDs). The HammerCores RS encoder is optimized for all Altera FLEX® devices, while the HammerCores RS decoder, which is a more complex algorithm, is optimized for Altera FLEX 10K devices. Because HammerCores RS functions are parameterized and optimized for Altera devices, they markedly increase your control over the design process and your time-to-market. Although the ability to implement RS codes in programmable logic is a very recent development, it is one that will be increasingly utilized as Altera PLDs become more economical and increase in performance.

Description

The two standard classifications of error control coding are Automatic Repeat reQuest (ARQ) and Forward Error Correction (FEC). ARQ coding is a detection-only type of coding that is useful for cleaner transmission mediums. One example of ARQ coding is cyclic redundancy code (CRC), which is effectively implemented by Altera's parameterized CRC MegaCore™ megafunction. Data sent via a poor transmission medium requires FEC, which provides both error detection and error correction. Using FEC significantly reduces the need for data retransmission, because retransmission of data errors is only required when the number of errors exceeds the error correction limit.

RS codes, which use FEC, are widely used because they have a relatively large error correction capability with minimal added overhead. RS codes are also easily scaled up or down to coincide with the error rates expected in a given system.

RS codes consist of a number of information symbols, followed by several check, or parity, symbols. Codes are described as (N,K), where N is the total number of symbols in the codeword, and K is the number of information symbols. The number of errors that can be corrected is half the number of check symbols. Errors are defined on a symbol basis. Therefore, any number of bits reversed in a symbol is counted as only one error for that symbol.

The maximum number of symbols in a message (codeword length) is determined by the size of the field, at 2^m-1 symbols, where m is the number of bits per symbol. Therefore, a message of 8-bit symbols, can contain up to 255 symbols, including check symbols. Any number of check symbols per codeword is valid, and is determined by the generator polynomial.

A system-level implementation of an RS code requires both an encoder and a decoder. On the transmitting end, the encoder takes in K information symbols, and outputs an N length codeword (K information symbols, followed by R check symbols). The codeword is then transmitted over a channel. The type of modulation, transmission, or packetization is irrelevant to the code. At the receiver end, the decoder determines if there are errors and corrects them. The following parameters are used in the decoding process:

- *N*—Total number of symbols per codeword
- *R*—Number of check symbols per codeword
- *m*—Number of bits per symbol
- *field*—Polynomial defining finite field
- *genstart*—The first root of the generator polynomial

With the HammerCores Reed-Solomon encoder and decoder, you are able to build an RS decoder or encoder for virtually any RS codec within minutes. Overall resource requirements will vary widely with parameter specification, but are linearly dependent on both the field size and number of check symbols.

Reed-Solomon Performance

Table 1 shows the performance of a Reed-Solomon function using 8-bit data symbols and the MAX+PLUS® II version 9.02 software for FLEX 10KA-1 devices.

Table 1. Reed-Solomon Performance				
Megafunction	**Megafunction Generation (Seconds)**	**Fitter (Seconds)**	**Performance (Mbits/second)**	**Logic Cells/Memory Bits**
RS Encoder, 16 Check Symbols	< 1	20	500	266/0
RS Encoder, 8 Check Symbols	< 1	11	550	170/0
RS Decoder, 16 Check Symbols	2	300	200	2,076/2,304
RS Decoder, 8 Check Symbols	1	120	400	1,240/2,304

Figure 1 shows the Reed-Solomon megafunction within the MAX+PLUS II software.

Design Flow

You can download a free evaluation of the HammerCores Reed-Solomon megafunction from the Internet at **http://www.hammercores.com**. The MAX+PLUS II OpenCore™ evaluation feature is a risk-free method to evaluate how any AMPP or MegaCore function performs with your design. The HammerCores library of parameterizable Reed-Solomon functions consists of three members:

■ High-Speed Reed-Solomon Encoder (500 Mbits/second)
■ Reed-Solomon Discrete Decoder (20-100 Mbits/second)
■ Reed-Solomon Streaming Decoder (40-400 Mbits/second)

Utilities are included to pass parameters, generate valid field polynomials, and create MAX+PLUS II test vectors based on the parameter list.

After entering the parameters, the utilities generate the customized module, which is ready to be compiled and simulated in the MAX+PLUS II software. The function can also be black-boxed in any third-party EDA tools and is therefore easy to integrate in any top-level project.

The RS MegaWizard Plug-In makes it easy to enter parameters in the following four steps:

1. Start the MegaWizard Plug-In Manager.
2. Select the output language—Verilog HDL, VHDL, or Altera Hardware Description Language (AHDL).
3. Select the Reed-Solomon parameters (see Figure 1).
4. Simulate and compile the function in the MAX+PLUS II software.

The RS MegaWizard Plug-In creates a hardware description language (HDL) instance of the function and a MAX+PLUS II simulation file for functional and timing simulation.

If you are planning to create programming or configuration files, you will need to license the RS function from HammerCores. You can get further information regarding the HammerCores RS function on the Internet at **http://www.hammercores.com**. For further information regarding Altera products mentioned in this article, visit the Altera web site at **http://www.altera.com**.

Figure 1. Reed-Solomon Megafunction

In Every

I S S U E

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for Altera devices. Algorithms are available from Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Micro-systems' BBS and with the MAX+PLUS® II software releases. Programming support for Configuration EPROM, MAX® 9000, and MAX 7000 devices is shown in the table below. All information is subject to change.

Third-Party Programming Hardware Support		
Device	**Data I/O**, *(1)*	**BP Microsystems**, *(2)*
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPC1441	✓	✓
EPM7032	✓	✓
EPM7032S	✓	✓
EPM7064	✓	✓
EPM7064S	✓	✓
EPM7064AE	*Note (3)*	*Note (3)*
EPM7096	✓	✓
EPM7128E	✓	✓
EPM7128S	✓	✓
EPM7128A	✓	✓
EPM7160E	✓	✓
EPM7192E	✓	✓
EPM7192S	✓	✓
EPM7256E	✓	✓
EPM7256A	*Note (4)*	*Note (5)*
EPM7256S	✓	✓
EPM9320	✓	✓
EPM9320A	✓	✓
EPM9400	✓	✓
EPM9480	✓	✓
EPM9560	✓	✓
EPM9560A	✓	✓

Notes:
(1) These devices are supported by Data I/O 3900 version 5.8 and UniSite version 5.8 programmers.
(2) These devices are supported by BP Microsystems' programmers version 3.36.
(3) Support for this device is planned for January 1999.
(4) Support for this device is planned for December 1998.
(5) Support for this device is planned for November 1998.

New Altera Publications

New publications are available from Altera® Literature Services. Individual documents are available on the Altera world-wide web site at **http://www.altera.com**. Always check the Altera world-wide web site for the latest version of a document, as revisions are not always printed. Document part numbers are shown in parentheses.

- *Configuration EPROMs for FLEX Devices Data Sheet* (A-DS-EPROM-09)
- **PCI MegaCore Function User Guide** (A-UG-PCI-01)
- *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* (A-AN-088-03)
- *AN 101: Improving Performance in FLEX 10K Devices with Synplify Software* (A-AN-101-01)
- *TB 49: Generating Post-Route Files in the MAX+PLUS II Software for Third-Party Verification Tools* (M-TB-049-01)
- *APEX 20K Programmable Logic Device Family Advance Information Brief* (A-AIB-APEX20K-01)
- *ATF1500AS Analysis Report White Paper* (M-WP-ATF1500-01)
- *Using Altera's 1.00-mm FineLine BGA Packages White Paper* (A-WP-BGA-01)

Current Software Versions

The latest version of Altera® software is shown below:

- MAX+PLUS II version 9.1 (PC, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 platforms)

Altera at DSP World 1998

Altera had a strong presence at this year's DSP World in Toronto, September 13 through 16, including a demonstration of a Reed-Solomon function, and an hourly product presentation.

Altera also sponsored a half-day product presentation entitled *DSP Oriented Communications Functions Optimized for PLD Architectures*. Tapan Mehta submitted a paper at the event: *Implementing High-Performance Error Control Coding Functions in Programmable Logic*.

Programming Hardware Support

The following tables contain the latest programming hardware information for Altera® devices. For correct programming, use the software version shown in "Current Software Versions" on the previous page. See Table 1.

Table 1. Altera Programming Adapters (Part 1 of 2) Note (1)		
Device	**Package**	**Adapter**
EPC1064 (2), EPC1064V (2) EPC1441 (3)	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 (3), EPC1213, (2)	DIP, J-lead	PLMJ1213
EPC2 (3)	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC (4)
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC (4) PLMR9000-240NC (4)
EPM7032, EPM7032V	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S, EPM7032AE	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7064S, EPM7064AE	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC (4)
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A	J-lead (84-pin) TQFP (100-pin) TQFP (144-pin)	PLMJ7000-84 PLMT7000-100NC (4) PLMT 7000-144NC (4)

Table 1. Altera Programming Adapters (Part 2 of 2) Note (1)		
Device	**Package**	**Adapter**
EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC (4) PLMT7000-100NC (4) PLMQ7128/160-160NC (4)
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC (4) PLMQ7128/7160-160NC (4)
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/256-160NC (4)
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A EPM7256S	PQFP (208-pin) RQFP (208-pin)	PLMR7256-208NC (4) PLMT7000-208NC (4)
EPM7384AE	TQFP (144-pin) PQFP (208-pin)	PLMT7000-144NC (4) PLMR7256-208NC (4)
EPM7512AE	TQFP (144-pin) PQFP (208-pin)	PLMT7000-144NC (4) PLMR7256-208NC (4)

Notes:
(1) Refer to the Altera *1998 Data Book* for device adapter information on MAX 5000 and Classic devices. Altera offers an adapter exchange program for 0.8-μm EPM5032, EPM5064, and EPM5130 programming adapters.
(2) FLEX 8000 Configuration EPROM.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 Configuration EPROM.
(4) These devices are not shipped in carriers.

Table 2 provides programming and configuration compatibility information for the BitBlaster™ serial port and the ByteBlasterMV™ parallel port download cables (the ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable).

Table 2. Download Cable Compatibility		
Device	**BitBlaster**	**ByteBlasterMV**
FLEX 10K	✓	✓
FLEX 10KA		✓
FLEX 10KE		✓
FLEX 8000	✓	✓
FLEX 6000	✓ (1)	✓
MAX 9000	✓	✓
MAX 9000A	✓	✓
MAX 7000S	✓	✓
MAX 7000A		✓

Note:
(1) This download cable is available for EPF6016 devices only.

Altera Device Selection Guide

All current information for the Altera® FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, and MAX 7000 devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide*. For the most up-to-date information about Altera products, go to the Altera world-wide web site at **http://www.altera.com**. Contact Altera or your local sales office for current product availablitiy.

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin PQFP	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-pin BGA[1], 484-pin BGA[1]	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1]	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-pin BGA	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-pin BGA[1], 356-pin BGA, 484-pin BGA[1]	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 484-Pin BGA[1], 672-Pin BGA[1]	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-pin BGA[1]	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	3.3 V	-1, -2, -3	12,160	40,960
EPF10K250E	250,000	599-Pin PGA, 672-Pin BGA[1]	2.5 V	-1, -2, -3	12,160	81,920

Note:
(1) This package is a space-saving FineLine BGA™ package.

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	5.0 V	-2, -3, -4	282	208
EPF8282AV	2,500	100-Pin TQFP	78	3.3 V	-3, -4	282	208
EPF8452A	4,000	160-Pin PQFP	120	5.0 V	-2	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	5.0 V	-3, -4	452	336
EPF8636A	6,000	208-Pin PQFP	136	5.0 V	-2	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136	5.0 V	-3, -4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	112, 120, 152	5.0 V	-2	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152	5.0 V	-3, -4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	5.0 V	-2, -3, -4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	5.0 V	-2, -3, -4	1,500	1,296

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	71, 81[2], 102, 139[2]	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 81[2], 117, 171, 171[2]	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218[2]	3.3 V	-1, -2, -3	1,960	1,960

Notes:
(1) This package is a space-saving FineLine BGA package.
(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-5, -7, -10
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-6, -7, -10
EPM7032	32	44-Pin PLCC/TQFP/PQFP	36	5.0 V	-6, -7, -10, -12, -15
EPM7032V	32	44-Pin PLCC/TQFP	36	3.3 V	-12, -15, -20
EPM7064AE	64	44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin BGA[1]	38, 68, 68	3.3 V	-5, -7, -10
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin PQFP/TQFP	36, 52, 68	5.0 V	-5, -6, -7, -10
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	5.0 V	-6, -7, -10, -12, -15
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	5.0 V	-7, -10, -12, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-5, -7, -10, -12
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-7, -10, -12, -15, -20
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-6, -7, -10
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 104	5.0 V	-10, -12, -15, -20
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7192E	192	160-Pin PQFP/PGA	124	5.0 V	-12, -15, -20
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 164, 164	3.3 V	-6, -7, -10, -12
EPM7256S	256	208-Pin RQFP/PQFP	164	5.0 V	-7, -10, -15
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	5.0 V	-12, -15, -20
EPM7384AE	384	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -12
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	120, 176, 212	3.3 V	-7, -10, -12

Note:
(1) This package is a space-saving FineLine BGA package.

Discontinued Devices Update

Altera has no new announcements regarding discontinued devices. Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera:

Information Type	Access	U.S. & Canada	All Other Locations
Literature, *Note (1)*	Altera Literature Services	(888) 3-ALTERA **lit_req@altera.com**	(408) 544-7144, *Note (2)* **lit_req@altera.com**
	World-Wide Web	**http://www.altera.com**	**http://www.altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
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Technical Support	Telephone Hotline (6 a.m. to 6 p.m. Pacific Time)	(800) 800-EPLD (408) 544-7000	(408) 544-7000, *Note (2)*
	Fax	(408) 544-6401	(408) 544-6401, *Note (2)*
	Electronic Mail	**sos@altera.com**	**sos@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104, *Note (2)*
	World-Wide Web	**http://www.altera.com**	**http://www.altera.com**

Notes:
(1) The **MAX+PLUS II Getting Started** manual is available from the Altera world-wide web site. To obtain other MAX+PLUS II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

PLD World '98 Draws a Crowd

The fifth annual Altera® PLD World was held on October 23 in Tokyo, Japan. This year's event drew record attendance and showcased the Quartus™ software, Altera's next-generation development system for programmable logic. Also featured were presentations by Rodney Smith, President and CEO of Altera; Aart de Geus, Chairman and CEO of Synopsys; Ken Yamaguchi, Editor in Chief of Nikkei Electronics; and Kazuhiko Shirai, General Manager, 3rd Transmission Division Transmission Operations Unit of NEC Corporation; as well as a variety of presentations by other Altera and Altera distributor personnel, ACCESS℠ partners, and AMPP℠ partners.

Next year's PLD World will be held on November 5, 1999 at the Tokyo Forum.

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