The Altera Advantage News & Views

Newsletter for Altera Customers ◆ First Quarter ◆ February 1999

FLEX 10KE Devices Meet the 66-MHz/64-Bit PCI Compliance Challenge

The Altera® FLEX® 10KE family meets the 66-MHz / 64-bit peripheral component interconnect (PCI) compliance challenge. Flexibility and density make programmable logic devices (PLDs) an ideal choice for implementing PCI designs. FLEX 10KE devices meet the PCI I / O timing specification of 3-ns setup time (t_{SU}) and 6-ns clock-to-output time (t_{CO}), and are 66-MHz, 64-bit PCI-compliant.

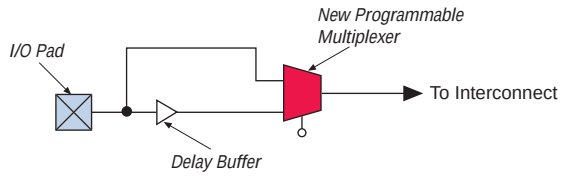
Innovative Programmable Delay Feature

FLEX 10KE devices have an innovative programmable delay feature that allows them to meet the most stringent PCI timing specifications. Designers can now use a new programmable multiplexer to bypass the delay buffer in the I / O element (IOE), improving I / O timing requirements. See Figure 1.

FLEX 10KE devices will include a programmable delay feature with a delay buffer that can be used or bypassed if unnecessary. For non-PCI designs, the delay buffer can be implemented to introduce the required delay to guarantee a zero hold time at the pin. PCI designs have a sufficient amount of combinatorial logic between the register and the pin; therefore, an extra delay is not needed at the register to guarantee a zero hold time. Bypassing the delay buffer gives better setup times by enabling the signal to reach the input of the register faster, allowing FLEX 10KE devices to meet the setup times required for 66-MHz, 64-bit PCI compliance.

In the existing EPF10K50E and EPF10K200E devices, the I / O element introduces a delay from the input pin to the input of the register to ensure a zero hold time for all designs. These devices will be enhanced to include the programmable delay feature. Although the existing EPF10K50E devices are already compliant without this feature, adding a programmable delay increases the flexibility of PCI designs.

Figure 1. Programmable Delay Feature



Support for Programmable Delay with MAX+PLUS II Version 9.2

Support for programmable delay is available with version 9.11 and higher of the MAX+PLUS® II development software. The MAX+PLUS II version 9.2 software supports 66-MHz / 64-bit PCI-compliant timing for Altera PCI MegaCore™ functions and Altera Megafunction Partners Program (AMPP℠) megafunctions.

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PCI MegaCore Functions & AMPP Megafunctions Maximize Performance

In addition to the increased power and flexibility of the PCI solution with the new FLEX 10KE devices, Altera is also introducing a new PCI MegaCore function. This new function will help maximize the performance of PCI designs. Altera plans to release the new `pci_c` MegaCore function in the March 1999. This high-performance PCI master / target MegaCore function is fully hardware-tested and can be flexibly implemented as a 66-MHz / 64-bit PCI master / target interface. Through this megafunction, designers can parameterize their function to meet exact design requirements for optimal use of the PLD. Implemented in FLEX 10KE devices, the `pci_c` function is 66-MHz PCI-compliant. Table 1 lists the Altera PCI MegaCore functions.

Table 1. PCI MegaCore Megafunctions

Megafunction	Description	Availability
`pci_c`	66 MHz, 64-bit; master/target 33 MHz, 64-bit; master/target	March 1999
`pci_a`	33 MHz, 32-bit; master/target	Now
`pci_b`	33 MHz, 32-bit; master/target	Now
`pcit1`	33 MHz, 32-bit; target only	Now

The AMPP program also offers a number of 32- and 64-bit, 33-MHz PCI megafunctions that are optimized for Altera devices. Table 2 lists the AMPP megafunctions currently available.

Universal PCI Board Tests PCI Functionality

To expedite the process of testing PCI designs and boost productivity, Altera is offering the new universal PCI board. After implementing a PCI design and downloading it to the FLEX 10KE device on the universal PCI board, the designer can exercise the design and verify its functionality. The board reduces the time required to implement and test a PCI design. The universal PCI board supports all Altera PCI MegaCore functions and is scheduled to ship in the second quarter of 1999.

Table 2. AMPP Megafunctions

AMPP Partner	Description	Availability
Eureka Technology	32-bit target with burst	Now
Eureka Technology	64-bit target only	Now
Eureka Technology	32-bit master/target with burst	Now
PLD Applications	32-bit target only	Now
PLD Applications	32-bit master/target	Now
PLD Applications	64-bit target only	Now
PLD Applications	64-bit master/target	Now

Conclusion

With the introduction of the new FLEX 10KE devices including the innovative programmable delay feature, Altera offers a solution to the PCI challenge. The new 66-MHz, 64-bit master / target MegaCore function and universal PCI board maximize the performance of these new devices. The combination of the device, function, and board simplifies the implementation and testing of PCI designs. Altera has developed the winning solution to meet your PCI design challenges.

Coming Soon: The Altera 1999 Data Book

The Altera® ***1999 Data Book*** will be available in March 1999 from Altera Literature Services. This book contains comprehensive literature on Altera devices, including:

- Current information on the new APEX™ architecture, including the *APEX 20K Programmable Logic Device Family Data Sheet*
- All current Altera device family data sheets
- Application notes on device timing
- Ordering information for Altera devices and software

Altera will release a data book on device packaging in the second quarter of 1999, and another data book on Altera tools in the second half of 1999.

APEX Update

APEX 20K Family

The APEX™ 20K family, with a system performance of over 125 MHz, will have densities ranging from 100,000 to 1 million gates. This family uses the revolutionary MultiCore™ architecture, which combines look-up table (LUT) logic, product-term logic, and embedded memory into a single device, to provide a System-on-a-Programmable-Chip™ solution. The first APEX 20K device, the 2.5-V EP20K400, will be available in March 1999. The 1.8-V APEX 20KE devices will be available in 1999 and offer an enhanced superset of features.

MegaLAB Structures in APEX 20K Devices

APEX 20K devices combine logic elements (LEs) and memory into MegaLAB™ structures (see Figure 1). MegaLAB structures contain 16 logic array blocks (LABs) composed of 10 LEs each, an advanced embedded structure called an embedded system block (ESB), and a local interconnect that connects all 16 LABs and the ESB.

APEX 20K High-Performance PLL & I/O Support

APEX 20K devices offer enhanced ClockLock™ and ClockBoost™ features and support peripheral component interconnect- (PCI-) compliant I/O pins. The MultiVolt™ I/O interface, which is ideal for mixed-voltage systems, is also a standard feature. APEX 20KE devices extend to the highest integration density and support advanced I/O standards, including LVTTL, LVCMOS, Gunning transceiver logic (GTL+), stub-series terminated logic (SSTL-2 and SSTL-3), low-voltage differential signaling (LVDS), advanced graphics port (AGP), center tap terminated (CTT), and high speed transceiver logic (HSTL). These devices also offer further enhancements to the ClockLock and ClockBoost features.

APEX 20K devices will be offered in a variety of packages, including space-saving FineLine BGA™ packages. Table 1 shows the device features of the APEX 20K family.

Figure 1. APEX 20K MegaLAB Structure

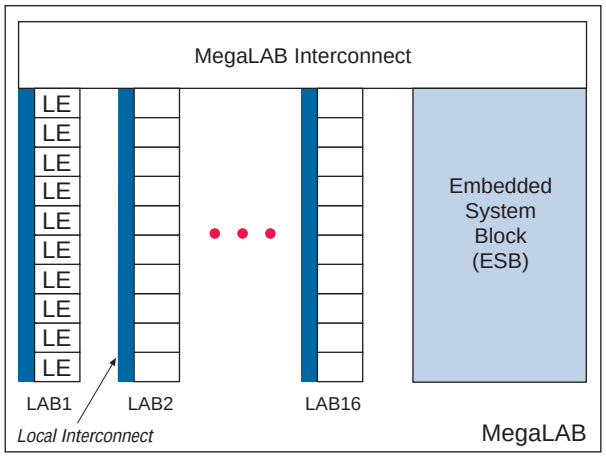

Table 1. APEX 20K Devices

Feature	EP20K100E EP20K100	EP20K160E	EP20K200E EP20K200	EP20K300E	EP20K400E EP20K400	EP20K600E	EP20K1000E
Maximum Gates	263,000	404,000	526,000	728,000	1,052,000	1,537,000	2,670,000
Typical Gates	53,000 to 106,000	82,000 to 163,000	106,000 to 211,000	147,000 to 293,000	213,000 to 423,000	311,000 to 618,000	541,000 to 1,073,000
Logic Elements	4,160	6,400	8,320	11,520	16,640	24,320	42,240
Maximum Macrocells	416	640	832	1,152	1,664	2,432	4,224
Maximum RAM Bits	53,248	81,920	106,496	147,456	212,992	311,296	540,672

ESBs Offer Memory Advantages

APEX ESBs, which contain 2,048 programmable bits, can be configured as product-term logic, LUT-based logic, or three different types of memory: dual-port RAM, ROM, or content addressable memory (CAM). Configuring the ESB as product-term logic enables the APEX 20K device to achieve unmatched integration efficiencies. For more information on ESB product-term mode functionality, see "APEX 20K Devices Feature Product-Term Mode" on page 20.

The ESB also supports dual-port RAM and the wide range of RAM widths and depths required in a system-level design. The APEX 20KE ESB supports CAM, a parallel processing memory that accelerates applications requiring fast searches. CAM takes data input and then supplies the address that contains the data input. APEX ESBs can be cascaded together to implement larger functions.

SignalTap Logic Analysis Speeds Verification

APEX 20K devices can be used with the Quartus™ development software to implement SignalTap™ logic analysis, which allows users to capture and analyze any internal APEX 20K device signal. SignalTap logic analysis allows for reduced verification times by enabling engineers to conduct at-speed, on-the-fly functional verification.

FLEX Update

High-Density EPF10K200E Devices Available

The high-density EPF10K200E devices—featuring dual-port RAM with independent read / write ports, 9,984 logic elements (LEs), and 98,304 bits of on-chip RAM—are now available. EPF10K200E devices offer the most on-chip RAM of any device in the FLEX® 10K family; they are available today in 600-pin ball-grid array (BGA), 672-pin FineLine BGA, and 599-pin pin-grid array (PGA) packages.

PLL Available in FLEX 10KE Devices

A phase-locked loop (PLL) is available in EPF10K200E devices and is designated with a "-X" suffix in the ordering code (i.e., EPF10K200EBC600-1X). The PLL feature will be offered in all FLEX 10KE device densities in both the -1 and -2 speed grades. PLLs provide the ClockLock and ClockBoost options, which reduce clock delay and skew, and perform internal clock multiplication for simpler board designs.

Software support for FLEX 10KE PLLs is available in the MAX+PLUS® II version 9.21 and higher software.

Programmable Delay in FLEX 10KE Devices

FLEX 10KE devices provide a programmable delay feature that aids in the FLEX 10KE-1 device's compliance to the 66-MHz / 64-bit peripheral component interconnect (PCI) specification; for -2 and -3 speed grade devices, the programmable delay feature provides I / O timing enhancements for performance-critical designs. The EPF10K100E device is the first with this feature; the EPF10K130E and EPF10K30E devices will be the next devices released with this feature. EPF10K50E and EPF10K200E devices, which have already been released, will be enhanced to include the programmable delay feature. Due to its performance characteristics, the existing EPF10K50E-1 device is already compliant to 66-MHz / 64-bit PCI specifications. Software support for the programmable delay feature is available in the MAX+PLUS II version 9.2 and higher software.

More FLEX 10K Devices in BGA Packages

Altera plans to offer more FLEX 10KE devices in 1.27-mm pitch BGA packages. In addition to the EPF10K100E device in 356-pin BGA packages and the EPF10K200E device in 600-pin BGA packages, Altera is planning to offer EPF10K50E, EPF10K130E, and EPF10K200E devices in 356-pin BGA packages, and EPF10K130E devices in 600-pin BGA packages. See Table 2 on page 6 for device package availability.

FLEX 10K Product Transitions

Altera is migrating the EPF10K100A, EPF10K30A, and EPF10K10A devices from a 0.35-µm process to a 0.30-µm process. Additionally, the EPF10K50 devices are migrating from a 0.50-µm process to a 0.42-µm process. Table 1 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notification page on the Altera web site at **http://www.altera.com**.

Table 1. FLEX 10K Migration Schedule

Device	Transition Date	Reference	Process (µm)
EPF10K100A	February 1999	PCN 9810	0.30
EPF10K30A	April 1999	PCN 9810	0.30
EPF10K10A	July 1999	PCN 9810	0.30
EPF10K50	June 1999	PCN 9901	0.42

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FLEX 10K Device Availability

Table 2 shows the expected availability of all 2.5-V FLEX 10KE devices. The only FLEX 10KA device not yet released is the EPF10K50V in the 484-pin FineLine BGA package (shown in Table 2). All other 3.3-V FLEX 10KA devices are available today. MAX+PLUS II design support is currently available for most device package options.

Table 2. FLEX 10KE Device Availability

Device	Package	Speed Grade	Availability
EPF10K30E	144-pin TQFP	-1, -2, -3	June 1999
	208-pin PQFP	-1, -2, -3	June 1999
	256-pin FineLine BGA	-1, -2, -3	August 1999
	484-pin FineLine BGA	-1, -2, -3	August 1999
EPF10K50V	484-pin FineLine BGA	-1, -2, -3	March 1999
EPF10K50E	144-pin TQFP	-1, -2, -3	Now
	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FineLine BGA	-1, -2, -3	Now
	356-pin BGA	-1, -2, -3	July 1999
	484-pin FineLine BGA	-1, -2, -3	Now
EPF10K100B	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FineLine BGA	-1, -2, -3	Now
EPF10K100E	208-pin PQFP	-1, -2, -3	March 1999
	240-pin PQFP	-1, -2, -3	March 1999
	256-pin FineLine BGA	-1, -2, -3	April 1999
	356-pin BGA	-1, -2, -3	April 1999
	484-pin FineLine BGA	-1, -2, -3	April 1999
EPF10K130E	240-pin PQFP	-1, -2, -3	April 1999
	356-pin BGA	-1, -2, -3	June 1999
	484-pin FineLine BGA	-1, -2, -3	May 1999
	600-pin BGA	-1, -2, -3	June 1999
	672-pin FineLine BGA	-1, -2, -3	May 1999
EPF10K200E	240-pin RQFP *(1)*	-1, -2, -3	June 1999
	356-pin BGA	-1, -2, -3	June 1999
	484-pin FineLine BGA	-1, -2, -3	July 1999
	599-pin PGA	-1, -2, -3	Now
	600-pin BGA	-1, -2, -3	Now
	672-pin FineLine BGA	-1, -2, -3	March 1999

Note:
(1) RQFP: power quad flat pack.

FineLine BGA Packages Coming Soon for FLEX 6000 Devices

FLEX 6000 devices in FineLine BGA packages are planned to be available in the second quarter of 1999. These area-efficient packages require less than half the board space of traditional BGA packages. Table 3 shows the expected availability for FLEX 6000 devices.

Table 3. FLEX 6000 Device Availability

Package	Device			
	EPF6010A	EPF6016	EPF6016A	EPF6024A
100-Pin TQFP	✓		✓	
100-Pin FineLine BGA	Q2 1999		Q2 1999	
144-Pin TQFP	✓	✓	✓	✓
208-Pin PQFP		✓	✓	✓
240-Pin PQFP		✓		✓
256-Pin BGA		✓		✓
256-Pin FineLine BGA	Q2 1999		Q2 1999	Q2 1999

Industrial-Temperature FLEX 6000 Devices Available

FLEX 6000 devices are now available in industrial-temperature grades. There are five devices currently shipping in either 144-pin thin quad flat pack (TQFP) or 208-pin plastic quad flat pack (PQFP) packages. A sixth device in the 100-pin TQFP package is planned for release in March 1999. Table 4 lists the availability of industrial-temperature grade FLEX 6000 devices.

Table 4. Industrial-Temperature FLEX 6000 Device Availability

Device	Package	Availability
EPF6016TI144-3	144-pin TQFP	Now
EPF6016QI208-3	208-pin PQFP	Now
EPF6016ATI100-3	100-pin TQFP	March 1999
EPF6016ATI144-3	144-pin TQFP	Now
EPF6016AQI208-3	208-pin PQFP	Now
EPF6024AQI208-3	208-pin PQFP	Now

Configuration Device Update

EPC2 Reprogrammable Configuration Device Available

The EPC2, Altera's first reprogrammable configuration device, is now available. This device is offered in 20-pin plastic J-lead chip carrier (PLCC) and 32-pin TQFP packages and is pin compatible with all existing

Altera configuration devices in the same packages. A single EPC2, which can configure any FLEX device with up to 130,000 gates, can be programmed in-system using IEEE Std. 1149.1 Joint Test Action Group (JTAG) test ports. The EPC2 supports Serial Vector Format (SVF) and the Jam test programming language. The EPC2 operates at 3.3 V or 5.0 V and is supported in the MAX+PLUS II version 9.2 software.

MAX Update

MAX 9000A Device Availability

With propagation delays as fast as 10 ns, MAX® 9000A devices offer significant performance enhancements and cost reduction over existing MAX 9000 devices. All packages for the EPM9320A and EPM9560A devices are available in production quantities. Table 1 summarizes commercial- and industrial-temperature MAX 9000A device availability.

Table 1. MAX 9000A Device Availability *Note (1)*

Device	t_{PD}	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	356-Pin BGA
EPM9320A	10 ns	C, I	C, I		C
EPM9560A	10 ns		C, I	C, I	C

Note:
(1) A "C" designates commercial and an "I" designates industrial temperature.

MAX 7000A Availability

Altera has improved the performance of MAX 7000A devices, which include devices with 4.5-ns propagation delays. MAX 7000A devices support in-system programmability (ISP) and MultiVolt I/O pins, and provide pin compatibility with industry-standard MAX 7000 devices. EPM7032AE, EPM7064AE, EPM7128A, EPM7256A, and EPM7512AE devices are now shipping. Table 2 shows MAX 7000A device availability.

MAX 7000S Family

All MAX 7000S devices are now available. These devices offer features such as speed grades of 5 ns, in-system programming, open-drain output, and IEEE Std. 1149.1 (JTAG) boundary-scan testing (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in industrial temperature grades. Table 3 shows the packages and

Table 2. MAX 7000A Device Availability

Device	Package	Speed Grade	Availability
EPM7032AE	44-pin PLCC	-4, -7, -10	Now
	44-pin TQFP	-4, -7, -10	
EPM7064AE	44-pin PLCC	-4, -7, -10	Now
	44-pin TQFP	-4, -7, -10	
	100-pin TQFP	-4, -7, -10	
	100-pin FineLine BGA	-4, -7, -10	
EPM7128A	84-pin PLCC	-6, -7, -10, -12	Now
	100-pin TQFP	-6, -7, -10, -12	
	100-pin FineLine BGA	-6, -7, -10, -12	
	160-pin PQFP	-6, -7, -10, -12	
	256-pin FineLine BGA	-6, -7, -10, -12	
EPM7128AE	84-pin PLCC	-5, -7, -10	Q2 1999
	100-pin TQFP	-5, -7, -10	
	100-pin PQFP	-5, -7, -10	
	160-pin PQFP	-5, -7, -10	
	256-pin FineLine BGA	-5, -7, -10	
EPM7256A	100-pin TQFP	-7, -10, -12	Now
	144-pin TQFP	-7, -10, -12	
	208-pin PQFP	-7, -10, -12	
	256-pin FineLine BGA	-7, -10, -12	
EPM7256AE	100-pin TQFP	-6, -7, -10	Q2 1999
	100-pin FineLine BGA	-6, -7, -10	
	144-pin TQFP	-6, -7, -10	
	208-pin PQFP	-6, -7, -10	
	256-pin FineLine BGA	-6, -7, -10	
EPM7512AE	144-pin TQFP	-7, -10, -12	Now
	208-pin PQFP	-7, -10, -12	
	256-pin BGA	-7, -10, -12	
	256-pin FineLine BGA	-7, -10, -12	

Table 3. MAX 7000S Device Packages

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

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speed grades available for commercial temperature grade devices.

MAX 7000 & MAX 9000 Device Transitions

Altera has completed the migration of MAX 7000 and MAX 9000 devices from a 0.65-µm process to a 0.5-µm process. Table 4 outlines the devices that were migrated and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com**.

Table 4. MAX 7000 & MAX 9000 Process Migrations *Note (1)*

Device	Reference *(2)*	Date	Process (µm)
EPM7032	PCN 9703 ADV 9803	Complete	0.5
EPM7064 EPM7064S	PCN 9703 ADV 9708	Complete	0.5
EPM7128E EPM7128S	PCN 9703 ADV 9708	Complete	0.5
EPM7160E	PCN 9703 ADV 9803	Complete	0.5
EPM7192E EPM7192S	PCN 9703 ADV 9708	Complete	0.5
EPM7256S EPM7256E	PCN 9703 ADV 9708	Complete	0.5
EPM9320	PCN 9703 ADV 9803	Complete	0.5
EPM9560	PCN 9703 ADV 9803	Complete	0.5

Notes:
(1) The process transition will not result in any changes to data sheet parameters or ordering codes.
(2) Altera provides advisories and process change notices. Go to the Altera web site for these reference documents.

Tools Update

NativeLink Integration Offers Seamless Interface with EDA Tools

Designers developing 400,000-gate designs for the APEX 20K devices are likely to follow a flow involving the use of third-party EDA synthesis, simulation, and verification tools together with Altera's Quartus software. One of the problems with such a flow is how to pass design information between different tools. The NativeLink™ feature found in Altera's Quartus software provides an unmatched level of integration with third-party EDA tools, allowing designs to be compiled much faster and more efficiently. Third-party applications can be launched from within the Quartus software and run in the background during compilation.

The Quartus NativeLink feature was developed to ensure a seamless interface with Altera's partners. Altera provided third-party EDA partners with the application programming interface (API) specifications for the Quartus software to allow feature and database access by third-party EDA tools using C++, TCL, or Visual Basic. Through this process of integrated development, the NativeLink feature allows Quartus to easily interface with other tools.

By using the NativeLink feature to integrate third-party EDA tools with the Quartus software, the design process is simplified. Designers are not required to learn a new software package; the Quartus software will interface to a tool with which the designer is already familiar. This close integration allows error and warning messages to be traced directly back to the source file. Through the Quartus software with the NativeLink feature, information is passed more efficiently between tools, accelerating compilation and providing better timing estimates for optimal synthesis. This tightly integrated system will allow engineers to achieve high quality results when implementing designs in Altera APEX 20K devices.

Discontinued Devices Update

Altera has no new announcements regarding discontinued devices. Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

CoreSyn Synthesis

The Quartus nSTEP™ Compiler includes incremental compilation and the CoreSyn™ synthesis capability. The CoreSyn synthesis feature invokes the appropriate synthesis technology to determine the optimal mapping of a design to an Altera device's architecture.

When a design is compiled, the CoreSyn feature partitions functions into the appropriate architectural element within an APEX 20K device. For example, state machines are implemented into the product-term-based macrocell, first-in first-out (FIFO) functions are placed in ESBs, and data-paths utilize the LUT-based LEs. The engineer can also direct where a particular portion of a design is mapped within an APEX 20K device. Figure 1 illustrates the CoreSyn synthesis feature.

The CoreSyn feature, along with incremental compilation, allows designers to use the nSTEP Compiler to compile, change, and recompile a design in a fraction of the time once needed for the same process. Each piece of a design is placed in the appropriate type of APEX architecture, to ensure optimal implementation.

Altera Subscription Program Now Available

The new Altera Subscription Program offers customers a simple way to obtain Altera development software and support. With a subscription, customers receive updates to all Altera software (including both the MAX+PLUS II and Quartus software) for 12 months. Customers who have purchased subscription products will receive the Quartus software when it is released. For the duration of their 12-month subscription, they will continue to receive full-featured versions of the MAX+PLUS II and Quartus development software. At the end of your current 12-month subscription, you must purchase a renewal to use subsequent releases.

The new subscription program provides a significant reduction in cost, and is priced at only $2,000 (fixed-node product) for 12 months. Under the old Altera maintenance program, the same support would cost over $6,000 ($4,995 for the PLS-MAGNUM, and $1, 495 for one year of software maintenance). Table 1 provides a description of the Altera Subscription Program options.

Table 1. Altera Subscription Program Product Line

Product	Description of Coverage	List Price
FIXEDPC	PCs using software guards	$2,000
FLOATPC	Networked environment consisting of PC clients only	$2,200
FLOATNET	Networked environment consisting of PC, UNIX, or a combination of clients	$2,400
RENEWAL	Renew existing subscription program for additional 12 month period	$2,000
ADD-FLOATPC	Additional seats to add on to FLOATPC product	$2,200
ADD-FLOATNET	Additional seats to add on to FLOATNET product	$2,400

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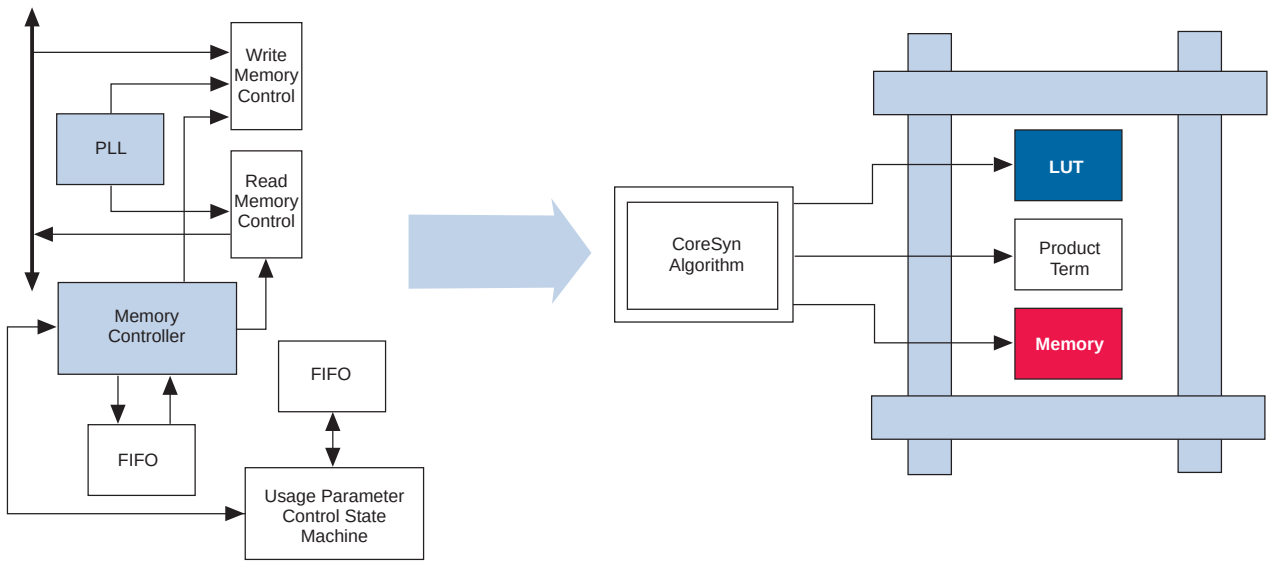
Figure 1. Quartus CoreSyn Feature



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New Adapters for Programming MAX 7000A & MAX 7000AE Devices

The MAX+PLUS II version 9.2 software offers support for new MAX 7000A and MAX 7000AE devices in FineLine BGA and BGA packages. While most designers will program these devices in-system, three new programming adapters for all speed grades are available to program these devices using the Master Programming Unit (MPU). Table 2 lists the new adapters.

See "Altera Programming Adapters" on page 26 for a list of programming adapters for MAX 9000, MAX 7000, and configuration devices.

Table 2. New MAX 7000 Adapters

Altera Part Number	Device Package	Devices Supported
PLMF7000-100	100-pin FineLine BGA	EPM7064AEFC100 EPM7128AFC100 EPM7128AEFC100 EPM7256AEFC100
PLMF7000-256	256-pin FineLine BGA	EPM7128AFC256 EPM7128AEFC256 EPM7256AFC256 EPM7256AEFC256 EPM7512AEFC256
PLMB7000-256	256-pin BGA	EPM7512AEBC256

Altera Ships MAX+PLUS II Version 9.21 Software

The MAX+PLUS II version 9.21 software is now shipping to all customers who have an active subscription or software maintenance agreement.

The MAX+PLUS II version 9.21 software will provide support for new FLEX 10KE devices with the ClockLock and ClockBoost features. To support high-speed designs, FLEX 10KE devices offer ClockLock and ClockBoost circuitry containing a phase-locked loop (PLL). The MAX+PLUS II version 9.21 software update provides support for these new features in EPF10K200EB600 and EPF10K200EF672 devices.

This latest version of the MAX+PLUS II software adds many useful features for the full line of Altera devices, including support for various new FLEX 10KE and MAX 7000AE device package combinations. Table 3 lists the new device package combinations supported by the software.

Table 3. New Devices Supported by MAX+PLUS II Software Version 9.21

Device Family	Device	Package
MAX 7000	EPM7032AE	44-pin PDIP, 44-pin TQFP
	EPM7064AE	100-pin FineLine BGA
	EPM7128A	256-pin FineLine BGA
	EPM7512AE	144-pin TQFP, 208-pin PQFP, 256-pin BGA, 256-pin FineLine BGA
FLEX 10K	EPF10K10	256-pin FineLine BGA
	EPF10K30A	256-pin FineLine BGA
	EPF10K50E	256-pin FineLine BGA, 484-pin FineLine BGA
	EPF10K200E	599-pin PGA, 600-pin BGA

The MAX+PLUS II version 9.21 software also allows designers to use the new features available in the EPC2 configuration device. This version supports programmable pull-up resistors and the programmable JTAG USERCODE instruction for the EPC2 device. With version 9.21, users can also issue a JTAG command in software that causes the EPC2 device to initiate configuration of a FLEX device on the board.

Obtain MAX+PLUS II License Files on the Web

You can go to the Altera web site to obtain your license file for the latest version of MAX+PLUS II software.

You need a new license file if you are using the MAX+PLUS II software for the first time or if you have recently renewed your subscription with Altera. Every time your subscription is renewed (typically once a year), you must obtain a new license file.

To request your license file, you need your software guard ID number (which is a 10-digit number beginning with a T), host ID, or network interface card (NIC) number and your Altera ID. Your Altera ID is printed on the mailing label of all communication you receive from Altera, including the quarterly *News & Views*.

The web-based license generator also generates licenses for the MAX+PLUS II BASELINE software.

New MAX+PLUS II BASELINE Software

The MAX+PLUS II BASELINE software is a free, entry-level version of the MAX+PLUS II software that replaces the PLS-WEB software and the ES Site License software.

The MAX+PLUS II BASELINE software version 9.2 includes a timing and functional simulator. The extensive device support capability makes the MAX+PLUS II BASELINE software the most full-featured programming logic development software available for free download from the web.

Designers can license the MAX+PLUS II BASELINE software for six months by requesting a license file from the Altera web site at **http://www.altera.com**.

Table 4 outlines the features of the MAX+PLUS II BASELINE software version 9.2.

The MAX+PLUS II BASELINE software is available for download from the Altera web site; it is also available on the ***Altera Digital Library CD-ROM***.

Table 4. MAX+PLUS II BASELINE Software Version 9.2 Features

Feature	Property
Device Support	EPF10K10, EPF10K10A, EPF8452A, EPF8282A, EPF6010A, EPF6016, EPF6016A, EPM9320, and EPM9320A devices; as well as the MAX 7000 (including MAX 7000E, MAX 7000S, MAX 7000A, and MAX 7000AE), MAX 5000, and Classic device families
Design Entry	– Schematic design entry – Text-based design entry using the Altera Hardware Description Language (AHDL) – Interfaces to popular EDA tools – Floorplan editing – Hierarchical design management – Library of parameterized modules (LPM)
Design Compilation	– Logic synthesis and automatic fitting – Automatic error location – OpenCore™ evaluation for Altera MegaCore™ functions and megafunctions from Altera Megafunction Partner Program (AMPP℠) partners
Design Verification	– Functional and timing simulation – Timing analysis – Creates output files for use with third-party simulators
Programming	Device programming *(1)*
Other Features	On-line help

Note:

(1) You can use the Altera Stand-Alone Programmer (ASAP2) software, which is a stand-alone version of the MAX+PLUS II Programmer application, to program, verify, examine, and test Altera devices without having the full version of the MAX+PLUS II software. The ASAP2 software can be downloaded from the Altera FTP site at **ftp.altera.com**.

Technical ARTICLES

Using Altera Devices in Multiple Voltage Systems

Although the 5.0-V interface has been a standard for decades, the move towards advanced process technology requires a shift to lower voltage levels. In today's market, printed circuit boards (PCBs) are assembled with a mixture of 5.0-V, 3.3-V, and 2.5-V devices. To accommodate this mixture, it is essential that these devices interface with systems of differing supply voltages.

Altera's MultiVolt™ I/O interface meets the increasing demand for compatibility with devices of different voltages. The MultiVolt interface separates the power supply voltage from the output voltage, enabling Altera devices powered at a specific core voltage level to interface with devices of other voltage levels.

MultiVolt Interface

A 3.3-V power supply is required for 0.35-µm process technologies, and 0.25-µm process technologies require a 2.5-V power supply. Therefore, many of today's devices require a 5.0-V, 3.3-V, or 2.5-V interface. In the future, even lower voltage levels will be required for smaller geometry processes.

To accommodate future trends, Altera has developed the broadest range of devices that support the MultiVolt I/O interface for mixed-voltage system integration (see Table 1). The MultiVolt I/O interface enables devices of different voltages to communicate in a mixed-voltage design environment. The `VCCINT` pins power the device core, and the `VCCIO` pins power the I/O buffers. Therefore, the device core and I/O pins can be powered up with separate supply voltages. However, all of the `VCCIO` pins on a device with MultiVolt capability should be supplied from the same voltage level (e.g., 2.5 V, 3.3 V, or 5.0 V).

2.5-V, 3.3-V & 5.0-V Device Compatibility

In 2.5-V FLEX® 10KE devices, the `VCCINT` pins must always be connected to a 2.5-V power supply. With a 2.5-V V_{CCINT} level, input voltages are compatible with 2.5-V, 3.3-V, and 5.0-V inputs. The `VCCIO` pins can be

Table 1. Altera MultiVolt I/O Support *Note (1)*

Device	V_{CCINT} (V)	V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
			1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
FLEX 10K, FLEX 8000 *(2)*, FLEX 6000 (5.0 V), MAX 9000, MAX 7000S	5.0	5.0			✓	✓				✓
		3.3			✓	✓			✓	✓
EPF10K130V, EPF10K50V	3.3	3.3			✓	✓			✓	✓
FLEX 10KA, FLEX 6000 (3.3 V), MAX 7000A, MAX 7000AE	3.3	3.3		✓	✓	✓			✓	✓
		2.5		✓	✓	✓		✓		
FLEX 10KE	2.5	3.3		✓	✓	✓			✓	✓
		2.5		✓	✓	✓		✓		
APEX 20K	2.5	3.3		✓	✓			✓	✓	
		2.5		✓	✓			✓		
APEX 20KE	1.8	3.3	✓	✓	✓			✓	✓	
		2.5	✓	✓	✓			✓		
		1.8	✓	✓	✓		✓			

Notes:

(1) All FLEX 10K devices support 3.3-V I/O pins with a 5.0-V core, except 84-pin plastic J-lead chip carrier (PLCC) and 240-pin quad flat pack (QFP) packages. In the MAX 7000 family, EPM7032S and EPM7064S devices in the 44-pin PLCC and thin quad flat pack (TQFP) packages do not support 3.3-V I/O pins with a 5.0-V core. These devices do not have separate `VCCINT` and `VCCIO` pins.

(2) The I/O pins on the EPF8282V device are not 5.0-V tolerant. Altera does not recommend driving 5.0-V signals to these 3.3-V devices.

connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems.

When using Altera's newer 3.3-V devices—including 3.3-V FLEX 6000 devices, as well as all FLEX 10KA and MAX® 7000AE devices—the VCCINT pins must be connected to a 3.3-V power supply. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. EPF10K50V and EPF10K130V devices must have their VCCIO pins connected to 3.3 V. Inputs can be driven by 2.5-V, 3.3-V, or 5.0-V systems with the exception of the EPF10K50V and EPF10K130V devices, which can only be driven by 3.3-V and 5.0-V systems.

Altera's 5.0-V MAX 7000, MAX 7000S, MAX 9000, FLEX 8000, FLEX 6000, and FLEX 10K devices support interfaces to 3.3-V and 5.0-V devices. When the VCCIO pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems.

5.0-V TTL Compatibility

All Altera devices are 5.0-V TTL compatible. Therefore, a 3.3-V device can drive a 5.0-V device and, in turn, can be driven by 5.0-V devices. Also, when the VCCIO pin of Altera devices are connected to 3.3 V, the I/O pins can still be driven by 5.0-V signals because the I/O buffers are still 5.0-V tolerant. The only exception is in the EPF8282V device, whose I/O pins are not 5.0-V tolerant (see Table 1, Note 2).

5.0-V CMOS Compatibility

Altera 5.0-V devices with NMOS-only output buffers will meet 5.0-V TTL levels. When voltage at the output pin exceeds approximately 3.8 V, the NMOS pull-up transistor is in cut-off mode. Therefore, the output pin can be reach the full 5.0-V level with an external pull-up resistor.

To make the output signals from Altera 3.3-V devices compatible with 5.0-V CMOS, configure the output pins as open-drain pins. The 3.3-V devices have a CMOS driver; if $V_{OUT} > V_{CCIO}$, the PMOS pull-up transistor will continue to conduct, preventing an external pull-up resistor from pulling the signal to 5.0 V. To pull up the output of a 3.3-V device to the VIH level of a 5.0-V CMOS device, use an open-drain pin driving a trace that is pulled up to 5.0 V through an external pull-up resistor.

The open-drain pin never drives high, only low or tri-state. When the open-drain pin is active, it drives low. When the open-drain pin is inactive, the pin is tri-stated, and the trace pulls-up to 5.0 V—within the device's operating conditions—by the external resistor.

Conclusion

The Altera MultiVolt interface allows designers to seamlessly incorporate newer generation devices with devices of varying voltage levels. PCBs are often a mix of 2.5-V, 3.3-V, and 5.0-V devices. The MultiVolt interface enables the device core to run at a specific voltage (2.5 V, 3.3 V, or 5.0 V), while keeping the I/O pins compatible with 5.0-V, 3.3-V, or 2.5-V logic levels. The combination of MultiVolt I/O and hot-socketing (see "Hot-Socketing" on this page) allow Altera devices to fulfill any design requirement.

Hot-Socketing

Hot-socketing or hot plug-in refers to the practice of inserting or removing a board or device from a system board while system power is on. When the board is plugged in or removed, it cannot disturb the system operation.

Altera has designed devices to support hot-socketing. The following features have been implemented in Altera devices to ease the hot-socketing process:

- Devices can be driven before power-up without damaging the device.
- Devices do not drive out before or during power up.
- Signal pins cannot drive the V_{CCIO} or V_{CCINT} power supply.

Most 3.3-V and 2.5-V Altera devices are designed to support hot-socketing without any special design requirements. These devices include FLEX 10KA, FLEX 10KE, FLEX 6000 (3.3-V), and MAX 7000AE devices.

continued on page 15

Embedded Programming Using the 8051 Microprocessor & Jam Byte-Code

In-system programming and in-circuit reconfiguration via an embedded processor enables easy design prototyping, streamlines production, and allows quick and efficient in-field upgrades. Devices that support in-system programmability (ISP) or in-circuit reconfigurablity (ICR) can be upgraded in the field by downloading new design information using ROM, FLASH cards, modems, or other data links.

This article outlines Altera® support for embedded programming and configuration using the 8051 family of microprocessors and a Jam™ Byte-Code File (**.jbc**). The MAX+PLUS® II software generates JBC Files, which contain specific design information for a given IEEE Std. 1149.1 Joint Test Action Group (JTAG) chain topology. See *Application Note 111 (Embedded Programming Using the 8051 Processor & Jam Byte-Code)* and *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* for more information on 8051 processor support and Jam Byte-Code.

8051 Architecture

The 8051 family of microprocessors is inexpensive, easy to use, and a proven platform for managing simple processing tasks. The 8051 architecture consists of separate ROM and RAM addressing. Figure 1 illustrates the 8051 architecture as it applies to memory.

The 8051 microprocessor retrieves and executes instructions from ROM or "program memory". Part of the instruction execution involves controlling I/O pins that provide access to ROM, RAM, I/O ports, and addresses. For example, when the 8051 microprocessor receives an instruction to access external data, or RAM, the processor automatically toggles the !RD pin such that the information in the RAM is retrieved and stored in the appropriate internal registers. These actions are performed automatically by the processor.

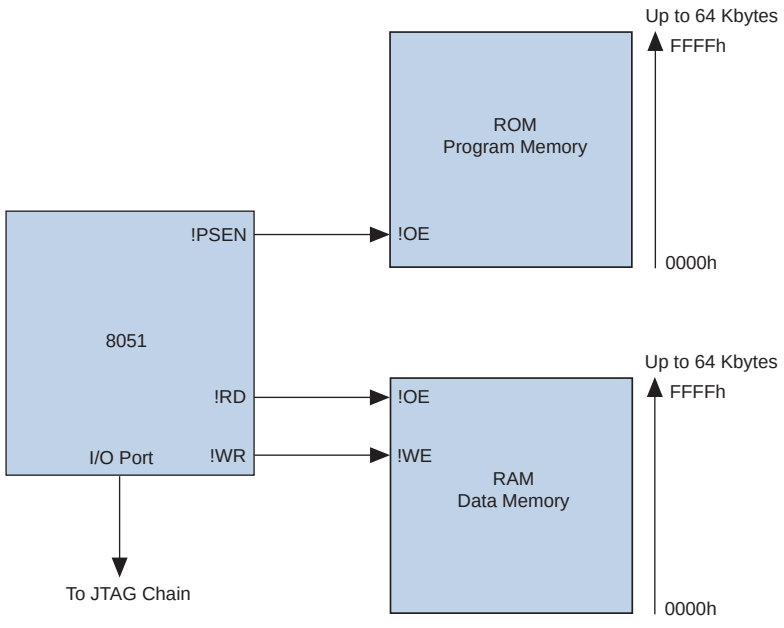
The 8051 processor can retrieve programming or configuration information from EPROM or FLASH devices. The 8051 can access up to 64 Kbytes of ROM and 64 Kbytes of RAM, and can be extended by paging additional memory. However, paging memory requires additional discrete logic between the 8051 micro-processor and associated memory, which slows access and programming times.

Many variants of the basic 8051 architecture exist, including different clock speeds (12 to 50 MHz), 8- or 16-bit functions, and 0 to 24 Kbytes of on-chip ROM. When programming devices that contain more than 64 macrocells, Altera recommends using the fastest 8051 microprocessor for the best programming times.

Jam Byte-Code Software

The Jam Byte-Code Player, which is coded in the C programming language, and a JBC File are needed to program or configure Altera devices using an 8051 processor. If the default configuration of the source code is not compatible with a particular processor, the code can be customized for a specific 8051 microprocessor. However, the supporting compiler must be able to compile C code. The Jam Byte-Code Player source code can be obtained by contacting Altera Applications at (800) 800-EPLD, or

Figure 1. 8051 Architecture



sending e-mail to **sos@altera.com**. For more information on how to customize source code, see *Application Note 111 (Embedded Programming Using the 8051 Processor & Jam Byte-Code).*

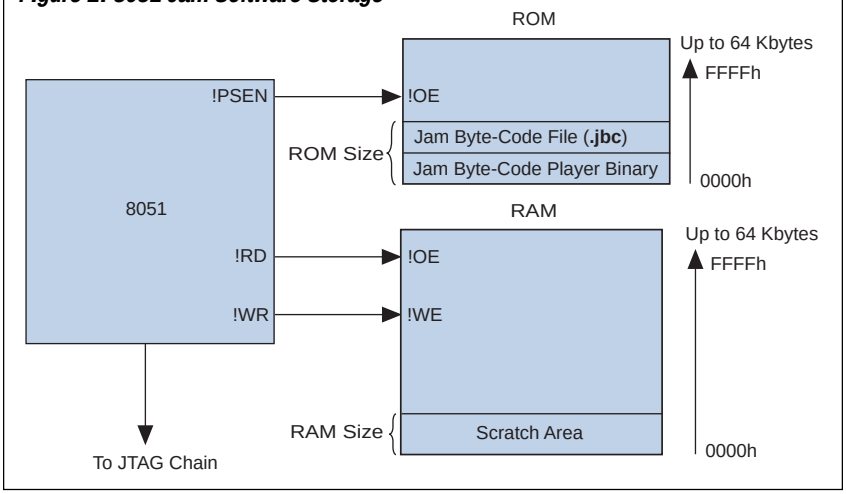
The JBC File can be generated using the MAX+PLUS II software, or by compiling an existing ASCII-based Jam File (**.jam**) into a Jam Byte-Code equivalent using the stand-alone Jam Byte-Code Compiler. The compiler is available from the Jam web site **http://www.jamisp.com**. Figure 2 shows one way to store the Jam software in an 8051 embedded system.

Although Figure 2 shows the JBC File stored in ROM, the file could also be stored and executed in RAM. In either case, the Jam Byte-Code Player must be run by the 8051 processor, and must have access to the JBC File.

Conclusion

The 8051 Jam Byte-Code Player supports ISP, giving the designer the option of performing in-field upgrades. ISP and ICR, also supported by the 8051 microprocessor, work together to speed up the design process. To simplify things further, the source code is provided to make porting easier and to support the ability to upgrade to a variety of device densities. This source code is specific to the 8051 family of microprocessors and its configuration can be altered to fit any 8051 microprocessor variant. Additionally, programming file generation is offered in the MAX+PLUS II software.

Figure 2. 8051 Jam Software Storage



Hot-Socketing, continued from page 13

These user I/O pins and dedicated input or dedicated clock pins on these devices can be driven before and during power up without any device damage. Their pins do not drive out before or during power up and configuration. Additionally, there is no leakage current from I/O, dedicated input, or dedicated clock pins to VCCIO or VCCINT pins before V_{CCIO} and V_{CCINT} are powered up. Therefore, these devices may be inserted into (or removed from) a powered-up system board without damage or without interfering with the operation of the system board.

During normal operation, these devices have an input leakage current specified under the DC operating conditions in each device data sheet. This leakage current is 10 µA for devices that support hot-socketing. Table 1 shows the leakage current that may occur during hot-socketing.

For better system flexibility, Altera has designed these devices to support hot-socketing operation.

Table 1. Hot-Socket DC Leakage Current for Altera Devices

Device	Condition	Maximum
FLEX 10KA FLEX 10KE FLEX 6000 (3.3 V)	V_{CC} = 0 V $V_{IN} \leq$ 5.75 V *(1)*	300 µA *(2)*
MAX 7000AE	V_{CC} = 0 V $V_{IN} \leq$ 3.6 V *(3)*	300 µA *(2)*
	V_{CC} = 0 V $V_{IN} \leq$ 5.75 V *(3)*	

Notes:

(1) These devices are 5.0-V tolerant.

(2) Includes current from weak pull-up resistors in the I/O cell.

(3) The OE1 and GCLRn pins in MAX 7000AE devices may be driven up to 3.6 V during hot-socketing. All other pins may be driven to 5.75 V during hot-socketing. After hot-socketing, all pins are 5.0-V tolerant.

Customer Application

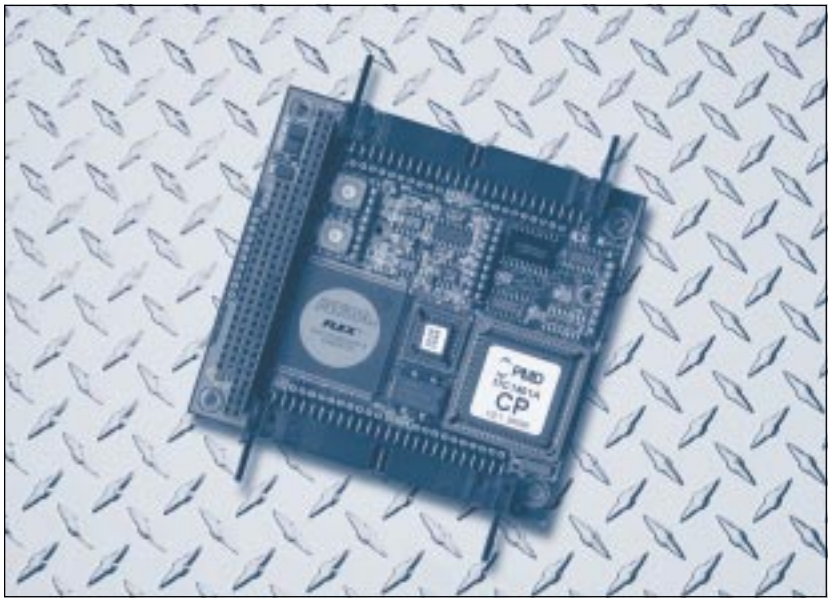
FLEX 10K Device Is Key in Creating a Fully Featured, Compact Motion Controller

The architecture and capacity of the FLEX 10K device enabled the Tech 80 engineers to include all the digital functionality of the 5950B on a single FLEX 10K device.

Recently, engineers at Technology 80, Inc. (Tech 80), a manufacturer of motion control products, set a goal: design a new, fully featured four-axis servo motion controller that would be compliant with the PC/104 specification version 2.3. The challenge was to fit all the functionality of this complex controller onto a board measuring just 3.55 × 3.78 inches. The product would be the industry's first fully featured four-axis motion controller to fit the PC/104 industry-required form factor. The solution they chose was simple: they took an existing design that had required a larger board and several devices and ported it to a single Altera® FLEX® 10K device.

The resulting product is the 5950B four-axis PC/104 servo motion controller (see Figure 1). Because of its small size, the controller is useful in packaging machinery, robotics, and medical instrumentation. The 5950B chipset consists of a PMD 1401A digital signal processing (DSP) device and an Altera EPF10K30 device.

Figure 1. Technology 80 Inc. 5950B Four-Axis PC/104 Servo Motion Controller



FLEX 10K Device Allows Enhancements

The architecture and capacity of the FLEX 10K device enabled the Tech 80 engineers to include all the digital functionality of the 5950B in a single FLEX 10K device, not just the PC/104 bus interface, as shown in Figure 2. They were also able to add a number of enhancements to the design to make the controller more precise and easier to use.

For the Tech 80 engineers, precision control was a top priority in designing the 5950B. The FLEX 10K device made it possible to design the board's analog output section using a true instrumentation-quality 16-bit digital-to-analog converter (DAC). In the 5950B, the DAC is monotonic, adjusting to compensate for any low-level deviations in the analog output circuitry and ensuring servo loop stability.

To simplify the set-up of the 5950B, the Tech 80 engineers eliminated all jumpers and potentiometers. The default configuration for the board is programmed into the FLEX 10K device at the factory; users can easily reconfigure the 5950B using the setup software.

The embedded array block (EAB) architecture of the FLEX 10K device, with its capability to implement on-chip memory, allowed the Tech 80 engineers to configure RAM for an internal register overlay and ROM for powerful register addressing capabilities.

In addition, the board space saved by using the FLEX 10K device gave Tech 80 designers the opportunity to add other

enhancements to the product, such as greater I/O protection, enhanced interface specifications, and a fuller set of axis I/O signals.

MAX+PLUS II Software Speeds Development

The powerful simulation and timing analysis features of the MAX+PLUS II software shortened the development time of the 5950B design project. The MAX+PLUS II Simulator allowed the engineers to verify the project before it was committed to hardware, shortening the time needed to transform their original design to fit the FLEX 10K device. With the Timing Analyzer, they could analyze the project performance, tracing all the signal paths in the project to determine the critical speed paths. "The power and ease of use of the MAX+PLUS II development software helped minimize the amount of bench time needed to bring the product from design to release," said Jim Sandell, senior engineer at Tech 80.

Four New Products, One PCB

During the development process, the engineers decided to move the analog circuitry onto a plug-in daughter board. The 5950B could then be sold without the analog circuitry and offer cost savings to customers who only use a digital motor interface. That way, the company could use the same PCB design for three other new products in addition to the 5950B. "This decision will allow us to maximize the volume and minimize the cost of the PCB," said Jim Burkett, Tech 80 COO.

The basic Altera design has worked so well that Tech 80 plans to port it to other platforms where they already have designs. Designing and exchanging the bus interface will be a simple task that will minimize nonrecoverable engineering (NRE) costs and development time. Converting the core Altera design and the support circuitry will help the company maximize its product family coherence and minimize costs.

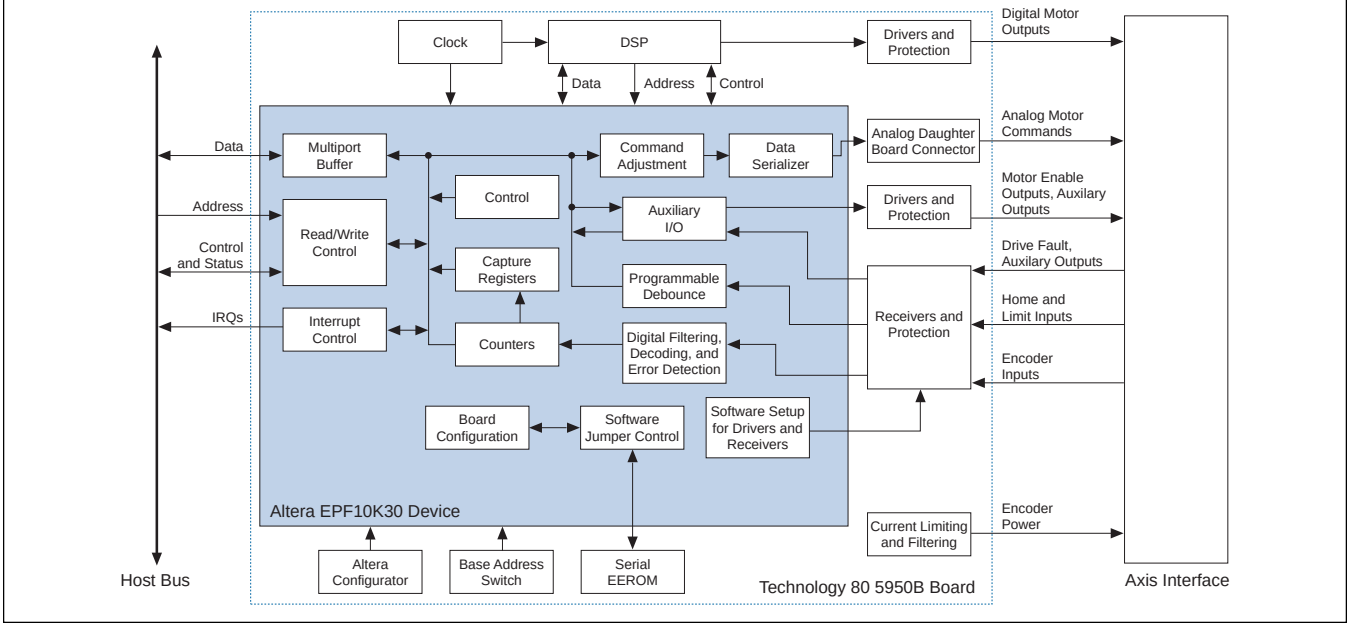
"The power and ease of use of the MAX+PLUS II development software helped minimize the amount of bench time needed to bring the product from design to release."
—Jim Sandell, Senior Engineer, Tech 80

Conclusion

Moving all the digital functionality of the 5950B into a single EPF10K30 device saved Tech 80 board space, design time, and implementation costs. At the same time, the new design increased the ease of use, precision, and flexibility of the 5950B motion controller. With Altera devices and software, current and future Tech 80 motion control designs will benefit from the easy integration of a system into a single device.

Contact Information:
Technology 80, Inc.
658 Mendelssohn Ave. No.
Minneapolis, MN 55427
(612) 542-9545
http://www.tech80.com

Figure 2. 5950B Design Architecture



Questions & ANSWERS

Q *Does the Programmer Object File (**.pof**) change between versions of MAX+PLUS® II software?*

A If you recompile a design created in an older software version in a newer software version, the POF may not be identical, for example, because of different logic synthesis or improved routing algorithms. Back-annotating your design locks down the location of the logic, not the routing. Therefore, even if you do not change the design or the assignments, the routing may still differ, resulting in a different programming file.

The latest version of the MAX+PLUS II Programmer can always read POFs created in previous versions of MAX+PLUS II software.

Q *Why do I receive the error: "Can't program or configure device 'EPFxxxx' in a multi-device JTAG chain—delete programming file from device information?"*

A You will receive this error if you try to create a Serial Vector Format File (**.svf**) for a device chain that contains a FLEX® device; FLEX devices do not support SVF Files.

Because of the file size and configuration time, SVF Files cannot be used to configure FLEX devices. SVF Files are used primarily by in-circuit testers. Configuring FLEX devices with in-circuit testers is not recommended because when the board with the FLEX device is removed from the tester, the configuration information is lost.

To configure FLEX devices via the IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface using in-circuit testers or embedded processors, you can use the Jam™ or Jam Byte-Code language. The Jam language is an interpreted language that is optimized for configuring devices via the JTAG interface.

For more information on the Jam language, refer to the Jam web site at **http://www.jamisp.com**.

Q *What are the FLEX 10KE voltage supply levels for V_{CCIO} and V_{CCINT}?*

A For FLEX 10KE devices, V_{CCINT} must be 2.5 V, but V_{CCIO} can be either 2.5 V or 3.0 V. For more information on the MultiVolt™ capabilities of FLEX 10KE devices, see the *FLEX 10KE Embedded Programmable Logic Family Data Sheet* or "Using Altera Devices in Multiple Voltage Systems" on page 12.

Q *Why do MAX® 7000A, MAX 7000AE, MAX 7000S, and MAX 9000 device programming times vary depending on whether I use a Master Programming Unit (MPU), PC, or a third-party programmer?*

A Programming times for MAX 7000A, MAX 7000AE, MAX 7000S, and MAX 9000 devices using different programming hardware may vary. Additionally, you may notice slower programming times when using slower programming hardware.

If you are particularly sensitive to variations in programming times, Altera recommends using in-circuit testers and fixed-algorithm devices (these devices have an "F" suffix at the end of the ordering code). When using "F" devices with in-circuit testers, programming times are the same for each device. If you cannot use in-circuit testers and "F" devices, you can use a faster PC to reduce the overall programming time. A faster PC will not eliminate differences in programming times, but it does reduce the overall programming time.

Q *Why doesn't my PLS-WEB license work with the MAX+PLUS II BASELINE software?*

A The PLS-WEB version 9.01 and BASELINE version 9.1 software are both licensed using a **license.dat** file and have the same feature set. However, because the products are different versions, the licensing scheme and the contents of the FEATURE line in the **license.dat** file are different. You must use the appropriate FEATURE line for the software to work properly.

A sample license file for PLS-WEB version 9.01 is shown below:

```
FEATURE max2.es alterad 0000.00 15-jun
    1999 uncounted D64F2D5DAE78 \
HOSTID=DISK_SERIAL_NUM=d8452f2f
```

A sample license file for BASELINE version 9.1 is shown below (the red text differs from the PLS-WEB license):

```
FEATURE maxplus2web alterad 1999.06
    15-jun-1999 uncounted \
626CE8C32D52
    HOSTID=DISK_SERIAL_NUM=d8452f2f
```

If you want to license *both* versions of software with the same license file, you can combine the two FEATURE lines in one **license.dat** file. Then, point to this file in both the PLS-WEB and BASELINE software.

Q *How do I convert Jam Files (**.jam**) and Jam Byte-Code Files (**.jbc**) for storage in embedded memory?*

A Jam Files (**.jam**) and Jam Byte-Code Files (**.jbc**) are ASCII and binary file types, respectively. Although the information contained in each file is unique, the files have a consistent format. Therefore, you can use your EPROM or FLASH memory programmer to convert these files to a format the programmer can use. For example, a device programmer can read ASCII files and program an EPROM or FLASH device automatically. For FLASH devices that are programmed in system, contact the FLASH vendor for information about the format of the data that is sent to the FLASH device during programming.

Additionally, a wide variety of conversion utilities are available that can convert ASCII and binary files to any number of required output formats for programming various memory technologies.

Q *Why do I get the error: "Can't open file <filename>**.pof**" (JTAG Chain File)?*

A JTAG Chain Files (**.jcf**) contain the name and location of the Programmer Object File(s) (**.pof**) needed to program a device. The JCF does not contain the actual POFs.

You may receive this error message if you load a JCF into the MAX+PLUS II software using the Multi-Device JTAG Chain dialog box (JTAG menu) if the location of any POFs referenced in the file has changed.

To avoid this error, make sure the location of the POFs does not change, for example by saving the JCF and the POFs in the same directory.

Q *Do EPF10K100B devices have weak I/O pull-up resistors for use during configuration?*

A No, EPF10K100B devices do not have weak I/O pull-up resistors. During configuration, I/O pins are tri-stated and the voltage at these pins is undefined. If these pins are connected to input pins that must be at a known voltage level, these pins should be pulled-up (or down depending on your design requirements) externally through a pull-up (or down) resistor.

Other FLEX 10KE devices have weak I/O pull-up resistors that are activated before and during configuration. See the *FLEX 10KE Embedded Programmable Logic Family Data Sheet* for more information.

Q *How do I perform JTAG testing for a JTAG chain containing EPM7032S and/or EPM7064S devices, which do not have boundary-scan test circuitry?*

A EPM7032S and EPM7064S devices do not contain JTAG boundary-scan test circuitry; however, they do contain a JTAG test access port (TAP) controller. Additionally, these devices contain the circuitry necessary to ensure that they do not interfere with any JTAG test operation. Therefore, systems that support in-system programmability (ISP) can have these devices in the JTAG chain. The devices allow the following JTAG instructions:

- ISP Instructions—The devices' JTAG controller allows JTAG-compliant ISP instructions, which are used to send instructions and data to the device for in-system programming.
- BYPASS—When either device is included in a JTAG chain, the device must be bypassed. To support this function, these devices contain the JTAG BYPASS instruction.
- EXTEST and SAMPLE/PRELOAD—These devices support the EXTEST and SAMPLE/PRELOAD instructions even though they cannot be tested because test tools often send EXTEST and SAMPLE/PRELOAD instructions to all devices in the chain. Although EPM7032S and EPM7064S devices cannot be tested when these instructions are loaded, a boundary-scan register length of one is selected. The JTAG specification allows the EXTEST and SAMPLE/PRELOAD instructions to have any bit pattern. The EPM7032S and EPM7064S devices have different bit patterns than other members of the family that do have full JTAG boundary-scan test circuitry.

The boundary-scan description language (BSDL) file for these devices represents the bit patterns to select these instructions. All JTAG information on these devices is contained in their respective BSDL files, which are available on the Altera web site.

APEX 20K Devices Feature Product-Term Mode

Altera® APEX™ 20K devices feature the revolutionary MultiCore™ architecture, which combines the strengths of look-up table (LUT) and product-term logic. The integration of these two architectures makes APEX 20K devices well suited for System-on-a-Programmable-Chip™ designs.

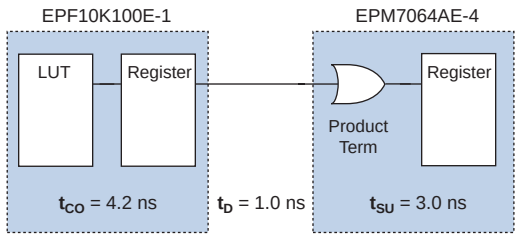
APEX 20K Architecture

The basic building block of the APEX 20K family is the MegaLAB™ structure, which contains 16 logic array blocks (LABs), each comprised of 10 logic elements (LEs). An APEX 20K MegaLAB structure also has an embedded system block (ESB) that is configurable as 2,048-bit RAM, ROM, or content addressable memory (CAM), or as 16 product-term macrocells. Each macrocell contains two product terms that can be combined through an OR gate or an XOR gate, and a programmable inverter for wide-input OR functions. The output of each macrocell can be registered, with each register containing a clock enable and an asynchronous clear. Additionally, the ESB macrocell includes parallel expanders that can feed or be fed by an adjacent macrocell. Parallel expanders improve system performance and routability, making the ESB product-term architecture ideal for applications that require wide multiplexing and high fan-in.

Improved Performance

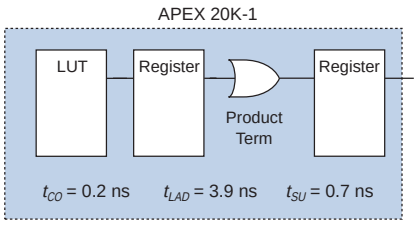
The MultiCore architecture improves system performance because the product-term architecture provides higher performance for combinatorial functions such as address decoding and state machines, while the LUT architecture contributes superior performance for registered data path functions. Off-chip delays that would occur if the design used separate LUT and product-term devices are eliminated. Figure 1 shows system performance using separate LUT and product-term devices, including a typical off-chip delay. Figure 2 shows system performance with integrated LUT and product-term architectures.

Figure 1. System Performance Using Separate Devices



Delay = 4.2 ns + 1.0 ns + 3.0 ns = 8.2 ns

Figure 2. System Performance For APEX 20K-1 Devices



Delay = 0.2 ns + 3.9 ns + 0.7 ns = 4.8 ns

Table 1. APEX Performance for Common Applications

Function	Performance Comparison					
	Product Terms		LUTs		Ideal Solution	
	Performance (MHz)	Utilization	Performance (MHz)	Utilization	Product Term	LUT
32-bit AND gate with registered inputs and outputs	192	1 product term (die size equivalent to 1.6 logic elements) *(1)*	172	8 logic elements *(1)*	✓	
8-state, 6-input/11-output, 148-transition state machine	76	204 product terms (die size equivalent to 319 logic elements)	66	366 logic elements	✓	
16-to-1 registered I/O multiplexer	149	20 product terms (die size equivalent to 30 logic elements) *(1)*	185	10 logic elements *(1)*		✓
8 × 8 registered I/O multiplier	52	702 product terms (die size equivalent to 1,097 logic elements) *(1)*	188	135 logic elements *(1)*		✓

Note:
(1) Count does not include input registers.

Design functionality such as wide-input functions and state machines are implemented more efficiently because the two architectures in one device results in better performance and device utilization.

Table 1 shows the performance for common functions implemented in product terms and LUTs, and gives the corresponding device utilization for each implementation. 32 product terms require the same die area as 50 LEs. The wide-input AND gate and state machine are faster and implemented more efficiently in the product-term architecture, while the multiplier and multiplexer are better implemented in the LUT.

Quartus Software Support

You can use the Quartus™ software to configure the ESB to act as a block of macrocells on an ESB-by-ESB basis, allowing maximum flexibility. The following ESB modes are available: product-term, RAM, ROM, CAM, or LUT.

For more information on the APEX 20K devices and Quartus software, contact Altera Applications at (800) 800-EPLD or visit the Altera web site at **http://www.altera.com**.

Altera NEWS

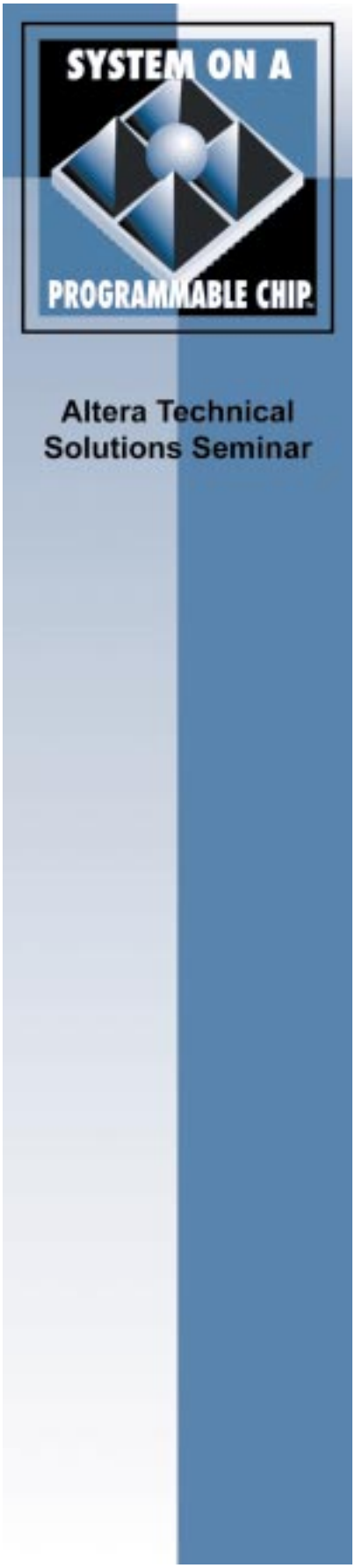
Revolutionary Quartus Software Enhances Design Process

Programmers can design and compile much more efficiently with Altera's new Quartus™ development system. This revolutionary software, combined with the Altera® APEX™ architecture, allows designers to exceed the one-million-gate mark. The size and complexity of the APEX 20K devices create additional challenges when implementing a design. The Quartus software simplifies the entire design process, allowing programmers to work more efficiently and shorten their time-to-market.

There are many new features found in the Quartus development system to enhance design productivity:

- *Workgroup computing*—Multiple designers can work on a single project with global file management and design revision control.
- *Integrated logic analysis functionality*—The SignalTap™ logic analyzer within the software offers system-level verification of devices running at speed, which significantly reduces verification times.
- *EDA tool integration*—The NativeLink™ interface connects the Quartus software seamlessly to and from other synthesis and design verification tools, also reducing verification times. For more information on the NativeLink feature, see "NativeLink Integration Offers Seamless Interface with EDA Tools" on page 8.
- *Multi-processor support*—Computer-intensive functions are distributed to multiple processors locally, across networks, and across operating systems, reducing compilation times.
- *Incremental compilation*—The nSTEP™ Compiler permits fast, multiple iterations for small portions of a design, offering huge savings in compilation time.
- *Intellectual property (IP) integration*—A block-based design orientation allows easy integration of megafunctions with OpenCore™ evaluation and MegaWizard™ Plug-In parameterization; blocks are placed to optimize timing.
- *Improved quality of results*—The CoreSyn™ synthesis capability is used to invoke the appropriate synthesis technology and determine the optimal mapping of a design to the device architecture. The Compiler analyzes the design and then partitions functions into the appropriate type of memory within the APEX 20K architecture. For more information on the CoreSyn feature, see "CoreSyn Synthesis" on page 9.
- *Internet connectivity*—The Quartus software is "web-aware," with the latest Internet browser technology built in.

All customers who have purchased an Altera subscription product will receive the Quartus software when it is released. To purchase an Altera subscription product, contact your local Altera sales office.



Altera Technical Seminars Provide System-on-a-Programmable-Chip Solution

Altera invites you to attend a free technical seminar, providing you with the information you need to stay ahead of your competition. You'll learn the details of the new Altera® APEX™ architecture, see demonstrations of the revolutionary Quartus™ development system, and learn how the devices and software support System-on-a-Programmable-Chip™ solutions. These revolutionary products offer the design flexibility, performance, and density you need to get your products to market faster, more easily, and at a lower cost than you ever imagined possible.

North American customers can reserve their space at the nearest free Altera technical seminar by either registering on the Altera web site at **http://www.altera.com/seminar** or calling (800) 9-ALTERA. International customers should register on the Altera web site or call their local Altera representative to register for any of the European or Asian seminars.

North America

Arizona	
Phoenix	March 18
California	
Rohnert Park	March 8
Santa Clara	March 9
Santa Clara	March 10
Woodland Hills	March 15
Costa Mesa	March 16
San Diego	March 17
Canada	
Mississauga	March 16
Kanata	March 17
Colorado	
Westminster	March 11
Florida	
Tampa	March 15
Georgia	
Norcross	March 18
Illinois	
Itasca	March 9
Maryland	
Gaithersburg	March 17
Massachusetts	
Westford	March 23
Minnesota	
Minneapolis	March 10
New Jersey	
Cherry Hill	March 22
Warren	March 24
New York	
Rochester	March 18
North Carolina	
Raleigh, Research Triangle Park	March 16
Ohio	
Fairborn	March 8
Oregon	
Beaverton	March 16
Texas	
Austin	March 11
Richardson	March 12
Utah	
Salt Lake City	March 15
Washington	
Bellevue	March 17

Europe

France	
Paris	March 24
Germany	
Munich	March 23
Italy	
Milan	March 22
Sweden	
Stockholm	March 26
United Kingdom	
Berkshire	March 25

Asia Pacific

Japan	
Tokyo	May 14
Osaka	May 21
Yokahoma	May 19
Taiwan	
Hsinchu	May 24

Newest AMPP Partner Offers SONET, ATM & POS Test Boards

Altera's latest Altera Megafunction Partner Program (AMPP[SM]) partner, Innocor, is a licenser and original equipment manufacturer (OEM) of data communication products based in Ontario, Canada. The company provides its customers with design services that target Altera® devices. Founder Randy Gill first designed with Altera devices and tools while working at Nortel. In 1995, he used his knowledge of data communication designs to build an 11-person engineering team: Innocor.

Innocor has developed an OC-1 / OC-3 tester product from their data communication megafunctions. The Innocor TestPoint OC-1 / OC-3 tester, shown in Figure 1, includes a customizable embedded web server and showcases Innocor's Synchronous Optical Network (SONET), asynchronous transfer mode (ATM), and Packet Over SONET (POS) functions optimized for Altera devices. By using a retargetable architecture featuring an Altera EPF10K100A device, Innocor is able to provide a cost-effective feature migration path. With its SONET, ATM, and POS test capabilities, this premier product supports an extensive feature set. Additionally, when the TestPoint OC-1 / OC-3 tester is configured with a modified software image, it can be used as a versatile SONET, ATM, and POS intellectual property demonstration and development platform.

Figure 1. Altera EPF10K100A Device Featured in Innocor's TestPoint OC-1/OC-3 Tester

Innocor offers megafunctions that are designed, optimized, and marketed exclusively for Altera's programmable logic devices (PLDs). Their list of Altera-specific products includes:

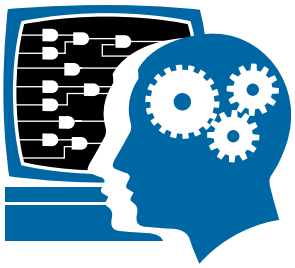
- 8030 serial commmunications controller
- Monosync / bisync controller
- SDLC / HDLC controller
- Data encoder / decoder
- Cyclic redundancy code (CRC) generator / detector
- Digital phase-locked loop (PLL)
- 8036 CIO
- 8259 programmable interrupt controller (PIC)
- SONET byte telecommunication bus interface
- SONET VT1.5 mapper
- SONET VT1.5 extractor
- PPP over SONET controller

Innocor has extensive experience in producing high quality designs for real-world data communication applications using Altera devices. Partnering with Altera and Innocor can greatly reduce your design costs and time-to-market. The Innocor solution extends well beyond megafunctions to include extensive customer support, design consultation, and a commitment to product evolution.

For additional information, including pricing, contact Innocor Ltd. at:

Innocor Ltd.
Attn: Randy Gill
7 Mill Street, Suite 300
Almonte, ON
Canada K0A 1A0
Tel: (613) 256-5339
Fax: (613) 256-5161
info@innocor.com
http://www.innocor.com

Altera Technical Training Program



The Altera Technical Training Program offers customers a wealth of information on how to use Altera devices efficiently. These classes explain how designs can be implemented to achieve optimal performance. Courses that focus on almost all of Altera's devices are available, and software courses highlight the MAX+PLUS® II software, VHDL, and Verilog HDL. These classes teach you how to increase productivity, accelerate product development, and use resources effectively from these classes.

The following courses are currently offered by the Altera Technical Training Program:

- Introduction to Altera
- Achieving High Performance & Optimal Utilization in FLEX® 10K Devices
- Achieving High Performance & Optimal Utilization in FLEX 6000 & FLEX 8000 Devices
- Optimizing Designs for MAX® 9000 Devices
- Optimizing Designs for MAX 7000 Devices
- Designing with the MAX+PLUS II Software
- Designing with the MAX+PLUS II Software Using AHDL
- Introduction to VHDL
- Designing with the MAX+PLUS II Software Using VHDL
- Introduction to Verilog HDL
- Optimizing Verilog HDL Code for Altera Devices and Tools
- Optimizing FLEX Designs with Synopsys and MAX+PLUS II

Training classes are offered throughout North America during the entire year. You can enroll for classes in North America on the Altera web site at **http://www.altera.com**. Classes are also offered internationally in Asia, Europe, and Middle and South America. For information on international class availability and enrollment, go to the Altera web site.

ASSET Provides First Tools Suite Supporting Both Jam & SVF Programming

ASSET InterTech, a market leader in boundary-scan testing and in-system programmability (ISP) and a longtime leader in the standardization process, has released version 2.3 of the ASSET suite of tools. In addition to providing several new boundary scan test features, this release makes ASSET the first boundary-scan system that supports both the Jam™ programming and test language and the Serial Vector Format (SVF) test and programming language.

With release 2.3 of ASSET, Jam files from any programmable logic device (PLD) vendor can be used to perform in-system programming in either a stand-alone programming station or as an integrated part of a manufacturing test flow.

ASSET supports Jam version 1.1 as it was submitted to JEDEC in September 1997 for standardization. Both Altera and ASSET look forward to the approval of Jam as a JEDEC standard because a standard language eases the development of tool support for ISP and boundary-scan testing. SVF is an open specification that can be used to perform ISP and to develop boundary-scan tests.

For specific product information or details on ASSET version 2.3, visit the ASSET web site or contact the company directly.

ASSET InterTech, Inc.
2201 N. Central Expressway, Suite 105
Richardson, TX 75080
Tel: (972) 437-2800
Toll-free: (888) 694-6250
http://www.asset-intertech.com

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for selected Altera devices. Algorithms are supplied via Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Microsystems' BBS. Programming support for configuration, MAX® 9000, and MAX 7000 devices is shown in Table 1. All information is subject to change.

Table 1. Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPC1441	✓	✓
EPM7032	✓	✓
EPM7032S	✓	✓
EPM7032AE	*(3)*	*(3)*
EPM7064	✓	✓
EPM7064S	✓	✓
EPM7064AE	*(3)*	*(3)*
EPM7096	✓	✓
EPM7128E	✓	✓
EPM7128S	✓	✓
EPM7128A	✓	✓
EPM7160E	✓	✓
EPM7192E	✓	✓
EPM7192S	✓	✓
EPM7256E	✓	✓
EPM7256A	*(3)*	*(3)*
EPM7256S	✓	✓
EPM7512AE	*(3)*	*(3)*
EPM9320	✓	✓
EPM9320A	✓	✓
EPM9400	✓	✓
EPM9480	✓	✓
EPM9560	✓	✓
EPM9560A	✓	✓

Notes:

(1) These devices are supported by Data I/O 3900 version 5.9 and UniSite version 5.9 programmers.
(2) These devices are supported by BP Microsystems programmers version 3.38.
(3) Please contact Data I/O or BP Microsystems for programming support for these devices.

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on the Altera web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- ***Altera Digital Library CD-ROM***, *version 5* (P-CD-ADL-05)
- *APEX 20K Programmable Logic Device Family Data Sheet* (A-DS-APEX20K-01)
- *AN 71: Guidelines for Handling J-Lead, QFP & BGA Devices* (A-AN-071-04)
- *AN 80: Selecting Sockets for Altera Devices* (A-AN-080-03)
- *AN 81: Reflow Soldering Guidelines for Surface-Mount Devices* (A-AN-081-03)
- *AN 90: SameFrame Pin-Out Design for FineLine BGA Packages (A-AN-090-01)*
- *AN 102: Improving Performance in FLEX 10K Devices with Leonardo Spectrum Software* (A-AN-102-01)
- *AN 106: Designing with 2.5-V Devices (A-AN-106-01)*
- *SB 38: SDRAM Controller Megafunction* (A-SB-038-01)

Programming Hardware Support

Table 1 provides programming and configuration compatibility information for the BitBlaster™ serial port and the ByteBlaster MV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlaster MV cable.)

Table 1. Download Cable Compatibility

Device	BitBlaster	ByteBlasterMV
FLEX 10K	✓	✓
FLEX 10KA		✓
FLEX 10KE		✓
FLEX 8000	✓	✓
FLEX 6000	✓ *(1)*	✓
MAX 9000	✓	✓
MAX 9000A	✓	✓
MAX 7000S	✓	✓
MAX 7000A		✓

Note:

(1) For the FLEX® 6000 family, this download cable is only compatible with EPF6016 devices.

continued on page 26

Programming Hardware Support, continued from page 25

Altera Programming Adapters

The following table contains the latest programming hardware information for Altera® devices. For correct programming, use the software version shown in "Current Software Version" on page 29. Table 2 lists Altera programming adapters for MAX® 9000, MAX 7000, and configuration devices.

Table 2. Altera Programming Adapters (Part 1 of 2) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)*, EPC1064V *(2)*, EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)*, EPC1213 *(2)*	DIP, J-lead	PLMJ1213
EPC2 *(3)*	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(4)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(4)* PLMR9000-240NC *(4)*
EPM7032, EPM7032V	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S, EPM7032AE	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7064AE	FineLine BGA (100-pin)	PLMF7000-100
EPM7064S, EPM7064AE	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(4)*
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

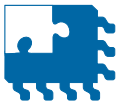
Table 2. Altera Programming Adapters (Part 2 of 2) *Note (1)*

Device	Package	Adapter
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A	J-lead (84-pin) TQFP (100-pin) TQFP (144-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMJ7000-84 PLMT7000-100NC *(4)* PLMT7000-144NC *(4)* PLMF7000-100 PLMF7000-256
EPM7128AE	FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMF7000-100 PLMF7000-256
EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(4)* PLMT7000-100NC *(4)* PLMQ7128/7160-160NC *(4)*
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(4)* PLMQ7128/7160-160NC *(4)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC *(4)*
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A	FineLine BGA (256-pin)	PLMF7000-256
EPM7256A EPM7256S	PQFP (208-pin) RQFP (208-pin)	PLMR7256-208NC *(4)* PLMT7000-208NC *(4)*
EPM7256AE	FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMF7000-100 PLMF7000-256
EPM7384AE	TQFP (144-pin) PQFP (208-pin)	PLMT7000-144NC *(4)* PLMR7256-208NC *(4)*
EPM7512AE	TQFP (144-pin) PQFP (208-pin) BGA (256-pin) FineLine BGA (256-pin)	PLMT7000-144NC *(4)* PLMR7256-208NC *(4)* PLMB7000-256 PLMF7000-256

Notes:

(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on MAX 5000 and Classic™ devices. Altera offers an adapter exchange program for 0.8 µm EPM5032, EPM5064, and EPM5130 programming adapters.
(2) FLEX® 8000 configuration device.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(4) These devices are not shipped in carriers.

Altera Offers Over 50 DSP Megafunctions



The Altera® digital signal processing (DSP) solutions provide optimized performance that is ideal for real-time, high-performance applications such as satellite communications, digital image processing, and spread-spectrum systems. Altera offers a variety of DSP products from basic building block megafunctions, such as FIR filters and high-speed multipliers, to more complex megafunctions such as Reed-Solomon and Viterbi Decoders.

Megafunctions are ready-made, pre-tested blocks of intellectual property (IP) that are optimized to make use of the target architecture efficiently. By using megafunctions, designers can focus more time and energy on improving and differentiating their system-level product, rather than redesigning common functions. You can download an Altera MegaCore function from the Altera web site and evaluate it for free before purchase using the OpenCore™ feature found in the MAX+PLUS® II software. You can also email a request for an OpenCore version of almost every Altera Megafunction Partner Program (AMPP℠) megafunction via the Altera website. For the most up-to-date information about Altera megafunctions, go to the Altera web site. Contact Altera or your local sales office for more information.

DSP Building Block Megafunctions

Function	Source
FIR Filter Compiler	Altera MegaCore Function
Convolutional Interleaver/Deinterleaver	Altera MegaCore Function
Fast Fourier Transform	Altera MegaCore Function
Fast Fourier Transform (FFT/IFFT)	Integrated Silicon Systems
FIR Filter Library	Integrated Silicon Systems
Floating-Point Adder	Integrated Silicon Systems
Floating-Point Divider	Integrated Silicon Systems
Floating-Point Multiplier	Integrated Silicon Systems
IIR Filter Library	Integrated Silicon Systems
Median Filter Library	Integrated Silicon Systems
Multi-Standard ADPCM	Integrated Silicon Systems
Rank Order Filter Library	Integrated Silicon Systems
Parameterized Floating-Point Adder/Subtractor	Altera Reference Design
Parameterized Integer Divider	Altera Reference Design
Parameterized Floating-Point Multiplier	Altera Reference Design
Data Word Rounder	Altera Reference Design
Data Word Saturator	Altera Reference Design

DSP Error Control Coding Megafunctions

Function	Source
CRC Checker/Generator	Altera MegaCore Function
Convolutional Encoder	Integrated Silicon Systems
Convolutional Interleaver	KTech Communications
Reed-Solomon Encoder	HammerCores
Intermediate Data Rate (IDR) Framer/Deframer	Integrated Silicon Systems
Reed-Solomon Decoder	Integrated Silicon Systems
Reed-Solomon Decoder	HammerCores
Reed-Solomon Encoder	Integrated Silicon Systems
Viterbi Decoder	CAST
Viterbi Decoder	Integrated Silicon Systems

DSP Wireless & Broadband Communication Megafunctions

Function	Source
Adaptive Equalizer	HammerCores
Adaptive Equalizer	Integrated Silicon Systems
Adaptive Filter	Integrated Silicon Systems
Binary Pattern Correlator	Nova Engineering, Inc.
Convolutional Encoder	Integrated Silicon Systems
Block and Convolutional Interleavers/Deinterleavers	Integrated Silicon Systems
Complex Mixer/Multiplier	Nova Engineering, Inc.
Convolutional Interleaver (Cable Modem and PCS)	KTech Communications
Cordpol Function	HammerCores
DES-Core	CAST
DES-Core (US and Canada Only)	HammerCores
DES-Core	Sican Microelectronics
Digital Modulator	Nova Engineering, Inc.
Early/Late Gate Symbol Synchronizer	Nova Engineering, Inc.
FFT/IFFT	Integrated Silicon Systems
Linear Feedback Shift Register	Nova Engineering, Inc.
LMS and Zero-Forcing Equalizers	Nova Engineering, Inc.
Numerically Controlled Oscillator	HammerCores
QPSK Equalizer	Integrated Silicon Systems

DSP Imaging Megafunctions

Function	Source
RGB2YCrCb and YCrCb2RGB Color Space Converters	Altera MegaCore Function
Image Processing Library	Integrated Silicon Systems
IDR Framer/Deframer	Integrated Silicon Systems
JPEG Decoder/Encoder	Integrated Silicon Systems
Laplacian Edge Detector	Integrated Silicon Systems
Parameterized Discrete Cosine Transform	Integrated Silicon Systems

Altera Device Selection Guide

Current information for the Altera APEX™ 20K, FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, and MAX 7000 devices is listed here. Information on other Altera products is located in the ***Altera Component Selector Guide***. For the most up-to-date information, go to the Altera web site at **http://www.altera.com**. Some of the products listed may not be available yet. Contact Altera or your local sales office for current product availability.

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[2]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	MACROCELLS
EP20K100	100,000	144-Pin TQFP, 196-Pin BGA[1], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[1], 356-Pin BGA	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 196-Pin BGA[1], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[1]	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 400-Pin BGA[1]	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 672-Pin BGA[1]	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 484-Pin BGA[1]	1.8 V	8,320	106,496	832
EP20K300E	300,000	208-Pin RQFP, 240-Pin RQFP, 672-Pin BGA[1]	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin BGA[1]	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	208-Pin RQFP, 240-Pin RQFP, 672-Pin BGA[1]	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	672-Pin BGA[1], 900-Pin BGA[1]	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	900-Pin BGA[1], 984-Pin PGA	1.8 V	42,240	540,672	4,224

Notes:
(1) This package is a space-saving FineLine BGA™ package.
(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 256[2], 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	147, 189, 191, 274[2], 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA 672-Pin BGA[1]	186, 274[2], 369, 426[2], 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 599-Pin PGA, 600-Pin BGA, 672-Pin BGA[1]	182[2], 274[2], 380[2], 470 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

Notes:
(1) This package is a space-saving FineLine BGA package.
(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	5.0 V	-2, -3, -4	282	208
EPF8282AV	2,500	100-Pin TQFP	78	3.3 V	-3, -4	282	208
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 68, 120	5.0 V	-2, -3, -4	452	336
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136, 136	5.0 V	-2, -3, -4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152, 152, 152	5.0 V	-2, -3, -4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184, 184	5.0 V	-2, -3, -4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208, 208	5.0 V	-2, -3, -4	1,500	1,296

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP, 100-Pin BGA[1], 256-Pin BGA[1]	81, 117, 81[2], 139[2]	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 81, 117[2], 171, 218[2]	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218[2]	3.3 V	-1, -2, -3	1,960	1,960

Notes:
(1) This package is a space-saving FineLine BGA package.
(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[1]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[1]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[1]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX and FLEX devices

Note:
(1) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

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Current Software Version

The latest version of Altera software product is MAX+PLUS® II version 9.21. The MAX+PLUS II development system is available for Windows-based PC, Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 platforms.

Device Selection Guide, continued from page 29

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032	32	44-Pin PLCC/TQFP/PQFP	36	5.0 V	-6, -7, -10, -12, -15
EPM7064AE	64	44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin BGA[1]	38, 68, 68	3.3 V	-4, -7, -10
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	5.0 V	-6, -7, -10, -12, -15
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	5.0 V	-7, -10, -12, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-5,-7,-10
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-7, -10, -12, -15, -20
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 104	5.0 V	-10, -12, -15, -20
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7192E	192	160-Pin PQFP/PGA	124	5.0 V	-12, -15, -20
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 100-Pin BGA[1], 256-Pin BGA[1] 256-Pin BGA	84, 120, 164, 84, 164	3.3 V	-6, -7, -10
EPM7256S	256	208-Pin RQFP/PQFP	164	5.0 V	-7, -10, -15
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	5.0 V	-12, -15, -20
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 256-Pin BGA	120, 176, 212, 212	3.3 V	-7, -10, -12

Note:
(1) This package is a space-saving FineLine BGA package.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera:

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	Altera Literature Services	(888) 3-ALTERA **lit_req@altera.com**	(408) 544-7144 *(2)* **lit_req@altera.com**
	World-Wide Web	**http://www.altera.com**	**http://www.altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline (6 a.m. to 6 p.m. Pacific Time)	(800) 800-EPLD (408) 544-7000	(408) 544-7000 *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**sos@altera.com**	**sos@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com**	**http://www.altera.com**

Notes:
(1) The ***MAX+PLUS II Getting Started*** manual is available from the Altera web site. To obtain other MAX+PLUS II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

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