News & Views
Second Quarter, May 1999
Newsletter for Altera Customers

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The Programmable Solutions Company™

APEX Devices & Quartus Software: The System-on-a-Programmable-Chip Solution

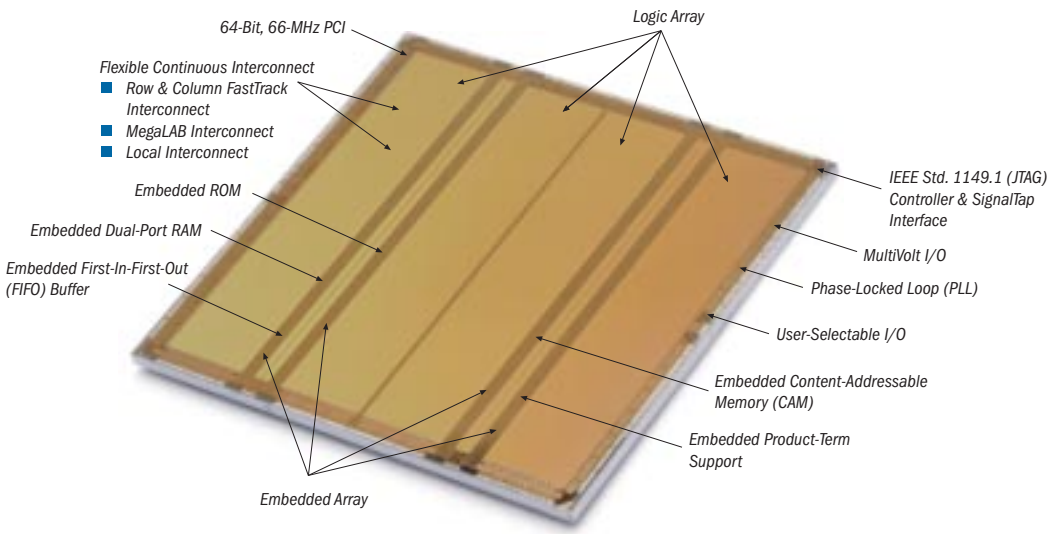
Designing for system-level integration requires devices with the density and flexibility to support a new design methodology and enhance productivity. Altera's new APEX™ device family and Quartus™ software have launched this new era in programmable logic design.

With over 1 million typical gates (2.67 million system gates), APEX devices are the first PLDs designed with the MultiCore™ architecture, which integrates RAM, product-term logic, and look-up table (LUT) logic on a single device. To meet the challenges of designing for multi-million-gate devices, the powerful Quartus software offers features never before seen in a programmable logic development tool. Together, APEX devices and Quartus software offer designers the ideal solution for implementing high-performance System-on-a-Programmable-Chip™ designs.

Matching Architecture & Software

Altera's high-density, high-performance APEX MultiCore architecture is designed for system-level integration (see Figure 1). The MultiCore architecture combines LUT logic, product-term logic, and memory features into one embedded architecture. Designers can integrate a complex system design onto a single APEX device,

Figure 1. APEX Device Architecture



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The System-on-a-Programmable-Chip Solution

Visit the Altera Main Booth 3016 and qualify for an Altera pool cue.

High Performance

High-Speed Programmable Logic Devices with System Performance over 200 MHz

Density

APEX™ Device Family Offering up to 1 Million Gates

Cutting-Edge Software

Quartus™ and MAX+PLUS® II Software — The Industry's Best Development Tools

Powerful Megafunctions

Powerful Megafunctions from Altera's MegaCore™ Function Library and AMPP℠ Partners

EDA Teamwork

NativeLink™ EDA Tool Integration

Visit Our AMPP IP Partners at Booth 1716

ISS, Lexra, Nova, PLD Applications & Sapien

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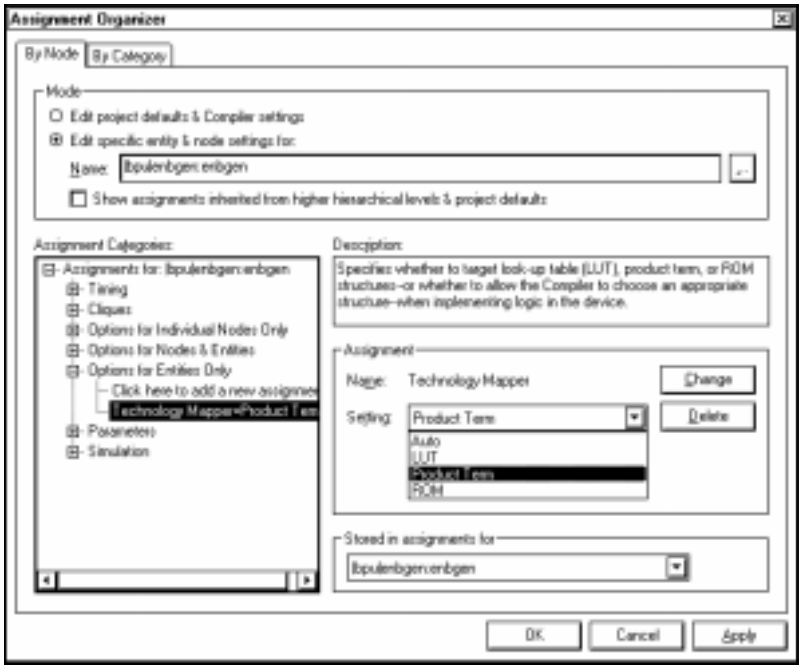
eliminating the need to use multiple devices. Not only does the APEX architecture save valuable board space, it also simplifies design implementation.

The APEX architecture is composed of a series of MegaLAB™ structures connected by the fast, continuous FastTrack® Interconnect. Each MegaLAB structure contains 16 logic array blocks (LABs), an embedded system block (ESB), and a MegaLAB local interconnect that connects the LABs and the ESB. The ESB can be configured as LUT logic, product-term logic, or memory, including dual-port RAM, first-in first-out (FIFO) buffers, ROM, or content-addressable memory (CAM).

To ensure that logic is mapped correctly to the APEX architecture, the Quartus Compiler uses the CoreSyn™ capability. The Compiler analyzes the design and implements functions using the optimal technology for that block: LUT-based logic elements, product-term-based macrocells, or ESBs in the APEX architecture.

As shown in Figure 2, logic options can be set block-by-block. The Assignment Organizer allows the designer to specify whether blocks or modules in the project hierarchy should be mapped to LUT logic, product-term logic, or memory. Alternatively, designers can use the *AUTO* mode in the Quartus Technology Mapper, which instructs the Quartus software to determine the best implementation.

Figure 2. Technology Mapper in Quartus Software



Attaining Clock Rates of 622 MHz

To help designers verify the performance of their APEX designs, the Quartus software offers extensive timing information. Timing analysis is performed automatically during each compilation because the Timing Analyzer is incorporated into the Quartus Compiler. Designers can monitor the device's actual system operating frequency, the internal operating frequency, and other timing parameters. System $\mathbf{f}_{MAX}$ takes into account t_{SU} and t_{CO} times of external devices as well as off-chip delays (where they have been specified). Figure 3 on page 5 shows the $\mathbf{f}_{MAX}$ of a design displayed in the Quartus Report Window.

To increase system clock rates, APEX devices feature up to four phase-locked loops (PLLs) with output frequencies reaching 200 MHz. These PLLs support the performance-based ClockLock™, ClockBoost™, and ClockShift™ clock management circuitry. The ClockLock circuitry reduces clock delay and skew and minimizes clock-to-output times while maintaining zero hold times. The ClockBoost circuitry offers flexible-rate clock multiplication and division. The ClockShift circuitry allows the clock phase and delay to be adjusted. These features provide significant improvements in system performance and bandwidth. The Quartus Timing Analyzer supports the APEX clock management circuitry and can perform timing analysis on designs with multiple related clocks.

APEX Devices: The First PLDs with CAM

The APEX device family is the first programmable logic device (PLD) family to offer CAM. When in CAM mode, the APEX ESB implements 32-word, 32-bit CAM. Wider and deeper CAMs can be implemented by combining multiple CAMs. To create larger CAMs, the CoreSyn synthesis capability of the Quartus software automatically combines ESBs and the necessary logic elements (LEs). Because the logic and CAM are integrated into the

device, APEX CAM provides much faster system performance than traditional discrete CAM. The APEX CAM accelerates fast search applications by integrating the parallel comparators into a single block and eliminating on-chip and off-chip delays.

Million-Gate Designs Require Innovative Approaches

Because of their density and performance, APEX devices give designers the flexibility to address much larger designs in a broader range of applications than traditionally possible in PLDs. However, to deal with such density and to bring complex designs to market on time, teams of designers often need to work on separate sections of a project. The Quartus software is designed specifically for collaborative design projects.

Integrated into the Quartus software is a centralized object-oriented database that can be accessed by multiple engineers across a network. The Quartus software lets you use industry-standard revision control systems to track all of the changes in each project file and link them to a database. Users can check out files, work on them, and then check them back in, documenting the changes that have been made. A log tracks users and the changes they make to a file. Using a revision control system together with the Quartus software safeguards the integrity of a project; users cannot overwrite the work of others, changes are documented, and it is easy to roll back to a previous version of the design if the need arises.

Another consideration when designing for large devices is the time needed for full compilation. Complex designs often require several iterations before the desired results are achieved. The Quartus software includes two new features to speed design processing: multi-processor support and the nSTEP™ Compiler.

The Quartus software was designed from the start for multi-processor support. Processor-intensive tasks like compilation can be distributed to multiple processors locally, across a network, and across multiple operating systems. Tying together the power of several PCs and workstations can considerably reduce the time needed for compilation.

Figure 3. System f_{MAX} in the Quartus Software

Before the Quartus software, each design iteration required a full compilation. Now, the nSTEP Compiler permits incremental recompilation. Designers can make changes and obtain results without running a full compilation and without affecting placement and timing in the rest of the design. This process allows you to easily evaluate changes, saving valuable time.

LVDS Support

APEX devices offer support for multiple high-bandwidth, low-voltage I/O interfacing standards. The APEX family is the first PLD family to support the low-voltage differential signaling (LVDS) standard with performance up to 622 Mbits per second. Other standards supported by APEX devices include low-voltage transistor-to-transistor logic (LVTTL), stub-series terminated logic (SSTL-3/2), advanced graphics port (AGP), high-speed transceiver logic (HSTL), and Gunning transceiver logic (GTL+). Designers can use the Quartus software to specify high-speed interfaces between SDRAMs, processors, and system backplanes to APEX devices to achieve the desired performance.

APEX JTAG BST Circuitry Connects to the SignalTap Embedded Logic Analyzer

The verification of multi-million gate designs is the most time-consuming part of the design

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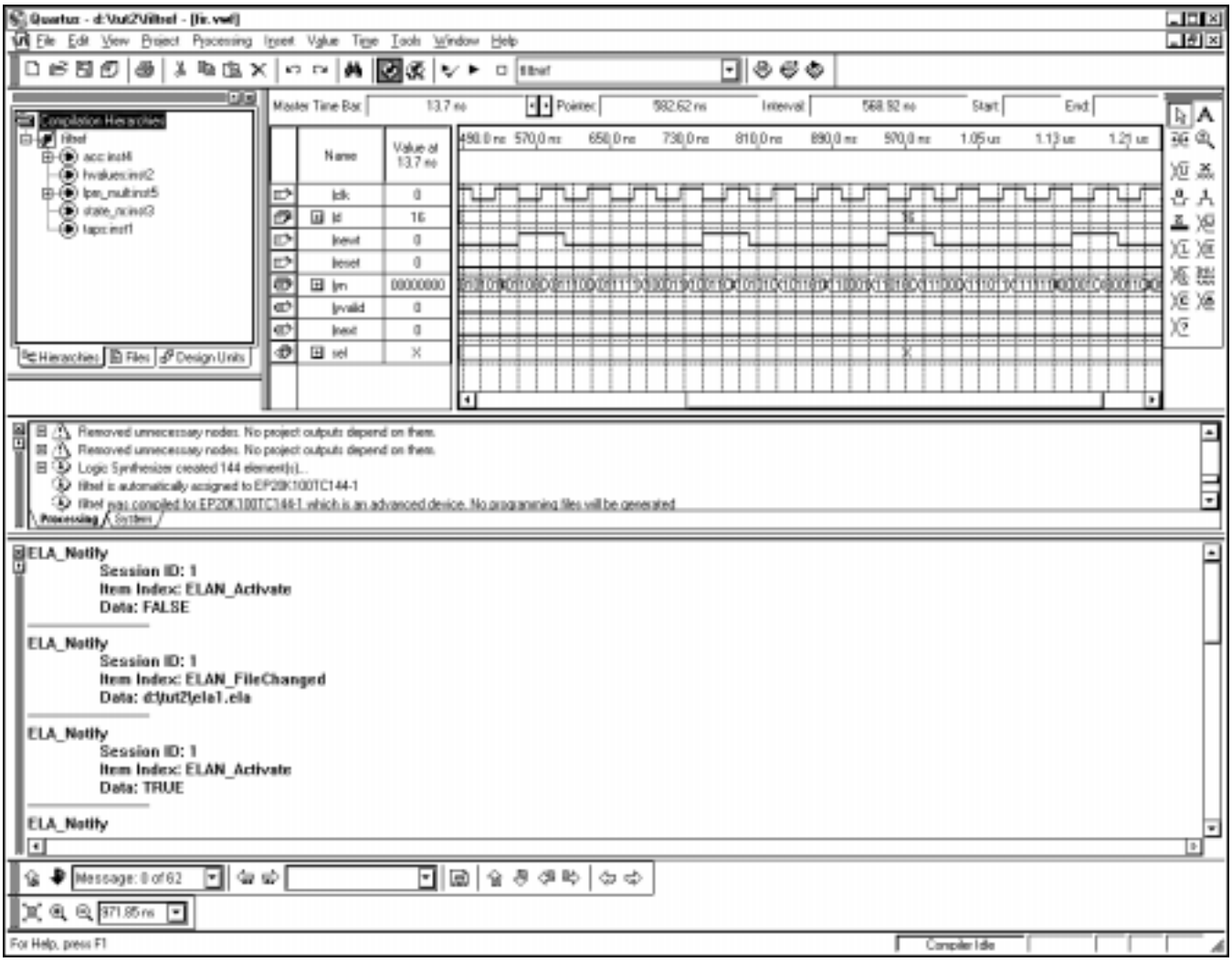
process. However, the APEX device family and Quartus software simplify the process and reduce verification time. The APEX device family has dedicated IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that can be used to monitor the internal logic operation of the devices with the software-implemented Quartus SignalTap™ logic analyzer (see Figure 4). The SignalTap logic analyzer allows designers to perform hardware debugging while the circuit is running at speed, significantly enhancing the board-level verification process. The MasterBlaster™ communications cable connects the platform running the Quartus software to the printed circuit board (PCB), allowing the SignalTap logic analyzer to monitor the APEX device. For details on the SignalTap logic analyzer, see "SignalTap Embedded Logic Analyzer Provides Visibility of Internal PLD Signals" on page 24.

Conclusion

The powerful features of the Quartus software allow designers to realize the full potential of the state-of-the-art APEX devices, shortening design time and increasing productivity. Together, Altera's Quartus software and APEX devices provide the real solution for implementing System-on-a- Programmable-Chip designs.

APEX devices and the Quartus software are available now. For further details, visit the Altera web site (**http://www.altera.com**) or contact your local sales representative.

Figure 4. SignalTap Embedded Logic Analyzer



APEX

EP20K400 Devices Now Available

The first APEX™ device is now available (see Table 1). The 400,000-gate (1 million maximum system gates) EP20K400 device features the MultiCore™ architecture, which includes integrated look-up table (LUT) logic, product-term logic, and flexible memory. The APEX MultiCore architecture offers designers complete system-level integration on a single device, eliminating the need for multiple devices, saving board space, and simplifying the implementation of complex designs. The flexible memory structure supports dual-port RAM with independent read/write ports, synchronous or asynchronous operation, and 161-MHz first-in first-out (FIFO) performance in a wide range of widths and depths.

Table 1. APEX Device Availability

Device	Package *(1)*	Availability
EP20K100	144-pin TQFP 208-pin PQFP 240-pin PQFP	June 1999
	196-pin FineLine BGA 324-pin FineLine BGA 356-pin BGA	Q3 1999
EP20K200	208-pin RQFP 240-pin RQFP 356-pin BGA 484-pin FineLine BGA	Q3 1999
EP20K400	652-pin BGA 655-pin PGA	Now
	672-pin FineLine BGA	Q3 1999
EP20K400E	208-pin RQFP 240-pin RQFP	Q3 1999
	652-pin BGA 672-pin FineLine BGA	Q4 1999
EP20K600E	652-pin BGA 672-pin FineLine BGA 784-pin FineLine BGA	Q4 1999
EP20K1000E	784-pin FineLine BGA 984-pin PGA	Q4 1999

Note:
(1) PQFP: plastic quad flat pack, RQFP: power quad flat pack, TQFP: thin quad flat pack.

APEX devices are fully 64-bit, 66-MHz peripheral component interconnect (PCI) compliant and deliver clock rates up to 622 MHz. The EP20K400 device has a phase-locked loop (PLL), which features enhanced ClockLock™ and ClockBoost™ circuitry. The PLL circuitry offers 1×, 2×, and 4× multiplication over an extended frequency range. The device also provides the MultiVolt™ I/O interface, which is ideal for mixed-voltage systems, and supports hot-socketing. EP20K400 devices are available in 652-pin ball-grid array (BGA) and 655-pin pin-grid array (PGA) packages, and will be available soon in the 672-pin FineLine BGA™ package. For the latest information on APEX devices, go to the Altera web site at **http://www.altera.com**.

FLEX

0.22-µm EPF10K100E Devices Available

EPF10K100E devices are now available. These devices use a state-of-the-art 0.22-µm, 5-layer-metal process that provides high-performance and low-power advantages. In addition to 4,992 logic elements (LEs) and 49,152 bits of on-chip dual-port RAM, EPF10K100E devices also feature a programmable delay to support 64-bit, 66-MHz PCI compliance and a PLL for improved pin-to-pin timing. EPF10K100E devices are offered in 208-pin PQFP, 240-pin PQFP, 256-pin FineLine BGA, 484-pin FineLine BGA, and 356-pin BGA packages.

Introducing EPF10K200S & EPF10K50S Devices

Enhanced versions of the EPF10K200E and EPF10K50E devices, called EPF10K200S and EPF10K50S devices, respectively, include a migration from a 0.25-µm process to a 0.22-µm process for increased performance and lower power consumption, and a programmable delay to provide full 64-bit, 66-MHz PCI compliance. (EPF10K100E, EPF10K130E, and EPF10K30E devices all feature a programmable delay and are

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fabricated on a 0.22-µm process.) EPF10K200S and EPF10K50S devices offer the ClockLock and ClockBoost features.

In addition to the 600-pin BGA and 672-pin FineLine BGA packages already offered for EPF10K200E devices, EPF10K200S devices will be offered in the 240-pin RQFP, 356-pin BGA, and 484-pin FineLine BGA packages. EPF10K50S devices will be available in the same packages as the EPF10K50E device. Advanced support for EPF10K200S and EPF10K50S devices is available in the MAX+PLUS II software version 9.24.

Software Support for New FLEX 10KE Packages

Altera is offering many new device-package combinations, including 1.27-mm BGA packages and cost efficient quad flat pack (QFP) packages. Advanced software support is shown in Table 2. You can obtain software updates from the Altera web site at **http://www.altera.com**.

Table 2. FLEX 10KE Device Software Support

Device	Package	MAX+PLUS II Software Version
EPF10K50S	356-pin BGA	9.23
EPF10K130E	356-pin BGA	9.23
EPF10K130E	600-pin BGA	9.23
EPF10K200S	240-pin RQFP	9.24
EPF10K200S	356-pin BGA	9.25
EPF10K200S	484-pin FineLine BGA	9.25

FLEX 10K Device Availability

With the introduction of EPF10K50V devices in 484-pin FineLine BGA packages, all FLEX® 10KA devices have been introduced. Table 3 shows the expected availability of all 2.5-V FLEX 10KE devices. MAX+PLUS® II design support is currently available for all device package options.

FLEX 10K Product Transitions

Altera is migrating selected 3.3-V FLEX 10KA devices from a 0.35-µm process to a 0.30-µm process. Additionally, selected 5.0-V FLEX 10K devices are moving from a 0.50-µm process to a 0.42-µm process. Table 4 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com**.

FLEX 10KE Industrial-Temperature Devices

Table 5 lists the availability of industrial-temperature FLEX 10KE devices.

Table 3. FLEX 10KE Availability

Device	Package *(1)*	Speed Grade	Availability *(2)*
EPF10K30E	144-pin TQFP	-1, -2, -3	July
	208-pin PQFP	-1, -2, -3	July
	256-pin FBGA	-1, -2, -3	August
	484-pin FBGA	-1, -2, -3	August
EPF10K50E	144-pin TQFP	-1, -2, -3	Now
	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FBGA	-1, -2, -3	Now
	356-pin BGA	-1, -2, -3	August
	484-pin FBGA	-1, -2, -3	Now
EPF10K50S	144-pin TQFP	-1, -2, -3	July
	208-pin PQFP	-1, -2, -3	July
	240-pin PQFP	-1, -2, -3	July
	256-pin FBGA	-1, -2, -3	September
	356-pin BGA	-1, -2, -3	August
	484-pin FBGA	-1, -2, -3	August
EPF10K100E	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FBGA	-1, -2, -3	June
	356-pin BGA	-1, -2, -3	June
	484-pin FBGA	-1, -2, -3	June
EPF10K130E	240-pin PQFP	-1, -2, -3	Now
	356-pin BGA	-1, -2, -3	June
	484-pin FBGA	-1, -2, -3	June
	600-pin BGA	-1, -2, -3	June
	672-pin FBGA	-1, -2, -3	June
EPF10K200E	599-pin PGA	-1, -2, -3	Now
	600-pin BGA	-1, -2, -3	Now
	672-pin FBGA	-1, -2, -3	Now
EPF10K200S	240-pin RQFP	-1, -2, -3	June
	356-pin BGA	-1, -2, -3	August
	484-pin FBGA	-1, -2, -3	August
	600-pin BGA	-1, -2, -3	August
	672-pin FBGA	-1, -2, -3	August

Notes:
(1) FBGA: FineLine BGA packages.
(2) All dates refer to calendar-year 1999.

FLEX 10KE Devices Available with PLLs

FLEX 10KE devices will be offered with the PLL feature in -1 and -2 speed grades. These devices will have a "-X" suffix (e.g., EPF10K200EBC600-1X). Table 6 lists the availability of FLEX 10KE devices with PLLs.

FLEX 10KE devices will be offered with the PLL feature in -1 and -2 speed grades.

Table 4. FLEX 10K Device Migration

Device	Core Voltage (V)	Date	Reference	Process (µm)
EPF10K10A	3.3	July 1999	PCN 9810	0.30
EPF10K30A	3.3	Done	PCN 9810	0.30
EPF10K50V	3.3	Done	PCN 9810	0.30
EPF10K100A	3.3	Done	PCN 9810	0.30
EPF10K10	5.0	October 1999	PCN 9901 ADV 9909	0.42
EPF10K20	5.0	July 1999	PCN 9901 ADV 9909	0.42
EPF10K30	5.0	July 1999	PCN 9901 ADV 9909	0.42
EPF10K40	5.0	October 1999	PCN 9901 ADV 9909	0.42
EPF10K50	5.0	July 1999	PCN 9901 ADV 9909	0.42
EPF10K70	5.0	October 1999	PCN 9901 ADV 9909	0.42
EPF10K100	5.0	October 1999	PCN 9901 ADV 9909	0.42

Table 5. FLEX 10KE Industrial-Temperature Device Availability

Device	Availability
EPF10K50ETI144-2	Now
EPF10K50EQI240-2	Now
EPF10K50EFI256-2	Now
EPF10K50SQI208-2	Q3 1999
EPF10K50SBI356-2	Q3 1999
EPF10K50SFI484-2	Q3 1999
EPF10K100EQI208-2	Q3 1999
EPF10K100EFI256-2	Q3 1999
EPF10K100EFI484-2	Q3 1999
EPF10K130EQI240-2	Now
EPF10K130EBI356-2	Q3 1999
EPF10K130EFI484-2	Q3 1999
EPF10K200EBI600-2	Now
EPF10K200SRI240-2	Q3 1999
EPF10K200SBI356-2	Q3 1999
EPF10K200SFI672-2	Q3 1999

Industrial-Temperature FLEX 6000 Devices Available

Altera provides a broad range of FLEX 6000 devices in industrial-temperature grades. Seven device package combinations are shipping in a variety of packages, including TQFP, PQFP, and BGA packages. Table 7 lists available industrial-temperature grade FLEX 6000 devices.

FineLine BGA Packages Coming Soon for FLEX 6000 Devices

FLEX 6000 devices in FineLine BGA packages are planned to be available in August 1999. These area-efficient packages require less than half the board space of traditional BGA packages. Table 8 on page 10 shows FLEX 6000 device expected availability.

Table 6. FLEX 10KE Devices with PLLs

Device	Package *(1)*	Availability
EPF10K30E	144-pin TQFP, 208-pin PQFP, 256-pin FBGA, 484-pin FBGA	August 1999
EPF10K50S	144-pin TQFP, 208-pin PQFP, 240-pin PQFP, 356-pin BGA	August 1999
	256-pin FBGA, 484-pin FBGA	Sept. 1999
EPF10K100E	208-pin PQFP, 240-pin PQFP	July 1999
	256-pin FBGA, 356-pin BGA, 484-pin FBGA	August 1999
EPF10K130E	240-pin PQFP, 356-pin BGA, 484-pin FBGA, 600-pin BGA, 672-pin FBGA	August 1999
EPF10K200S	240-pin RQFP, 356-pin BGA, 484-pin FBGA, 600-pin BGA, 672-pin FBGA	Sept. 1999

Note:
(1) FBGA: FineLine BGA packages.

Table 7. Industrial-Temperature FLEX 6000 Device Availability

Device	Package	Availability
EPF6016TI144-3	144-pin TQFP	Now
EPF6016QI208-3	208-pin PQFP	Now
EPF6016ATI100-2	100-pin TQFP	Now
EPF6016ATI144-3	144-pin TQFP	Now
EPF6016AQI208-3	208-pin PQFP	Now
EPF6024AQI208-3	208-pin PQFP	Now
EPF6024ABI256-2	256-pin BGA	Now

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Table 8. FLEX 6000 Device Availability

Package	Device			
	EPF6010A	EPF6016	EPF6016A	EPF6024A
100-pin TQFP	✓		✓	
100-pin FineLine BGA	August 1999		August 1999	
144-pin TQFP	✓	✓	✓	✓
208-pin PQFP		✓	✓	✓
240-pin PQFP		✓		✓
256-pin BGA		✓		✓
256-pin FineLine BGA	August 1999		August 1999	August 1999

MAX

MAX®

MAX 7000S Device Availability

All MAX® 7000S devices are now available. These devices feature speed grades of 5 ns, in-system programmability (ISP), an open-drain output option, and IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in industrial-temperature grades. Table 9 shows the packages and speed grades available in the commercial-temperature grade.

Table 9. Commercial-Temperature MAX 7000S Device Packages

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

MAX 7000A Device Availability

All MAX 7000A devices are now available. MAX 7000A devices range from 32 to 512 macrocells with propagation delays as fast as 4.5 ns. MAX 7000A devices support ISP, MultiVolt I/O pins, hot-socketing, and pin compatibility with the industry-standard MAX 7000 devices. All MAX 7000A devices are available in industrial-temperature grades. Table 10 shows MAX 7000A device commercial package and speed grade options.

Table 10. MAX 7000A Commercial-Temperature Device Packages

Device	Package	Speed Grade
EPM7032AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM7064AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
EPM7128A	84-pin PLCC	-6, -7, -10, -12
	100-pin TQFP	-6, -7, -10, -12
	100-pin FineLine BGA	-6, -7, -10, -12
	144-pin TQFP	-6, -7, -10, -12
	256-pin FineLine BGA	-6, -7, -10, -12
EPM7128AE	84-pin PLCC	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	100-pin PQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7256A	100-pin TQFP	-7, -10, -12
	144-pin TQFP	-7, -10, -12
	208-pin PQFP	-7, -10, -12
	256-pin FineLine BGA	-7, -10, -12
EPM7256AE	100-pin TQFP	-6, -7, -10
	100-pin FineLine BGA	-6, -7, -10
	144-pin TQFP	-6, -7, -10
	208-pin PQFP	-6, -7, -10
	256-pin FineLine BGA	-6, -7, -10
EPM7512AE	144-pin TQFP	-7, -10, -12
	208-pin PQFP	-7, -10, -12
	256-pin BGA	-7, -10, -12
	256-pin FineLine BGA	-7, -10, -12

New MAX 7000B Device

The new MAX 7000B devices are 2.5-V, product-term-based programmable logic devices (PLDs). The devices support new I/O standards, such as Gunning transceiver logic (GTL+), stub-series terminated logic-

(SSTL-) 2, and SSTL-3, offer propagation delays as fast as 3.5 ns, and range in density from 32 to 512 macrocells (see Table 11). MAX 7000B devices support ISP, MultiVolt I/O pins, hot socketing, and pin compatibility with the industry-standard MAX 7000 devices.

Table 11. MAX 7000B Commercial-Temperature Device Packages

Device	Package	Speed Grade
EPM7032B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
EPM7064B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	100-pin FineLine BGA	-3, -5, -7
	100-pin TQFP	-3, -5, -7
EPM7128B	100-pin FineLine BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	144-pin TQFP	-4, -7, -10
	256-pin FineLine BGA	-4, -7, -10
EPM7256B	100-pin FineLine BGA	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512B	144-pin TQFP	-6, -7, -10
	208-pin PQFP	-6, -7, -10
	256-pin FineLine BGA	-6, -7, -10

New MAX 3000A Devices

The MAX 3000A device family is a new 3.3-V product-term-based PLD family targeted for high-volume, low-cost applications. The devices have enhanced support for ISP and densities from 32 to 256 macrocells (see Table 12). With propagation delays as fast as 4.5 ns, MAX 3000A devices provide customers with the highest performance at the lowest price per macrocell.

Table 12. MAX 3000A Devices

Device	Package	Speed Grade
EPM3032A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM3064A	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	100-pin TQFP	-4, -7, -10
EPM3128A	100-pin TQFP	-5, -7, -10
	144-pin PQFP	-5, -7, -10
EPM3256A	144-pin TQFP	-6, -7, -10
	208-pin PQFP	-6, -7, -10

TOOLS

Download the Quartus Preview Today

For an early look at Altera's fourth-generation design software for System-on-a-Programmable-Chip™ solutions, visit the Altera web site at **http://www.altera.com** and download the Quartus Preview. The Quartus Preview presents self-running demos of the Quartus software's latest features.

The Quartus Preview demonstrates the seamless integration of the NativeLink™ feature and accelerated verification process using the SignalTap™ embedded logic analyzer. You can also see the ease of submitting a service request to Altera Applications directly from the Quartus software, the first fully Internet-aware PLD software. As device densities increase, design methodologies for PLDs must continue to evolve. Download the Quartus Preview to see first-hand how the Quartus software is reshaping programmable logic design.

New Quartus Simulator Features

The Quartus Simulator has several new features, including support for testbenches. The new Simulator supports both waveform entry (which provides compatibility with existing MAX+PLUS II simulation files) and testbench entry.

You can set multiple time bars in the Waveform Editor. The Quartus Simulator supports nine different signal level values (1, 0, X, U, Z, H, L, W, and DC).

The new Node Finder allows users to create customized filters to extract nodes from the post-synthesis or floorplan netlist, making it easy to locate nodes. The Node Finder can also add output pins to Vector Waveform Files (**.vwf**) and check the output values against expected values at the end of simulation.

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Devices & Tools, continued from page 11

Quartus Static Timing Analyzer Features

The Quartus static Timing Analyzer has several new features.

- Multi-clock frequency analysis allows you to analyze timing for designs containing register-to-register paths that are controlled by different clocks.
- The ability to detect combinatorial loops drastically reduces the analysis times of designs that contain combinatorial loops.
- The Timing Analyzer can display either the system f_{MAX} or the internal f_{MAX}. The system f_{MAX} has the ability to include delays to the device.
- Timing for critical paths can be broken down into data path, clock path, and setup time. Each delay path can also be broken down into increments.
- You can perform pin-to-pin or combinatorial timing analysis. This process is analogous to the delay matrix in the MAX+PLUS II software.

Quartus License Files

If you have a current software subscription, you will automatically receive the Quartus software when it is released. However, you may need a new license file to enable the software.

To ensure a smooth transition for the release of the Quartus software, in April 1999, the Altera web-based license server started issuing license files that enable both the MAX+PLUS II and Quartus software to all users with a current software subscription. If your **license.dat** file has a Quartus FEATURE line, your license will enable the Quartus software. Figure 1 shows a sample license file that enables both the Quartus and MAX+PLUS II software.

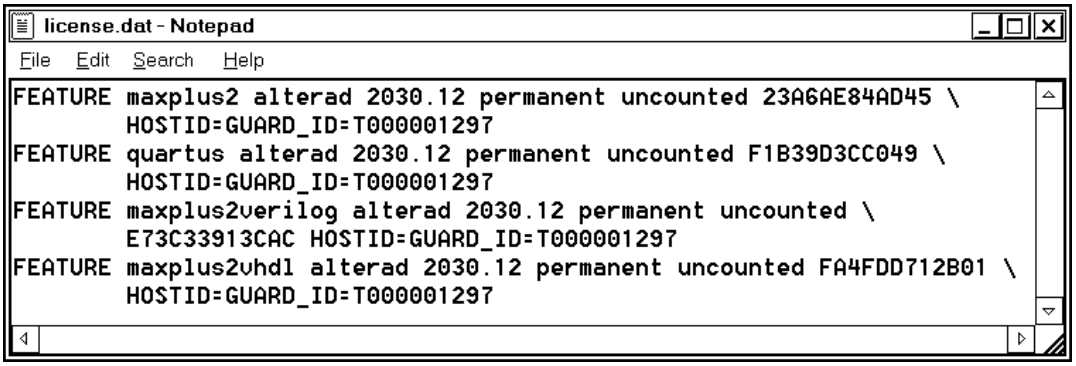
If you have a current software subscription, you can obtain a new license file that enables both the Quartus and MAX+PLUS II software from the Altera web-based license server at **http://www.altera.com**.

MAX+PLUS II BASELINE Version 9.23 Now Available

The MAX+PLUS II BASELINE software version 9.23 includes a full-featured functional and timing gate-level simulator, making it the industry's complete free PLD development software. The software is available for free download from the Altera web site at **http://www.altera.com**.

The MAX+PLUS II BASELINE software version 9.23 supports a wide range of programmable logic devices including EPF10K10, EPF10K10A, EPM9320, EPM9320A, EPF8452A, EPF8282A, EPF6010A, EPF6016, EPF6016A, MAX 7000, MAX 7000E, MAX 7000S, MAX 7000A, MAX 7000AE, MAX 5000, and Classic devices. Features supported include schematic and text-based (AHDL) design entry; full-featured timing simulation, and static timing analysis. It is an ideal development tool for low- to mid-density programmable logic design.

Figure 1. Example License File



Simplified Designs through Selectable I/O Standards

High-performance, low-voltage I/O standards have been introduced into the market to keep pace with increasing clock speeds and new low-voltage levels. These I/O standards must support memory, microprocessors, backplanes, and peripheral devices. Designers who want to use these new standards with programmable logic need flexible, high-performance, multi-standard I/O buffers. Altera's revolutionary APEX™ 20KE devices meet this challenge by providing the highest density, highest performance programmable logic solution with the necessary I/O standards for the communication and computer industries.

With the new programmable I/O standards supported by APEX 20KE devices, a single device can interface with high-speed, low-voltage memory buses and backplanes at up to 622-MBPS data rates. APEX 20KE devices are the first programmable logic devices (PLDs) to support the low-voltage differential signaling (LVDS) standard. Combined with the highest densities available, APEX devices are the perfect programmable solution.

Programmable I/O standards help simplify your board design. For example, you do not need dedicated devices such as LVDS drivers to interface APEX PLDs to backplanes.

With the new programmable I/O standards supported by APEX 20KE devices, a single device can interface with high-speed, low-voltage memory buses and backplanes.

Supported APEX 20KE I/O Standards

APEX 20KE I/O blocks support 17 I/O standards. The APEX 20KE I/O buffers meet the voltage, drive strength, and AC characteristics necessary to comply with the I/O standards listed in Table 1.

Table 1. APEX 20KE Supported I/O Standards

I/O Standard *(1)*	Type	Reference Voltage (V_{REF}) (V) *(2)*	Output Supply Voltage (V_{CCIO}) (V) *(2)*	Board Termination Voltage (V_{TT}) (V) *(2)*
LVTTL	Single-ended	N/A	3.3	N/A
LVCMOS	Single-ended	N/A	3.3	N/A
2.5 V	Single-ended	N/A	2.5	N/A
1.8 V	Single-ended	N/A	1.8	N/A
PCI	Single-ended	N/A	3.3	N/A
LVDS	Differential	N/A	3.3	N/A
GTL+	Open-drain	1.0	N/A	1.5
SSTL-2 Class I and II	Voltage referenced	1.25	2.5	1.25
SSTL-3 Class I and II	Voltage referenced	1.5	3.3	1.5
HSTL Class I	Voltage referenced	0.75	1.5	0.75
HSTL Class II	Voltage referenced	0.75	1.5	0.75
HSTL Class III	Voltage referenced	0.9	1.5	0.9
HSTL Class IV	Voltage referenced	0.9	1.5	0.9
AGP	Voltage referenced	1.32	3.3	N/A
CTT	Voltage referenced	1.5	3.3	1.5

Notes:

(1) AGP: advanced graphics port, CTT: center-tap-terminated, GTL+: Gunning transceiver logic, HSTL: high-speed transceiver logic, LVCMOS: low-voltage complementary metal-oxide semiconductor, LVTTL: low-voltage transistor-to-transistor logic, PCI: peripheral component interconnect, SSTL: stub-series terminated logic.

(2) The values shown for V_{REF}, V_{CCIO}, and V_{TT} are typical values.

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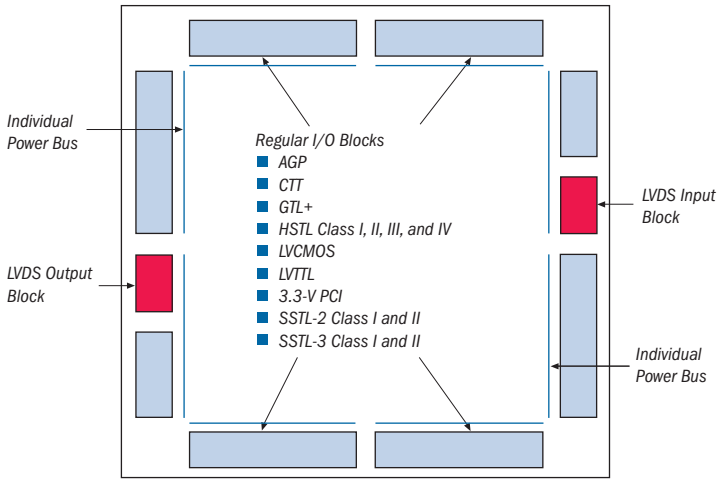
Simplified Designs through Selectable I/O Standards, continued from page 13

APEX 20KE devices have six programmable I/O blocks and two dedicated LVDS I/O blocks. The LVDS I/O blocks can also support any other I/O standard. Figure 1 shows the representation of the I/O blocks.

Figure 1. APEX 20KE I/O Blocks



The programmable I/O blocks have individual power planes with separate `VCCIO` pins for each I/O block. Each `VCCIO` plane supports 3.3-V, 2.5-V, or 1.8-V levels.

LVDS

The LVDS I/O standard is a high-speed, low-voltage swing, low-power, general-purpose I/O interface standard that is independent of process and architecture. LVDS requires a differential input, but does not need an input reference voltage. Typical uses for LVDS interfaces are high-bandwidth data transfer, backplane driver, and clock distribution applications.

Two key industry standards define LVDS: IEEE Std. 1596.3 SCI-LVDS and ANSI/TIA/EIA-644. Both standards have similar key features, but the IEEE standard supports a maximum data transfer of 250 MBPS. APEX 20KE devices are designed to meet the ANSI/TIA/EIA-644 standard at up to 622 MBPS.

Conclusion

Altera remains the programmable solutions leader by offering devices that meet designers' needs. The I/O standards and features allow programmers to interface APEX 20KE devices directly with microprocessors, memory devices, and backplanes, without using interface logic. This process saves board space, decreases time-to-market, and increases profits.

CAM Accelerates Applications in APEX Devices

Because CAM is embedded inside APEX 20KE devices, it provides faster system performance than traditional discrete CAM.

Most memory devices store and retrieve data by addressing specific memory locations. Searching for an item in memory can take many clock cycles. The time required to find an item stored in memory can be reduced if it can be identified for access by the data content, rather than its address. Content-addressable memory (CAM) works in this way, making it ideal for high-speed search applications. Altera® APEX™ 20KE devices contain integrated blocks of CAM.

CAM Integration

Traditionally, most applications have used discrete CAM, in which the CAM is implemented as an individual device. A designer who wanted to use CAM had to add a CAM device to their printed circuit board (PCB), which increased design time and reduced the amount of useable PCB space. Discrete CAM also reduced system performance because it introduced additional on-chip and off-chip delays.

APEX 20KE devices, which contain on-chip CAM, eliminate the disadvantages of discrete CAM. Because CAM is embedded inside APEX 20KE devices, it provides faster system performance than traditional discrete CAM.

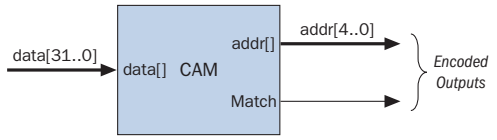
Using APEX 20KE CAM

Each embedded system block (ESB) in APEX 20KE devices can implement 32-word × 32-bit CAM. CAM searches all data in parallel and flags the address in which a particular word is stored.

CAM can be pre-loaded with data during configuration, or it can be written during system operation. A design can write "don't care" bits into words of the CAM; bits set to "don't care" do not affect matching.

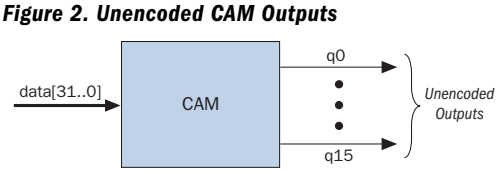
Output from CAM is either encoded or unencoded. The ESB can output an encoded address of the data location, which is better suited for designs without duplicate data in the memory. Reading this type of output only takes one clock cycle. See Figure 1.

Figure 1. Encoded CAM Outputs



If it is necessary for duplicate data to be written to multiple locations, an unencoded output should be used. In this mode, an ESB uses 16 outputs and reads the outputs in two cycles, 16 bits at each cycle, for a 32-bit word line. Each output represents one word of the CAM and goes high if the data matches that word of the CAM. See Figure 2.

Figure 2. Unencoded CAM Outputs



CAM Applications

CAM is used to optimize telecommunications, file-storage management, table look-up, pattern recognition, and other applications. This section describes how APEX CAM can be used in the following applications:

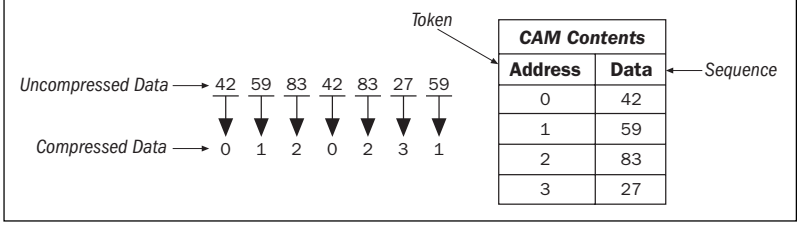
- Data Compression
- Network Switches
- Internet Protocol Filters
- PCI Applications

CAM is used to optimize telecommunications, file-storage management, table look-up, pattern recognition, and other applications.

Data Compression

Data compression removes redundancy in a piece of information, producing an equivalent but shorter message (see Figure 3). CAM look-up is performed after each word is presented. If the specific code is not found in the CAM, another word is shifted in. When the code is found, the CAM outputs the appropriate symbol and the input register is flushed. CAM generates a result in a single transaction regardless of the table size or length of the search list.

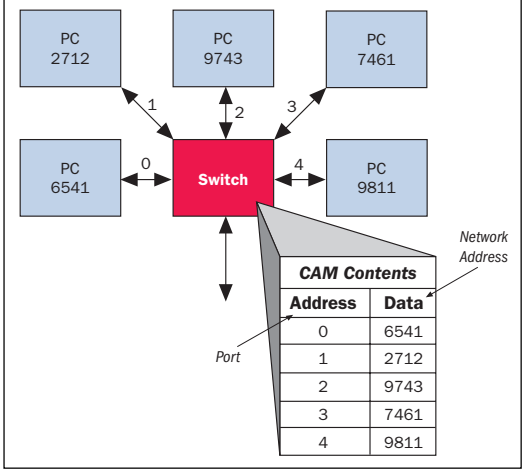
Figure 3. Data Compression Using Tokens



Switch Applications

CAM is used in switch applications to extract and process the address information from incoming packets. To switch a packet to the correct outgoing port, the incoming network address is compared with a table of network addresses stored in CAM. CAM outputs the destination for each data packet. See Figure 4.

Figure 4. Network Switch



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Hierarchical Instantiation Organizes Your Design

This article is the last of a four-part series that discusses practical design tips from Altera Applications, and focuses on the importance of hierarchical instantiation.

Hierarchical instantiation plays a particularly large role in VHDL designs and large digital designs. You should consider using a hierarchical design methodology to maximize your design's effectiveness and to focus your project.

Hierarchical instantiation involves dividing projects into an extensive tree of smaller design entities. Each entity has a specific purpose and a carefully declared method for interacting with other entities.

The principal benefit of hierarchical instantiation is organization. Each block serves a specific purpose and can be considered its own entity, allowing designers to focus on one design functionality at a time. This design technique also permits a high-level view of the design's overall structure, making it easier to uncover critical paths and potential trouble spots.

Labor Division

Well-divided projects lend themselves to proper labor division. Designers must often split a project between multiple engineers, and well-defined barriers can ease this task. Designers can easily separate projects and assign sections for individual attention.

Documentation & Revision Control

The organized nature of hierarchical designs creates key benefits in documentation and revision control. Individual, well-focused modules lead to the creation of complete documentation describing each block's functionality and how it interfaces with others. Thorough documentation also aids the debugging process and helps bring new engineers up to speed quickly. Revision control is also improved, because each change serves a well-defined purpose and can be carefully monitored and fully documented.

Error Detection

Hierarchical instantiation can facilitate error detection in assembled projects. Simulated nodes are easier to find because they can be referenced by their hierarchical location. Critical paths in timing analysis also stand out, especially within parallel modules that are instantiated in multiple locations.

Hierarchical Methodologies

Two fundamental design practices critical to hierarchical design include top-down design and bottom-up design methodology. Both methodologies contain their own strengths and break large designs into more manageable pieces. The best designs often use a mixture of these two design methodologies.

Top-Down Designs

Top-down designs start with a high-level understanding of a design's overall flow. Each design block's general functionality is described prior to developing the building blocks themselves. Top-down methodologies tend to create more organized designs, because designers must first evaluate the design's overall structure. In addition, by focusing on structure and leaving details of a design undefined, designers can delay technical considerations until they are at more manageable levels.

Bottom-Up Designs

In a bottom-up methodology, designers first create the lower-level blocks and then integrate these blocks into higher-level structures. Designers focus their attention on individual

sub-blocks rather than the design as a whole. Thus, individual blocks can be verified prior to building the entire design.

Bottom-up designs also highlight the benefits of reusable code. Splitting projects into smaller modules helps designers find redundant sections in a project. Designers can then reuse individual blocks of code, which saves time. In addition, designers can assemble commonly used functions into their regular design library, allowing blocks of code to be reused from project to project.

Re-useable code also lends itself to more efficient synthesis, as seen in the third article of this series, *Using Arithmetic Operators in MAX+PLUS II VHDL*. In that example, the careful placement of multiplexers allowed the use of one adder module where two might have been required otherwise. However, if the adder was not located in an instantiated block, it would have been difficult to discern this optimization.

Finally, parameterizable code can enhance design reuse. By creating parameterizable code, specific blocks can be targeted for multiple uses in the same design. This ability is what makes library of parameterized modules (LPM) functions, as well as numerous Altera functions, so effective.

For more information on creating an effective hierarchical design, contact Altera Applications at **sos@altera.com** or at (800) 800-EPLD.

Designers can assemble commonly used functions into their regular design library, allowing blocks of code to be reused from project to project.

CAM Accelerates Applications in APEX Devices, continued from page 15

Internet Protocol Filters

An Internet protocol filter is a security feature that allows you to keep unauthorized users from accessing local-area network (LAN) resources. The feature can also restrict Internet protocol traffic over a wide-area network (WAN) link. With an Internet protocol filter, LAN users can be restricted to specific applications on the Internet (such as e-mail). CAM works as a filter to block all access except for packets that have permission. The addresses with certain permissions are written into the CAM; when the address is sent to the memory, CAM reports whether it contains the address. If the address resides within CAM, it has permission for a particular activity. See Figure 5.

Figure 5. Using CAM as an IP Filter

CAM Contents	
Address	**Data**
0	01
1	27
2	3A
3	4D

Routed Packet	Permission
27	Permit
3A	Permit
4F	Denied
25	Denied

PCI Applications

On power-up, the peripheral component interconnect (PCI) bus must be configured so that each device's I/O and memory functions occupy mutually exclusive address ranges. Therefore, the system must be able to detect how many memory and I/O address ranges a device requires and the size of each. The base address registers permit this relocation and provide a mechanism for mapping devices into address spaces. Each interface can have up to six registers. CAM can be used to report which register is being accessed. Using CAM for a PCI application speeds up the register search, while using fewer logic elements (LEs).

CAM Speeds Applications

Altera's new APEX devices have integrated CAM into the ESB architecture. By searching for data instead of a location, CAM minimizes search times, allowing designers to make full use of APEX device speed and features.

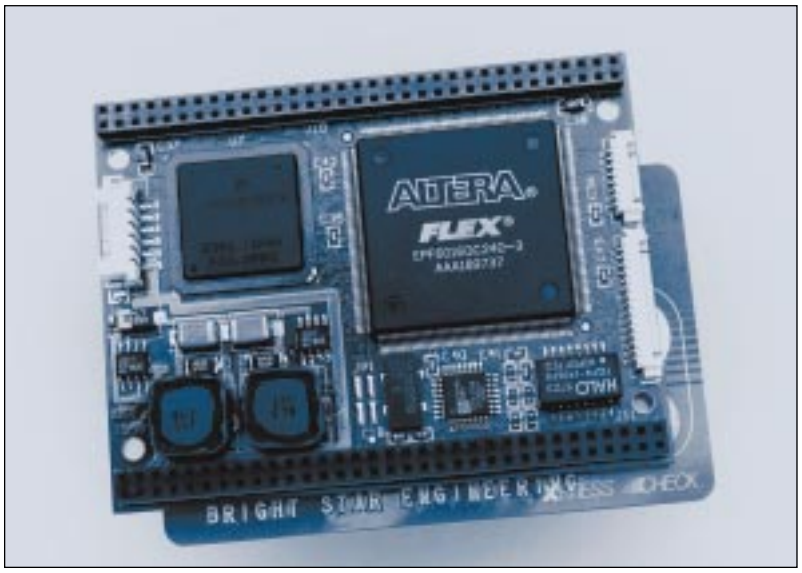
Bright Star Engineering & FLEX 6000 Devices Connect Products to the Internet

"Unlike traditional board-level products with fixed interfaces, the ipEngine-1 is capable of adapting itself to the user's hardware requirements. The Altera EPF6016 device provides extraordinary flexibility."
Stuart Adams, President, Bright Star Engineering

The Internet revolution is entering a new phase. Manufacturers everywhere want their embedded products to be "network-enabled"—that is, to have the ability to connect to the Internet. Users can communicate with a product that is linked to the Internet through their browser from anywhere in the world, offering significant benefits in a wide range of applications. For example, an engineer can troubleshoot network-enabled manufacturing equipment, solve problems, and get production back on track—all from a remote location using a laptop. With network-enabled diagnostic equipment, a doctor can evaluate vital data and give qualified advice to a patient hundreds of miles away. A large portion of our lives will soon be affected by the addition of network-enabled products.

Although adding network connectivity to a product is enticing, it can be expensive and time-consuming, especially if the manufacturer chooses to develop the hardware and software in house. Development and long-term maintenance costs may be prohibitive, and crucial time-to-market advantages can be lost. Bright Star Engineering (BSE) has developed a solution to eliminate these problems: the ipEngine-1. The ipEngine-1 is a miniature network computer on a board that comes complete with the hardware, software, and development environment required to network-enable a product. An Altera® FLEX® 6000 device is an integral piece of this product, as shown in Figure 1.

Figure 1. The ipEngine-1 Compares in Size to a Credit Card



Credit-Card-Size Board with Built-in Operating System & Web Server

The ipEngine-1 network computer uses a Motorola PowerPC MPC823 processor as its central processing unit (CPU). This device is set in a board only 3.4 inches wide by 2.6 inches long (see Figure 2).

The processor features a variety of on-chip peripherals including:

- 10Base-T Ethernet interface
- Universal serial bus (USB) host/slave controller
- Two serial ports
- Liquid-crystal display (LCD) video controller
- I_2C serial bus

The MPC823 processor also supports a variety of low-power operating modes, making it suitable for use in battery-powered applications. The ipEngine-1 16-Mbyte DRAM and a 2-Mbyte FLASH memory system provide storage for the operating system as well as the original equipment manufacturer's (OEM's) own application software and data.

For users who need a real-time operating system, the ipEngine-1 ensures full connectivity from the PowerPC processor to local area networks (LANs) and the Internet. The ipEngine-1 includes the BSE POSIX-based pKernel real-time network operating system (OS). The pKernel OS can integrate the following elements:

- TCP-IP networking
- Embedded Apache web server
- Local RAM file system
- Access to Internet files via FTP and HTTP
- Interactive command shell
- Software development kit

Alternatively, for those who prefer a non-real-time OS, the BSE Embedded Linux configuration fits the full Linux kernel plus network utilities, the Apache web server, and a Java Virtual Machine into the ipEngine-1 on-board FLASH memory.

Using the ipEngine-1

The ipEngine-1 makes converting an existing product into a network-enabled one a simple, two-step process. For example, a manufacturer might want to re-work a small control device with a matrix keypad into one with a network command interface. The first step is to remove the original matrix keypad, define a virtual matrix keypad in the EPF6016 device, and connect the I/O connector pins to the keypad input in the product. The second step is to write a small network-command-processor module for the PowerPC processor that translates the network commands into matrix keyboard "presses." The matrix keyboard information is then sent through the EPF6016 virtual interface to the control device. The new product is now ready.

Altera EPF6016 Device Provides Extraordinary Flexibility

For the external interface from the ipEngine-1 to the OEM product, BSE chose an Altera EPF6016QC240-3 programmable logic device (PLD). "Unlike traditional board-level products with fixed interfaces, the ipEngine-1 is capable of adapting itself to the user's hardware requirements. The Altera EPF6016 device provides extraordinary flexibility," said Stuart Adams, President of BSE. BSE has been working with Altera devices for several years and appreciates the abundance of features at a low cost. The company chose the EPF6016 device for the ipEngine-1 primarily because of these

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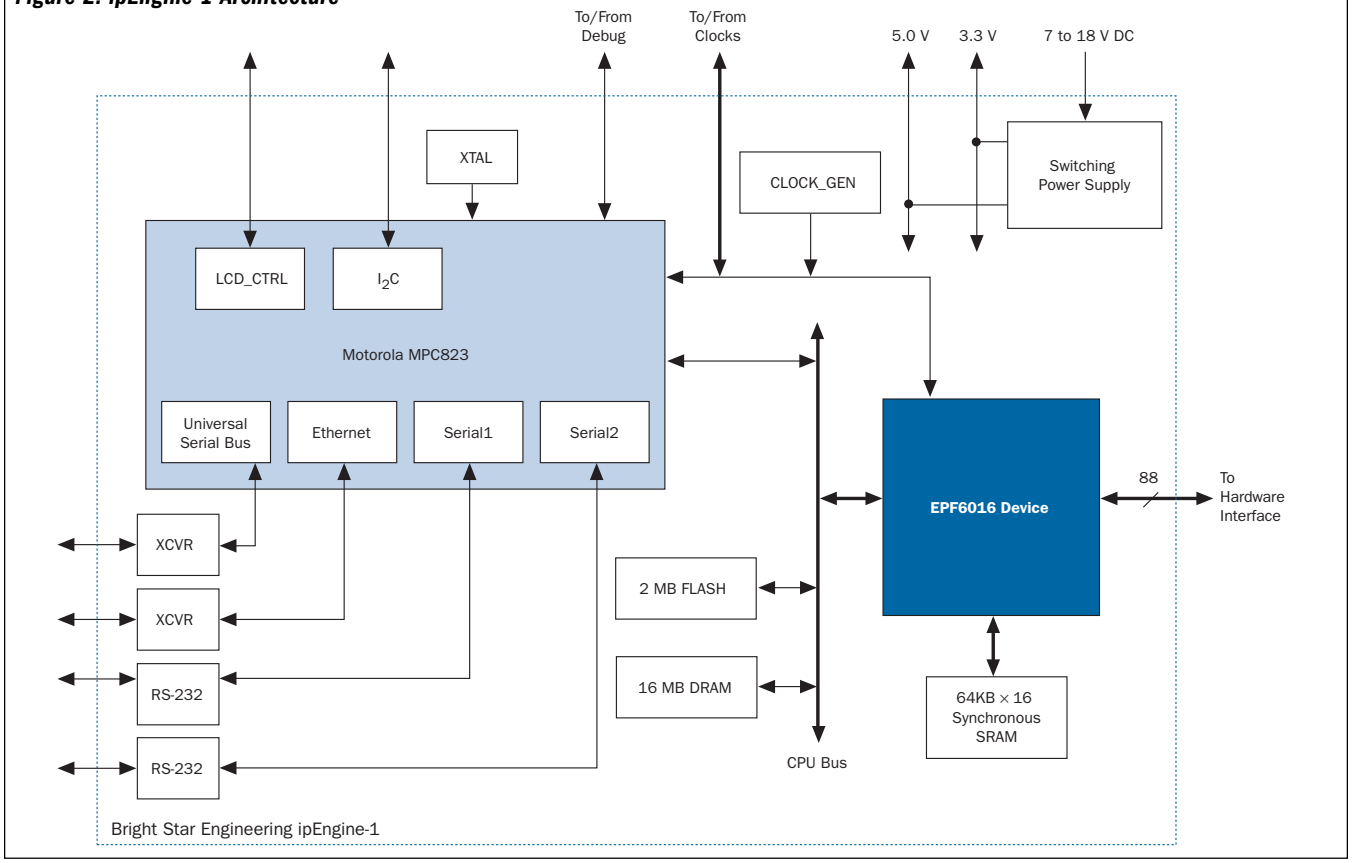
Figure 2. ipEngine-1 Architecture



Bright Star Engineering & FLEX 6000 Devices Connect Products to the Internet, continued from page 19

two reasons. "The EPF6016 device has the lowest cost per flipflop in the industry, so it lends itself to volume production, unlike expensive FPGAs from other companies," said Stuart Adams.

"With the freely available and easy-to-use BASELINE software and sample code from BSE, developers can get started right away."

The EPF6016 device forms an 88-pin "virtual interface" that is configured according to the manufacturer's particular needs. It can be used to either communicate with the existing I/O of an OEM product or to control and monitor the product's hardware. The EPF6016 device can emulate a variety of bus architectures as well as implement peripheral functions such as universal asynchronous receiver/transmitters (UARTs), pulse width modulation (PWM) controls, memory emulation, data capture and synthesis, and interfaces to a variety of devices. A synchronous 128-Kbyte × 16 SRAM is connected to the EPF6016 device. The SRAM can be used as a high-speed shared buffer storage for data coming from or going to the virtual interface.

MAX+PLUS II BASELINE Software Makes Configuration Free & Easy

For BSE and their customers, an added advantage of using an Altera device in the ipEngine-1 is the Altera MAX+PLUS® II BASELINE development software. By downloading the software free of charge from the Altera web site, **http://www.altera.com**, any developer can configure the EPF6016 device. Sample configuration files in the Altera Hardware Description Language (AHDL) and VHDL can be found on the BSE web site at **http://www.brightstareng.com**. "With the freely available and easy-to-use Altera BASELINE software and sample code from BSE, developers can get started right away," said Stuart Adams. To further simplify the process of configuring the EPF6016 device and defining the virtual interface, BSE is developing a library of pre-compiled configurations for the ipEngine-1 that will be available on their web site.

Conclusion

In the future, network-enabled products will change the way that we interact with the devices in our homes and workplaces. By integrating an Altera FLEX 6000 device into the ipEngine-1 and using the MAX+PLUS II BASELINE software for configuration, Bright Star Engineering is able to offer a miniature, highly flexible, and cost-effective network computer that can connect third-party products to the Internet today.

Bright Star Engineering, Inc.
19 Enfield Drive
Andover MA 01810
sales@brightstareng.com
http://www.brightstareng.com

Current Software Version

The latest version of Altera software is MAX+PLUS® II version 9.24. The MAX+PLUS II development system is available for Windows-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 platforms.

$20K for APEX 20K

Win $20,000 for charity and a Palm VII for yourself. Altera is celebrating the release of the new APEX 20K device family by giving away $20,000 to charity. The winner of the $20K for APEX 20K sweepstakes will be able to choose the recipient from a list of approved organizations, and will also receive a Palm VII to keep. For your chance to win or for more information about the speepstakes, visit the Altera web site at **http://www.altera.com/apex/20kfor20k.html**.

No purchase necessary. Void where prohibited. Open only to legal residents of the Continental U.S. who are 18 years of age or older as of 6/15/99, and who are engineers or engineering management currently employed by a company that uses programmable logic devices (semiconductors) manufactured by Altera Corporation. Internet entries must be received by 5 :00 p.m. on 7/15/99. Mail entries must be postmarked by 7/15/99 and received by 7/22/99. For complete rules and how to enter send a self addressed stamped envelope to P.O. Box 2032, Hollywood, CA 90078.

NWL Provides SDRAM Controller Integration with PCI/C

Northwest Logic Design (NWL), a new Altera Megafunction Partners Program (AMPP℠) partner, has developed an SDRAM controller with the three important characteristics of an intellectual property (IP) solution: performance, extensibility, and ease of use. The function also offers full integration with the Altera® `pci_c` 64-bit, 66-MHz peripheral component interconnect (PCI) MegaCore™ function.

This new controller offers upwards of 100-MHz performance when implemented in Altera FLEX® 10KE devices while providing a high degree of flexibility through multiple interface modules and user-defined parameters. The SDRAM controller features include:

- Clock speeds up to 100 MHz in FLEX 10KE devices
- 32- or 64-bit wide data bus support
- Full byte enable support
- Variable burst lengths
- Memory depths up to 64 Mbytes
- 168-pin DIMM and 144-pin SO-DIMM support
- Redundant I/O for large memory systems
- Parameterized timing specifications
- Pipelined access to maximize throughput
- Efficient bank management
- Automatic SDRAM initialization
- Automatic refresh

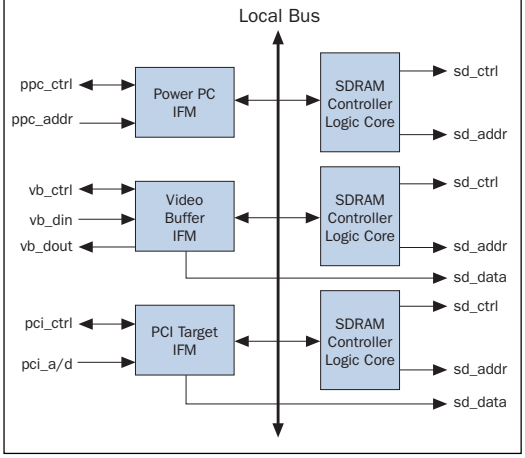
Performance

The SDRAM controller achieves performance of up to 100 MHz in most FLEX 10KE devices. Utilizing the latest timing models in the MAX+PLUS® II software, NWL provides a solution for systems requiring high-speed memory access.

Extensibility

As a natural addition to its design, the SDRAM controller features a set of interface modules—blocks that help integrate the SDRAM controller into a system. Figure 1 illustrates the extensions that are currently available, including the

Figure 1. SDRAM Controller Extensions



Motorola PowerPC 60x/750 interface, a video frame buffer interface, and a PCI target interface to the Altera `pci_c` MegaCore function. Table 1 describes the performance and utilization of these three extensions using the SDRAM controller in Altera FLEX 10KE devices.

Ease of Use

The SDRAM controller includes many features that make it easy to use. Currently, the SDRAM controller is available as an OpenCore™ megafunction. The design is fully parameterized. Support is available to help customers integrate NWL's SDRAM controller quickly and easily. In the future, MegaWizard™ Plug-In support will be available for this megafunction.

Table 1. SDRAM Controller Performance in FLEX 10KE Devices

Interface	Performance			
	Device	Speed (MHz)	Utilization	
			LEs	EABs
PowerPC	EPF10K200E-1	113	564	0
Video Buffer	EPF10K50E-1	100	960	8
PCI	EPF10K50E-1	66	2,041	5

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Synplify/Quartus Integration Streamlines APEX Designs & Design Flows

APEX™ devices allow designers to implement complex designs while achieving system performance requirements. The Quartus™ development system addresses designers' needs by supporting larger devices, enabling workgroup computing, and incremental compilation. The Synplify software builds on these capabilities by providing HDL-enhanced synthesis and graphical debugging. This article describes this integration and how it can help APEX designers.

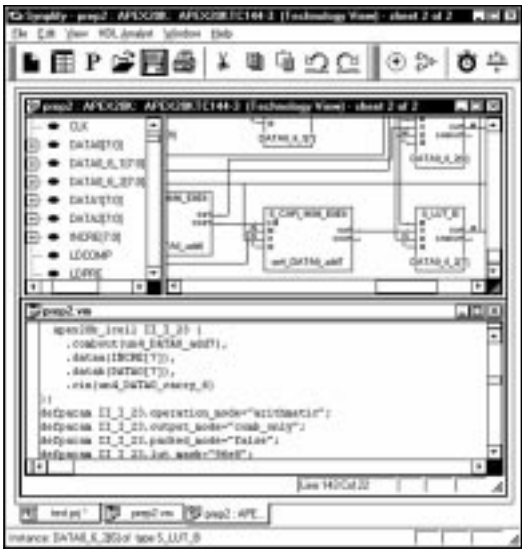
Under-the-Hood Integration

The Quartus software provides under-the-hood integration via the NativeLink™ feature, improving the synthesis power of the Synplify software. Enhancements in the Quartus development system allow the Synplify software to map the synthesized logic more efficiently into the APEX architecture. By understanding the exact structures used with this enhanced mapping, the Synplify software can optimize the design to meet system requirements.

The Quartus software provides a more powerful mapping element called an ATOM primitive that controls the mapping for all aspects of the APEX architecture, from logic elements (LEs) to memory elements to I/O cells. The Synplify software uses ATOM primitives in its netlist files, resulting in improved performance and logic utilization (see Figure 1). The use of the new ATOM primitive is automated within the Synplify software and does not require any extra effort from designers. The real impact is on the quality of results.

In addition to general improvements in the quality of results, the precise control over the logic implementation in APEX devices gives the Synplify software more accurate timing estimates. The Synplify software uses these timing estimates and the timing constraints set by the user to make synthesis decisions affecting utilization and performance. Underconstraining or overconstraining could cause inefficiencies that reduce overall system performance. By interpreting the timing delays, the Synplify software can accurately constrain and optimize the design.

Figure 1. APEX Logic Element Mapping



Streamlined Design Flow For Designers

In addition to improved optimization, there are a number of integration features that enable the Quartus and Synplify software to operate seamlessly together. The Quartus software has the ability to launch the Synplify software automatically as the default synthesis tool; the Synplify software is launched in batch mode to perform synthesis. All Synplify compile messages are displayed in the Quartus Message Window. After successful synthesis in the Synplify software, the Quartus software will place and route the design.

Alternatively, the Quartus development system allows the Synplify application to launch, compile, and access Quartus databases. Additionally, the Synplify software provides key

information that allows the Quartus software to cross-probe to the original Verilog HDL/VHDL code instead of the intermediate netlists.

As an example, the Synplify software can both launch and compile APEX designs for the Quartus software. After launching the Quartus development system, the user can start a Quartus project and compile the post-synthesis netlist file created by Synplify. Productivity is increased by speeding up and enhancing the communication between the Synplify and Quartus software.

Additionally, a "Quartus compile" step within the Synplify software automatically goes through the entire Altera place-and-route flow and generates log files and static timing analysis information. See Figure 2. This process saves time by combining multiple setup steps and makes the entire design flow more user friendly. After the Quartus compile step is done, the Synplify software has access to the post-place-and-route information to evaluate the results and make further refinements, if necessary.

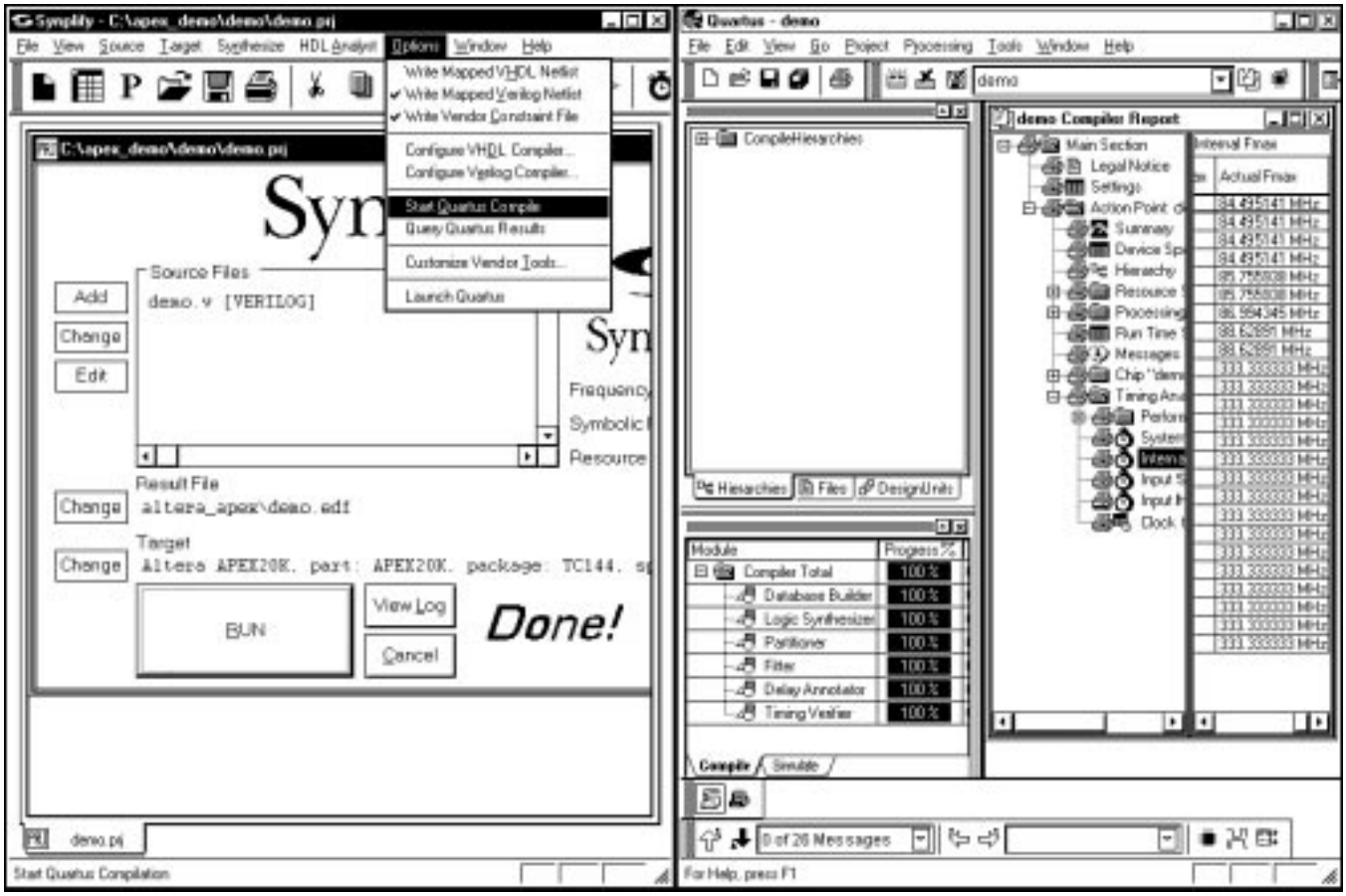
To enhance how designers debug and improve designs using both tools, the Synplify software links the Quartus software back to the source code. Designers no longer need to worry about tracing signals through intermediate netlists such as EDIF.

Summary

Through NativeLink integration, the Quartus software provides a powerful interface that allows the Synplify software to improve the design flow as well as the overall synthesis. The combination of the Quartus and Synplify software can create smaller, faster designs with less work for the designer.

Synplicity will release a version of the Synplify software in June 1999 that supports the Quartus development system. This release will add the Quartus integration that provides streamlined design flows and efficient mapping for APEX devices. Synplicity is committed to providing APEX designers the highest level of integration with the Quartus software.

Figure 2. Using the Quartus Compiler through the Synplify Software



SignalTap Embedded Logic Analyzer Provides Visibility of Internal PLD Signals

With the introduction of the SignalTap™ embedded logic analyzer, Altera takes the leadership role as a provider of development tools for multi-million gate designs. While these large devices enable System-on-a-Programmable-Chip™ designs, they also create new challenges.

System devices containing several "virtual components" can make it difficult for design engineers to access signals from internal programmable logic device (PLD) nodes for debugging and verification. Traditional tools cannot be used because they do not have access to internal nodes.

The solution: place the debugging tools inside the device as a megafunction. Design engineers can use the SignalTap logic analyzer to access internal nodes and signals on I/O pins.

Bench-Top Logic Analyzer Inside APEX Devices

The SignalTap embedded logic analyzer is a powerful new debugging tool that provides non-intrusive visibility of signals from internal nodes running at speed. It functions like a bench-top logic analyzer inside an APEX™ device, and includes the following features:

- *Channel width and acquisition depth*—Users can specify the number of input channels and depth of the sample buffer.
- *"At speed" acquisition*—The embedded logic analyzer captures signals synchronous to an internal global clock.
- *Powerful triggering*—The SignalTap logic analyzer contains a four-level trigger "sequencer" for triggering on a complex sequence of events.
- *Selective data storage*—Users can specify which data to save and which to ignore.
- *Integration with the Quartus™ software*—The analyzer controls and display are integrated within the Quartus development software.

Scalable Architecture

The SignalTap parameterized megafunction lets you choose how many internal signals to capture. Input channels may be selected in any power of two, limited only by the number of logic elements (LEs) and embedded system blocks (ESBs) available. Table 1 shows the impact of channel count on LE usage.

Table 1. LE Usage

Analyzer Channels	LEs	EP20K400 Usage
1	136	0.82%
2	144	0.87%
4	160	0.96%
8	192	1.15%
16	256	1.54%
32	384	2.31%
64	640	3.85%

Acquisition data may be saved in internal memory blocks, then transferred off-chip via the IEEE Std. 1149.1 Joint Test Action Group (JTAG) port. The number of ESBs used by the SignalTap logic analyzer depends on the number of input channels used and the depth of the sample buffer. Table 2 shows the ESB usage based on channel width and buffer depth.

The SignalTap logic analyzer is a synchronous (state) analyzer, capturing internal signals synchronous to a user-selected internal global clock. The acquisition data represents the "states" of the internal circuitry running at speed.

Table 2. Embedded System Block Usage					
Channels	Buffer Samples				
	128	256	512	1,024	2,048
1	1	1	1	1	1
2	1	1	1	1	2
4	1	1	1	2	4
8	1	1	2	4	8
16	1	2	4	8	16
32	2	4	8	16	32
64	4	8	16	32	64

Powerful Triggering

One of the biggest challenges while debugging a design is isolating improper circuit operation. The SignalTap logic analyzer provides powerful multi-level triggering with selective data storage to locate the problem and capture the information of interest.

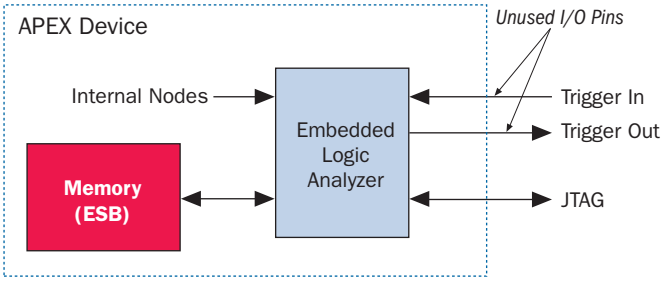
SignalTap trigger resources include:

- *Four pattern recognizers*—Patterns define logic events based on a combination of high, low, rising edge, falling edge, and "don't care" conditions across all input channels.
- *Time and count qualification*—Each pattern may be further qualified by its duration (time) or number of occurrences (count).
- *Delayed trigger*—A trigger delay can be used to postpone triggering by a specified period after a pattern is recognized.
- *Four-level trigger sequence*—Patterns can be linked together using an `IF/THEN/ELSE/STORE` structure to create a sequence of events that must occur before the analyzer triggers.
- *Selective data storage*—This feature, which can be set on each trigger level, lets you save important data and ignores meaningless information.
- *Trigger I/O*—External trigger input and trigger output signals can be used to synchronize the logic analyzer with external test equipment (or vice versa).

Multiple Analyzer Configurations

The SignalTap logic analyzer has been designed to handle all types of problems. It can be used in any of several configurations to match the debugging task at hand. The entire analyzer is contained within the APEX device (see Figure 1). Acquisition data is saved to internal RAM, then streamed off-chip after being triggered.

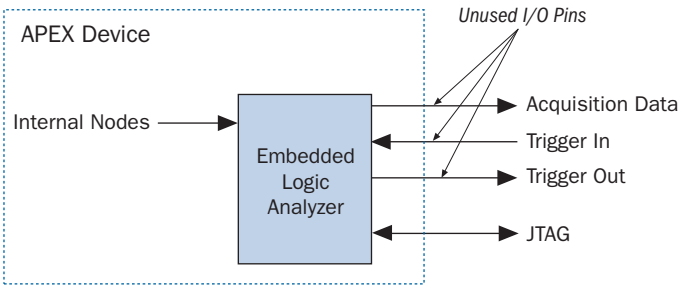
Figure 1. Embedded Logic Analyzer



You can connect analyzer trigger input and output signals to unused I/O pins for synchronization to external devices or events.

The debugging port configuration routes internal signals to unused I/O pins for acquisition by an external logic analyzer (see Figure 2).

Figure 2. Debug Port



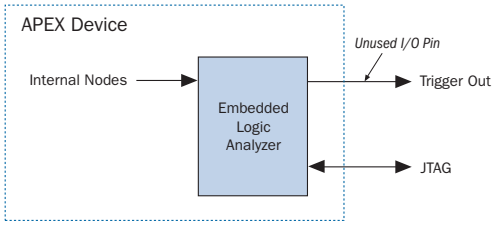
In the one-wire equivalent mode, the trigger logic of the SignalTap function generates an output based on the occurrence of an internal event (see Figure 3 on page 26). The width of the trigger output pulse can be set to represent the duration of a pattern or trigger level.

continued on page 26

SignalTap Embedded Logic Analyzer Provides Visibility of Internal PLD Signals, continued from page 25

The SignalTap logic analyzer is an integral part of the Quartus development software, providing a single environment for PLD development, debugging, and verification.

Figure 3. One-Wire Equivalent



The trigger output, when captured by an external logic analyzer or oscilloscope, can be used to determine specific information about the trigger event, such as:

- Whether the event occurred
- How many times it occurred
- The duration of the internal event
- The duration variation (jitter)

MasterBlaster Communications Cable

The MasterBlaster™ communications cable shown in Figure 4 is used for downloading designs to the device. It also provides set up, control, and data transfer information from the SignalTap logic analyzer.

Figure 4. MasterBlaser Communications Cable

The MasterBlaster communications cable connects to a host PC via a standard serial or universal serial bus (USB) port, and to the target system using a 10-pin female connector. It provides a multi-voltage interface to the target system, supporting V_{CC} levels between 1.8 V and 5.0 V, and future lower-voltage standards.

Integrated with Quartus Software

The SignalTap logic analyzer is an integral part of the Quartus development software, providing a single environment for PLD development, debugging, and verification.

Internal nodes are selected using the Quartus Node Finder and then dropped onto the logic analyzer window, automatically assigning them for capture. Analyzer setup—including triggering, sample buffer configuration and run control—is provided by a single, intuitive user interface in the Quartus software.

Once the analyzer is created and configured, it is compiled with the rest of the design and downloaded to the target device. Triggering changes can be made on-the-fly without recompiling the design. Data acquired by the logic analyzer is presented in the Quartus software as a waveform for analysis.

SignalTap Plus System Analyzer

During system integration, designers face a new set of challenges—interfacing the PLD with the rest of the system. Understanding how all elements on the board interact from a system level becomes the critical task. The SignalTap Plus system analyzer from Boulder Creek Corporation addresses this need. For more information on the SignalTap Plus system analyzer, go to the Boulder Creek Corporation web site at **http://www.bcreek.com**.

Conclusion

The SignalTap logic analyzer provided with the Quartus development software lets you view signals within a device. This new technology allows you to spend less time debugging, resulting in increased productivity.

Questions & Answers

Q *Why should the* TCK *port be pulled low instead of high?*

A When a device with TMS and TCK both pulled high is powered up, the IEEE Std. 1149.1 Joint Test Action Group (JTAG) TAP controller should stay within the base, or TEST_LOGIC/RESET state. However, during some power-up processes, the transition from the unpowered low level to a powered high level occurs at slightly different moments in time between TMS and TCK. See Figure 9 in *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)*.

If TMS and TCK rise to a high level at the same time, or if TMS rises before TCK, you should not have a problem. However, if TCK rises before TMS, the JTAG TAP controller recognizes a rising edge on the state machine clock, with a TMS signal equal to 0, and shifts the device into the RUN_TEST/IDLE state. The device stays in this state until it receives further control signals from the JTAG port. Therefore, TCK should be pulled low through a 1-kΩ resistor, both for blank and programmed devices. See Figure 4 in *Application Note 95 (In-System Programmability in MAX Devices)*.

Q *Why doesn't my multi-clock design function properly on the board even though the simulation shows the proper results?*

A When using multiple clocks, you should follow good asynchronous design practices, such as:

- Use registers to synchronize data when transferring from one clock domain to another.
- Use a first-in first-out (FIFO) buffer to transfer data from one clock domain to another.

Without following these techniques, registers in the device may have setup and hold time violations when driven by data synchronized with different clocks. You can view this type of error in your simulation if you turn on the *Setup/Hold* option in the MAX+PLUS® II or Quartus™ Simulator.

This guideline does not apply to circuits with different clock domains that do not interact with each other.

Q *Why does the MAX+PLUS II software issue the error "Device 'device name' does not have JTAG attribute information" for a non-Altera device after I have entered in the JTAG attribute information?*

A You may receive this error if you entered the JTAG attribute information for a non-Altera device and included a space character in the *Device Name* field of the **JTAG Device Attributes** dialog box. To avoid this error, remove the space character from the name.

Q *Can I use a Memory Initialization File (.**mif**) to initialize memory created using the* lpm_ram_dq *function and implemented with logic elements (LEs) or macrocells?*

A No, MIFs are only used to initialize memory in FLEX® 10K embedded array blocks (EABs) or APEX™ embedded system blocks (ESBs) during device configuration. You cannot use MIFs to initialize RAM blocks that have not been implemented in EABs because all registers in LEs or macrocells initialize to zero after power-up or configuration.

If you want to use an initialized RAM block, use a MIF to initialize a block that is implemented in EABs or APEX ESBs.

Q *How can I improve my t_{SU} and t_{CO} timing requirements for FLEX 10K device bidirectional pins?*

A It is possible to improve t_{SU} and t_{CO} on a FLEX 10K bidirectional pin by breaking it up into an input and output pin and using the I/O element (IOE) registers for both pins. Using the global clock to drive the IOE registers for both input and output pins gives the best possible times for t_{SU} and t_{CO} for the signal.

continued on page 28

Questions & Answers, continued from page 27

Q *Why can't my pick-and-place machine distinguish the solder balls on a ball-grid array (BGA) package from the underside of the device when trying to mount the device?*

A The underside of some BGA packages are too shiny for pick-and-place machines to distinguish the solder balls from the bottom of the device. Many pick-and-place machines expect the underside to be a dark, dull color in which the balls are easily distinguishable from the background. To help distinguish the balls from the shiny underside, recalibrate the pick-and-place machine. Contact the machine's vendor for help with the recalibration.

Q *Why do I receive the warning: "Current device family <device family> does not support dual-port synchronous RAM - implementing the synchronous RAM as a* `dffe` *array instead. (*`dcfifo`*, FLEX 10K)?"*

A The `dcfifo` function is most efficiently implemented in EABs or embedded system blocks (ESBs) that support dual-port RAM (e.g., FLEX 10KE or APEX devices).

If you are not using a FLEX 10KE or APEX 20K device, the `dcfifo` function will be implemented as an array of `dffe` functions to achieve the dual-clocked behavior that is an integral part of the `dcfifo` function.

If you do not require a dual-clock FIFO buffer, use the `scfifo` function, which only requires single-clocked EABs. This megafunction can be implemented using EABs in any FLEX 10K device.

Q *Does the EPC2 device have a fixed programming pulse width?*

A Yes, EPC2 devices have a fixed programming pulse width, which allows them to be programmed on in-circuit testers using Serial Vector Format Files (**.svf**). You do not need to order special fixed-algorithm EPC2 devices.

Q *Can I program MAX® devices and configure FLEX devices in the same JTAG chain using the Jam™ Player?*

A Yes, you can program MAX devices and configure FLEX devices in the same JTAG chain using a Jam Byte-Code File (**.jbc**) or Jam File (**.jam**). You should pass both the `DO_PROGRAM=1` and `DO_CONFIGURE=1` initialization variables to the Jam Player version 1.1 to perform both functions.

Q *Why can't I generate an SVF File from the MAX+PLUS II software to program MAX 7000AE devices via my test platform?*

A To program MAX 7000AE devices with an SVF File, you must use devices that support a "fixed" or constant programming algorithm. Altera has not yet released fixed programming algorithm MAX 7000AE devices. When the devices are released, the MAX+PLUS II software will be updated to support SVF File generation. For more information about planned release dates and other availability details, contact your local Altera representative or Altera Customer Marketing.

Q *Can I configure a subset of the FLEX devices in a Multi-Device FLEX Chain?*

A No, you must configure all of the devices in the FLEX chain. You cannot selectively configure a device, like you can in a JTAG chain.

Q *Why do I get the error "I/O error: cannot open device \\. \ALTLPT1. Check port number and device driver installation." when running the Jam Player on my Windows NT workstation?*

A The most likely cause of this error is that the ByteBlaster™ download cable driver has not been installed on your PC. Search for "ByteBlaster" in the Atlas Solutions database on the Altera web site (**http://www.altera.com**) for details on how to install the driver.

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on the Altera web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- *MasterBlaster Serial/USB Communications Cable Data Sheet* (A-DS-MASTERBL-01)
- *MAX 3000A Programmable Logic Device Family Data Sheet* (A-DS-M3000A-01)
- *Quartus Programmable Logic Development System & Software Data Sheet* (A-DS-QUARTUS-01)
- *SignalTap Embedded Logic Analyzer Megafunction Datasheet* (A-DS-SIGNALTAP-01)
- *AN 109: Using the HP 3070 Tester for In-System Programming* (A-AN-109-01)
- *AN 110: Gate Counting Methodology for APEX 20K Devices* (A-AN-110-01)
- *AN 111: Embedded Programming Using the 8051 & Jam Byte-Code* (A-AN-111-01)
- *AN 112: Integrating Product-Term Logic in APEX 20K Devices* (A-AN-112-01)
- *AN 115: Using the ClockLock & ClockBoost Features in APEX Devices* (A-AN-115-01)
- *AN 116: Configuring APEX 20K, FLEX 10K & FLEX 6000 Devices* (A-AN-116-01)
- *Component Selector Guide* (M-SG-COMP-06)
- *Development Tools Selector Guide* (M-SG-TOOLS-14)

Altera Programming Support

Altera® and third-party programming support is available for your Altera devices.

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for selected Altera devices. Algorithms are supplied via Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Microsystems' BBS. Programming support for configuration, MAX® 9000, and MAX 7000 devices is shown in Table 1. All information is subject to change.

Table 1. Third-Party Programming Hardware Support

Device	Data I/O (1)	BP Microsystems (2)
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPC1441	✓	✓
EPM7032	✓	✓
EPM7032AE	(3)	(3)
EPM7032S	✓	✓
EPM7064	✓	✓
EPM7064AE	(3)	(3)
EPM7064S	✓	✓
EPM7096	✓	✓
EPM7128A	✓	✓
EPM7128S	✓	✓
EPM7128AE	(3)	(3)
EPM7128E	✓	✓
EPM7160E	✓	✓
EPM7192S	✓	✓
EPM7192E	✓	✓
EPM7256A	(3)	✓
EPM7256AE	(3)	(3)
EPM7256S	✓	✓
EPM7256E	✓	✓
EPM7512AE	(3)	(3)
EPM9320	✓	✓
EPM9320A	✓	✓
EPM9400	✓	✓
EPM9480	✓	✓
EPM9560	✓	✓
EPM9560A	✓	✓

Notes:
(1) These devices are supported by Data I/O 3900 version 6.0 and UniSite programmers version 6.0.
(2) These devices are supported by BP Microsystems programmers version 3.40.
(3) Please contact Data I/O or BP Microsystems about programming support for these devices.

Programming Hardware Support

The following table contains the latest programming hardware information for Altera devices. For correct programming, use the software version shown in "Current Software Version" on page 20. Table 2 lists Altera programming adapters for MAX 9000, MAX 7000, and configuration devices.

Table 2. Altera Programming Adapters (Part 1 of 2) *Note (1)*

Device	Package *(2)*	Adapter
EPC1064 *(3)* EPC1064V *(3)* EPC1441 *(4)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(4)* EPC1213 *(3)*	DIP, J-lead	PLMJ1213
EPC2 *(5)*	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(6)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(6)* PLMR9000-240NC *(6)*
EPM7032	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032V	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7064AE	FBGA (100-pin)	PLMF7000-100
EPM7064S	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(6)*
EPM7064AE	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC *(6)*
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

Table 2. Altera Programming Adapters (Part 2 of 2) *Note (1)*

Device	Package *(2)*	Adapter
EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A EPM7128AE	J-lead (84-pin) TQFP (100-pin) TQFP (144-pin) FBGA (100-pin) FBGA (256-pin)	PLMJ7000-84 PLMT7000-100NC *(6)* PLMT7000-144NC *(6)* PLMF7000-100 PLMF7000-256
EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(6)* PLMT7000-100NC *(6)* PLMQ7128/7160-160NC *(6)*
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(6)* PLMQ7128/7160-160NC *(6)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC *(6)*
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A	TQFP (100-pin) TQFP (144-pin) PQFP (208-pin) FBGA (256-pin)	PLMT7000-100NC PLMT7000-144NC PLMR7256-208NC PLMF7000-256
EPM7256A EPM7256S	PQFP (208-pin) RQFP (208-pin)	PLMR7256-208NC *(6)* PLMT7256-208NC *(6)*
EPM7256AE	TQFP (100-pin) FBGA (100-pin) TQFP (144-pin) FBGA (256-pin)	PLMT7000-100NC PLMF7000-100 PLMT7000-144NC PLMF7000-256
EPM7512AE	TQFP (144-pin) PQFP (208-pin) BGA (256-pin) FBGA (256-pin)	PLMT7000-144NC *(6)* PLMR7256-208NC *(6)* PLMB7000-256 PLMF7000-256

Notes to Table 2:
(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on MAX 5000 and Classic™ devices. Altera offers an adapter exchange program for 0.8-µm EPM5032, EPM5064, and EPM5130 programming adapters.
(2) FBGA: FineLine BGA™ packages.
(3) FLEX® 8000 configuration device.
(4) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(5) APEX 20K, FLEX 10K, or FLEX 6000 configuration device.
(6) These devices are not shipped in carriers.

Download Cables

Table 3 provides programming and configuration compatibility information for the MasterBlaster™ serial or universal serial bus (USB) communications cable, and the BitBlaster™ serial and ByteBlasterMV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable.)

Table 3. Download Cable Compatibility

Device	BitBlaster	ByteBlasterMV	MasterBlaster
APEX 20K		✓ *(1)*	✓
APEX 20KE		✓ *(1)*	✓
FLEX 10K	✓	✓	✓
FLEX 10KA		✓	✓
FLEX 10KE		✓ *(1)*	✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓ *(2)*	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A		✓	✓

Notes:
(1) The ByteBlasterMV download cable must operate at 3.3 V for these devices. Therefore, set `VCCIO` pins to 3.3 V.
(2) For the FLEX 6000 family, this download cable is only compatible with EPF6016 devices.

Altera Device Selection Guide

Current information for the Altera® APEX™ 20K, FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, MAX 7000, MAX 3000A, and configuration devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide*.

For the most up-to-date information, go to the Altera web site at **http://www.altera.com**. Some of the devices listed may not be available yet. Contact Altera or your local sales office for the latest device availability.

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	MACROCELLS
EP20K100	100,000	144-Pin TQFP, 196-Pin FBGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin FBGA[2], 356-Pin BGA	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 196-Pin FBGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin FBGA[2], 356-Pin BGA	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 400-Pin FBGA[2]	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin FBGA[2]	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin FBGA[2], 652-Pin BGA, 672-Pin FBGA[2]	1.8 V	8,320	106,496	832
EP20K300E	300,000	208-Pin RQFP, 240-Pin RQFP, 652-Pin BGA, 672-Pin FBGA[2]	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin FBGA[2]	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	208-Pin RQFP, 240-Pin RQFP, 652-Pin BGA, 672-Pin FBGA[2]	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	652-Pin BGA, 672-Pin FBGA[2], 784-Pin FBGA[2]	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	784-Pin FBGA[2], 984-Pin PGA	1.8 V	42,240	540,672	4,224

Notes:
(1) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.
(2) This package is a space-saving FineLine BGA™ package.

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin FBGA[1]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin FBGA[1], 356-Pin BGA, 484-Pin FBGA[1]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin FBGA[1], 484-Pin FBGA[1]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin FBGA[1]	189, 189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin FBGA[1], 356-Pin BGA, 484-Pin FBGA[1]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin FBGA[1], 356-Pin BGA, 484-Pin FBGA[1]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin FBGA[1], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin FBGA[1]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin FBGA[1], 356-Pin BGA, 484-Pin FBGA[1]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin FBGA[1], 600-Pin BGA 672-Pin FBGA[1]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin FBGA[1]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin FBGA[1], 600-Pin BGA, 672-Pin FBGA[1]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

FLEX 8000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	5.0 V	-2, -3, -4	282	208
EPF8282AV	2,500	100-Pin TQFP	78	3.3 V	-3, -4	282	208
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 68, 120	5.0 V	-2, -3, -4	452	336
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 118, 136, 136	5.0 V	-2, -3, -4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	112, 120, 152, 152, 152	5.0 V	-2, -3, -4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184, 184	5.0 V	-2, -3, -4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208, 208	5.0 V	-2, -3, -4	1,500	1,296

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP, 100-Pin FBGA[1], 256-Pin FBGA[1]	81, 117, 81[2], 139[2]	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin FBGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin FBGA[1]	81, 81, 117[2], 171, 218[2]	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin FBGA[1]	117, 171, 199, 218, 218[2]	3.3 V	-1, -2, -3	1,960	1,960

Notes to tables:

(1) This package is a space-saving FineLine BGA package.

(2) This data is preliminary. For the most up-to-date information, contact Altera Applications at (800) 800-EPLD.

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[1]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[1]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[1]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX, FLEX 10K, FLEX 10KE, and FLEX 6000 devices

Note:
(1) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032	32	44-Pin PLCC/TQFP/PQFP	36	5.0 V	-6, -7, -10, -12, -15
EPM7064AE	64	44-Pin PLCC/TQFP, 100-Pin TQFP, 100-Pin FBGA[1]	38, 68, 68	3.3 V	-4, -7, -10
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68, 68	5.0 V	-6, -7, -10, -12, -15
EPM7096	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	5.0 V	-7, -10, -12, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin FBGA[1], 144-Pin TQFP, 256-Pin FBGA[1]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin FBGA[1], 144-Pin TQFP, 256-Pin FBGA[1]	68, 84, 84, 100, 100	3.3 V	-5,-7,-10
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-7, -10, -12, -15, -20
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 104	5.0 V	-10, -12, -15, -20
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7192E	192	160-Pin PQFP/PGA	124	5.0 V	-12, -15, -20
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin FBGA[1]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 100-Pin FBGA[1], 256-Pin FBGA[1]	84, 120, 164, 84, 164	3.3 V	-6, -7, -10
EPM7256S	256	208-Pin RQFP/PQFP	164	5.0 V	-7, -10, -15
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164, 164	5.0 V	-12, -15, -20
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin FBGA[1], 256-Pin BGA	120, 176, 212, 212	3.3 V	-7, -10, -12

Note:
(1) This package is a space-saving FineLine BGA package.

MAX 3000A Devices					
DEVICE	**MACROCELLS**	**PIN/PACKAGE OPTIONS**	**I/O PINS**	**SUPPLY VOLTAGE**	**SPEED GRADE**
EPM3032A	32	44-pin PLCC, 44-pin TQFP	34, 34	3.3 V	-4, -7, -10
EPM3064A	64	44-pin PLCC, 44-pin TQFP, 100-pin PQFP	34, 34, 64	3.3 V	-4, -7, -10
EPM3128A	128	100-pin TQFP, 144-pin PQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-pin TQFP, 208-pin PQFP	116, 158	3.3 V	-6, -7, -10

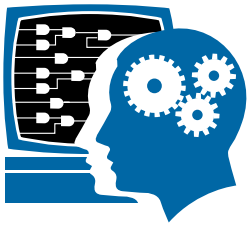
How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera:

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	Altera Literature Services	(888) 3-ALTERA **lit_req@altera.com**	(408) 544-7144 *(2)* **lit_req@altera.com**
	World-Wide Web	**http://www.altera.com**	**http://www.altera.com**
Non-Technical	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
Customer Service	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline (6 a.m. to 6 p.m. Pacific Time)	(800) 800-EPLD (408) 544-7000	(408) 544-7000 *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**sos@altera.com**	**sos@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com**	**http://www.altera.com**

Notes:
(1) The *MAX+PLUS II Getting Started* manual is available from the Altera web site. To obtain other MAX+PLUS II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

Altera Tools for Training Program



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PCI Megafunctions

Megafunction	Source
64-Bit PCI Master/Target Function	Altera MegaCore Function
64-Bit PCI Bus Master/Target (EC240)	Eureka Technology
64-Bit PCI Bus Master/Target Interface	PLD Applications
64-Bit PCI Target	Eureka Technology
64-Bit PCI Bus Target Interface	PLD Applications
Parameterized 32-Bit PCI Master/Target	Altera MegaCore Function
32-Bit PCI Bus Target Interface	PLD Applications
32-Bit PCI Master/Target with Burst	Eureka Technology
32-Bit PCI Master/Target with Burst	PLD Applications
32-Bit PCI Master/Target with DMA Controller	Altera MegaCore Function
32-Bit PCI Target with Burst	Altera MegaCore Function
32-Bit PCI Target with Burst	Eureka Technology
PCI Hostbridge	Eureka Technology

MegaCore™

Other Bus Interface Megafunctions

Megafunction	Source
CAN Bus	Sican Microelectronics
IEEE 1284 Parallel Slave Interface	SIS
IEEE 1394-Compatible Link Layer Controller (LLC-1)	Phoenix Technologies
IEEE 1394A Function	SIS
IIC Master	Sican Microelectronics
IIC Slave	Sican Microelectronics
PowerPC Bus Arbiter (EP300)	Eureka Technology
PowerPC Bus Master (EP200)	Eureka Technology
PowerPC Bus Slave (EP100)	Eureka Technology
SDRAM Controller	Northwest Logic Design
SDRAM Controller	Stargate Solutions
Si-Enable USP-86: USB Host Controller	Simple Silicon
Si-Function: USB Function Controller	Simple Silicon
Si-Function: USB Hub Controller	Simple Silicon
Si-Link: IEEE 1394 Link Layer Controller	Simple Silicon
USB Function Controller	Sapien Design
USB Host Controller	Sapien Design
VUSB Embedded Host Controller	VAutomation

AMPP℠ ALTERA MEGAFUNCTION PARTNERS PROGRAM

OpenCore™

Discontinued Devices Update

Altera has no new announcements regarding discontinued devices. Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.