News & Views
Third Quarter, August 1999
Newsletter for Altera Customers

ALTERA®
The Programmable Solutions Company™

MAX 7000B Devices Provide Solutions for High-Performance Applications

The feature-rich, product-term-based MAX® 7000B devices offer propagation delays as fast as 3.5 ns and support for advanced I/O standards such as Gunning transceiver logic plus (GTL+). These features make MAX 7000B devices ideal for high-performance applications such as telecommunications switches, high-density storage systems, and medical imaging equipment. The devices range in density from 32 to 512 macrocells and feature 2.5-V in-system programmability (ISP) and Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71 support. MultiVolt™ I/O operation allows MAX 7000B devices to interface with 1.8-V, 2.5-V, and 3.3-V devices. Table 1 compares MAX 7000 device features.

High Performance

MAX 7000B devices offer propagation delays (t_{PD}) as fast as 3.5 ns. At such fast speeds, MAX 7000B devices can implement counters operating at frequencies in excess of 200 MHz. With peripheral component interconnect (PCI)-compatible, high-performance devices across the entire product family, MAX 7000B devices are ideal for a variety of high-speed applications ranging from address decoding to complex control circuits.

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Table 1. MAX 7000 Performance Enhancements Over Time

Feature	MAX 7000	MAX 7000S	MAX 7000A	MAX 7000B
Macrocell Range	32 to 256	32 to 256	32 to 512	**32 to 512**
Supply Voltage	5.0 V	5.0 V	3.3 V	**2.5 V**
Fastest t_{PD}	7.5 ns	5.0 ns	4.5 ns	**3.5 ns**
MultiVolt I/O	✓	✓	✓	✓
ISP Support		✓	✓	✓
Hot Socketing			✓	✓
FineLine BGA and 0.8-mm BGA Packaging			✓	✓
Advanced I/O Standards				✓
Year of Introduction	1991	1995	1998	**1999**

64-Bit, 66-MHz PCI
Master/Target Core

- 64-Bit, 66-MHz Peripheral Component Interconnect (PCI)-Compliant Solution with APEX™ 20K and FLEX® 10KE Devices
- Up to 528-Mbytes/Second Throughput
- 64-Bit Addressing
- Up to Six Base Address Registers (BARs)
- Compact PCI Hot-Swap
- Host Bridge Support

100% PCI-Compliant Solutions

MegaCore Solutions		
Megafunction	**Features**	**Logic Elements Utilized**
PCI/C	64-Bit, 66-MHz PCI Compliant, Master/Target Interface, Up to 528-Mbytes/Second Throughput, Zero-Wait-State Master and Target	1,200
PCI/B	32-Bit, 33-MHz Master/Target Interface, Supports Host Bridge Applications, Independent Master and Target Operations, Up to 132-Mbytes/Second Read and Write	1,050
PCI/A	32-Bit, 33-MHz Master/Target Interface, Integrated DMA and EAB Buffer, Zero Wait-State	1,050
PCIT1	32-Bit, 33-MHz Burst Target Only Interface, Zero Wait-State, Type Zero Configuration Space	550

Test-drive the megafunction before purchase with the OpenCore™ feature from the Altera web site.

http://www.altera.com/IPmegastore

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Call your local Altera field sales representative today for more information.

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MAX 7000B device features include global clocking, fast input registers, and programmable slew-rate control.

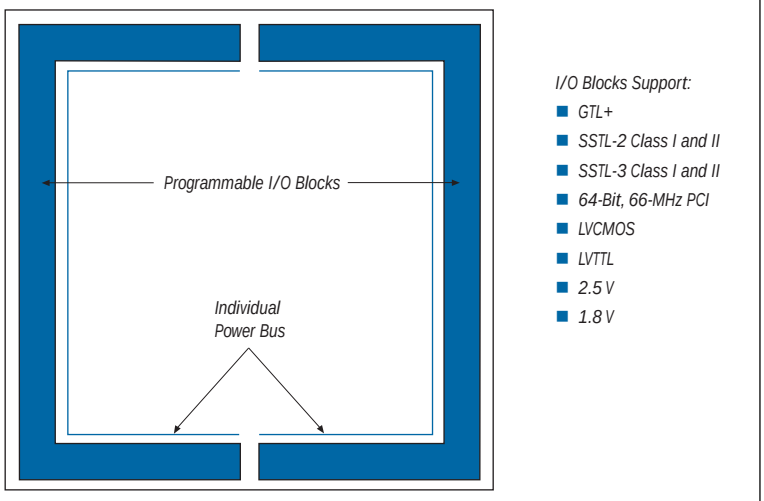
MAX 7000B Devices Provide Solutions for High-Performance Applications, continued from page 1

Advanced I/O Interface Standard Support

Figure 1 shows the MAX 7000B I/O blocks. Each of the two I/O blocks can be configured separately, allowing multiple I/O standards on the same device. MAX 7000B devices are the product-term leader in I/O standard support, and are the only product-term-based devices to support the following I/O standards:

- GTL+
- Stub series terminated logic, 2.5 V (SSTL-2) Class I, II
- SSTL-3, Class I, II

Figure 1. MAX 7000B I/O Blocks



Altera® MAX 7000B devices also support the following I/O standards:

- 64-bit, 66-MHz PCI applications
- Low-voltage transistor-to-transistor logic (LVTTL)
- Low-voltage CMOS (LVCMOS)

Feature Rich

Altera MAX 7000B devices offer ISP, Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry, and support for Jam STAPL, which is a vendor-independent JEDEC-approved language. MAX 7000B devices also provide paths to migrate to higher densities in the same package. Table 2 shows vertical migration available for the MAX 7000B family. Users can migrate their designs between check-marked devices in the same column.

MAX 7000B device features include global clocking, fast input registers, and programmable slew-rate control. A programmable power-saving feature allows 50% or greater power reduction in each macrocell. High-speed global clocks, 3.5-ns propagation delays, and fast setup times create superior system performance with high-speed device-to-device communication. Advanced support for MAX 7000B devices is available in the MAX+PLUS® II version 9.3 software. Table 3 lists MAX 7000B features.

State-of-the-Art Packaging Solutions

Altera MAX 7000B devices are available in innovative FineLine BGA™ and 0.8-mm BGA

Table 2. MAX 7000B PIn Migration

Device	Package										
	44-Pin PLCC	44-Pin TQFP	48-Pin TQFP	49-Pin 0.8-mm BGA	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	169-Pin 0.8-mm BGA	208-Pin PQFP	256-Pin FineLine BGA	256-Pin BGA
EPM7032B	✓	✓	✓								
EPM7064B	✓	✓	✓	✓	✓	✓					
EPM7128B	✓	✓	✓		✓	✓	✓	✓		✓	✓
EPM7256B						✓	✓		✓	✓	✓
EPM7512B						✓	✓		✓	✓	✓

packages. These 1.0-mm and 0.8-mm ball pitch packages are ideal for space-constrained designs. FineLine BGA and 0.8-mm BGA packages are available with the SameFrame™ pin-out feature, which provides footprint compatibility between packages with different ball counts. This layout feature permits easy migration from one FineLine BGA package to another FineLine BGA package, or one 0.8-mm BGA package to another 0.8-mm BGA package, without the need to redesign the board.

Support for High-Performance Applications

With fast timing and support for multiple I/O interfacing standards, MAX 7000B devices provide high-performance, product-term-based solutions in the smallest possible board space. Features such as ISP, low-power modes, and state-of-the-art packaging make these MAX devices ideal for a variety of applications.

These 1.0-mm and 0.8-mm ball pitch packages are ideal for space-constrained designs.

Table 3. MAX 7000B Device Features

Feature	EPM7032B	EPM7064B	EPM7128B	EPM7256B	EPM7512B
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	3.5	3.5	4.5	5.0	6.0
f_{CNT} (MHz)	200	200	192	178.6	147.1
Packages *(1)*	44-pin PLCC 44-pin TQFP 48-pin TQFP	44-pin PLCC 44-pin TQFP 48-pin TQFP 49-pin 0.8-mm BGA 100-pin TQFP 100-pin FineLine BGA	44-pin PLCC 44-pin TQFP 48-pin TQFP 49-pin 0.8-mm BGA 100-pin TQFP 100-pin FineLine BGA 144-pin TQFP 169-pin 0.8-mm BGA 256-pin FineLine BGA 256-pin BGA	100-pin TQFP 144-pin TQFP 208-pin PQFP 256-pin FineLine BGA 256-pin BGA	100-pin TQFP 144-pin TQFP 208-pin PQFP 256-pin FineLine BGA 256-pin BGA

Note:
(1) PLCC: plastic J-lead chip carrier; PQFP: plastic quad flat pack; TQFP: thin quad flat pack.

Current Software Versions

The Quartus™ version 1999.06 software is currently available for the Microsoft Windows 98, Windows NT 4.0, and Sun Solaris 2.6 operating systems. The Quartus version 1999.06 software will be available for the HP-UX operating system in the fourth quarter of 1999.

The MAX+PLUS® II version 9.3 software is currently available for the following operating systems:

- Microsoft Windows 95 and Windows 98
- Microsoft Windows NT version 3.51 and higher
- Sun Solaris version 2.5 and higher
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported
- AIX version 4.1 and higher

APEX

EP20K100 & EP20K200 Devices Now Available

Two new APEX™ devices, the 100,000-gate (263,000 maximum system gates) EP20K100 device and the 200,000-gate (526,000 maximum system gates) EP20K200 device, are now available. EP20K100 devices are available in 144-pin thin quad flat pack (TQFP), 208-pin plastic quad flat pack (PQFP), and 240-pin PQFP packages. EP20K200 devices, with 8,320 logic elements (LEs) and 106,496 bits of on-chip RAM, are available in 208-pin and 240-pin power quad flat pack (RQFP) packages. EP20K100 and EP20K200 devices are also offered in 1.27-mm ball-grid array (BGA) packages and 1.0-mm FineLine BGA™ packages that support SameFrame™ migration. For the latest information on APEX devices, see the Altera® web site at http://www.altera.com.

Tables 1 and 2 list the APEX 20K and APEX 20KE software support schedules. All 2.5-V APEX 20K devices are now available. The first 1.8-V APEX 20K device, the EP20K400E device, will be available in September 1999, followed by the EP20K600E in November 1999.

Table 1. APEX 20K Devices & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K100	144-pin TQFP	Now
	196-pin FineLine BGA	October 1999
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	October 1999
EP20K200	208-pin RQFP	Now
	240-pin RQFP	Now
	356-pin BGA	October 1999
	484-pin FineLine BGA	Now
EP20K400	652-pin BGA	Now
	655-pin PGA	Now
	672-pin FineLine BGA	Now

New APEX Family Members

Two new devices, the 1.5-million-gate EP20K1500E device and the 60,000-gate EP20K60E device, have been added to the

Table 2. APEX 20KE Devices & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K60E	144-pin TQFP	October 1999
	196-pin FineLine BGA	October 1999
	208-pin PQFP	October 1999
	240-pin PQFP	October 1999
	324-pin FineLine BGA	October 1999
	356-pin BGA	October 1999
EP20K100E	144-pin TQFP	Now
	196-pin FineLine BGA	October 1999
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	October 1999
EP20K160E	144-pin TQFP	October 1999
	208-pin PQFP	October 1999
	240-pin PQFP	October 1999
	356-pin BGA	October 1999
	484-pin FineLine BGA	October 1999
EP20K200E	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	October 1999
	484-pin FineLine BGA	Now
	652-pin BGA	October 1999
	672-pin FineLine BGA	October 1999
EP20K300E	208-pin RQFP	October 1999
	240-pin RQFP	October 1999
	652-pin BGA	October 1999
	672-pin FineLine BGA	October 1999
EP20K400E	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	October 1999
EP20K1000E	652-pin BGA	October 1999
	672-pin FineLine BGA	October 1999
	984-pin PGA	October 1999
	1,020-pin FineLine BGA	October 1999
EP20K1500E	652-pin BGA	February 2000
	984-pin PGA	February 2000
	1,020-pin FineLine BGA	February 2000

APEX device offerings. The EP20K1500E device offers 2,524,416 maximum system gates, and contains 54,720 LEs and 466,944 bits of on-chip RAM. EP20K1500E devices will be introduced in the second quarter of 2000. EP20K60E devices, which contain 2,560 LEs and 32,768 bits of on-chip RAM, will be introduced at the same time.

PLLs in APEX Devices

APEX devices have a phase-locked loop (PLL) capability, designated with an "X" suffix in the ordering code (e.g., EP20K400BC652-1X). All -1X and -2X speed grade APEX devices will contain the ClockLock™ and ClockBoost™ options, which reduce clock delay and skew and perform internal clock multiplications of 1×, 2×, and 4×, allowing for simpler board designs. APEX 20KE devices have up to four PLLs per device and also support the ClockShift™ feature, enabling programmable delays and phase shifting. The APEX 20K PLL option is currently supported by the Quartus software.

FLEX

Newest 0.22-µm FLEX 10KE Devices

The newest FLEX® 10KE devices are now on a 0.22-µm, 5-layer-metal process and are loaded with features. These devices, which include EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices, contain all FLEX 10KE features, such as a programmable delay, to provide full 64-bit, 66-MHz PCI compliance, and a PLL in -1 and -2 speed grades.

The MAX+PLUS® II version 9.3 software currently supports all FLEX 10KE devices, including the PLL feature, and will be sent to customers with a current software subscription. You can obtain software updates from the Altera web site at http://www.altera.com.

FLEX 10K Device Availability

MAX+PLUS II design support is available now for all 2.5-V FLEX 10KE device/package combinations, as shown in Table 3. This includes FLEX 10KE devices in -1 and -2 speed grades offered with the ClockLock feature, and designated with an "X" suffix (e.g., EPF10K100EQC240-1X).

Table 3. FLEX 10KE Devices & MAX+PLUS II Software Support Availability

Device	Package	Speed Grade	Software Support Availability
EPF10K30E	144-pin TQFP	-1, -2, -3	Now
	208-pin PQFP	-1, -2, -3	Now
	256-pin FineLine BGA	-1, -2, -3	Now
	484-pin FineLine BGA	-1, -2, -3	Now
	PLL (all packages)	-1X, -2X	Now
EPF10K50S	144-pin TQFP	-1, -2, -3	Now
	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FineLine BGA	-1, -2, -3	Now
	356-pin BGA	-1, -2, -3	Now
	484-pin FineLine BGA	-1, -2, -3	Now
	PLL (all packages)	-1X, -2X	Now
EPF10K100E	208-pin PQFP	-1, -2, -3	Now
	240-pin PQFP	-1, -2, -3	Now
	256-pin FineLine BGA	-1, -2, -3	Now
	356-pin BGA	-1, -2, -3	Now
	484-pin FineLine BGA	-1, -2, -3	Now
	PLL (all packages)	-1X,-2X	Now
EPF10K130E	240-pin PQFP	-1, -2, -3	Now
	356-pin BGA	-1, -2, -3	Now
	484-pin FineLine BGA	-1, -2, -3	Now
	600-pin BGA	-1, -2, -3	Now
	672-pin FineLine BGA	-1, -2, -3	Now
	PLL (all packages)	-1X, -2X	Now
EPF10K200S	240-pin RQFP	-1, -2, -3	Now
	356-pin BGA	-1, -2, -3	Now
	484-pin FineLine BGA	-1, -2, -3	Now
	600-pin BGA	-1, -2, -3	Now
	672-pin FineLine BGA	-1, -2, -3	Now
	PLL (all packages)	-1X, -2X	Now

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FLEX 10K Product Transitions

Selected 3.3-V FLEX 10KA devices are migrating from a 0.35-µm process to a 0.30-µm process

Selected 3.3-V FLEX 10KA devices are migrating from a 0.35-µm process to a 0.30-µm process, and all 5.0-V FLEX 10K devices are moving from a 0.50-µm process to a 0.42-µm process. EPF10K50E and EPF10K200E devices are migrating from a 0.25-µm process to a 0.22-µm process. Table 4 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at http://www.altera.com.

Table 4. FLEX 10K Device Migration

Device	Core Voltage (V)	Date	Reference	Process (µm)
EPF10K10A	3.3	Done	PCN 9810	0.30
EPF10K30A	3.3	Done	PCN 9810	0.30
EPF10K50V	3.3	Done	PCN 9810	0.30
EPF10K100A	3.3	Done	PCN 9810	0.30
EPF10K10	5.0	October 1999	PCN 9901 ADV 9909	0.42
EPF10K20	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K30	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K40	5.0	October 1999	PCN 9901 ADV 9909	0.42
EPF10K50	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K70	5.0	October 1999	PCN 9901 ADV 9909	0.42
EPF10K100	5.0	October 1999	PCN 9901 ADV 9909	0.42
EPF10K50E	2.5	Q4 1999	PCN 9911	0.22
EPF10K200E	2.5	Q4 1999	PCN 9911	0.22

FLEX 10KE Industrial-Temperature Devices

Table 5 lists the expected availability of industrial-temperature FLEX 10KE devices.

Table 5. FLEX 10KE Industrial-Temperature Devices & MAX+PLUS II Software Support Availability

Device	Software Support Availability
EPF10K50ETI144-2	Now
EPF10K50EQI240-2	Now
EPF10K50EFI256-2	Now
EPF10K50SQI208-2	Now
EPF10K50SBI356-2	Now
EPF10K50SFI484-2	Now
EPF10K100EQI208-2	Now
EPF10K100EFI256-2	Now
EPF10K100EFI484-2	Now
EPF10K130EQI240-2	Now
EPF10K130EBI356-2	Now
EPF10K130EFI484-2	Now
EPF10K200EBI600-2	Now
EPF10K200SRI240-2	Now
EPF10K200SBI356-2	Now
EPF10K200SFI672-2	Now

FLEX 6000 FineLine BGA Package Support

Support for FLEX 6000 devices in area-efficient FineLine BGA packages is available now in the MAX+PLUS II version 9.3 software. Selected FLEX 6000 FineLine BGA devices are currently available. Table 6 shows FLEX 6000 device expected availability.

Table 6. FLEX 6000 Device Availability & MAX+PLUS II Software Support

Package	Device			
	EPF6010A	EPF6016	EPF6016A	EPF6024A
100-pin TQFP	Now		Now	
100-pin FineLine BGA			Now	
144-pin TQFP	Now	Now	Now	Now
208-pin PQFP		Now	Now	Now
240-pin PQFP		Now		Now
256-pin BGA		Now		Now
256-pin FineLine BGA			Now	Now

MAX

MAX 7000B Devices

2.5-V MAX® 7000B devices range from 32 to 512 macrocells with propagation delays (t_{PD}) as fast as 3.5 ns. MAX 7000B devices support advanced I/O standards such as Gunning transceiver logic plus (GTL+), stub series terminated logic for 2.5 V (SSTL-2), and SSTL-3. These devices also feature enhanced in-system programmability (ISP), MultiVolt™ I/O pins, hot socketing, and pin compatibility with the industry-standard MAX 7000 devices.

MAX 7000A Devices

All MAX 7000A devices are now available. 3.3-V MAX 7000A devices have propagation delays as fast as 4.5 ns and range from 32 to 512 macrocells. These devices support enhanced ISP, MultiVolt I/O pins, and hot socketing, and are pin compatible with the industry-standard MAX 7000 devices. All MAX 7000A devices are available in both industrial- and commercial-temperature grades. Table 7 shows MAX 7000AE device commercial package and speed grade options.

MAX 7000S Devices

5.0-V MAX 7000S devices are all available and feature 5-ns speed grades, ISP, an open-drain output option, and IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in both industrial- and commercial-temperature grades. Table 8 shows the packages and speed grades available in the commercial-temperature grade.

MAX 3000A Devices

The 3.3-V MAX 3000A devices are targeted for high-volume, low-cost designs. These devices have an enhanced ISP feature set and range in density from 32 to 256 macrocells (see Table 9 on page 10). With propagation delays as fast as 4.5 ns, MAX 3000A devices provide exceptional performance at the lowest price per macrocell among Altera MAX products.

Table 7. MAX 7000AE Device Packages

Device	Package	Speed Grade
EPM7032AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM7064AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	49-pin 0.8-mm BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
EPM7128AE	84-pin PLCC	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin 0.8-mm BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7256AE	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512AE	144-pin TQFP	-7, -10, -12
	208-pin PQFP	-7, -10, -12
	256-pin BGA	-7, -10, -12
	256-pin FineLine BGA	-7, -10, -12

Table 8. Commercial-Temperature MAX 7000S Device Packages

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

MAX 7000A devices have propagation delays as fast as 4.5 ns and range from 32 to 512 macrocells.

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Table 9. MAX 3000A Devices

Device	Package	Speed Grade
EPM3032A	44-pin PLCC 44-pin TQFP	-4, -7, -10 -4, -7, -10
EPM3064A	44-pin PLCC 44-pin TQFP 100-pin TQFP	-4, -7, -10 -4, -7, -10 -4, -7, -10
EPM3128A	100-pin TQFP 144-pin PQFP	-5, -7, -10 -5, -7, -10
EPM3256A	144-pin TQFP 208-pin PQFP	-6, -7, -10 -6, -7, -10

CONFIGURATION

Expanded Support for EPC2 Configuration Device

The FLASH-based reprogrammable EPC2 configuration device is now offered in industrial-temperature grades in both 32-pin TQFP and 20-pin PLCC packages.

TOOLS

Obtain a License File that Enables Quartus Version 1999.06 Software

The Quartus version 1999.06 software requires a license file with a Quartus FEATURE line. You can request license files using Altera's web-based license generator at http://www.altera.com. You can also access Altera's web-based license generator directly from within the Quartus software.

You must provide your Altera ID in addition to either your software guard number, host ID, or NIC number to access the license file generator. Your Altera ID is printed on the mailing label of all communication you receive from Altera, including the quarterly *News & Views*. The ID is also available from the Quartus support web site at https://websupport.altera.com. You must have a current software subscription to receive the license file with the Quartus FEATURE line.

Quartus Software is Now Shipping

The Quartus version 1999.06 software is now shipping to all customers who have a current software subscription. With revolutionary features like SignalTap™ logic analysis and NativeLink™ integration with third-party EDA tools, the Quartus software truly enables System-on-a-Programmable-Chip™ designs.

The Quartus version 1999.06 software supports the APEX 20K devices listed in Table 10.

Table 10. Quartus Version 1999.06 Support for APEX Devices

Support	Device	Package
Compilation and Programming Support	EP20K100	144-pin TQFP 208-pin PQFP 240-pin PQFP
	EP20K200	208-pin RQFP 240-pin RQFP
	EP20K400	652-pin BGA 655-pin PGA 672-pin FineLine BGA
Compilation Support Only	EP20K100	324-pin FineLine BGA
	EP20K100E *(1)*	144-pin TQFP 208-pin PQFP 240-pin PQFP 324-pin FineLine BGA
	EP20K200	484-pin FineLine BGA
	EP20K200E	208-pin RQFP 240-pin RQFP 484-pin FineLine BGA
	EP20K400	652-pin BGA *(2)* 672-pin FineLine BGA *(2)*
	EP20K400E *(1)*	652-pin BGA 672-pin FineLine BGA
	EP20K600E *(1)*	652-pin BGA 672-pin FineLine BGA

Notes:
(1) The Quartus version 1999.06 software will only support the speed and density features of these devices.
(2) Devices with the ClockLock feature are available in these packages.

Quartus Operating System Support

The initial Quartus software release version 1999.06 supports the operating systems listed in Table 11.

Table 11. Quartus Operating System Support

Platform	Operating System
PC	Windows NT/Windows 98
UNIX	Solaris *(1)*
	HP-UX *(2)*

Notes:
(1) Version 2.6.
(2) Support for the HP-UX operating system will be available in Q4 1999.

Quartus System Requirements

Table 12 lists the minimum system configuration requirements necessary to run the Quartus software on either a PC or UNIX operating system. In addition to the hardware listed in Table 12, the amount of RAM and hard drive swap space necessary varies with the density of the target APEX device. Table 13 lists the required RAM and additional hard drive swap space for different design densities.

Table 12. Minimum Quartus System Requirements (PC & UNIX Workstation)

Platform	System	Minimum Hard Drive Space (Mbytes)
PC	400-MHz Pentium	750
UNIX	300-MHz Ultra Sparc II	2,000

Table 13. Device-Specific Quartus System Requirements (PC & UNIX Workstation)

Target APEX Device	Minimum Main Memory (RAM) (Mbytes)	Minimum Additional Hard Drive Swap Space (Mbytes)
EP20K100 EP20K100E EP20K200 EP20K200E	256	256
EP20K400 EP20K400E EP20K600E	512	512
EP20K1000E	1,024	1,024

Help Using the Quartus Software

The Quartus software ships with manuals to allow you to get started on your multi-million-gate designs immediately. Additional documentation such as application notes and technical briefs are available for customers to learn more about the Quartus software. Table 14 lists some of the documentation available from the Altera web site or Altera Literature Services. Altera has introduced many new features with the Quartus software including SignalTap logic analysis, NativeLink support, and integration capabilities with revision control software. You can request additional documentation describing these and many other features of the Quartus software.

Table 14. Quartus Documentation

Document Title	Description
SignalTap Embedded Logic Analyzer Megafunction Data Sheet (A-DS-SIGNALTAP-01)	Description of the SignalTap megafunction, which is provided with the Quartus software.
AN 118: Scripting with Tcl in the Quartus Software (A-AN-118-01)	Explains how to develop and run scripts in Tcl to perform a wide range of functions in the Quartus software.
TB 51: Advantages of Quartus Internet Integration (M-TB-051-01)	Brief overview of Quartus Internet integration capabilities.
TB 52: Increasing Performance using ATOM Netlist Files (M-TB-052-01)	Description of improved results for designs synthesized from third-party tools into ATOM netlists.
TB 54: Quartus Revision Control Software Support (M-TB-054-01)	Overview of the Quartus software's abilities to integrate with standard revision control software packages.

Additional documentation such as application notes and technical briefs are available for customers to learn more about the Quartus software.

MAX+PLUS II Version 9.3 Software Reduces Compilation Times

MAX+PLUS II version 9.3 software compilation algorithms are optimized to speed up timing-driven compilation times. 70 designs were benchmarked for compilation times using the MAX+PLUS II software versions 9.2 and 9.3. These designs were compiled for the FLEX 10K device family, ranging in density from EPF10K20 to EPF10K250A devices. On average, compilation times for version 9.3 were one-third the times obtained with version 9.2. The registered performance did not vary significantly.

continued on page 12

Devices & Tools, continued from page 11

Timing-driven compilations with clock-to-output delay (t_{CO}) and clock setup time (t_{SU}) assignments allow the MAX+PLUS II version 9.3 software to place appropriate registers in the I/O cells of the device. This capability significantly improves I/O performance for a design.

MAX+PLUS II version 9.3 software also offers a Jam Composer and Player that supports Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71 format and full compilation support for over 30 new device/package combinations, including 2.5-V MAX 7000B and 0.22-µm FLEX 10KE devices.

MAX+PLUS II BASELINE Version 9.3 Software Expands Device Support

MAX+PLUS II BASELINE version 9.3 software adds compilation support for EPF10K30, EPF10K30A, EPF10K30E, EPF6024A, MAX 7000B, and MAX 3000A devices. You can download the MAX+PLUS II BASELINE software for free from the Altera web site (http://www.altera.com), or install it from the Altera digital library (ADL) or MAX+PLUS II installation CD-ROM. A six-month license to enable the software is available from the Altera web site.

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on the Altera web site at http://www.altera.com. Document part numbers are shown in parentheses.

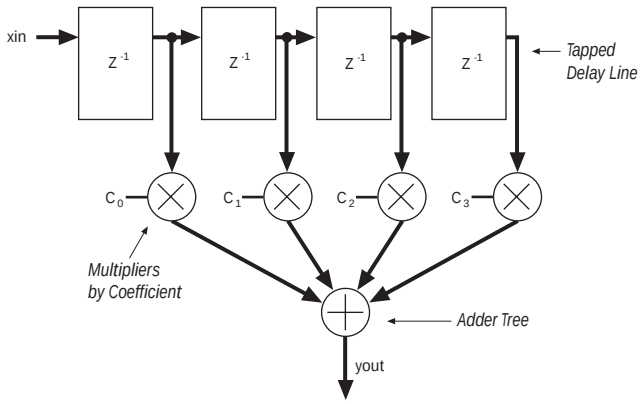
- *Altera Digital Library CD-ROM, version 6* (P-CD-ADL-06)
- *APEX 20K Programmable Logic Device Family Data Sheet* (A-DS-APEX20K-02.01)
- *FIR Compiler MegaCore Function User Guide* (A-UG-FIRCOMPILER-01)
- *Quartus Installation & Licensing for PCs* (P25-04731-01)
- *SignalTap User's Guide* (P25-04733-00)
- *AN 100: In-System Programmability Guidelines* (A-AN-100-03)
- *AN 107: Using Altera Devices in Multiple Voltage Systems* (A-AN-107-01)
- *AN 118: Scripting with Tcl in the Quartus Software* (A-AN-118-01)
- *AN 119: Implementing High-Speed Search Applications with APEX CAM* (A-AN-119-01)
- *SB 39: I²C Master Interface Megafunction* (A-SB-039-01)
- *SB 40: I²C Slave Interface Megafunction* (A-SB-040-01)
- *SB 41: FIR Compiler MegaCore Function* (A-SB-041-01)
- *SB 42: Interleaver/Deinterleaver MegaCore Function* (A-SB-042-01)
- *SB 44: 64-Bit PCI Master/Target MegaCore Function* (A-SB-045-01)
- *TB 51: Advantages of Quartus Internet Integration* (M-TB-051-01)
- *TB 53: Comparison of Quartus Software with Xilinx Alliance Series Version 2.1i Software* (M-TB-053-01)

FIR Compiler Speeds Design Cycles

Many communications systems use digital processing to remove unwanted noise, to provide spectral shaping for communications channels, or to perform signal detection and analysis. Finite impulse response (FIR) filters have an inherently stable structure and are used in many systems which require linear phase. Typical filter applications include signal preconditioning, band selection, and low-pass filtering.

The FIR compiler is the first complete digital signal processing (DSP) development tool in the programmable logic device (PLD) industry to boost the design cycle of high-performance FIR filters. The FIR compiler generates highly optimized FIR filter megafunctions and cycle accurate simulation models for system-level analysis tools (e.g., MATLAB, Simulink) and hardware description languages (HDL) for simulation (VHDL, Verilog HDL).

Figure 1. Basic FIR Filter



FIR Filter Overview

The filter design process involves identifying coefficients that match the frequency response specified for the system. The coefficients determine the structure of the filter. You can change which signal frequencies pass through the filter by changing the coefficient values or adding more coefficients. Figure 1 shows a diagram of a basic FIR filter.

A FIR filter design cycle has two main phases: system-level specification and hardware implementation. The number of taps (*N*) and the value of each coefficient are based on the system requirements such as the sample frequency, filter type, cut-off frequencies, stop-band reject, and pass-band ripple. After defining the bus precision, the designer selects a device to which the function should be mapped. The FIR compiler allows the user to enter floating-point coefficients and perform the floating-to-fixed-point conversion all within the tool. The user can select an architecture that is optimal for a particular design. The FIR compiler provides a complete integration of these two phases. The user can optimize their design for either speed or area by adjusting a few parameters in the DSP designer.

High-Performance FIR Filter

When implementing the FIR filter in a traditional DSP processor, the amount of filter data throughput is shown in the following equation:

$$\text{throughput} = \frac{\text{processor clock}}{N}$$

Therefore, high-performance filters that require a large number of taps are quickly limited by the data rates they can handle. However, with PLDs, the increase in filter length does not affect the throughput.

A fully parallel, pipelined FIR filter implemented in a PLD can operate at data rates above 100 megasamples per second (MSPS), making PLDs ideal for high-speed filtering applications. The FIR compiler offers multiple architectures, such as parallel or serial implementations; the designer can decide to

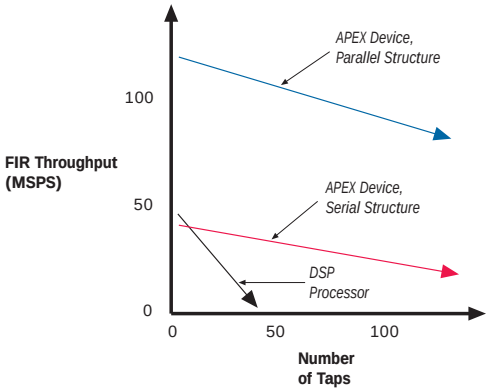
continued on page 14

FIR Compiler Speeds Design Cycles, continued from page 13

trade resource usage for performance. The user can choose to have the design run faster or be more resource efficient, depending on the priority. Figure 2 illustrates the difference in performance between the different hardware architectures.

The FIR compiler takes advantage of the APEX MultiCore architecture to reduce resource usage while maintaining high throughput.

Figure 2. FIR Throughput vs. Number of Taps

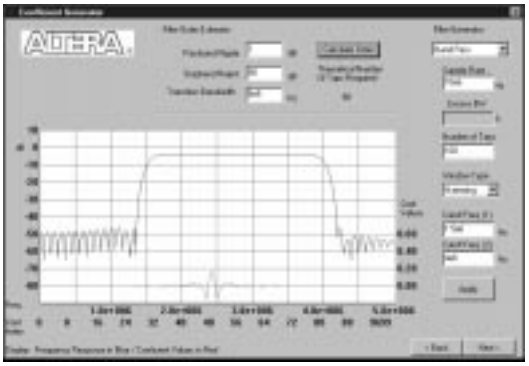


The FIR compiler creates FIR filters that run between 70 to 140 MHz. Depending on the options chosen, these implementations use a few hundred to several thousand logic cells. The FIR compiler takes advantage of the APEX™ MultiCore™ architecture to reduce resource usage while maintaining high throughput. For example, the FIR tap delay line is mapped to ESBs, and the multiplication and addition operations of the filter (e.g., the partial product and the adder tree) are mapped to look-up tables (LUTs).

Design Entry

The FIR compiler can import coefficient values from third-party DSP tools such as MATLAB, SPW, or COSSAP in floating point or fixed point format. You can use the FIR compiler MegaWizard plug-in (see Figure 3) to compute the floating-point value of the coefficients. The coefficient generator supports high pass, low pass, band pass, band reject, raised cosine, and root raised cosine filter types, as well as rectangular, Hamming, Hanning, and Blackman

Figure 3. Coefficient Generator Window



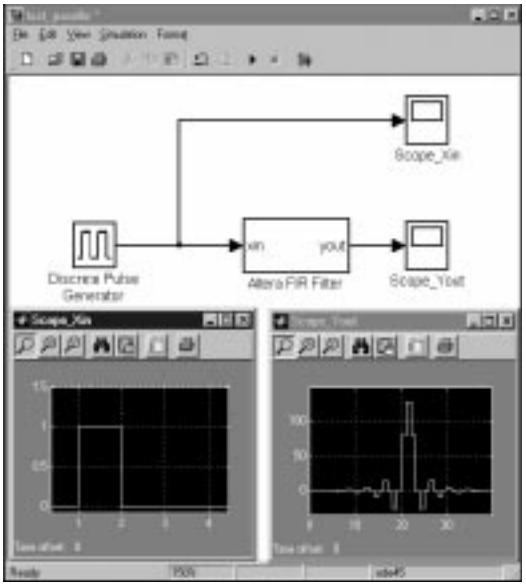
window types. The coefficient generator displays the frequency response of the filter based on the parameters.

The FIR compiler generates a system-level model for MATLAB Simulink (see Figure 4) as well as a HDL model for VHDL and Verilog HDL simulators.

Conclusion

The FIR compiler is highly optimized for Altera device architectures, and supports parallel or serial arithmetic architectures. The MegaWizard Plug-In allows the designer to easily design the filter and create MATLAB Simulink, VHDL, and Verilog HDL simulation models.

Figure 4. MATLAB Simulink Window

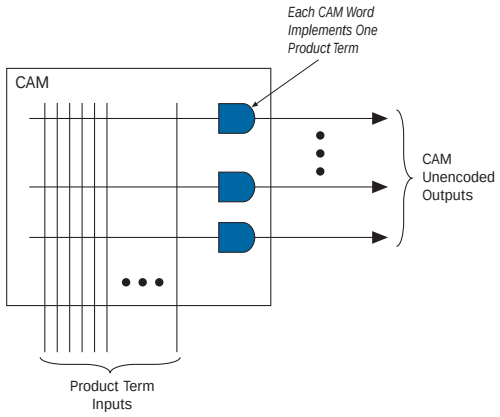


Implementing Programmable Product Terms with CAM

Content addressable memory (CAM) is memory accessed by its content rather than its address. CAM provides a performance advantage over other memory search algorithms, such as binary or tree-based searches or look-aside tag buffers, by comparing the desired information against the entire list of pre-stored entries simultaneously, often resulting in a large reduction in the search time. One application that takes advantage of CAM's fast searches is a programmable product term.

Each APEX™ 20KE embedded system block (ESB) can implement a 32-word × 32-bit CAM block. Within the ESB, each word in CAM corresponds to a product term (see Figure 1). Since CAM can be re-written during configuration or system operation, the product terms linked to each CAM line can be re-programmed to perform different functions. The CAM output should be in an unencoded format so there is only one output per CAM word line. The unencoded outputs can use look-up tables (LUTs) to make combinatorial logic.

Figure 1. Each CAM Word Line Corresponds to a Product Term



Multi-Format Video Decoding Application with CAM

Programmable product terms in CAM can be used for multi-feature video decoding. In most broadcast video applications, a number of decodes from a set of master line and pixel counters are required to control the operation of the device or system. Traditionally, this function has been performed using a number of comparators and multiplexors. However, problems arise in systems that require a large number of decodes. In this instance, the number of required comparators becomes very large and can cause a performance bottleneck, especially at high-definition television (HDTV) clock rates.

The problem is further compounded if the device supports multiple formats; the number of decodes required is multiplied by the number of formats supported. For example, if a device requires 32 decodes from a mixture of line and pixel counters per format, it would require 96 decodes or comparators to support three formats. An alternative is to use dynamic comparators; the decode values are downloaded by the system's CPU when it switches from one format to another. The drawback is that dynamic comparators can consume many logic elements (LEs).

A better solution is to use APEX 20KE CAM to perform these decodes at very high speeds. Each CAM word line is a decode of the inputs (line and pixel counters). An unencoded output acts as a system or device decode, which controls the rest of the system or device. With unencoded outputs, each ESB reads 16 outputs in two cycles: 16 bits at each cycle to represent 32 words in the CAM block. (Although an ESB supports 32 input bits, only 31 input bits are used for data in unencoded output form; one input bit is used by the select line to choose one

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Implementing Programmable Product Terms with CAM, continued from page 15

of the two 16-bit banks to output.) Figure 2 on page 18 shows how CAM can help to decode the incoming data and distinguish which format has been requested.

APEX CAM Advantages

APEX CAM provides other advantages. The design performance is improved, only limited by the CAM access time (4 ns). The printed circuit board (PCB) space used with APEX CAM is small and fixed compared to the dynamic decoder design. Additionally, CAM can be configured at system power-up with the default format's decode.

The use of programmable product terms can be extended to any design requiring a relatively large number of decodes, especially those requiring dynamically alterable decodes. Because CAM searches through its contents simultaneously, it can implement programmable product terms efficiently to improve a design. See *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)* for more information on APEX CAM.

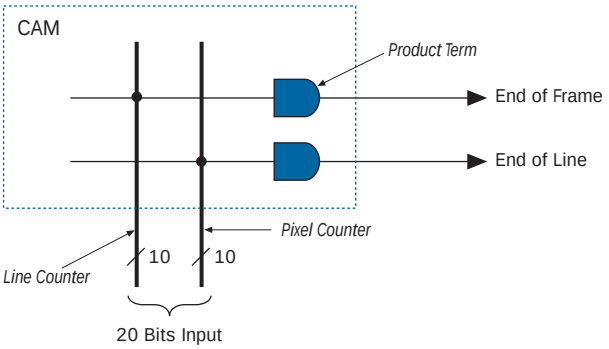
Programmable product terms in CAM can be used for multi-feature video decoding.

Figure 2. Multi-Format Video Decode with APEX CAM

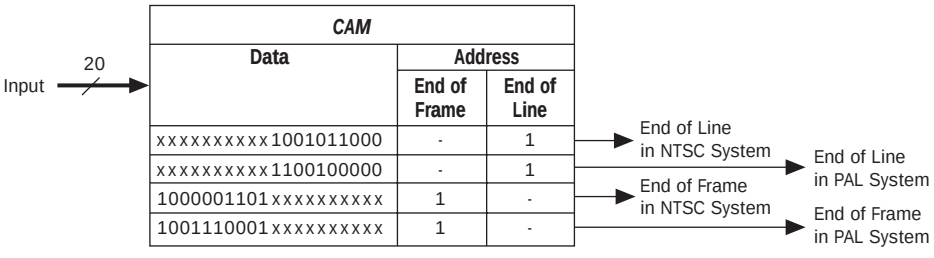
HDTV Pixel & Line Count

HDTV Pixel & Line Count				
System	Pixels		Lines	
	Decimal	Binary	Decimal	Binary
PAL	800	1100100000	625	1001110001
NTSC	600	1001011000	525	1000001101

CAM Block Diagram



CAM Outputs



Faster Programming Times with the HP 3070 Tester

Introduction

In-system programming has become a mainstream feature in programmable logic devices (PLDs), offering system designers and test engineers significant cost benefits by integrating PLDs into board-level testing. These benefits include reduced inventory of pre-programmed devices, lower costs, fewer devices damaged by handling, and increased flexibility in engineering changes. Altera® provides software and device support that integrates in-system programmability (ISP) into existing test flows for the HP 3070 system (ISP is occasionally referred to as "on-board programming"). This article discusses how to use the HP 3070 test system to achieve faster programming times for Altera devices that support ISP.

Device Support

In-system programming is achieved with either an adaptive or a constant (i.e., fixed) algorithm. Altera devices tested with a constant algorithm should be used when programming with HP 3070 systems. These devices are designated by an "F" suffix in the ordering code and are marked with an "F" in the bottom right-hand corner of the device. Table 1 shows which devices are supported when programming with the HP 3070 test system.

"F" devices allow programming hardware to program all devices from a set of pre-defined vectors. This process allows in-circuit testers, such as the HP 3070, to apply programming vectors in the simplest and fastest manner possible. In addition, fixed algorithm devices provide a uniform "beat-rate" (number of devices programmed per minute). Because these devices use the same algorithm and vector set, each device has the same programming time. This scenario is desirable in a production environment where a consistent, predictable beat-rate is necessary for smooth operation of the manufacturing line.

Table 1. "F" Device Support for the HP 3070 Test System

Family	Supported Devices
MAX 7000S	"F"
MAX 7000A	MAX 7000AE
MAX 7000AE	All Ordering Codes
MAX 9000, MAX 9000A	"F"

HP 3070 Development Flow

Programming devices with the HP 3070 tester requires several simple steps, which are not specific to an on-board programming flow. Rather, the flow is identical to the development of any other kind of test that requires a specific vector set. See Figure 1 on page 14.

The MAX+PLUS® II software tool makes generating Serial Vector Format Files (.svf) for every Joint Test Action Group (JTAG) device chain simple and straightforward. Once generated, the SVF File is converted to HP Pattern Capture Format File (.pcf) via the Altera svf2pcf utility. This utility can be downloaded from the Altera ftp site (ftp.altera.com) and supports both Windows and HP-UX operating systems.

Once the programming vectors are placed in the PCF format, the remaining flow is identical to any other test. For more detailed information on printed circuit board (PCB) layout, software flow, or debugging, see *Application Note 109 (Using the HP 3070 Tester for In-System Programming)*.

Programming Times

Programming times on the HP 3070 are very consistent; the only variable is the TCK frequency, which affects programming times. The faster the clock, the less time is spent

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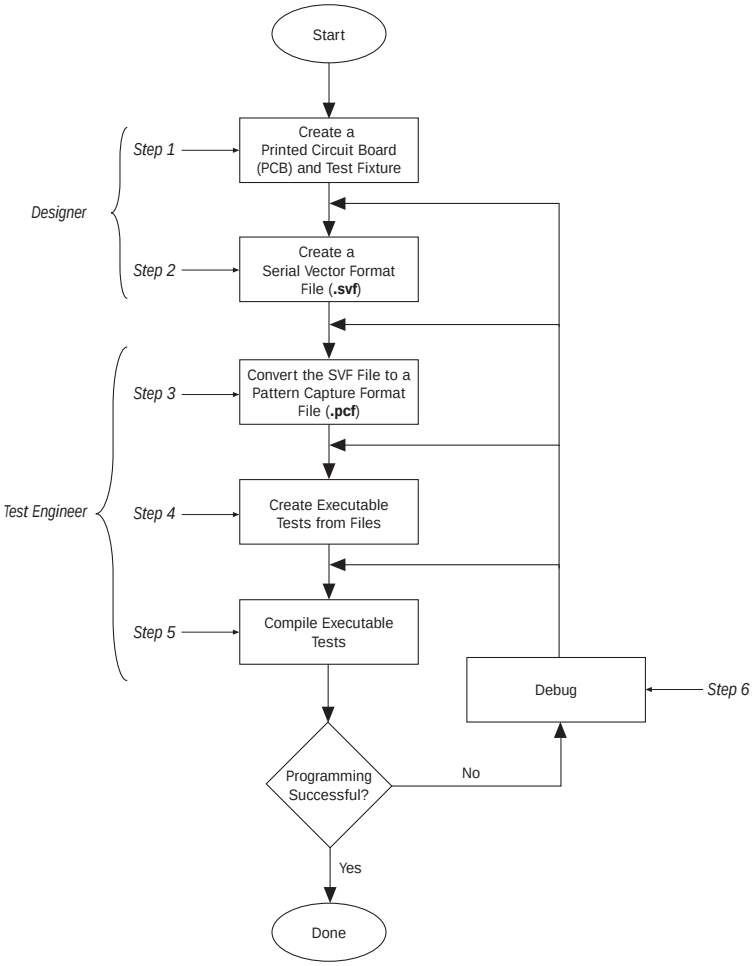
The MAX+PLUS II software tool makes generating Serial Vector Format Files (.svf) for every Joint Test Action Group (JTAG) device chain simple and straightforward.

Faster Programming Times with the HP 3070 Tester, continued from page 17

Figure 1. HP 3070 Development Flow for In-System Programming



shifting data into the device. *Application Note 85 (In-System Programming Times for MAX Devices)* provides detailed programming time data for in-circuit testers.

The following example provides detailed data points from a specific test case. The data shown provides a general idea of the typical programming times that can be expected, as well as information on file sizes and resources utilized on the host workstation. In this example, four EPM7128SQC160-7F devices are programmed in a chain, using the HP 3070. An SVF File is generated targeting all four EPM7128S devices, and the test flow is used to convert the PCF Files into executable vectors. The results are shown in Tables 2 and 3.

Table 2. Data for Programming Four EPM7128SQC160-7F Devices

Description	Results
HP 3070 software revision	B.02.54
Controller type	725/100
Number of PCF Files created	15
Number of vectors per file	About 700,000
Total number of vectors executed	9,925,512
Size of each PCF File	5.4 Mbytes
Total disc storage for PCF Files	78.7 Mbytes
Total size of each object file (15 object files)	1.5 Mbytes (about 100,000 bytes each)
Total size of each debug object (15 objects)	430,901 (about 28,800 bytes each)
Total compilation time	3 hours, 17 minutes

Table 3. Programming Times—Four EPM7128SQC160-7F Devices

Description	TCK = 500 kHz	TCK = 2 MHz
Vector cycle time	1,000 ns (1 µs)	250 ns
Test time to program all four devices (first run)	52 seconds	41 seconds
Test time to program all four devices (subsequent runs)	23 seconds	6 seconds

Application Note 85 (In-System Programming Times for MAX Devices) lists programming times as a function of the TCK frequency and the number of devices being programmed. The data provided in this article is based on theoretical calculations. However, as tests have shown, these numbers are accurate to within less than one second of actual programming times on the HP 3070 tester. The programming times stated are for MAX® 7000S devices. Programming times for MAX 7000AE devices are reduced even further (up to 50%).

As expected, the programming time is a function of the TCK clock rate. Over this frequency range, the relationship between the frequency and programming time is linear. At higher frequencies, the programming time begins to asymptotically approach the theoretical programming time reported in *Application Note 85 (In-System Programming Times for MAX Devices)*. Additionally, the example shows that the concurrent algorithm

reduces the programming time of the four devices to the programming time of only one EPM7128S device.

Conclusion

Altera provides complete solutions for programming all ISP-capable devices using the HP 3070 test system. Fast programming times are achieved within the existing test flow for the HP 3070 tester. Additionally, Altera offers "F" devices, which provide fast, consistent programming times in a production environment. With both software and device support, the opportunity for cutting costs and increasing manufacturing productivity is available to any HP 3070 user.

Developing Tcl Scripts for Quartus Software

Introduction

The Quartus™ software allows designers to develop and run scripts in the tool command language (Tcl) to perform a wide range of simple or complex functions (e.g., compiling a design or writing procedures to automate common tasks). This article describes how to develop Tcl scripts for the Quartus software.

What is Tcl?

Tcl is a popular scripting language that is similar to many shell scripting and high-level programming languages. It provides enough programmability with its syntax to support control structures, variables, network socket access, and application programming interfaces (APIs) for integration.

Compared to languages like C++, Tcl is easy to learn and use. Because Tcl is an interpretive language, development is easier and faster than with other languages. When the desired functionality is not available, Tcl allows you to create your own commands or procedures from existing commands. You can use Tcl for multi-platform programming because it works seamlessly across development platforms such as UNIX and Windows NT.

Using Tcl

The Quartus API details a set of interface functions that can be called from different languages (e.g., Tcl or C++). Users with some knowledge of Tcl can use the API to write scripts that automate tasks within the Quartus software. A single script can control the project design, start and stop compilation, make assignments, and run simulations.

The basic syntax for a Tcl command is:

<*command*> [<*argument1*> <*argument2*> <*argument3*>...]

The command syntax is either the name of the built-in command, a procedure, or a set of commands. Spaces separate a command and its arguments, and a new line or semicolon terminates commands. Arguments to commands are passed as strings.

When the desired functionality is not available, Tcl allows you to create your own commands or procedures from existing commands.

Running Tcl Scripts Interactively

You can enter Tcl commands directly in the Quartus Tcl/Tk Console window. To launch the Tcl/Tk Console window, choose Auxiliary Windows > Tcl/Tk Console (View menu). See Figure 1.

Figure 1. Tcl/Tk Console

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Developing Tcl Scripts for Quartus Software, continued from page 19

The Tcl/Tk Console window supports a command history. It does not allow commands to span more than one line. Tcl messages appear in the System tab in the Messages window.

Running Tcl Scripts in Batch Mode

Once you create a Tcl script file (.tcl), you can run it by typing the following command in the Tcl/Tk Console window:

`source <script file>` ↵

You can also run a script by choosing Run Script (Tools menu).

Running Tcl Scripts from DOS or UNIX

The Quartus software also supports "`-f <script file>`" command line arguments. This command is equivalent to choosing Run Script (Tools menu). Use the following syntax for running commands from the DOS or UNIX prompt:

`quartus_cmd –f <script file>` ↵

For a detailed list of Tcl commands, search for "Tcl Script API" in Quartus Help.

Sample Tcl File

Figure 2 shows a sample file that creates a project, makes assignments, and runs a simple compilation in Tcl.

Altera provides extensive documentation to help you design with the Quartus software. For technical support, contact Altera® Applications at (800) 800-EPLD. You can also e-mail your technical questions to Altera at sos@altera.com or connect directly to the Quartus Web Support web site from within the Quartus software. The Quartus software supports Tcl version 8.03, which is supplied by Scriptics Corporation (http://www.scriptics.com).

Figure 2. Running a Simple Compilation in Tcl

```
# Change to the working directory
cd E:/Tcl
# Create a project called myproject
project create myproject
# Open the project
project open myproject
# Add a source file to the Project
project add_assignment "" "" "" "" SOURCE_FILE my_design.v
# Create compilation settings
project create_cmp my_design_entity
# Make this setting the active compiler setting
project set_active_cmp my_design_entity
# Assign a device
cmp add_assignment my_design_entity "" "" DEVICE AUTO
# Start compilation
cmp start
while { [cmp is_running] } {
       after 10
       FlushEventQueue
       }
cmp stop
```

Verifying PLD Designs Using SmartModels

Effective verification of complex systems, printed circuit boards (PCBs), and programmable logic devices (PLDs) requires accurate simulation models of the devices in the target system. Designers can create and maintain these models themselves, but it would detract from the main task of actually designing. A better alternative are the Logic Modeling SmartModels from Synopsys.

All PLD models in the Synopsys SmartModel library include the SmartCircuit feature, which provides the designer with the advanced verification and debugging features that are required to verify a PLD design quickly and successfully. Models with the SmartCircuit feature are basically templates of unconfigured devices, and a design netlist is loaded into the model in the EDIF format.

SmartModel Overview

The SmartCircuit feature allows the designer to focus on the design and system verification tasks rather than on simulation details. To generate an EDIF output file (.edo) that targets SmartModels from Altera's Quartus™ or MAX+PLUS® II Compiler, choose EDIF Netlist Writer Settings (Interfaces menu). Select Synopsys from the *Vendor* drop-down list, and select *EDIF 3 0 0* as the EDIF version.

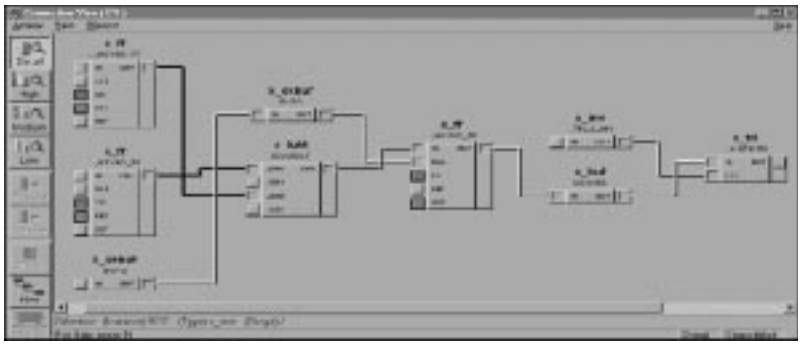
SmartModels are behavioral simulation models that offer complete representations of device behavior and timing. Each model includes unique automatic error-checks to put design analysis power right into the model, making it easier to use the component properly. SmartModels are compatible with most third-party VHDL, Verilog HDL, and board-level simulators.

Advanced Debugging

A key factor in successfully verifying a design is the ability to debug functional and timing errors. The schematic of the design is a good starting point for a debugging effort. Visual SmartBrowser (VSB), a tool within PLD SmartModel models, displays the PLD netlist using an on-demand viewing technique. Users can expand or collapse the view of their design depending on the level of detail they require. With today's large, complex designs, such as Altera® FLEX® 10KE designs, designers are usually interested in debugging only a small section of the netlist at one time. VSB allows the designer to concentrate on only the section in which they are interested. Figure 1 shows the connection view of the VSB.

SYNOPSYS®

Figure 1. VSB Connection View



Causal Tracing

SmartModel models feature the causal tracing tool, which allows the designer to trace the root cause of a logic event or timing error. Without causal tracing, the designer would be forced to manually analyze hundreds of possible paths to identify a logic or timing error. Figure 2 on page 24 shows the causal tracing function.

If the designer encounters functional or timing errors during a simulation run, it is imperative to trace the event back to its root cause. In a large design, this task is usually very complex to achieve. The causal tracing feature uses an automated history mechanism that does not significantly slow simulation performance. Additionally, the causal tracing feature works

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The SmartCircuit feature allows the designer to focus on the design and system verification tasks rather than on simulation details.

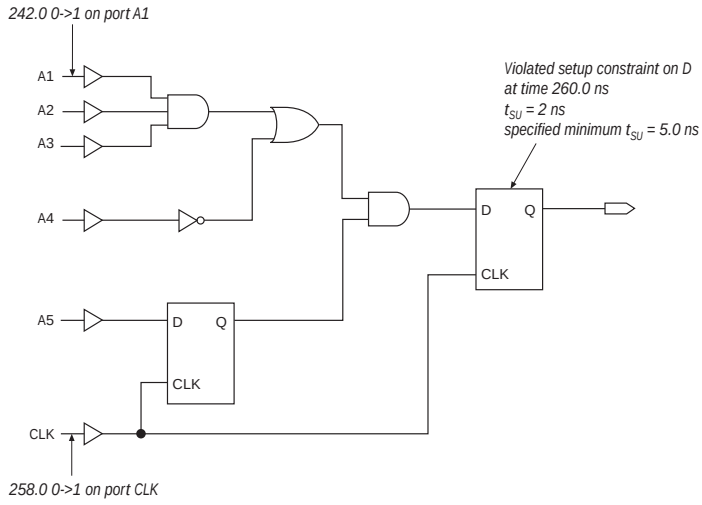
Verifying PLD Designs Using SmartModels, continued from page 21

from user-specified trigger points to perform the following tasks:

- Trace back to locate the root cause of any logic event error.
- Trace forward to find the effects of any specific logic event.
- Identify the root cause of any timing constraint violation.

The reports generate a list of events internal to the PLD that are causally related to the problem event so that you can quickly identify the root of the logic or timing error. Although the causal tracing tool generates text reports, these reports can be loaded into the VSB to examine the paths graphically.

Figure 2. Causal Tracing Diagram



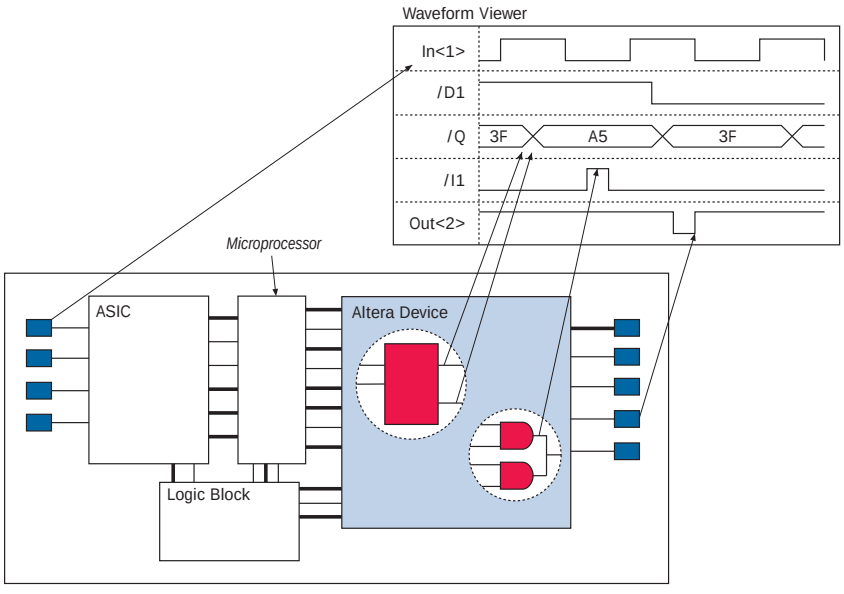
Windows

Visibility into the PLD design during simulation is another critical factor. The ability to trace the contents of an internal net or register aids the debugging of the overall design. SmartCircuit PLD models can look inside the PLD design using the Windows feature (shown in Figure 3)—the PLD is no longer a concealed black box within the simulation. The Windows feature allows the designer to trace any nets, ports, or states internal to the design in the simulation waveform window. The designer has full visibility into the PLD design at a level that simplifies the verification process and subsequent debugging. Figure 3 shows the use of the Windows feature to debug internal signal values.

Conclusion

Synopsys SmartModel PLD models allow you to simulate entire designs, including large designs, within the software. With simulation, you can debug the design before it is programmed into an actual device. To see Altera PLD models or SmartModel documentation, go to http://www.synopsys.com.

Figure 3. Windows Feature Allows Visibility into PLD Design



Customer Application

Altera PLDs Allow GENICOM to Out-Print Competition

When GENICOM Corporation, a leading supplier of high-performance printers for the mid-range client-server market, was designing the new microLaser 320 series of departmental printers (see Figure 1), one of the key decisions was the type of device for the printer control block. Although competitors were using gate arrays for similar controllers, GENICOM engineers wanted a flexible solution that would allow them to go to market faster, to offer many models using the same controller architecture, and to upgrade printers without extensive re-engineering.

The microLaser 320 printer series is designed to be a highly versatile departmental printing solution with the widest possible range of options. With standard network connectivity to the most popular operating systems, it offers high-speed, high-resolution printing on a variety of media, advanced document handling, and remote print management.

To power the 32 page-per-minute, 1200 × 1200 dots per inch (DPI) output, the microLaser 320 printer series uses a 166-MHz RISC processor as its central processing unit and includes 32 Mbytes of EDO RAM (expandable to 96 Mbytes) and standard Ethernet networking connections. The optional duplexer, finisher/stapler, high-capacity sheet feeder, and 8 Mbytes of FLASH memory for storing fonts and forms make the microLaser 320 an ideal choice for improving office productivity.

The heart of the microLaser 320 is the Intelliprint controller architecture, which is implemented in an Altera® EPF6024AQC240-2 device (see Figure 2 on page 24). The controller is virtually printer-independent. Therefore, GENICOM can produce a number of different models that operate across platforms, migrate easily and rapidly to new document-handling technologies, and permit trouble-free customer upgrades, extending the life of the printer.

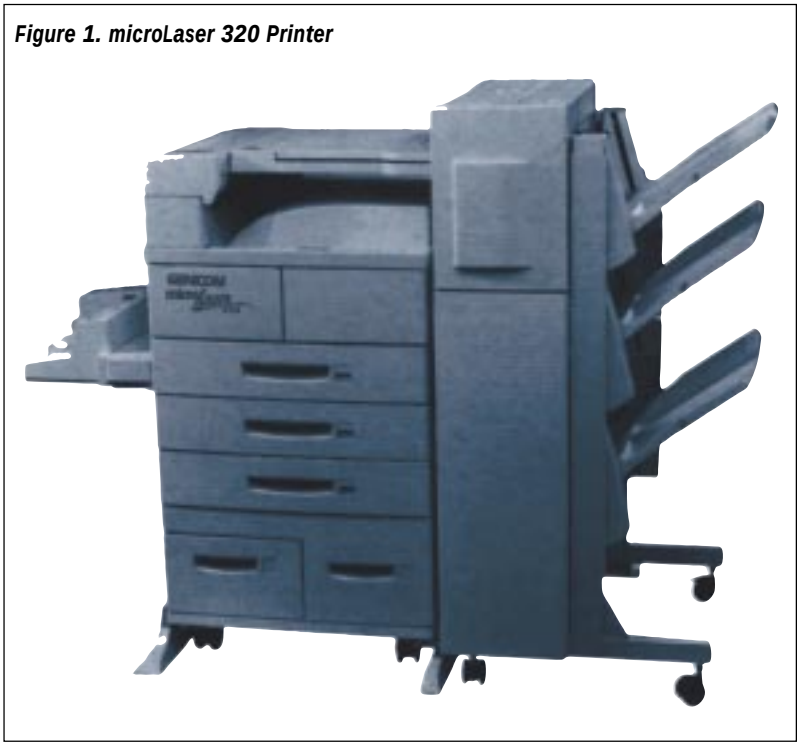
The FLEX 6000 Advantage

The GENICOM engineers decided to use an Altera FLEX® 6000 programmable logic device (PLD) for the printer controller of the microLaser 320 series for a number of reasons. Because of the planned variations between microLaser 320 models, GENICOM decided that using ASICs for their new printer series was impractical—they would probably need an ASIC for each product in the series. Also, because the model's life cycle would be short, given today's rapid advances in printer technology, GENICOM risked being left with excess inventory of ASICs.

When compared with the cost of a similar gate array, the unit cost of the FLEX 6000 devices was about the same.

As with all projects, time-to-market was a crucial consideration. "Engineering time was critical, so the reprogrammability of a PLD was a key advantage," said Eric Heineman,

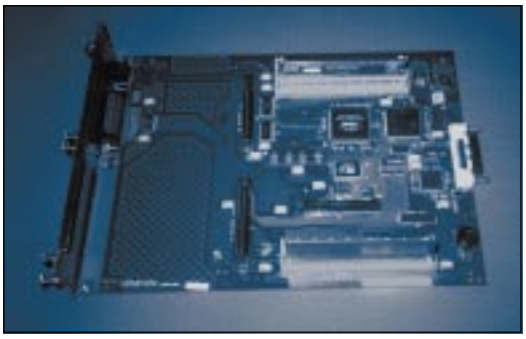
Figure 1. microLaser 320 Printer



continued on page 24

Altera PLDs Allow GENICOM to Out-Print Competition, continued from page 23

Figure 2. microLaser 320 Board with FLEX 6000 Device



marketing manager of the Page Printer Division at GENICOM. Not only did the company want the ability to migrate quickly to newer technology, they were also under pressure from a leading computer OEM to deliver a number of different models. Heineman continues, "At the request of the OEM, we even had to make some minor design changes during production, but we were able to respond quickly by reprogramming the FLEX 6000 devices. The flexibility of the devices saved us both time and money."

Another important factor in GENICOM's choice to use FLEX 6000 devices was cost. For GENICOM, the unit cost of FLEX 6000 devices was comparable to the cost of a similar gate array. Additionally, the company did not incur any of the non-recoverable engineering (NRE) costs associated with gate array development. Test vector generation—the most time-consuming part of the gate array design flow—was unnecessary with the FLEX 6000 devices, which are fully tested before shipment. The fast prototyping capabilities of the PLDs also enabled in-system testing early in the design cycle, shortening time-to-market.

The deciding factor for GENICOM was the FLEX 6000 OptiFLEX™ architecture. As Heineman explained, "The routing [in the FLEX 6000 device] is the best on the market, and the predictable timing is critical to the design and to our time-to-market. Also, all the needed functionality could fit into a relatively small device."

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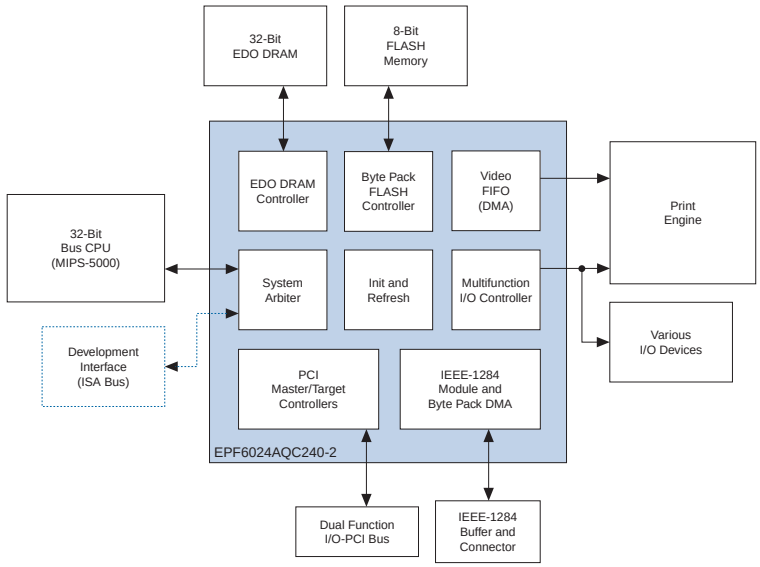
Figure 3. EPF6024AQC240-2 Device in Controller Block



Advanced Controller Architecture

The EPF6024AQC240-2 device is used in the microLaser 320 printer series as the interface and control block between the CPU and the printer engine. "We call it the 'GENICOM System Glue,' because this design is basically printer-independent," said Heineman. The peripheral component interconnect (PCI)-compatible FLEX 6000 device contains both the application-specific logic and the PCI bus interface that allows the printer series to offer a variety of options. Figure 3 shows the block diagram of the controller block.

Conclusion

Using FLEX 6000 devices enabled the designers at GENICOM to bring the innovative microLaser 320 printer series to the market in a short time. GENICOM now offers a number of models with different specifications and user options that use the FLEX 6000-based controller, and can make upgrades in the future without extensive reengineering. With the flexible Altera solution, they have created a complete range of options for themselves and their customers.

Questions & Answers

Q *Which revision control software packages does the Quartus™ version 1999.06 software support?*

A The Quartus version 1999.06 software supports PVCS, RCS, and SCCS. If you would like to use other revision control software packages, you can create your own interface using a tool command language (Tcl) script. Refer to "Developing Tcl Scripts for Quartus Software" on page 19 or Quartus Help for details.

Q *Why can't the Quartus version 1999.06 software find any nodes for my VWF after a successful compilation?*

A To generate nodes from your design files in a new VWF, you must initialize simulation to extract node names from the design database. If you do not extract nodes from the design database, the Quartus Node Finder indicates that no nodes were found (i.e., it issues a no matches message). For more information about creating VWFs, refer to "Copying Node Names to a Waveform File with the Node Finder" in Quartus Help.

Q *Do I need the ObjectStore software to run the Quartus software?*

A Yes. ObjectStore works together with the Quartus software to manage the project design database. If ObjectStore is installed improperly or is not running, the Quartus software cannot create projects or compile designs.

Altera recommends installing ObjectStore in its default location, c:\odi\ostore. If ObjectStore is installed in another location, the directory path cannot include spaces. ObjectStore is included on the Quartus installation CD-ROM and does not need to be purchased separately.

Q *Will I receive a copy of the Quartus software if I have an active software maintenance agreement for the MAX+PLUS® II software, but do not have an active subscription?*

A Altera has sent the Quartus version 1999.06 software to customers who have an active subscription (refer to the Altera Subscription Program page on Altera's web site for details about the program).

The subscription program replaced the software maintenance program as of November 1st, 1998. If you purchased software or renewed your software maintenance after this date, you have an active subscription and will receive the Quartus software version 1999.06. If you renewed your software maintenance before November 1st, 1998, you are still on the old maintenance program and will not receive the Quartus software.

Altera has sent the Quartus version 1999.06 software to customers who have an active subscription.

Design Automation Conference 1999: Where Tools & Design Methodology Meet

The Cajun setting of New Orleans, Louisiana served as the backdrop for this year's Design Automation Conference (DAC) held June 21-23. Altera® hosted a number of demonstrations featuring the APEX™ device family and Quartus software, as well as a multimedia presentation highlighting Altera's revolutionary System-on-a-Programmable-Chip™ solutions.

The "Wall of Fame," which displayed 25 live boards from customers such as 3COM, Lucent, Texas Instruments, and Toshiba, showed the versatility of Altera's programmable logic designs. Altera Megafunction Partners Program (AMPP℠) partners Integrated Silicon Systems, Lexra, Nova, and Sapien Design were also on hand to provide demonstrations of their intellectual property (IP) solutions optimized for Altera programmable logic devices (PLDs).

Altera Programming Support

Download Cables

Table 1 provides programming and configuration compatibility information for the MasterBlaster™ serial or universal serial bus (USB) communications cable and the BitBlaster™ serial and ByteBlasterMV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable.)

Table 1. Download Cable Compatibility

Device	MasterBlaster (1)	ByteBlasterMV	BitBlaster (2)
APEX 20K	✓	✓ (3)	
APEX 20KE	✓	✓ (3)	
FLEX 10K	✓	✓	✓
FLEX 10KA	✓	✓	✓
FLEX 10KE	✓	✓	✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A	✓	✓	✓
MAX 7000B	✓	✓ (3)	
MAX 3000	✓	✓	✓

Notes:
(1) The MasterBlaster communications cable can be used with the Quartus software for device download and SignalTap logic analysis. It can also be used with the MAX+PLUS II software version 9.3 for device downloads.
(2) The BitBlaster download cable must operate at 5.0 V.
(3) The ByteBlasterMV download cable must operate at 3.3 V for these devices. VCCIO pins can be set to either 2.5 V or 3.3 V.

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for selected Altera devices. Algorithms are supplied via Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Microsystems' BBS. Programming support information for configuration, MAX® 9000, and MAX 7000 devices is shown in Table 2. All information is subject to change.

Table 2. Third-Party Programming Hardware Support

Device	Data I/O (1)	BP Microsystems (2)
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPC1441	✓	✓
EPC2	(3)	✓
EPM3032A	(3)	(3)
EPM3064A	(3)	(3)
EPM3128A	(3)	(3)
EPM3256A	(3)	(3)
EPM7032	✓	✓
EPM7032AE	(3)	(3)
EPM7032S	✓	✓
EPM7064	✓	✓
EPM7064AE	(3)	✓
EPM7064S	✓	✓
EPM7096	✓	✓
EPM7128A	✓	✓
EPM7128S	✓	✓
EPM7128AE	(3)	(3)
EPM7128E	✓	✓
EPM7160E	✓	✓
EPM7192S	✓	✓
EPM7192E	✓	✓
EPM7256A	(3)	✓
EPM7256AE	(3)	(3)
EPM7256S	✓	✓
EPM7256E	✓	✓
EPM7512AE	(3)	✓ (4)
EPM9320	✓	✓
EPM9320A	✓	✓
EPM9400	✓	✓
EPM9480	✓	✓
EPM9560	✓	✓
EPM9560A	✓	✓

Notes:
(1) These devices are supported by Data I/O 3900 version 6.0 and UniSite programmers version 6.0.
(2) These devices are supported by BP Microsystems programmers version 3.
(3) Contact Data I/O or BP Microsystems about programming support for these devices.
(4) Contact Data I/O or BP Microsystems about programming support for 256-pin ball-grid array (BGA) and FineLine BGA™ packages.

Programming Hardware Support

The following table contains the latest programming hardware information for Altera devices. For correct programming, use the software version shown in "Current Software Versions" on page 5. Table 3 lists Altera programming adapters for MAX 9000, MAX 7000, MAX 3000, and configuration devices.

Table 3. Altera Programming Adapters (Part 1 of 3) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)* EPC1064V *(2)* EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)* EPC1213 *(2)*	DIP, J-lead	PLMJ1213
EPC2 *(4)*	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(5)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(5)* PLMR9000-240NC *(5)*
EPM7032	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032B	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7064S	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(5)*

Table 3. Altera Programming Adapters (Part 2 of 3) *Note (1)*

Device	Package	Adapter
EPM7064AE EPM7064B	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin) FineLine BGA (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC *(5)* PLMF7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A EPM7128AE	J-lead (84-pin) TQFP (100-pin) TQFP (144-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMJ7000-84 PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMF7000-100 PLMF7000-256
EPM7128B	TQFP (100-pin) TQFP (144-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMF7000-100 PLMF7000-256
EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMT7000-100NC *(5)* PLMQ7128/7160-160NC *(5)*
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMQ7128/7160-160NC *(5)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC *(5)*
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A	TQFP (100-pin) TQFP (144-pin) PQFP (208-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMF7000-256
EPM7256S	PQFP (208-pin) RQFP (208-pin)	PLMR7256-208NC *(5)* PLMT7256-208NC *(5)*

continued on page 28

Altera Programming Support, continued from page 27

Table 3. Altera Programming Adapters (Part 3 of 3) *Note (1)*

Device	Package	Adapter
EPM7256AE EPM7256B	TQFP (100-pin) FineLine BGA (100-pin) TQFP (144-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMF7000-100 PLMT7000-144NC *(5)* PLMF7000-256
EPM7512AE EPM7512B	TQFP (144-pin) PQFP (208-pin) BGA (256-pin) FineLine BGA (256-pin)	PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMB7000-256 PLMF7000-256
EPM3032A	J-lead (44-pin) TQFP (44-pin)	PLMJ3000-44 PLMT3000-44
EPM3064A	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ3000-44 PLMT3000-44 PLMT3000-100NC *(5)*
EPM3128A	TQFP (100-pin) TQFP (144-pin)	PLMT3000-100NC *(5)* PLMT3000-144NC *(5)*
EPM3256A	TQFP (144-pin) PQFP (208-pin)	PLMT3000-144NC *(5)* PLMR3256-208NC *(5)*

Notes:
(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on MAX 5000 and Classic™ devices. Altera offers an adapter exchange program for 0.8-µm EPM5032, EPM5064, and EPM5130 programming adapters.
(2) FLEX® 8000 configuration device.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(4) APEX 20K, FLEX 10K, or FLEX 6000 configuration device.
(5) These devices are not shipped in carriers.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera.

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	Altera Literature Services	(888) 3-ALTERA **lit_req@altera.com**	(408) 544-7144 *(2)* **lit_req@altera.com**
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline (6 a.m. to 6 p.m. Pacific Time)	(800) 800-EPLD (408) 544-7000	(408) 544-7000 *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**sos@altera.com**	**sos@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**

Notes:
(1) The *MAX+PLUS II Getting Started* and *Quartus Tutorial* manuals are available from the Altera web site. To obtain other MAX+PLUS® II and Quartus™ software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

Discontinued Devices Update

Altera has announced that EPM7032V devices will be discontinued. See Table 1 for recommended alternative devices. The date for last order acceptance is December 23, 1999; the date for last Altera® shipments is June 30, 2000. For more information, see reference document PDN 9907.

Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at http://www.altera.com.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at http://www.rocelec.com.

Table 1. Recommended EPM7032V Replacement Devices

Existing Ordering Codes	Recommended Alternative
EPM7032VLC44-20	EPM7032AELC44-10
EPM7032VLC44-15	EPM7032AELC44-10
EPM7032VLC44-12	EPM7032AELC44-10
EPM7032VTC44-20	EPM7032AETC44-10
EPM7032VTC44-15	EPM7032AETC44-10
EPM7032VTC44-12	EPM7032AETC44-10
EPM7032VTI44-20	EPM7032AETI44-7

Altera Device Selection Guide

Current information for the Altera® APEX™ 20K, FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, MAX 7000, MAX 3000A, and configuration devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide.*

For the most up-to-date information, go to the Altera web site at http://www.altera.com. Some of the devices listed may not yet be available. Contact Altera or your local sales office for the latest device availability.

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[2]	I/O PINS[2]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	MACROCELLS
EP20K60E	60,000	144-Pin TQFP, 196-Pin BGA[1], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[1], 356-Pin BGA	92, 143, 151, 183, 204, 204	1.8 V	2,560	32,768	256
EP20K100	100,000	144-Pin TQFP, 196-Pin BGA[1], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[1], 356-Pin BGA	101, 149, 159, 189, 252, 252	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 196-Pin BGA[1], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[1], 356-Pin BGA	92, 143, 151, 183, 246, 246	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1]	87, 143, 175, 273, 316	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1]	144, 174, 279, 382	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1], 652-Pin BGA, 672-Pin BGA[1]	136, 168, 273, 376, 376, 376	1.8 V	8,320	106,496	832
EP20K300E	300,000	208-Pin RQFP, 240-Pin RQFP, 652-Pin BGA, 672-Pin BGA[1]	120, 152, 408, 408	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin BGA[1]	502, 502, 502	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	652-Pin BGA, 672-Pin BGA[1]	488, 488	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	652-Pin BGA, 672-Pin BGA[1], 1,020-Pin BGA[1]	483, 508, 624	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin BGA[1], 984-Pin PGA, 1,020-Pin BGA[1]	498, 508, 716, 716	1.8 V	38,400	327,680	2,560
EP20K1500E	1,500,000	652-Pin BGA, 984-Pin BGA[1], 1,020-Pin BGA[1]	483, 858, 858	1.8 V	54,720	466,944	3,648

Notes:
(1) Space-saving FineLine BGA package.
(2) Preliminary. Contact Altera for latest information.

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA 672-Pin BGA[1]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[1]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA, 672-Pin BGA[1]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	71, 102	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 81, 117, 171, 171	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218	3.3 V	-1, -2, -3	1,960	1,960

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[1]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[1]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[1]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX, FLEX 10K, FLEX 10KE, and FLEX 6000 devices

Notes to Tables:

(1) This package is a space-saving FineLine BGA package.

(2) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-6, -7, -10
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032B	32	44-Pin PLCC/TQFP, 48-Pin TQFP	36, 36	2.5 V	-3, -5, -7
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68, 68	5.0 V	-6, -7, -10, -12, -15
EPM7064AE	64	44-Pin PLCC/TQFP, 49-Pin 0.8-mm BGA, 100-Pin TQFP, 100-Pin BGA[1]	38, 40, 40, 68	3.3 V	-4, -7, -10
EPM7064B	64	44-Pin PLCC/TQFP, 48-pin TQFP, 49-Pin 0.8-mm BGA, 100-Pin TQFP, 100-Pin BGA[1]	38, 40, 40, 68, 68	2.5 V	-3, -5, -7
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-7, -10, -12, -15, -20
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 256-Pin BGA[1]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 169-Pin 0.8-mm BGA, 256-Pin BGA[1]	68, 84, 84, 100, 100, 100	3.3 V	-5,-7,-10
EPM7128B	128	44-Pin PLCC/TQFP, 48-pin TQFP, 100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 169-Pin 0.8-mm BGA, 256-Pin BGA[1], 256-Pin BGA	36, 40, 84, 84, 100, 100, 100, 100	2.5 V	-4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 104	5.0 V	-10, -12, -15, -20
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7192E	192	160-Pin PQFP/PGA	124	5.0 V	-12, -15, -20
EPM7256S	256	208-Pin RQFP/PQFP	164	5.0 V	-7, -10, -15
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	5.0 V	-12, -15, -20
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	84, 84, 120, 164, 164	3.3 V	-5, -7, -10
EPM7256B	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 256-Pin BGA	84, 120, 164, 164, 164	2.5 V	-5, -7, -10
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 256-Pin BGA	120, 176, 212, 212	3.3 V	-7, -10, -12
EPM7512B	512	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 256-Pin BGA	84, 120, 212, 212, 212	2.5 V	-6, -7, -10

Note:
(1) Space-saving FineLine BGA package.

MAX 3000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM3032A	32	44-pin PLCC, 44-pin TQFP	34, 34	3.3 V	-4, -7, -10
EPM3064A	64	44-pin PLCC, 44-pin TQFP, 100-pin TQFP	34, 34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-pin TQFP, 144-pin PQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-pin TQFP, 208-pin PQFP	116, 158	3.3 V	-6, -7, -10