News & Views
Fourth Quarter, November 1999
Newsletter for Altera Customers

ALTERA®
The Programmable Solutions Company™

APEX 20KE Devices Provide Unmatched System-Level Performance

Altera's new APEX™ 20KE devices, which provide the highest performance in programmable logic devices (PLDs), are now shipping. Ranging from 60,000 to 1.5 million typical gates (160,000 to 2.5 million maximum system gates), the feature-rich APEX 20KE devices are engineered to implement System-on-a-Programmable-Chip™ designs and are optimal for advanced PLD applications easily.

The enhanced APEX 20KE MultiCore™ architecture integrates look-up table (LUT) logic, product-term logic, content-addressable memory (CAM), dual-port RAM, and ROM into a single device. APEX 20KE devices support advanced I/O standards, including the low-voltage differential signaling (LVDS) standard, and up to four phase-locked loops (PLLs). Powerful, off-the-shelf intellectual property (IP) functions optimized for APEX devices are available to further speed time-to-market and, together with the Quartus™ development software, provide for efficient designs.

New Process Technology

A cornerstone of the improved performance and capabilities of APEX 20KE devices is their industry-leading, 1.8-V, 0.18-µm, six-layer metal process technology. This leading-edge technology increases typical system speeds to over 160 MHz. In addition, the 1.8-V core voltage reduces power consumption by almost 50% compared to 2.5-V devices.

MultiCore Architecture Increases Performance

The APEX 20KE architecture combines the original APEX 20K MultiCore architecture with new enhancements, including the addition of CAM, to improve system-level integration.

APEX 20KE ESBs can be directly configured as embedded CAM, significantly increasing system performance compared to discrete CAM. APEX 20KE embedded system blocks (ESBs) also offer greater flexibility in CAM size as opposed to the fixed sizes of discrete CAM (see Figure 1 on page 4). For better performance and efficiency, APEX CAM is implemented in silicon and is not emulated as in competing programmable solutions. Embedded CAM is

continued on page 4

Inside This Issue:

M-NV-Q499-01

MAX... It's good for your system!

MAX 7000B Nutrition Facts

Serving Size	Macrocell
Servings Per Package	32 - 512
t_{PD}	3.5 - 6 ns
System Performance	200+ MHz
GTL+	Supported
SSTL-2	Class I & II
SSTL-3	Class I & II
64-Bit, 66-MHz PCI	Compatible
LVCMOS	Supported
LVTTL	Supported
2.5 V	Supported
1.8 V	Supported
Cost Effective	100%

Ingredients: 2.5-V V_{CC}, ISP, JTAG BST, Jam™ STAPL support, MultiVolt™ I/O, FineLine BGA™ packages, vertical migration, SameFrame™ pin-outs, hot socketing support

MAX ON BOARD

Formulated for Peak Performance

Altera® MAX® devices are the fastest product-term-based devices in the industry, offering propagation delays as fast as 3.5 ns. The MAX architecture can boost system performance to over 200 MHz—giving you the speed you need for even the most demanding applications.

Chock-Full of Advanced Features

The MAX architecture offers state-of-the-art features that allow top-system performance. Altera leads the industry in I/O standard support for product-term-based devices. MAX devices contain programmable I/O blocks that can be independently configured to interface to multiple I/O standards, including GTL+, SSTL-2, SSTL-3 and 64-bit, 66-MHz PCI. This advanced I/O interface support gives you the bandwidth you need to meet today's design challenges.

MAX devices support enhanced in-system programmability (ISP), giving you the flexibility to program your design on-the-fly, speeding time-to-market. Other essential ingredients include support for Joint Test Action Group (JTAG) boundary scan testing, and the Jam™ Standard Test and Programming Language (STAPL), JEDEC standard JESD-71—all in state-of-the-art FineLine BGA™ and Ultra FineLine BGA packages.

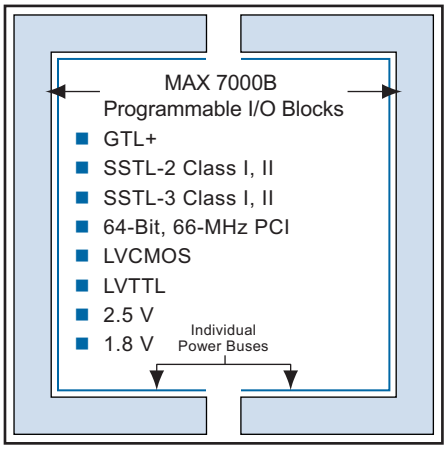


Table of *Contents*

I.S. EN ISO 9001

Ken Lau, Publisher
Greg Steinke, Technical Editor
101 Innovation Drive
San Jose, CA 95134
Tel: (408) 544-7000
Fax: (408) 544-7809
n_v@altera.com

APEX Devices Provide Unmatched System-Level Performance, continued from page 1

ideally suited for high-level pattern matching and data searching operations and will play a key role in applications such as:

- Ethernet address look-up
- Internet protocol filtering
- Data compression
- Pattern recognition
- Cache tags
- Fast look-up for routing tables
- High-bandwidth packet searches for data switches, firewalls, bridges, and routers
- Caching for a large, external CAM block

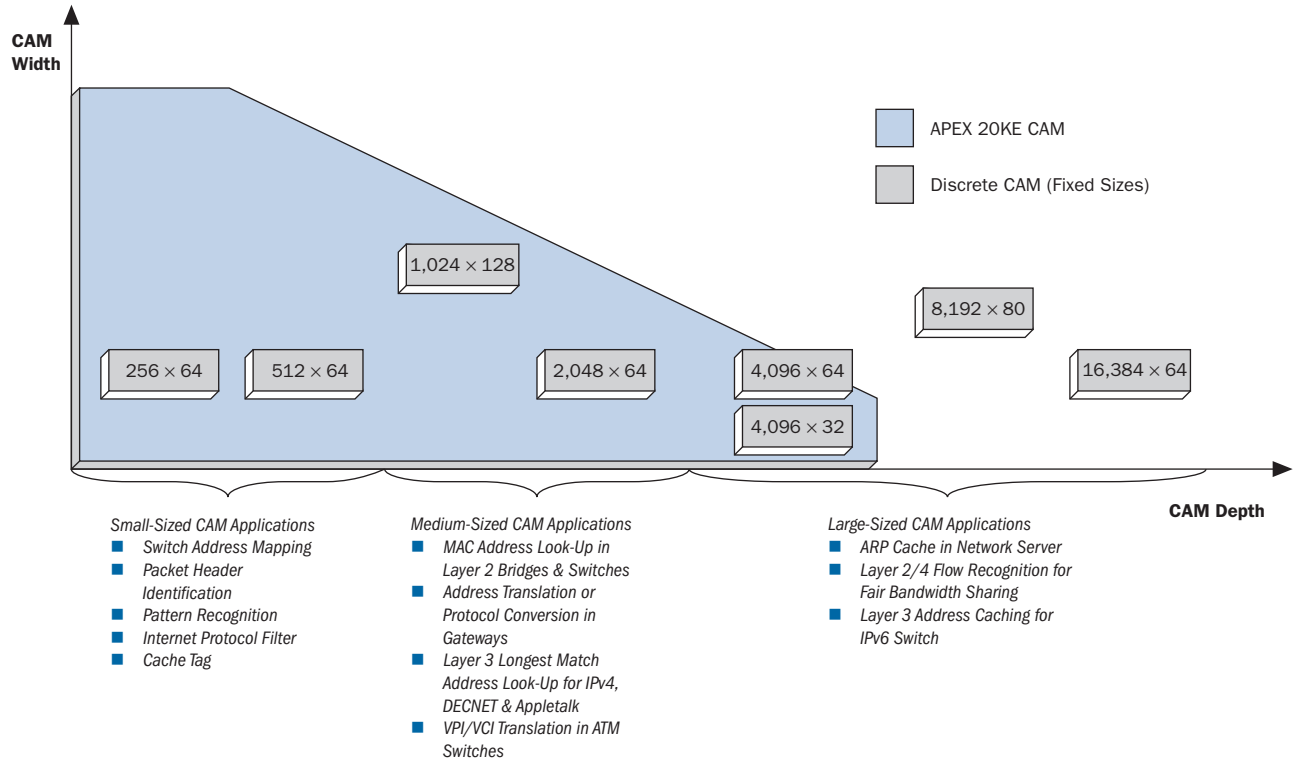
In addition to CAM, the APEX architecture also provides the ability to implement product-term logic using ESBs, a function first featured in APEX 20K devices. Product-term logic performance is further improved in APEX 20KE devices.

Advanced I/O Standard Support

High system performance depends on both the internal performance capabilities of a PLD and its ability to interface effectively in the system environment. For this reason, I/O performance is key when choosing a PLD. APEX 20KE devices support a variety of advanced, high-performance I/O standards.

APEX 20KE devices support the high-speed LVDS I/O standard, which permits I/O frequencies as high as 622.08 megabits per second (Mbps). LVDS, which is implemented using dedicated shift register circuitry and high-speed PLLs, is ideal for applications involving high-bandwidth data transfer. APEX LVDS supports up to 19.9-Gbit bandwidth. For more

Figure 1. APEX Embedded CAM Sizes vs. Discrete CAM Sizes



information on the LVDS I/O standard, see "APEX LVDS I/O Standard Offers Increased Performance" on page 15.

APEX 20KE devices also support other advanced I/O standards. Stub series terminated logic for 2.5 V (SSTL-2) and 3.3-V SSTL-3 are important for high-speed memory interfacing applications, and Gunning transceiver logic plus (GTL+) is commonly used for high-speed processor interfaces and backplane drivers. The advanced graphics port (AGP) standard is often used for interfacing graphics applications. Full support is provided for the low-voltage transistor-transistor logic (LVTTL), low-voltage CMOS (LVCMOS), and center-tap-terminated (CTT) I/O standards, enabling effective interaction with other devices in a variety of applications.

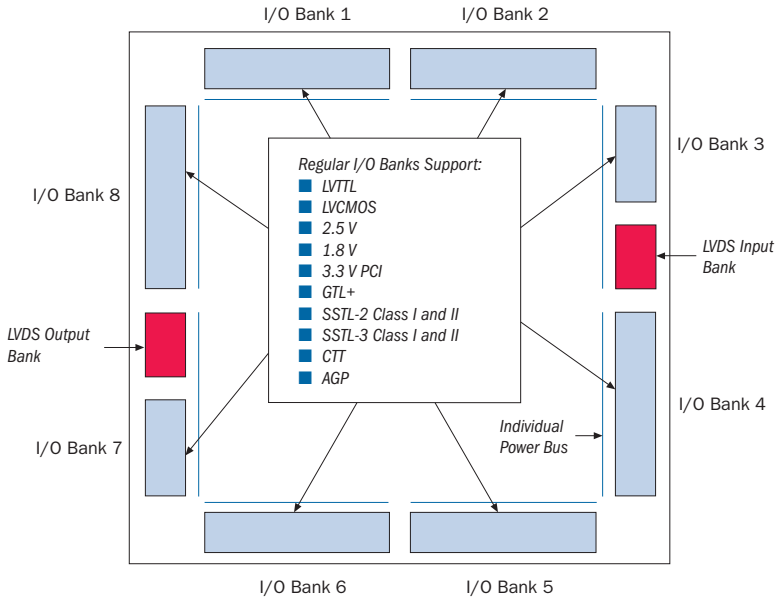
The I/O pins on APEX 20KE devices are accessible through eight programmable I/O banks (see Figure 2) and two LVDS I/O banks. With this architecture, multiple I/O standards can be used at the same time on a single APEX 20KE device. In addition, each I/O bank can be powered at a different V_{CCIO} voltage, allowing for effective MultiVolt™ interaction with other devices running at different voltage levels.

Advanced PLLs

The enhanced APEX 20KE PLLs increase device and board-level performance. Altera has included up to four PLLs in each APEX 20KE device, depending on the device. In addition to the ClockLock™ and ClockBoost™ circuitry in APEX 20K devices, each APEX 20KE PLL allows input clock signals to be adjusted by any number, $m/(n \times k)$ or $m/(n \times v)$, where m and k are integers between 2 and 256, n is an integer between 1 and 16, and v is an integer between 2 and 16 (see Figure 3). These adjustments to the clock signals broaden the capabilities of the ClockBoost feature and allow a wide range of new clock signals to be generated.

With the ClockShift™ capability, the phase of a clock signal can be adjusted by a wide variety of factors. APEX 20KE PLLs can also drive outputs off the device and can be combined with clock feedback inputs to remove board delay. Specific PLLs within APEX 20KE devices aid in

Figure 2. APEX 20KE I/O Block

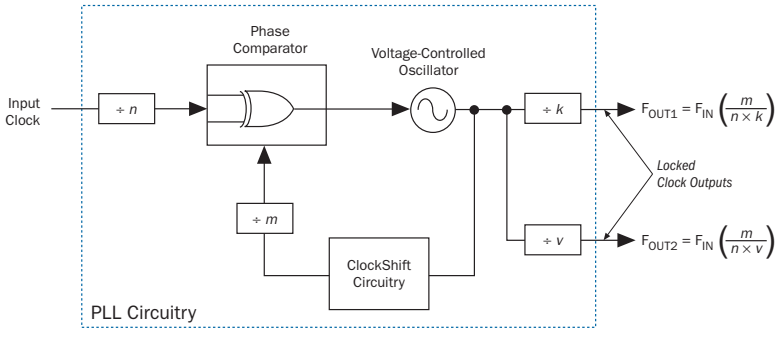


providing an LVDS throughput of up to 622.08 Mbps per channel.

Quartus Support

APEX 20KE devices are supported by the Quartus™ development system version 1999.10 and higher. Altera's fourth generation development tool comes with key features designed specifically for multi-million-gate designs. Multi-processor support cuts compilation time and shortens design cycles. The SignalTap™ embedded logic analyzer integrates the functionality of an external logic analyzer into the software so that it is possible to

Figure 3. PLL Circuitry in APEX Devices



continued on page 6

APEX Devices Provide Unmatched System-Level Performance, continued from page 5

verify a device running at system speeds. NativeLink™ integration seamlessly transfers information between the Quartus software and leading third-party EDA tools. Internet integration provides instant access to software updates and registration, intellectual property, and technical support.

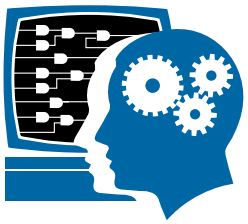
IP Integration

The large density and increased functionality of APEX 20KE devices create a strong need for off-the-shelf IP solutions. Designers save valuable development time by incorporating functions typically reserved for discrete components and application-specific standard products (ASSPs) into an APEX 20KE device. A wide variety of IP solutions are available as MegaCore™ IP functions or Altera Megafunction Partners Program (AMPP℠) IP megafunctions. Altera's OpenCore™ evaluation allows designers to instantiate, compile, and simulate a megafunction prior to purchase to ensure an accurate solution. For complete information on Altera's IP offering, visit the IP MegaStore™ web site at **http://www.altera.com/IPmegastore**.

Conclusion

The APEX 20KE family is available today and ready to meet the challenges of multi-million gate designs. The combination of APEX devices, the Quartus development system, and IP allows for a complete System-on-a-Programmable-Chip solution. For further details, visit the Altera web site (**http://www.altera.com**) or contact your local sales representative.

New Customer Training Classes Available



Three new customer training classes are now available to support designers using the Quartus™ software and APEX™ 20K devices. Customer training classes help you use the Quartus development system more effectively and design your systems efficiently around the APEX architecture. In addition to these three new classes, the Altera Technical Training Program offers classes on designing with FLEX® and MAX® devices as well as the MAX+PLUS® II software. For more information, go to the Altera web site at **http://www.altera.com**.

- *Introduction to the Quartus Software & the APEX 20K Device Family*
  Provides an overview of the Quartus design environment and the APEX 20K and APEX 20KE architectures.
- *Designing with the Quartus Software*
  Explains in depth how to use the Quartus software effectively for each stage of the design flow.
- *Optimizing Designs for APEX 20K Devices*
  Describes the architecture of the APEX 20K and APEX 20KE devices and explains how to optimize designs to achieve better performance and logic utilization in these devices.

Attendance Soars at PLD World '99

On November 5, 1999 Altera held the sixth annual PLD World event in Tokyo, Japan. PLD World '99 was both a technical conference and an exhibit featuring Altera and EDA and Altera Megafunction Partners Program (AMPP℠) partners. The event—which drew a record attendance of over 2,200—featured Altera's System-on-a-Programmable-Chip™ solutions, including APEX™ devices, Quartus™ software demonstrations, and Altera® MegaCore™ and AMPP IP megafuctions.

APEX

EP20K400E Devices Now Available

The first APEX™ 20KE device, the EP20K400E device, is now available. Tables 1 and 2 list the APEX 20K and APEX 20KE software support schedules, respectively.

EP20K400E devices provide 64-bit, 66-MHz peripheral component interconnect (PCI)-compliance and support multiple high-bandwidth, low-voltage I/O interfacing standards, including low-voltage transistor-transistor logic (LVTTL), low-voltage CMOS (LVCMOS), Gunning transceiver logic plus (GTL+), stub series terminated logic for 2.5 V (SSTL-2), 3.3-V SSTL-3, center-tap-terminated (CTT), and advanced graphics port (AGP). APEX 20KE devices also support the low-voltage differential signaling (LVDS) standard, with performance up to 622.08 megabits per second (Mbps). EP20K400E devices feature four phase-locked loops (PLLs) with enhanced ClockLock™, ClockBoost™, and ClockShift™

Table 1. APEX 20K Devices & Quartus Software Support Availability

Device	Package *(1)*	Software Support Availability
EP20K100	144-pin TQFP	Now
	144-pin FineLine BGA	February 2000
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	Now
EP20K200	208-pin RQFP	Now
	240-pin RQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
EP20K400	652-pin BGA	Now
	655-pin PGA	Now
	672-pin FineLine BGA	Now

Note:
(1) TQFP: thin quad flat pack, PQFP: plastic quad flat pack, RQFP: power quad flat pack, BGA: ball-grid array, PGA: pin-grid array.

Table 2. APEX 20KE Devices & Quartus Software Support Availability

Device	Package	Software Support Availability
EP20K60E	144-pin TQFP	February 2000
	144-pin FineLine BGA	February 2000
	208-pin PQFP	February 2000
	240-pin PQFP	February 2000
	324-pin FineLine BGA	February 2000
	356-pin BGA	February 2000
EP20K100E	144-pin TQFP	Now
	144-pin FineLine BGA	February 2000
	208-pin PQFP	Now
	240-pin PQFP	Now
	324-pin FineLine BGA	Now
	356-pin BGA	Now
EP20K160E	144-pin TQFP	February 2000
	208-pin PQFP	February 2000
	240-pin PQFP	February 2000
	356-pin BGA	February 2000
	484-pin FineLine BGA	February 2000
EP20K200E	208-pin PQFP	Now
	240-pin PQFP	Now
	356-pin BGA	Now
	484-pin FineLine BGA	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K300E	208-pin RQFP	Now
	240-pin RQFP	Now
	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K400E	652-pin BGA	Now
	672-pin FineLine BGA	Now
EP20K600E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	1,020-pin FineLine BGA	Now
EP20K1000E	652-pin BGA	Now
	672-pin FineLine BGA	Now
	984-pin PGA	February 2000
	1,020-pin FineLine BGA	Now
EP20K1500E	652-pin BGA	February 2000
	984-pin PGA	February 2000
	1,020-pin FineLine BGA	February 2000

continued on page 8

Devices & Tools, continued from page 7

The MultiCore architecture offers designers system-level integration on a single device, eliminating the need for multiple devices.

circuitry. The devices also provide the MultiVolt™ I/O interface, which is ideal for mixed-voltage systems. EP20K400E devices are available in 652-pin BGA and 672-pin FineLine BGA™ packages.

The 400,000-gate (1 million maximum system gates) EP20K400E device, which features an enhanced MultiCore™ architecture, including integrated look-up table (LUT) logic, product-term logic, and flexible memory, is now shipping. The MultiCore architecture offers designers system-level integration on a single device, eliminating the need for multiple devices. The flexible memory structure supports dual-port RAM with independent read/write ports, content addressable memory (CAM) for fast address search functions, and high-performance first-in first-out (FIFO) functions in a wide range of widths and depths. For the latest information on APEX devices, go to the Altera® web site at **http://www.altera.com**.

APEX 20KE PLL Offerings

PLL circuitry is available in APEX devices and is designated with an "X" suffix in the ordering code (e.g., EP20K400EBC652-1X). The PLL feature will be offered in all APEX device densities in both the -1 and -2 speed grades. APEX 20KE PLLs contain enhanced ClockLock circuitry for skew reduction, ClockBoost circuitry for flexible rate multiplication and division, and ClockShift circuitry for phase-shift and delay capability. APEX 20KE PLLs are also used in LVDS I/O interfaces to support high-speed data transfer rates and to convert between serial LVDS and parallel data. EP20K400E devices with the PLL feature are now shipping.

ACE

New Low-Cost ACE Device Family

Altera announced a new device family, targeted at low-cost, high-performance applications. Code-named "ACE," these devices are 1.8-V, 0.18-µm, SRAM-based devices, ranging from 20,000 to 150,000 gates. These devices are especially well-suited for high-volume, price-sensitive applications in the communications and computing market. ACE devices feature embedded memory, new I/O standard support, 64-bit, 66-MHz PCI compatibility, PLL support, and advanced packaging technologies.

FLEX

FLEX 10KE PLL Devices

FLEX® 10KE devices with PLLs are now available in all densities. PLLs improve the I/O timing and core performance of the device. Table 3 represents the clock-to-output (t_{CO}) and setup (t_{SU}) timing improvements when using the ClockLock feature for an EPF10K100E device.

Table 3. I/O Pin Performance with PLL

Parameter	Without PLL (ns)	With PLL (ns)
t_{CO}	5.2	4.2
t_{SU}	2.0	1.5

PLLs using the ClockBoost feature multiply the internal clock by 2×, simplifying high-speed board design and potentially reducing LE requirements through time-domain multiplexing.

0.22-µm FLEX 10KE Devices Are Shipping

All 0.22-µm FLEX 10KE devices are now available. The 0.22-µm EPF10K30E, EPF10K50S, EPF10K100E, EPF10K130E, and EPF10K200S devices have all the latest FLEX 10KE features, including devices in the -1 and -2 speed grades that support PLLs, and a programmable delay to provide full 64-bit, 66-MHz PCI compliance.

FLEX 10KE Device Offerings

Table 4 shows all of the 2.5-V FLEX 10KE device packages and speed grades. MAX+PLUS® II design support is currently available for all device package options.

Table 4. FLEX 10KE Offerings

Device	Offerings	Speed Grade
EPF10K30E	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL *(1)*	-1X, -2X
EPF10K50S	144-pin TQFP	-1, -2, -3
	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL *(1)*	-1X, -2X
EPF10K100E	208-pin PQFP	-1, -2, -3
	240-pin PQFP	-1, -2, -3
	256-pin FineLine BGA	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	PLL *(1)*	-1X, -2X
EPF10K130E	240-pin PQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL *(1)*	-1X, -2X
EPF10K200S	240-pin RQFP	-1, -2, -3
	356-pin BGA	-1, -2, -3
	484-pin FineLine BGA	-1, -2, -3
	600-pin BGA	-1, -2, -3
	672-pin FineLine BGA	-1, -2, -3
	PLL *(1)*	-1X, -2X

Note:
(1) All packages with the PLL feature are available in the -1X and -2X speed grade.

FLEX 10KE devices are offered with the PLL feature in -1 and -2 speed grades. These devices have an "X" suffix in the ordering code (e.g., EPF10K100EQC208-1X).

FLEX 10K Product Transitions

Altera is in the process of migrating 2.5-V EPF10K50E and EPF10K200E devices from a 0.25-µm process to a 0.22-µm process. All other members of the FLEX 10KE family are already on a 0.22-µm process. Altera is also in the process of migrating the EPF10K50V device from a 0.30-µm, 3-layer-metal process to a 0.30-µm, 4-layer-metal process. Altera has finished migrating select 3.3-V FLEX 10KA and 5.0-V FLEX 10K devices. Table 5 outlines the process migration schedule and lists the reference documentation associated with this migration. You can download these documents from the Customer Notifications page on the Altera web site at **http://www.altera.com**.

Altera is in the process of migrating 2.5-V EPF10K50E and EPF10K200E devices from a 0.25-µm process to a 0.22-µm process.

Table 5. FLEX 10K Device Migration

Device	Core Voltage (V)	Date	Reference	Process (µm)
EPF10K10A	3.3	Done	PCN 9810	0.30
EPF10K30A	3.3	Done	PCN 9810	0.30
EPF10K50V	3.3	Done	PCN 9810	0.30 *(1)*
		January 2000	PCN 9915	0.30 *(2)*
EPF10K100A	3.3	Done	PCN 9810	0.30
EPF10K10	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K20	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K30	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50	5.0	Done	PCN 9901 ADV 9909	0.42
EPF10K50E	2.5	Nov. 1999	PCN 9911	0.22
EPF10K200E	2.5	Nov. 1999	PCN 9911	0.22

Notes:
(1) 3-layer metal process.
(2) 4-layer metal process.

continued on page 10

Devices & Tools, continued from page 9

FLEX 10KE Industrial-Temperature Devices

EPF10K50S and EPF10K200S industrial temperature devices will be available by the end of 1999. Table 6 lists the availability of industrial-temperature FLEX 10KE devices.

Table 6. FLEX 10KE Industrial-Temperature Device Availability

Device	Availability
EPF10K50ETI144-2	Now
EPF10K50EQI240-2	Now
EPF10K50EFI256-2	Now
EPF10K50SQI208-2	December 1999
EPF10K50SBI356-2	December 1999
EPF10K50SFI484-2	December 1999
EPF10K100EQI208-2	Now
EPF10K100EFI256-2	Now
EPF10K100EFI484-2	Now
EPF10K130EQI240-2	Now
EPF10K130EBI356-2	Now
EPF10K130EFI484-2	Now
EPF10K200EBI600-2	Now
EPF10K200SRI240-2	December 1999
EPF10K200SBI356-2	December 1999
EPF10K200SFI672-2	November 1999

FLEX 6000 Devices

All FLEX 6000 devices offered in FineLine BGA packages are now available. FLEX 6000 devices are based on the OptiFLEX™ architecture, which minimizes die size while maintaining high performance and routability. The devices have reconfigurable SRAM elements, which give designers the flexibility to change their designs quickly during prototyping and testing. Table 7 shows FLEX 6000 device availability.

Table 7. FLEX 6000 Device & MAX+PLUS II Software Support Availability

Package	Device			
	EPF6010A	EPF6016	EPF6016A	EPF6024A
100-pin TQFP	Now		Now	
100-pin FineLine BGA			Now	
144-pin TQFP	Now	Now	Now	Now
208-pin PQFP		Now	Now	Now
240-pin PQFP		Now		Now
256-pin BGA		Now		Now
256-pin FineLine BGA			Now	Now

MAX

MAX 7000B Devices Support Advanced I/O Standards

MAX 7000B devices support advanced I/O standards such as GTL+, SSTL-2, and SSTL-3.

MAX® 7000B devices support advanced I/O standards such as GTL+, SSTL-2, and SSTL-3. These 2.5-V devices range from 32 to 512 macrocells with propagation delays as fast as 3.5 ns. MAX 7000B devices also feature enhanced in-system programmability (ISP) to allow devices to be mounted on a printed circuit board (PCB) before they are programmed, as well as MultiVolt I/O pins, hot-socketing capability, and pin compatibility with the industry-standard MAX 7000 devices. Table 8 shows all commercial package and speed grade options.

MAX 7000A Devices

3.3-V MAX 7000A devices range from 32 to 512 macrocells with propagation delays as fast as 4.5 ns. MAX 7000A devices support enhanced ISP, MultiVolt I/O pins, hot-socketing capability, and pin compatibility with the industry-standard MAX 7000 devices. All MAX 7000A devices are available in industrial temperature grades. Table 9 shows MAX 7000A device commercial package and speed grade options.

Table 8. MAX 7000B Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032B	44-pin PLCC *(1)*	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
EPM7064B	44-pin PLCC	-3, -5, -7
	44-pin TQFP	-3, -5, -7
	48-pin TQFP	-3, -5, -7
	49-pin Ultra FineLine BGA *(2)*	-3, -5, -7
	100-pin TQFP	-3, -5, -7
	100-pin FineLine BGA	-3, -5, -7
EPM7128B	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	48-pin TQFP	-4, -7, -10
	49-pin Ultra FineLine BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
	144-pin TQFP	-4, -7, -10
	169-pin Ultra FineLine BGA	-4, -7, -10
	256-pin BGA	-4, -7, -10
	256-pin FineLine BGA	-4, -7, -10
EPM7256B	100-pin TQFP	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512B	100-pin TQFP	-6, -7, -10
	144-pin TQFP	-6, -7, -10
	169-pin Ultra FineLine BGA	-6, -7, -10
	208-pin PQFP	-6, -7, -10
	256-pin BGA	-6, -7, -10
	256-pin FineLine BGA	-6, -7, -10

Notes:
(1) PLCC: plastic J-lead chip carrier.
(2) Ultra FineLine BGA pacakges are Altera's latest, 0.8-mm BGA packages.

MAX 7000S Devices

5.0-V MAX 7000S devices offer features such as 5-ns speed grades, ISP, open-drain output options, and IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells. All MAX 7000S devices are available in industrial temperature grades. Table 10 shows the packages and speed grades available in the commercial temperature grade.

Table 9. MAX 7000AE Commercial-Temperature Devices

Device	Package	Speed Grade
EPM7032AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
EPM7064AE	44-pin PLCC	-4, -7, -10
	44-pin TQFP	-4, -7, -10
	49-pin Ultra FineLine BGA	-4, -7, -10
	100-pin TQFP	-4, -7, -10
	100-pin FineLine BGA	-4, -7, -10
EPM7128AE	84-pin PLCC	-5, -7, -10
	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	169-pin Ultra FineLine BGA	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7256AE	100-pin TQFP	-5, -7, -10
	100-pin FineLine BGA	-5, -7, -10
	144-pin TQFP	-5, -7, -10
	208-pin PQFP	-5, -7, -10
	256-pin FineLine BGA	-5, -7, -10
EPM7512AE	144-pin TQFP	-7, -10, -12
	208-pin PQFP	-7, -10, -12
	256-pin BGA	-7, -10, -12
	256-pin FineLine BGA	-7, -10, -12

Table 10. Commercial-Temperature MAX 7000S Devices

Device	Package	Speed Grade
EPM7032S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
EPM7064S	44-pin PLCC	-5, -6, -7, -10
	44-pin TQFP	-5, -6, -7, -10
	84-pin PLCC	-5, -6, -7, -10
	100-pin TQFP	-5, -6, -7, -10
EPM7128S	84-pin PLCC	-6, -7, -10, -15
	100-pin TQFP	-6, -7, -10, -15
	100-pin PQFP	-6, -7, -10, -15
	160-pin PQFP	-6, -7, -10, -15
EPM7160S	84-pin PLCC	-6, -7, -10
	100-pin TQFP	-6, -7, -10
	160-pin PQFP	-6, -7, -10
EPM7192S	160-pin PQFP	-7, -10, -15
EPM7256S	208-pin PQFP	-7, -10, -15

continued on page 12

Devices & Tools, continued from page 11

Low-Cost MAX 3000A Devices

MAX 3000A devices are 3.3-V product-term-based programmable logic devices (PLDs) targeted for high-volume, low-cost designs. These devices have an enhanced ISP feature set and range in density from 32 to 256 macrocells. With propagation delays as fast as 4.5 ns, MAX 3000A devices provide you with exceptional performance at the lowest price per macrocell among Altera MAX products. Table 11 shows the packages and speed grades available for MAX 3000A devices.

Table 11. MAX 3000A Devices

Device	Package	Speed Grade
EPM3032A	44-pin PLCC 44-pin TQFP	-4, -7, -10 -4, -7, -10
EPM3064A	44-pin PLCC 44-pin TQFP 100-pin TQFP	-4, -7, -10 -4, -7, -10 -4, -7, -10
EPM3128A	100-pin TQFP 144-pin PQFP	-5, -7, -10 -5, -7, -10
EPM3256A	144-pin TQFP 208-pin PQFP	-5, -7, -10 -5, -7, -10

A new, 4-Mbit configuration device is scheduled to be available in the first half of 2000.

CONFIGURATION

New Configuration Device Coming Soon

A new, 4-Mbit configuration device is scheduled to be available in the first half of 2000, allowing designers to configure EP20K400E or EPF10K200S devices with a single configuration device. This new device has an enhanced feature set over the existing EPC configuration devices, including faster programming times, parallel programming, and intellectual property (IP) security features.

TOOLS

Enhanced Timing Analysis Capabilities in the Quartus Software

The Quartus™ software features an enhanced Static Timing Analyzer, which is an integral part of the Quartus Compiler that is automatically invoked during design compilation. Designers do not need to perform a separate timing analysis step manually at the end of each successful compilation.

The Quartus Timing Analyzer reports the maximum operating frequency (f_{MAX}) for each specified clock signal. In addition, the Timing Analyzer lists all register-to-register paths fed by the clock signal and the associated operating frequency. These results reflect the internal f_{MAX} calculations for the design.

The Quartus software accounts for pin-to-register (t_{SU}), register-to-pin (t_{CO}), and off-chip delays (which the designer must specify) to calculate a system f_{MAX}, providing designers with a more accurate estimate of their entire system's maximum frequency instead of only the device's internal maximum frequency.

During compilation, the Quartus Timing Analyzer automatically detects clock signals for the design. Single clock frequency analysis is performed automatically during each design compilation, and results are reported in the internal f_{MAX} calculations. Designers can also have the Quartus Timing Analyzer perform a multiple-clock frequency analysis on designs that contain register-to-register paths controlled by different clocks.

The Quartus Timing Analyzer also accommodates designs with multicycle paths, which are paths that intentionally require more than one clock cycle to propagate. Through the **Clock Requirement** section in the **Timing Analyses** folder of the Compilation Report, the Quartus Timing Analyzer reports the maximum register-to-register delay between all source and

destination registers in the current design entity or project.

Evolving design methodologies and aggressive process technologies allow larger and higher-performance designs in PLDs. These advanced designs create a need for an enhanced timing analysis tool to aid in timing verification. The Quartus Static Timing Analyzer incorporates a set of powerful new timing analysis features that are critical in enabling true System-on-a-Programmable-Chip™ designs.

Download All Quartus & MAX+PLUS II Manuals from the Web

You can download the Quartus and MAX+PLUS II manuals and related documents from the Altera web site. The manuals are in Portable Document Format (**.pdf**), so they can be viewed and printed from PCs or UNIX workstations using the free Adobe Acrobat Reader software. A link to download the latest version of Adobe Acrobat Reader is provided on the Altera web site.

Technical briefs, applications notes, and data sheets for the Quartus and MAX+PLUS II development systems are also available for downloading. Technical briefs and application notes provide detailed information on how to get the most out of your Altera programmable logic development systems and how to interface with third-party tools with minimal effort.

To download documentation from the Altera web site, go to **http://www.altera.com** and select Literature from the navigation bar at the top of the page. Then select either the Quartus or MAX+PLUS II links to view all available documentation for the selected product.

Purchase Altera Software Subscriptions & MegaCore Functions Directly from the Web

You will be able to buy new software subscriptions, renew subscriptions, and buy Altera MegaCore functions directly from the Altera web site 24 hours a day, seven days a week, beginning in December 1999.

When you purchase a subscription product, you receive full-featured versions of both the Quartus and MAX+PLUS II development systems, along with twelve months of software updates.

Prior to the purchase of a license, you can download, instantiate, and simulate Altera MegaCore IP products for free using Altera's OpenCore™ evaluation feature. If, after simulation, you decide that the function meets your needs, simply license the function directly from the web. Your license file allows you to generate a Programmer Object Files (**.pof**) for programming devices with the MegaCore function.

The Altera store is available for customers in the United States and Canada only, and accepts payment by Visa, MasterCard, or American Express credit cards. Store operation is scheduled to begin in December 1999.

Quartus Software Version 1999.10 Now Shipping

The Quartus software version 1999.10 is now shipping and supports Windows 98 and Windows NT for PCs, and Solaris 2.6 operating systems for UNIX workstations. Support for the HP-UX operating system is scheduled to be available later this year. Contact your Altera FAE or sales representative if you need a copy of the Quartus software for HP-UX.

The Quartus software version 1999.10 provides many new features to support designs using Altera APEX 20K and APEX 20KE devices. In addition to offering new device support, the Quartus software version 1999.10 allows designers to take advantage of APEX 20KE features such as CAM and advanced I/O standards (e.g., LVTTL, GTL+, SSTL-2, SSTL-3, CTT, and AGP). PLL support is also available for all APEX 20KE devices with an "X" suffix at the end of the ordering code. I/O pins on larger APEX 20KE devices with PLLs can also be configured for LVDS.

continued on page 14

Devices & Tools, continued from page 13

An enhanced Timing Analyzer included with the Quartus software version 1999.10 allows customers to perform traditional static timing analysis, as well as improved multi-clock and multicycle timing analyses.

Behavioral models for APEX 20KE device features are available with version 1999.10. These VHDL and Verilog HDL behavioral models allow you to simulate APEX 20KE device features such as CAM, LVDS, and PLLs using third-party simulation tools such as Verilog-XL and ModelSim before the synthesis and place-and-route processes. Tables 12 and 13 list new device support added to the Quartus software version 1999.10.

Table 12. New Devices with Full Support from the Quartus Software Version 1999.10

Device	Package
EP20K200	484-pin FineLine BGA
EP20K400	652-pin BGA *(1)*
EP20K400E	652-pin BGA, 652-pin BGA *(1)*, 672-pin FineLine BGA
EP20K600E	652-pin BGA

Note:
(1) These devices contain PLLs.

Table 13. New Devices with Advance Support from the Quartus Software Version 1999.10

Device	Package
EP20K60E	144-pin TQFP, 196-pin FineLine BGA, 208-pin PQFP, 240-pin PQFP, 324-pin FineLine BGA, 356-pin BGA
EP20K100	196-pin FineLine BGA, 356-pin BGA
EP20K100E	196-pin FineLine BGA, 356-pin BGA
EP20K200	356-pin BGA
EP20K200E	356-pin BGA, 652-pin BGA, 672-pin FineLine BGA
EP20K300E	208-pin RQFP, 240-pin RQFP, 652-pin BGA, 672-pin FineLine BGA
EP20K600E	672-pin FineLine BGA, 1,020-pin FineLine BGA
EP20K1000E	652-pin BGA, 672-pin FineLine BGA, 1,020-pin FineLine BGA

E+MAX Software Now Available for Free Download

Altera's new E+MAX™ software, a full-featured design tool that supports all devices in the MAX 7000 and MAX 3000 families, can be downloaded for free from the Altera web site. This new software includes schematic design entry, and AHDL, VHDL, and Verilog HDL functional and timing simulation and static timing analysis. The E+MAX software is a complete development system for designing with MAX 7000, MAX 7000S, MAX 7000A, MAX 7000AE, MAX 7000B, and MAX 3000A devices. You can download this new software from the web for free; you can also install the E+MAX software from the MAX+PLUS II version 9.4 CD-ROM.

MAX+PLUS II BASELINE Software Version 9.4 Now Available

You can now download the latest version of the MAX+PLUS II BASELINE software from the Altera web site. Version 9.4 of the MAX+PLUS II BASELINE software provides support for the new device package combinations listed in Table 14.

Table 14. Devices Supported by MAX+PLUS II BASELINE Software Version 9.4

Device	Package
EPM7128B	100-pin TQFP, 144-pin TQFP, 256-pin FineLine BGA
EPF6016A	100-pin FineLine BGA, 256-pin FineLine BGA
EPF6024A	256-pin FineLine BGA
EPF10K30E	256-pin FineLine BGA, 484-pin FineLine BGA

APEX LVDS I/O Standard Offers Increased Performance

As designs progress, they demand more bandwidth. To address this need, Altera has added support for low-voltage differential signaling (LVDS) to the APEX™ device family. LVDS meets new requirements for high data rates and low power consumption.

With LVDS, one device can interface with high-speed low-voltage backplanes or data channels. Board design can be simplified because dedicated circuitry such as LVDS is now integrated into the programmable logic device (PLD), saving board space, reducing pin usage, and improving performance.

Low-Voltage Differential Signaling

LVDS is a low-voltage swing, general-purpose I/O standard that has high-speed, low-power, and low-noise advantages. APEX 20KE devices are designed to meet the ANSI/TIA/EIA-644 standard up to 622.08 megabits per second (Mbps), making LVDS the fastest I/O standard used by PLDs.

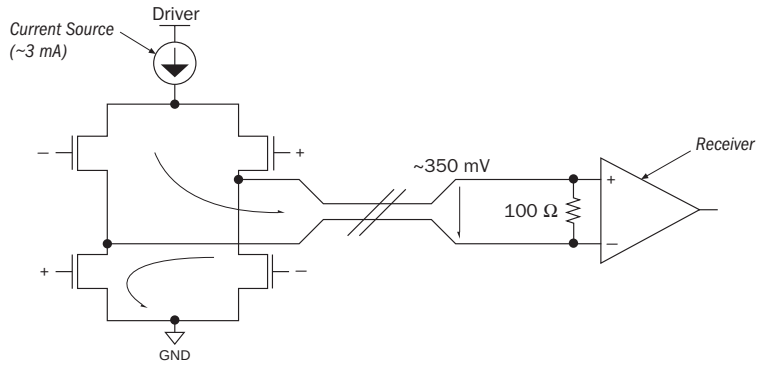
Differential transmission means that every LVDS signal uses two lines. The voltage difference between the two lines define the logic state of the LVDS signal. Each signal pair has a true signal and a complement signal. The differential signal is the true signal minus the complement signal.

Figure 1 shows how the current-mode LVDS driver works.

The LVDS standard has two key advantages over single-ended schemes, i.e., low-voltage CMOS (LVCMOS), low-voltage transistor-transistor logic (LVTTL), and 2.5-V and 1.8-V standards:

- The low-voltage swing reduces power consumption and increases performance.
- LVDS signals are less susceptible to electromagnetic interference (EMI).

Figure 1. LVDS Current-Mode Driver



Performance

Low-voltage swing is important for high performance. To provide switching speeds at high Mbps levels, the LVDS standard defines a typical voltage swing of 350 mV. The smaller the voltage swing, the faster a signal can change logic levels. The faster the transition (i.e., edge rate) time, the higher the potential data rate. Since the noise margin is very narrow with a small voltage swing, a differential data transmission scheme is used. The two signals are referenced to each other, not to ground or another static signal level; therefore, a differential standard can have a much smaller switching region.

The same bandwidth for a LVCMOS data bus can be achieved with LVDS using four times fewer pins by operating the LVDS signals (two pins per signal) at 8× the frequency. Figure 2 on page 16 shows a 128-bit LVCMOS data bus implemented with 16 LVDS channels (32 pins).

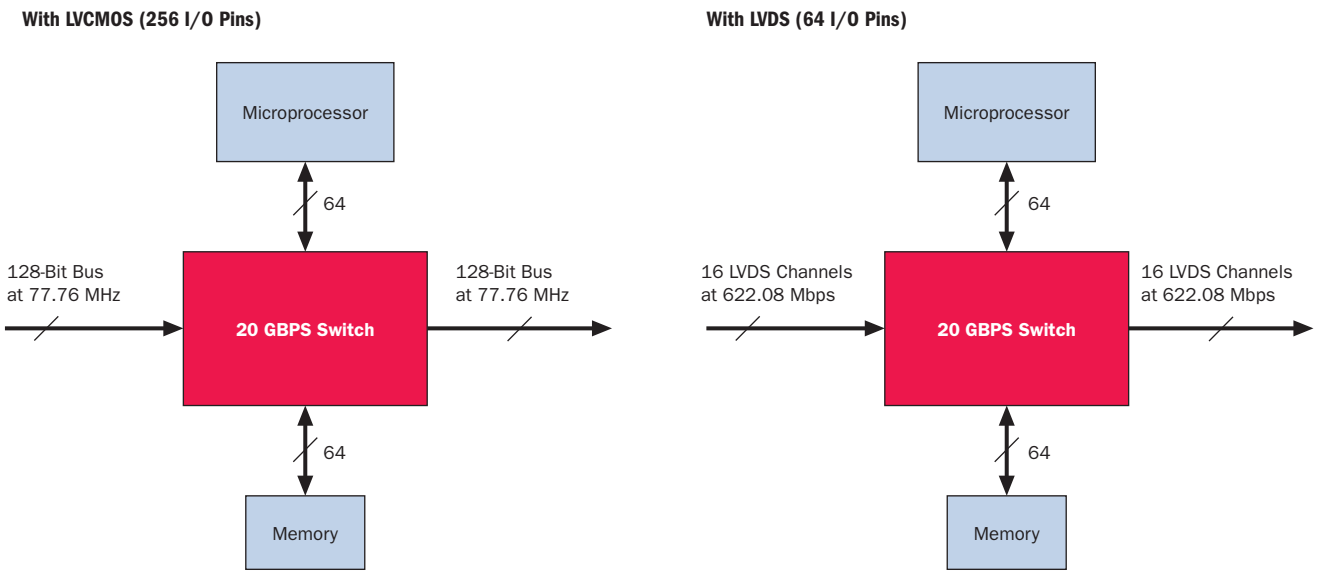
Reduced Power Consumption

LVDS is a power-efficient standard. To show how LVDS compares in power consumption to

continued on page 16

APEX LVDS I/O Standard Offers Increased Performance, continued from page 15

Figure 2. LVDS Uses Four Times Fewer Pins than LVCMOS



LVCMOS, consider the example shown in Table 1. Both LVDS and LVCMOS are operating at a 622.08-Mbps bandwidth.

Reduced System-Level Noise

LVDS is more resistant to common mode noise than single-ended standards like LVCMOS. Figure 3 shows that system and power supply noise is coupled equally to both LVDS signals; therefore, it does not affect signal quality. A logic level is determined by the relation of the two signals, not with respect to ground or another reference signal, as is the case for single-ended and voltage-referenced standards.

LVDS Interface

Figure 4 shows how the LVDS receiver and transmitter internally interface with the logic and other devices in the system. Two PLLs

Table 1. LVDS Consumes Less Power than LVCMOS

Parameter	LVDS	LVCMOS	Unit
Number of pins/channels	1 channel	8 pins	–
Frequency	622.08	77.75	MHz
Bandwidth	622.08	622.08	Mbps
Data voltage swing	0.35	3.3	V
Power per pin	–	3.387	mW
Total power	1.835	27.09	mW

Figure 3. System-Level Noise Rejection

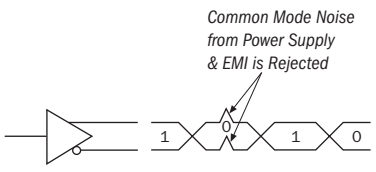
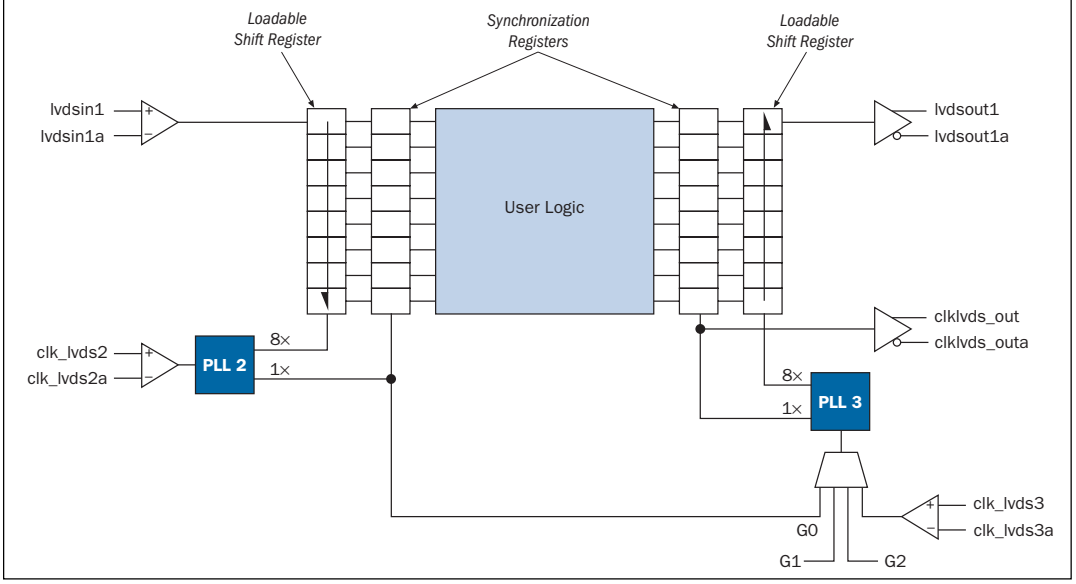


Figure 4. LVDS Receiver & Transmitter Interface



The internal LVDS PLL clocks have an 8× maximum multiplication rate. The LVDS transmitter has the ability to drive the 1× locked PLL clock off-chip.

(PLL2 for the receiver and PLL3 for the transmitter) generate phase-locked clock signals for the serial-to-parallel and parallel-to-serial data converters. The receiver has 16 input channels, and the transmitter has 16 output LVDS channels. The LVDS receiver converts a maximum of 16 LVDS signals into 128 data bits, which feed internal LEs within the device. Similarly, the LVDS transmitter re-converts a maximum of 128 data bits on-chip into 16 LVDS data streams using an 8-to-1 parallel-to-serial converter.

The internal LVDS PLL clocks have an 8× maximum multiplication rate. The LVDS transmitter has the ability to drive the 1× locked PLL clock off chip. The external clock input and output transmit clock signals are in phase with the LVDS data streams. Every cycle of transmit and receive clock data—up to 128 bits of input and output data—are sampled via the 16 LVDS I/O channels.

Conclusion

Altera's APEX 20KE devices offer an on-chip LVDS solution. The LVDS I/O standard simplifies board design by minimizing the number of devices used to interface with backplanes. APEX 20KE devices provide maximum I/O performance, low power consumption, and excellent noise immunity.

Current Software Versions

The Quartus™ version 1999.10 software is currently shipping for the following operating systems:

- Microsoft Windows 98
- Windows NT 4.0
- Sun Solaris 2.6

The Quartus version 1999.06 software will be available for the HP-UX operating system in the fourth quarter of 1999.

The MAX+PLUS® II version 9.4 software is currently available for the following operating systems:

- Microsoft Windows 95 and Windows 98
- Microsoft Windows NT version 3.51 and higher
- Sun Solaris version 2.5 and higher
- HP-UX version 10.20 and higher; however, HP-UX version 11.0 and higher are not yet supported
- AIX version 4.1 and higher

SIDSA Uses Altera FLEX & MAX Devices in Embedded-System Prototyping Platform

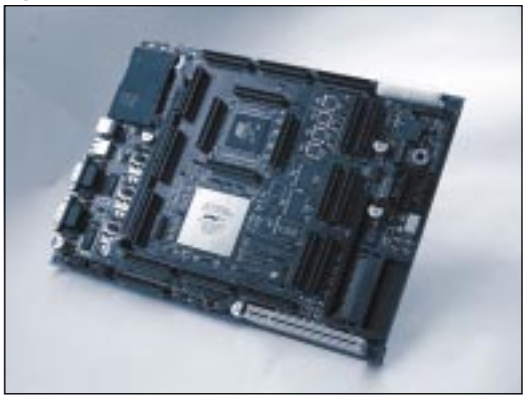
The HSDT100 is a prototyping development system that can accommodate designs with large memory and cache requirements.

Designing today's complex embedded integrated systems demands improved prototyping techniques. Current designs are usually too complex to be fully verified using only simulation, and hardware emulators are very expensive, offering only limited support for embedded microprocessors. Creating ad-hoc prototypes is not necessarily the answer either, because the prototype development process inevitably delays getting the final product to market. A better solution are the HSDT100 and HSDT200 prototyping boards from SIDSA (see Figure 1), a leading chip design house headquartered in Madrid, Spain. The HSDT100 is a prototyping development system that can accommodate designs with large memory and cache requirements. It offers a small, affordable yet powerful system for prototyping application-specific integrated circuits (ASICs).

FLEX 10KA & MAX 7000S Devices Provide the Key

The HSDT100 prototyping board is designed to support the ARM7TDMI embedded microprocessor, a 32-bit RISC microprocessor function developed by ARM Limited. The function is used in many embedded integrated circuits because it provides low power consumption, compact code, and high performance. However, the hardware development tools provided with the processor cannot easily integrate the complex new peripherals and bus configurations required for the development of ASICs. Until now, designers had to program several programmable logic devices (PLDs) and test the system bus with a simulator; to prototype any extra peripherals, designers had to add other hardware to the board.

Figure 1. HSDT200 Board



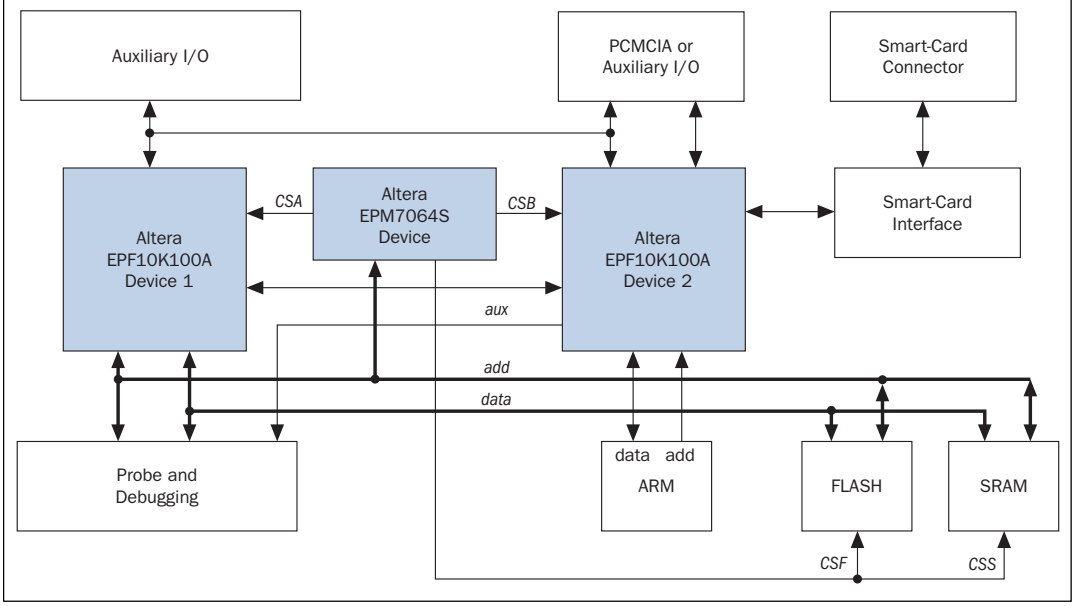
By using two Altera® FLEX® 10K devices and one MAX® 7000S device on the HSDT100 board, SIDSA is able to prototype ASIC designs of mid-range complexity. The Altera FLEX and MAX devices were chosen for their high density and performance. In addition, the MAX+PLUS® II development system provides excellent results and enables integration with other third-party tools.

The architecture of the HSDT100 board is shown in Figure 2.

The board uses an EPM7064STC100-7 device for memory decoding and bus control, which requires reliable high-performance timing. The EPM7064S device enables the bus to operate at a speed of 30 MHz, which is faster than other solutions that use several PLDs. Since SIDSA does not foresee the memory decoding and bus control logic changing, another advantage is gained by isolating the configuration into just one device: the device works with the system without mapping any of its logic onto other PLDs on the board.

The user's prototype logic is supported by two EPF10K100ARC240 devices. "The efficient

Figure 2. HSDT100 Board Architecture



"The efficient memory support of the EPF10K100 devices was a 'must' for SIDSA due to the large number of ASIC designs that require first-in first-out (FIFO) buffers and fast memory banks." Federico Ruiz, chief engineer, SIDSA

memory support of the EPF10K100 devices was a 'must' for SIDSA due to the large number of ASIC designs that require first-in first-out (FIFO) buffers and fast memory banks. Also, the FLEX 10K memory is similar to that used in ASICs," said Federico Ruiz, SIDSA's chief engineer.

SIDSA has launched a new prototyping board, called the HSDT200. Designs on the HSDT200 board will be mapped into just one Altera EP20K400 device. By using the APEX device, SIDSA will double the logic density of the board while using less board space, lowering power consumption, and, thanks to the Altera Quartus™ software, reducing compilation time.

Features

The main features of the HSDT100 board are:

- Logic complexity
  - 200,000 or 400,000 equivalent gate versions
  - 30-MHz system clock
- Software support
  - Compatible with ARM Multi-ICE and Software Development Toolkit
  - Software-compatible ARM PID7T development board
  - Provably secure operating system (PSOS) and real-time operating system (RTOS) baseband signal processor (BSP) option
- On-board peripherals
  - User-configurable resident memory map stored in PLDs
  - 2-Mbyte FLASH memory to store software, variables, and virtual disks
  - 1-Mbyte high-speed SRAM (15 ns)
  - Smart card interface, buffers ISO7816 card slot
  - Personal Computer Memory Card International Association (PCMCIA) extension
  - 100 external I/O pins
- Intellectual property (IP) included
  - ARM-standard 2× timers
  - ARM-standard programmable interrupt controller
  - Memory controller
  - 16450-compatible universal asynchronous receiver/transmitter (UART)

You can debug the ARM microprocessor system in the HSDT100 through a Joint Test Action Group (JTAG) interface using ARM Limited's Multi-ICE tools.

continued on page 20

SIDSA Uses Altera FLEX & MAX Devices in Embedded-System Prototyping Platform, *continued from page 19*

MAX+PLUS II Software Speeds Design Implementation

The HSDT100 ships with synthesizable source code for the standard timer, interrupt controller, UART, and bus controller. Currently, the source code is only available in Verilog HDL, but VHDL support will be available shortly. The default configuration of the HSDT100 can support operating systems such as PSOS, and a Verilog HDL netlist is provided so that the board can be fully simulated for an ARM7TDMI model.

"It is amazing how fast a new user can implement a design in the HSDT100. The Altera MAX+PLUS II tool makes the task of implementing custom logic on the board very easy." Federico Ruiz, Chief Engineer, SIDSA

With the HSDT100, new users receive a board that is ready to use, as well as examples of how to map logic onto the system. "It is amazing how fast a new user can implement a design in the HSDT100," said Federico Ruiz, SIDSA's chief engineer. "The Altera MAX+PLUS II tool makes the task of implementing custom logic on the board very easy."

Fast System Speed for Applications

The HSDT100 board has been used to prototype the following ASICs and systems, among others. The typical system frequencies for these examples are in the range of 30 MHz:

- Conditional access module DVB for MPEG-2 video descrambling and demultiplexing
- On-screen display for television systems
- 2,048-bit RSA cryptography coprocessor
- Multi-standard coin recognizer
- Power meter
- Game support

Conclusion

As ASIC designs become larger and more complex, designers need innovative and affordable ways to reduce prototyping time and get products to market quickly. By incorporating Altera FLEX 10K and MAX 7000S devices into the HSDT100 prototyping system, and by using the MAX+PLUS II software for configuration, SIDSA offers ASIC designers a development and debugging platform that is easy-to-use, flexible, and powerful enough for today's designs.

SIDSA
PTM Torres Quevedo, 1
E-28760 Tres Cantos
(Madrid) Spain
(34) 91 803 5052
http://www.sidsa.com
info@sidsa.com

MAX 5000 Device Transition

On October 4, 1999, Altera and Cypress announced that Cypress acquired Altera's MAX® 5000 business. Altera and its distributors will continue to accept and service orders for MAX 5000 devices until December 31, 1999. Cypress and its distributors are now accepting orders for all MAX 5000 devices. The equivalent Cypress devices are manufactured in the same facilities and are identical to the MAX 5000 devices that Altera is currently shipping.

Additionally, Cypress uses the exact manufacturing flow and contractors that Altera uses (including assembly, test, and finish). For more information about the transition, see the MAX 5000 transition web page (**http://www.max5k-transition.com**). You can find ordering code information, equivalent Cypress part numbers that correlate to Altera part numbers, and a list of Cypress distributors on this web page.

Designing Multi-Rate Filters with the FIR Compiler Version 1.1

Multi-rate filters are used in many high-speed digital applications such as quadrature modulation, modems, narrow-band and band-pass filters, and speech processing. "Multi-rate" means that there are multiple sampling rates within the filter; multi-rate filters change the effective sampling rate of an input signal. Decimation and interpolation are the two main types of multiple-sampling rate filters. Decimation, typically used in receivers, allows users to employ simpler and less-costly analog anti-aliasing filters and improves a system's signal-to-noise ratio. Interpolation is used in transmitters to increase the precision and signal-to-noise ratio of a system. A multi-rate filter can implement both decimation to decrease the sampling rate, and interpolation to increase the sampling rate.

Implementing Multi-Rate Filters in APEX Devices

Programmable logic is ideal for implementing multi-rate filters. For example, an interpolation filter with an input data width of 8 bits, 127 taps, and an interpolation factor of 8 runs at 100 mega-samples per second (Msps) and uses less than 15% of the resources of an EP20K100 device. The flexibility of the MultiCore™ APEX™ architecture enables the high performance necessary to combine serial-distributed arithmetic mapping algorithms and polyphase decomposition structures. The serial-distributed arithmetic algorithm breaks down the finite impulse response (FIR) arithmetic operation to the bit level by mapping the addition of four multiplications by a constant into a single logic element (LE). The polyphase decomposition re-maps the coefficients of a large filter operating at the highest rate, into smaller filters that operate at slower data rates, increasing the total system throughput.

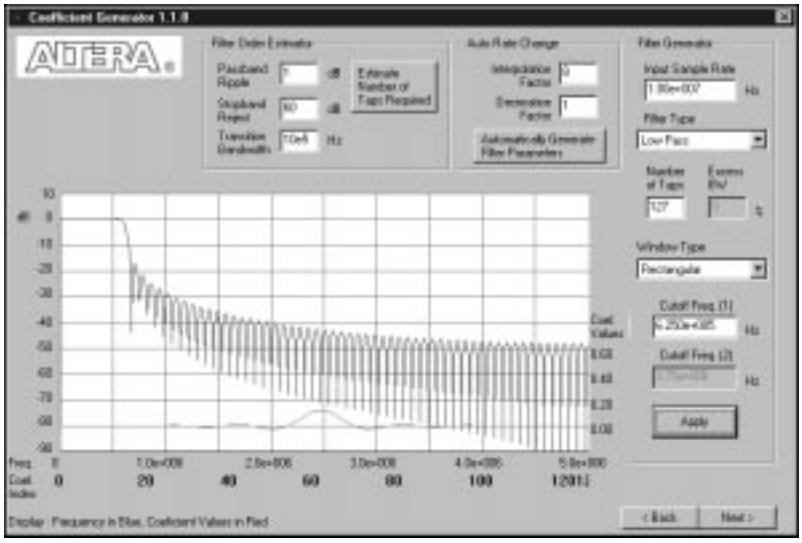
Design Flow with the FIR Compiler Version 1.1

The FIR Compiler version 1.1 automates the implementation of multi-rate filters into APEX and FLEX® devices through the MegaWizard™ Plug-In feature integrated into the Quartus™ and MAX+PLUS® II development tools. After downloading the FIR Compiler from the Altera web site (**http://www.altera.com**), designers can build any FIR filter for their applications by entering parameters such as data width, data type, number of taps, and interpolation or decimation factor. The development software automatically generates the optimized FIR Compiler MegaCore™ function with the chosen parameters. The compiler also provides multiple types of analysis support such as a floating-point-to-fixed-point coefficient analyzer as well as simulation models for third-party hardware description language (HDL) simulation (e.g., VHDL and Verilog HDL) and system-level digital signal processing (DSP) tools (e.g., MATLAB Simulink). The ***FIR Compiler MegaCore Function User Guide*** provides detailed instructions on using the MegaWizard Plug-In and simulation model.

MegaWizard™ Plug-In

Figure 1 shows the FIR Compiler coefficient generator used to specify decimation and interpolation factors.

Figure 1. FIR Compiler Coefficient Generator

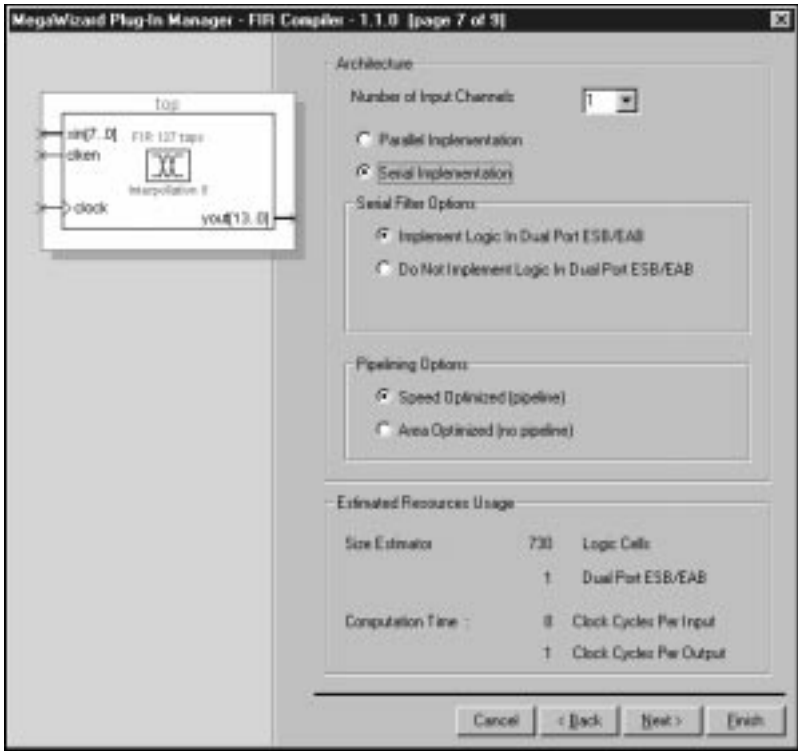


continued on page 22

Designing Multi-Rate Filters with the FIR Compiler Version 1.1, continued from page 21

Figure 2 shows the MegaWizard interface for the FIR Compiler used to set parallel or serial implementation, allowing the user to trade-off area versus speed. The size estimator returns the number of LEs as well as the number of embedded system blocks (ESBs) used for a given set of FIR parameters.

Figure 2. MegaWizard Interface for FIR Compiler

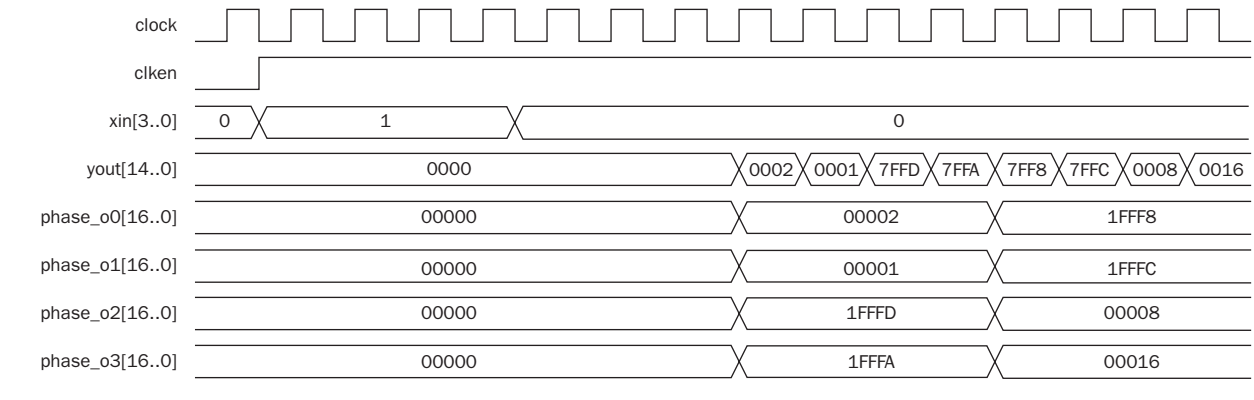


Example: Serial Interpolation Filter

In this example, consider a serial interpolation filter of 20 taps with a multiplication factor of 4. The FIR Compiler automatically creates a Vector File (**.vec**) for the Waveform Editor. Figure 3 shows a serial interpolation filter waveform in which the interpolation factor is equal to the input data width (both have a value of four). The structure runs at 4× the clock speed of the input data. `xin[3..0]` is held for four clock cycles, and each polyphase filter is computed every four clock cycles. The interpolation scheme cycles through the four outputs every clock cycle to generate `yout` (the final output). The FIR Compiler provides access to the polyphase outputs `phase_o0[]`, `phase_o1[]`, `phase_o2[]`, `phase_o3[]`, allowing you to multiplex through the outputs to suit the needs of your application (see Figure 3).

The FIR Compiler lets you achieve breakthrough performance with multi-rate filters using programmable logic devices (PLDs). By allowing the filters to operate at slower frequencies, the total system throughput is increased. For more information on the FIR Compiler version 1.1, see the ***FIR Compiler MegaCore Function User Guide***, available from the Altera web site (**http://www.altera.com**).

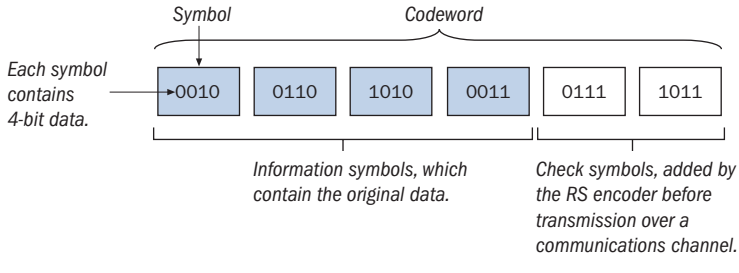
Figure 3. Serial Interpolation Filter Waveform



Reed-Solomon Functions Eradicate Errors

Systems that transmit or store digital data may experience data corruption. To help combat this problem, systems designers incorporate error correction coding (ECC) into their systems. ECCs work by adding redundant bits to data blocks as insurance against possible read/write errors. The Reed-Solomon (RS) encoder/decoder and interleaver/deinterleaver are two common ECC systems that designers use in their communications and digital signal processing (DSP) applications. The RS encoder appends parity information before transmitting data blocks over a communications channel; upon receipt, the decoder uses this information to locate and correct errors. The interleaver/deinterleaver makes it easier for RS functions to detect and correct burst errors (i.e., multiple errors in a row) by distributing them over multiple blocks. This article describes Altera's implementation of the Reed-Solomon encoder/decoder and interleaver/deinterleaver.

Figure 1. Reed-Solomon Codeword Structure



Reed-Solomon Encoders/Decoders

RS encoders/decoders split data streams into a series of codewords. Each codeword consists of several information symbols followed by several check, or parity, symbols. All symbols are limited to an arbitrary number of bits. See Figure 1.

RS codes are described as (*N*,*K*), where *N* is the total number of symbols per codeword and *K* is the total number of information symbols. Errors are defined on a symbol basis (i.e., a symbol containing many bit errors counts as only one error). An RS decoder can detect and correct one symbol error for every two check symbols in a codeword. However, if a codeword contains many errors, the decoder can only detect up to one error for each check symbol.

RS codes are based on finite-field (Galois field) arithmetic. All arithmetic operations (i.e., addition, subtraction, multiplication, and division) on field elements give results that are an element of the field. The number of bits per symbol determines the size of the Galois field. Specifically, the field has 2^m elements, where m is the number of bits per symbol. A specific Galois field is defined by a polynomial, which is user-defined for the RS MegaCore™ function.

The Altera® RS MegaCore function, optimized for APEX™ and FLEX® architectures, provides both discrete and streaming implementations. Through an innovative MegaWizard™ Plug-In, designers can customize the function quickly to fit their specific design requirements. Designers use this feature to set the function's parameters, which define the specific code for the encoder or decoder. Table 1 shows the function's parameters.

For more information on the Reed-Solomon MegaCore function, refer to *Solution Brief 43 (Reed-Solomon MegaCore Function)* or the ***Reed-Solomon MegaCore Function User Guide.***

MegaCore™

Interleaver/Deinterleaver

Interleaving is a simple way to spread dense errors that would otherwise overload an RS encoder/decoder. These functions are typically added to transport channels that require a bit error ratio (BER) on the order of 10^{-6}. When using an interleaver/deinterleaver, the RS encoder's output sequence is interleaved before transmission and deinterleaved before decoding (i.e., the interleaver rearranges the symbols'

continued on page 24

Reed-Solomon Functions Eradicate Errors, continued from page 23

order such that adjacent symbols in the data stream are not from the same codeword; the deinterleaver reverses the process to restore the original order). Thus, errors are distributed uniformly at the RS decoder's input. See Figure 2.

The Altera RS MegaCore function is optimized for APEX and FLEX architectures and provides both discrete and streaming implementations.

The Altera interleaver/deinterleaver MegaCore function operates in the same frequency range used by RS functions and supports continuous, streaming, and discrete modes, making the function compatible with any RS code. The MegaCore function can implement two types of

Table 1. RS MegaCore Function Parameters (Part 1 of 2)

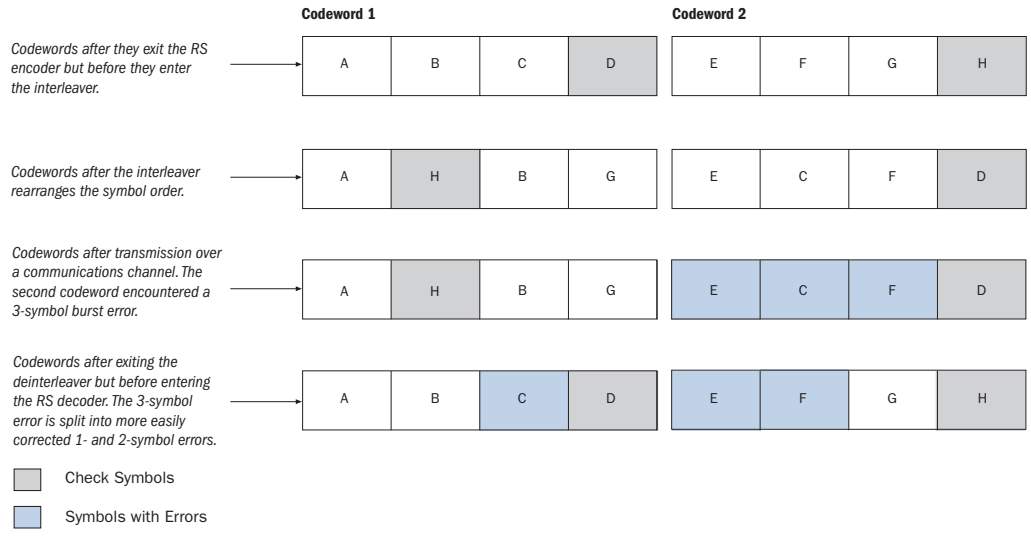
Parameter	Values	Description
N	$R + 1$ to $2^m - 1$	Specifies the total number of symbols per codeword.
R	4 to $(N - 1)$ Maximum of 50 *(1)*	Specifies the number of check symbols per codeword.
m	4 to 8	Specifies the number of bits per symbol.

Table 1. RS MegaCore Function Parameters (Part 2 of 2)

Parameter	Values	Description
field	Any valid polynomial	Specifies the polynomial defining the Galois field for the RS code.
genstart	0 to $(2^m - 1 - R)$	Indicates the first root of the generator polynomial.
architecture	Discrete or streaming	Specifies a discrete or streaming architecture. The discrete architecture processes one entire codeword before starting on the next. The streaming architecture creates a pipelined decoder with a depth of three codewords.
speed	Half or full	Controls the amount of logic used to determine the location and number of errors. The full-speed setting creates a large, high-performance function. The half-speed setting creates a small, lower-performance function.

Note:
(1) The decoder allows both an even and odd number of check symbols.

Figure 2. Interleaver/Deinterleaver Structure



interleavers/deinterleavers: convolutional or block. The convolutional version processes data in a continuous stream, making it ideal for high-speed applications that require correction for burst errors. For low-power applications like mobile phones, the block version processes data in a discrete stream. The MegaCore function is stored in internal or external single-port or dual-port RAM.

The interleaver/deinterleaver MegaCore function also includes a MegaWizard™ Plug-In, which reduces the design creation and simulation cycles from several weeks to several minutes. The wizard generates a highly optimized instance of a custom interleaver/deinterleaver function as well as a MAX+PLUS® II Vector File (**.vec**) that you can use to simulate the function. For example, by choosing a few simple settings, you can build an interleaver function to meet pre-defined specifications, such as DVB 802 or UTMS. Table 2 lists the parameters that you can change to customize the interleaver/deinterleaver MegaCore function.

For more information on the interleaver/deinterleaver MegaCore function, refer to *Solution Brief 42 (Interleaver/Deinterleaver MegaCore Function)* or the ***Symbol Interleaver/Deinterleaver MegaCore Function User Guide***.

Table 2. Interleaver/Deinterleaver Wizard Options

Option	Function	Description
Type	Block or convolutional	Specifies a block or convolutional interleaver/deinterleaver.
Number of columns	Block	Specifies the total length of the codeword (i.e., data symbol + checksum symbol).
Number of rows	Block	Specifies the maximum number of codewords in the function's memory.
Number of branches	Convolutional	Specifies the number of branches used by the function.
Unit delay element	Convolutional	Specifies the unit delay for each branch of the function.
Direction	Block or convolutional	Specifies an interleaver (transmitter) or a deinterleaver (receiver).
Memory type	Block or convolutional	Specifies internal or external memory. Convolutional interleaving uses synchronous dual-port RAM; block interleaving uses synchronous single-port RAM. For internal memory, the MegaWizard Plug-In instantiates the most optimum ESB/EAB configuration automatically.
Symbol width	Block or convolutional	Specifies the width of the input symbol.

New Altera Publications

New publications are available from Altera Literature Services. Individual documents are available on the Altera web site at **http://www.altera.com**. Document part numbers are shown in parentheses.

- ***Intellectual Property Catalog*** (M-CAT-AIPS-01)
- ***Device Package Data Book*** (A-DB-Package-01)
- ***PCI MegaCore Function User Guide*** (A-UG-PCI-01)
- ***Symbol Interleaver/Deinterleaver MegaCore Function User Guide*** (A-UG-INTERLEAVER-01)
- ***Reed-Solomon MegaCore Function User Guide*** (A-UG-SOLOMON-01)
- ***Altera Digital Library CD-ROM***, version 7 (P-CD-ADL-07)
- *APEX 20K Programmable Logic Device Family Data Sheet* (A-DS-APEX20K-02.02)
- *MAX 7000B Programmable Logic Device Family Data Sheet* (A-DS-MAX7000B-01)
- *AN 117: Using Selectable I/O Standards in Altera Devices* (A-AN-117-01)
- *AN 118: Scripting with Tcl in the Quartus Software* (A-AN-118-02)
- *TB 57: Power Consumption Comparison: APEX 20K vs. Virtex Devices* (M-TB-057-01)
- *TB 59: Hierarchical Design Methodology with the Quartus Software* (M-TB-059-01)

APEX 20KE CAM Accelerates GSM Applications

APEX™ 20KE devices offer integrated content-addressable memory (CAM) to accelerate applications requiring fast searches of databases, lists, and patterns. With CAM, input data is compared against a list of stored entries in a single clock cycle, significantly reducing search time when compared to RAM. By eliminating on- and off-chip delays, APEX integrated CAM provides greatly enhanced system performance over discrete CAM.

Because APEX 20KE CAM provides an extremely fast search method, it is ideal for use in global system for mobile communication (GSM) networks. A GSM network uses CAM to speed up the process of locating the address of a mobile phone. This article describes GSM and explains how APEX 20KE CAM can accelerate GSM applications.

GSM Provides A Digital Standard

GSM is an international standard for digital cellular networks, which are the support systems for wireless digital phones. This standard lets subscribers use their digital cellular phones where GSM is supported while ensuring their privacy and security. The digital nature of GSM permits users to transmit not only voice information, but also e-mail, fax, and other data from laptop computers. Because GSM is wireless—it uses radio frequencies to transmit data—customers can connect their computers to a phone and conduct their day-to-day correspondence without needing a phone jack, adapter, or cables.

GSM Elements

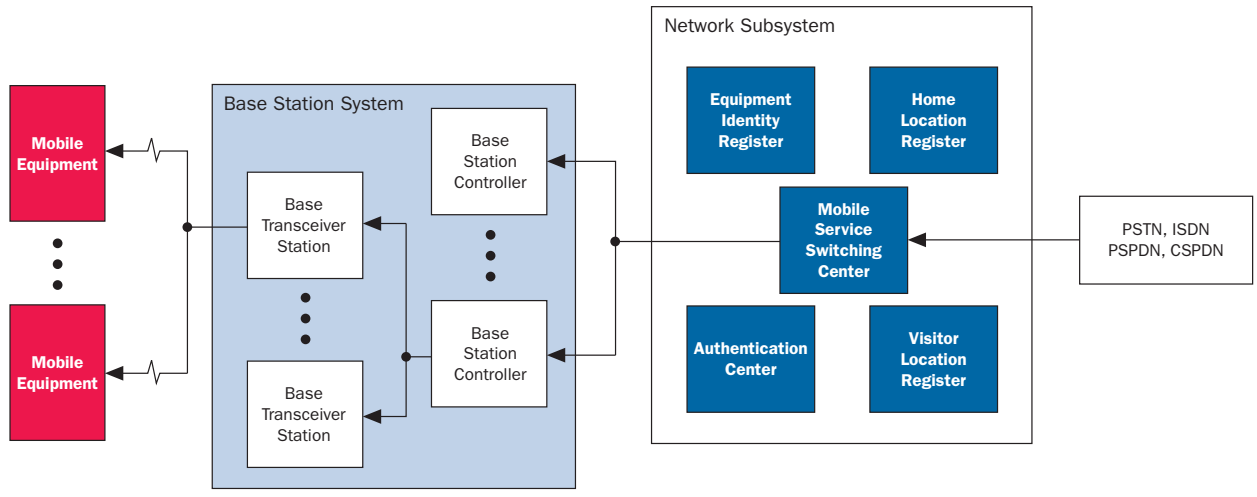
The GSM architecture is composed of three elements: the mobile station, or cellular phone, carried by the subscriber; the base station subsystem, which routes the call; and the network subsystem, which controls the call set up and routing procedures. Figure 1 shows a diagram of the GSM network.

Mobile Station

The mobile station, or cellular phone, contains a "smart card", which carries the subscriber's personal information (i.e., authorization codes, phone settings, and phone number). The unique encryption algorithm contained in every smart card makes it nearly impossible for outsiders to clone phone numbers or eavesdrop on conversations. In addition, because the smart card is removable, users can transfer their personal information to any GSM-compliant phone in the world without worrying about billing mistakes or disrupted phone calls.

When subscribers make phone calls or connections, the mobile station sends data

Figure 1. GSM Network Architecture



through a radio signal to the base station system, where the signal is routed to the proper destination.

Base Station System

The base station system (BSS) routes calls from mobile stations to their appropriate destination and controls the radio link between the mobile station and network subsystem. One component of the BSS, the base transceiver station (BTS), houses the radio reception and transmission equipment for a defined geographical area and is responsible for directing incoming calls. It contains the radio transceiver that specifies a cell (i.e., the geographical area covered by an individual BSS) and handles the radio link protocols with the mobile station. The second component of the BSS, the base station controller (BSC), manages the radio resources for one or more BTSs. The BSC acts as a small switch that controls the system's radio signals. It collects data about the geographical area, controlling the base station's transmission strength and modulating the signal to a wireless frequency for transmission to a cellular phone.

Network System

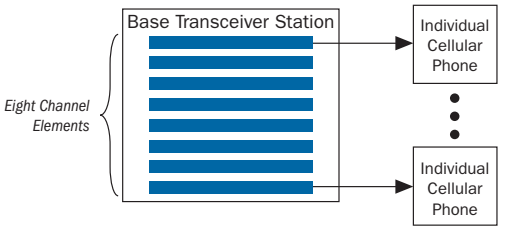
The central part of the network system is the mobile services switching center (MSC), a telephone switching office that processes all calls sent or received by mobile stations. The MSC controls the call setup and routing procedures by functioning as a switching node for the PSTN or ISDN. It also handles different tasks for a mobile subscriber such as registration, authentication, location updating, handovers, and call routing to a roaming subscriber.

CAM

Using APEX 20KE CAM in the BTS can significantly increase a GSM network's performance.

CAM implements channel elements, which support communication between the mobile station and the BTS. Channel elements are defined by frequency and time; each frequency supports communication between the mobile station and the network, with eight repetitive time slot periods. Each slot, or channel, is used for a single mobile station, so eight mobile stations can gain access to the network on the same frequency pair. Figure 2 shows eight slots in a BTS at one specific frequency. CAM aids the BTS with the routing process by sorting information and retrieving addresses for mobile stations in a geographical area at any specific frequency range. Figure 3 shows how the BTS uses CAM to determine a packet's destination.

Figure 2. Eight Channel Elements per Frequency



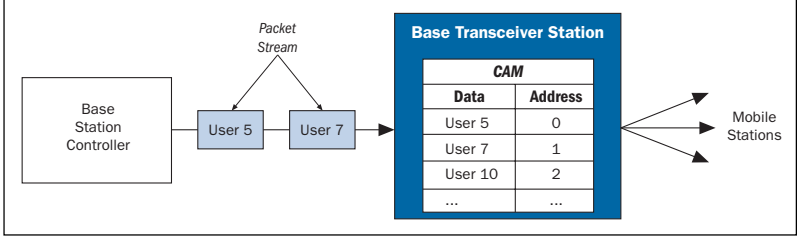
Using embedded CAM in APEX 20KE devices rather than discrete CAM further speeds the GSM network's routing process. Because CAM is embedded inside APEX 20KE devices, it eliminates the on- and off-chip delays associated with discrete CAM. It also cuts design time and reduces the amount of usable printed circuit board (PCB) space by eliminating the need for a second device on the board.

Conclusion

CAM is a fast search tool that can significantly improve the speed of GSM networks. CAM can be used in the BTS of a cell phone base station to route the network packet to its destination quickly.

For more information on APEX 20KE CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM)*.

Figure 3. CAM within the BTS



Packaged Power & the Quartus Design Environment

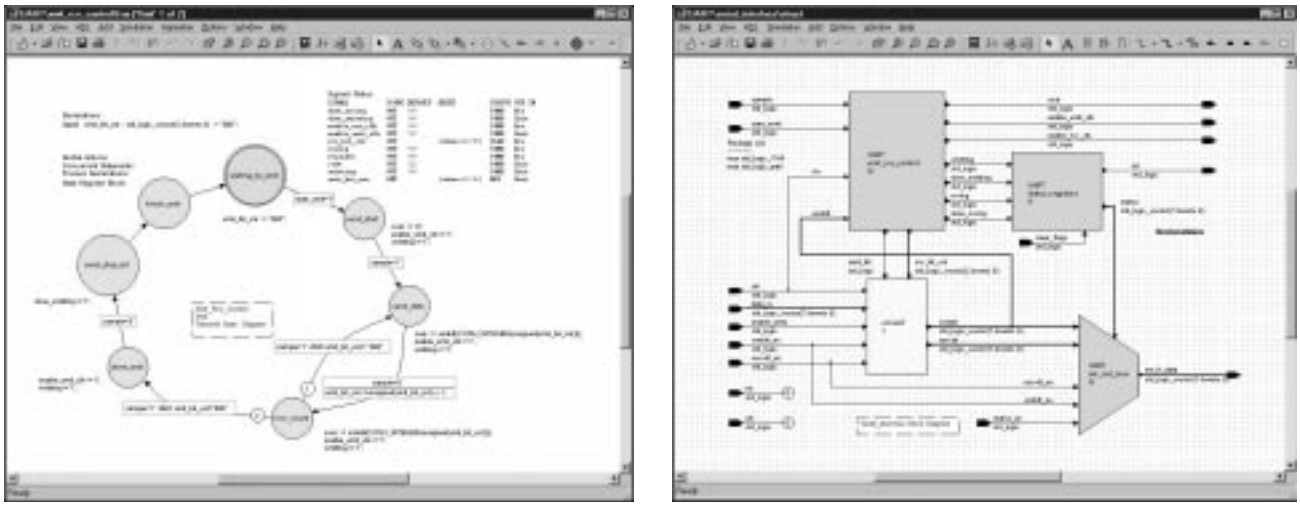
Mentor Graphics' latest product, Packaged Power, gives you the ability to design for APEX™ devices using powerful point tools in an integrated flow. Packaged Power combines three other Mentor Graphics tools in an efficient environment for hardware description language (HDL) design from start to finish: Renoir, for graphical design creation and management; ModelSim, for simulation; and Leonardo Spectrum, for APEX synthesis.

Renoir's Design Browser is the user interface of Packaged Power and the control center where capture, simulation, synthesis, and place-and-route functions are executed. Renoir serves as the starting point for HDL design creation. Mentor Graphics efficiently generates synthesizable HDL code for both novice HDL designers as well as seasoned design engineers. Packaged Power represents code in many different ways, selecting the most logical solution for the project (see Figure 1). For example, block diagrams are valuable for dividing the design into logical partitions, while a flow chart may be more suitable for showing control flow through a process. Each partition in a block diagram could then have its own representation, such as a truth table, a state machine diagram, a flow chart, or another block diagram. Whatever graphical representation you choose, Packaged Power will generate the corresponding HDL code from the graphical object.

In addition to design creation, graphics are beneficial for managing complex designs. Elaborate designs require a team approach where multiple designers work on different areas of the design, or when legacy or intellectual property (IP) code is incorporated into the design. Packaged Power accepts HDL code and imports it into the environment, either maintaining it purely as text or creating a graphical object for that piece of code. Packaged Power also stitches together multiple design blocks from the entire team to formulate the top level of the design.

A single button click initiates the simulation flow, automatically generates any HDL code

Figure 1. Packaged Power Renoir Design Browser



needed from the graphical objects, compiles them, and loads the design into the ModelSim simulator.

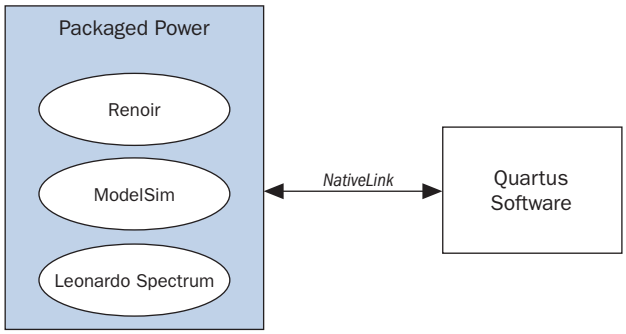
Once the design is loaded into ModelSim, you can take advantage of the enhanced debugging delivered in Packaged Power. Links between the simulation and the graphical objects provide such features as waving and listing from the graphical objects to the ModelSim Wave and List windows, cross referencing between the HDL source code and the original graphical objects, setting graphical and text breakpoints, adding simulation probes to the graphical objects, animating the simulation with color changes, and analyzing the "cause" of a signal transition between the simulation results and the generated graphical object.

Packaged Power provides a streamlined flow to post-route verification and debugging using the Quartus™ NativeLink™ interface (see Figure 2). Routed designs are automatically compiled and loaded into ModelSim by the Quartus software. Timing errors discovered during simulation are quickly traced back to the Quartus Floorplan Editor using integrated cross-probing functionality now available between the ModelSim and Quartus tools.

Once the design is verified at the register transfer level (RTL), the third step is to synthesize and optimize the design for the APEX architecture. The Leonardo Spectrum synthesis flow in the Design Browser automatically generates any HDL source code, if necessary, and loads the design into Leonardo Spectrum to specify design goals and optimize the design. Leonardo Spectrum employs advanced APEX mapping and placement technology to generate the quality results for APEX devices.

Packaged Power also makes it easy to specify synthesis constraints entered directly into Leonardo Spectrum or forward annotated into Leonardo Spectrum from design constraints entered on the graphical objects during design creation. This second approach simplifies the synthesis step by embedding these constraints as part of the design. Regardless of where these synthesis constraints originate, Packaged Power transfers them to Quartus, thus eliminating the need for re-entry (see Figure 2).

Figure 2. NativeLink Feature Connects Packaged Power with the Quartus Software



In the final step, Packaged Power launches the Quartus software, completing the design process by automatically executing place-and-route. The Quartus software can be launched either through the graphical user interface (GUI) or in batch mode. Packaged Power issues a series of Quartus commands to setup, execute, and analyze the device implementation.

After the design is synthesized, cross-referencing extends between Packaged Power and the Quartus software. Block diagrams, state machines, schematics and Quartus place-and-route can all be cross-referenced back to the original RTL source code.

Packaged Power comes in two configurations: Packaged Power Personal and Elite. The Elite version includes the flow chart and truth table editors as well as a revision control environment. Packaged Power is available in multiple configurations for VHDL, Verilog HDL, or mixed-HDL, and for programmable logic devices (PLDs), ASICs, or both. For an evaluation of Packaged Power, visit **http://www.packagedpower.com.**

Mentor Graphics Corporation
8005 SW Boeckman Rd
Wilsonville, OR 97070
(800) 547-3000
http://www.mentorgraphics.com

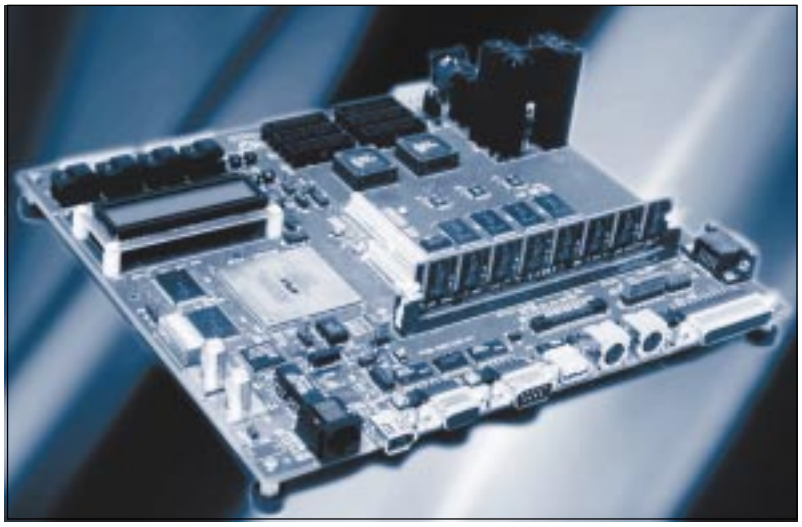
New System-on-a-Programmable-Chip Development Board Aids in Design Verification

The System-on-a-Programmable-Chip Development Board provides you with an off-the-shelf, pre-verified prototype-platform for early hardware and software integration.

A precise and reliable programmable logic device (PLD) design verification solution that also provides an effective debugging platform would help designers speed their products to market. Currently, both software simulation and hardware emulation (e.g., Quickturn) have shortcomings: neither approach reveals real-world device design problems that cause a system to fail. Additionally, software vectors do not expose glitches due to noise or ground bounce conditions. With a reprogrammable PLD-based development board, designers can now address these deficiencies. The new Altera® System-on-a-Programmable-Chip™ Development Board supplements the traditional debug and device verification approaches by providing an off-the-shelf, real-world environment. (See "System-on-a-Programmable-Chip Development Board Features" sidebar on page 31 for more information on this board.)

The Altera System-on-a-Programmable-Chip Development Board (see Figure 1) is a robust benchtop development platform designed for PLD and ASIC designers. This board enables users to implement a complete System-on-a-Programmable-Chip design using intellectual property (IP) functions such as a microprocessor, memory, peripheral devices, and I/O interfaces in an Altera APEX™ device. The board supports microprocessor development by incorporating high performance programmable logic with abundant cache memory and a rich variety of industry-standard I/O interfaces.

Figure 1. System-on-a-Programmable-Chip Development Board



The board allows the designer to vary conditions such as voltage when debugging and testing designs. Designers can also drive signals onto and off of PLDs to gauge performance more accurately and debug logic or memory timing problems.

The most significant advantage of the System-on-a-Programmable-Chip Development Board is that it dramatically cuts development time. The board provides an off-the-shelf, pre-verified prototype-platform for early hardware and software verification. By using a concurrent engineering approach, developers can program the initial design on a real hardware prototype. Traditionally, software engineering delays software execution on hardware until the platform is sufficiently debugged and verified. The System-on-a-Programmable-Chip Development Board delivers the prototype venue at the start of the design cycle, enabling integration of both hardware and software at the earliest possible development phase.

The board features an Altera EP20K400 PLD, which provides 16,640 logic elements (LEs) and over 200,000 bits of RAM. EP20K400 devices are optimal for implementing IP functions from Altera Megafunction Partners Program (AMPP℠) partners such as ARC Cores, Lexra, SICAN Microelectronics, Stargate Solutions, Tensilica, as well as MegaCore™ functions developed by Altera. These MegaCore and AMPP megafunctions are optimized for APEX

devices and the System-on-a-Programmable-Chip Development Board.

The board includes physical interfaces for widely used standard interconnects and a memory subsystem ideal for prototyping embedded systems, providing added flexibility. The board supports interconnect standards such as 10/100 Ethernet, a peripheral mezzanine connector (PMC), universal serial bus (USB), and IEEE Std. 1394A. The System-on-a-Programmable-Chip Development Board also features a memory subsystem, including synchronous SRAM, SDRAM DIMM socket, FLASH, and EPROM capabilities.

Furthermore, the board supports extended Joint Test Action Group (EJTAG) standards for development and debug of microprocessor functions, as well as JTAG. You can use the JTAG port in conjunction with the SignalTap™ embedded logic analyzer within Altera's Quartus™ development software to further examine the internal architecture of a design.

The System-on-a-Programmable-Chip Development Board includes the board, a MasterBlaster™ communications cable, and documentation.

System-on-a-Programmable-Chip Development Board Features

- Includes a 652-pin ball-grid array (BGA) EP20K400 device with 16,640 LEs and 212 Kbytes of device internal RAM
- Supports MegaCore and AMPP IP megafunctions
- 2.5-V and 3.3-V interface levels
- Supports up to six unique, selectable clocks and two configurable clock sources for complex communication system design
- Memory subsystem
  - 2 banks of 1-Mbyte cache memory
  - 64-Mbyte SDRAM in a DIMM socket
  - 4-Mbyte FLASH memory
  - 256-Kbyte EPROM
- On-board elements:
  - Two mezzanine connectors (PMC and custom)
  - LCD display and user definable LEDs
  - Voltage regulator automatically generates 2.5 V and 3.3 V from a 5.0-V power supply
- Features access to APEX SignalTap embedded logic analyzer capability
- Supports in-circuit reconfigurability with an EPC2 configuration device and the MasterBlaster communications cable for APEX devices

Oakland School Receives $20,000 Donation from $20K for APEX 20K Sweepstakes

Carlin Vieri, the winner of this summer's Altera $20K for APEX 20K sweepstakes, recently announced his choice for the recipient of the $20,000 donation: Marshall Elementary School, of the Oakland Unified School District in California. Considerable thought and effort went into Mr. Vieri's decision; he wanted the donation to have an immediate and long-term impact. After researching the California Board of Education web site, Mr. Vieri cross-referenced lists that rank school performances to find a school that needed assistance in the area of math, science, and technology. He eventually decided on the Marshall Elementary School. The school plans to use the funding to buy Apple iMac computers. Not only will the school receive a much-needed computer lab, its present and future students will be able to learn valuable computing and typing skills.

Carlin Vieri is a design engineer for the MicroDisplay Corporation. MicroDisplay produces small grayscale and color display screens for use in cellular phones, cameras, and other electronic devices. The screens use EPF10K50E devices for their memory interface, video decoding, and driver electronics.

In addition to the $20,000 donation, Mr. Vieri was presented with a Palm VII organizer for his own use.

Full Hot-Swap CompactPCI Applications Design with Altera Devices

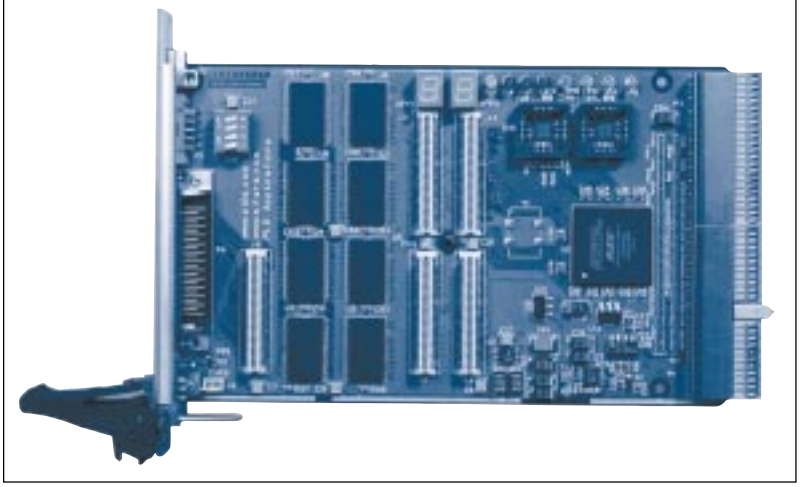
PLD Applications, a peripheral component interconnect (PCI) solutions company, recently released their new prototyping and production CPCI10K-PROD board, the programmable logic device (PLD) industry's first full hot-swap CompactPCI board (see Figure 1). In the past, boards designed with hot-swap capabilities required extensive board and PLD design, as well as significant funding for testing equipment or services. The CPCI10K-PROD prototyping board bypasses all those barriers and is used as a 5.0- or 3.3-V, 32- or 64-bit, 33- or 66-MHz CompactPCI development board, CompactPCI bus analyzer, data acquisition board, or full hot-swap CompactPCI design platform.

CompactPCI Boards

The use of CompactPCI development boards, which follow the industrial PCI board form factor, has expanded in the last few years. CompactPCI boards are increasingly used in telecommunications, where reliability, serviceability, and repair time are critical.

The CPCI10K-PROD board can be used either as a production platform or a prototyping board (design platform) to develop back-end applications. A designer has the control/command function as well as the ability to acquire and process data; daughter boards are available to extend the capabilities of the CPCI10K-PROD board. These daughter boards include an APEX™-based PLD Applications board that allows you to test your APEX designs before programming your device. Additionally, PLD Applications can design a custom daughter board to meet user demands.

Figure 1. CPCI10K-PROD Board



The CPCI10K-PROD board features include:

- CompactPCI function optimized for APEX and FLEX® devices
- 32- or 64-bit, 33-MHz PCI compliance
- 3U or 6U form factor
- Full hot-swap capability
- Accepts daughter boards for any additional analog-to-digital or digital-to-analog custom processing functions
- Device configuration via two chained EPC2 configuration devices or an Altera® BitBlaster™ or ByteBlasterMV™ download cable

About Hot-Swap

The CPCI10K-PROD board is an effective tool because it has a simple physical connection process (via the front panel of the CompactPCI chassis) as well as the hot-swap capability, which allows you to insert or extract these boards into or out of a live system. With full hot-swap, the user can insert or extract a board while the system is running, and the system manages it automatically. This capability simplifies the design process and shortens design times.

The designer does not need to power down or alert the system before removing a full hot-swap capable board. Per the CompactPCI standard, a blue LED and a microswitch inside the handle aid in the hot-swapping function of the CPCI10K-PROD board. The blue LED indicates whether the board is configured or unconfigured. The light is off when the board is connected to the system and configured. When the CPCI10K-PROD board is unconfigured, the

blue LED lights up, and you can remove the board without damaging any of the devices.

Designing for Hot-Swapping at the Board Level

Although the hot-swap concept is simple to grasp, it is difficult to implement. Many PLD and chipset vendors have released a CompactPCI demo kit, but none are full hot-swap capable. The CPCI10K-PROD board is not a demo kit, but a real development platform with full hot-swap capablities. To be considered fully hot-swap capable, a board must conform to the following specifications:

- CompactPCI bus loading:
  - A 10-Ω stub resistor between the connector and the PCI-compliant device (FLEX or APEX device), with a maximum trace length of 2.5 inches (63.5 mm)
  - A large resistor (10K Ω minimum) tied to a bias voltage source (1.0 V ±20%, or, for certain signals, 0 V or 3.3 V)
  - Precharge bias voltage source used during board insertion and extraction charges the on-board network to within 80% of the nominal 1.0-V precharge voltage within 5 µs
- Other electrical requirements include:
  - Maximum trace length of 2.5 inches (63.5 mm)
  - Management of the early-power plane and back-end power plane
    - Early-power plane supplies all the CompactPCI side components (FLEX, APEX, and EPC2 devices, supply manager)
    - Dedicated component handles supply management and power isolation; this component drives the back-end power plane and the powergood signal (powergood signal indicates to the system that the back-end power is in the required tolerance)
- Management of all CompactPCI signals' high impedance during extraction and insertion

The CPCI10K-PROD board simplifies the hot-swap process by incorporating the necessary design elements into the board (see Figure 2).

Hot-Swapping Options

To meet the hot-swap specifications, designers can implement the PLD Applications PCI/CompactPCI function in APEX 20K, FLEX 10K, or FLEX 6000 devices. The CPCI10K-PROD board offers designers three different options for their PLD design:

- A fully customized printed circuit board (PCB) from PLD Applications
- A custom daughter card for the specific portion of the design (PCB and VHDL back-end application), plugged into the CPCI10K-PROD board
- A whole project (custom PCB and VHDL back-end application) using PLD Applications' CompactPCI function as an interface to build for CompactPCI and full hot-swap

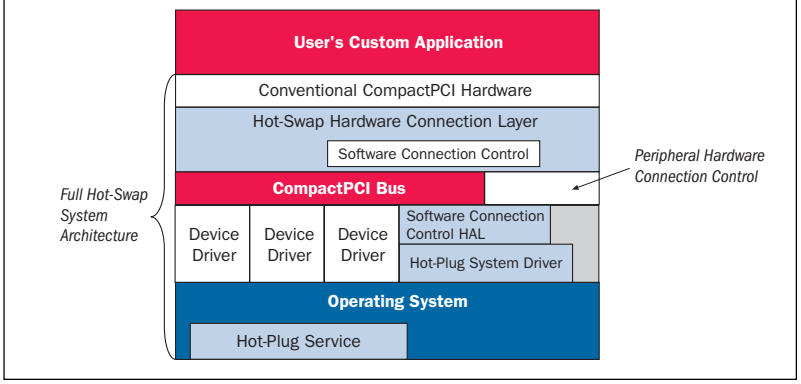
A daughter board system makes the CPCI10K-PROD board fully customizable. PLD Applications' basic daughter board is the first design that allows you to test the powerful target or master/target, 33-MHz, 32- or 64-bit PLD Application PCI functions. This board performs real-time data acquisition, control/command, and other critical system functions.

Conclusion

Designing a full hot-swap capable CompactPCI board requires significant design expertise at both the logic and board level. A company must make a costly investment in either testing equipment or services to verify that their board meets all the hot-swap requirements. PLD Applications developed this production-ready solution to remove the barriers to entry for designers using Altera devices.

PLD Applications
32, ZAC de Bompertuis
Avenue d'Armenie
13120 Gardanne
France
(33) 0 442 654 388
http://www.plda.com

Figure 2. CPCI10K-PROD Architecture



GOEPEL electronic Announces the First Jam STAPL Tools

GOEPEL has expanded the SYSTEM CASCON software in version 3.32 to support the Jam Standard Test and Programming Language (STAPL).

GOEPEL electronic, a leading manufacturer of IEEE Std. 1149.1-compliant BST systems, integrated the Jam Player into previous versions of its SYSTEM CASCON software, making it a proficient in-system programming tool. Now, GOEPEL has expanded the SYSTEM CASCON software in version 3.32 to support the Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71. Jam STAPL provides added performance and programming efficiency via the IEEE Std. 1149.1 Joint Test Action Group (JTAG) port to the SYSTEM CASCON software (see Figure 1).

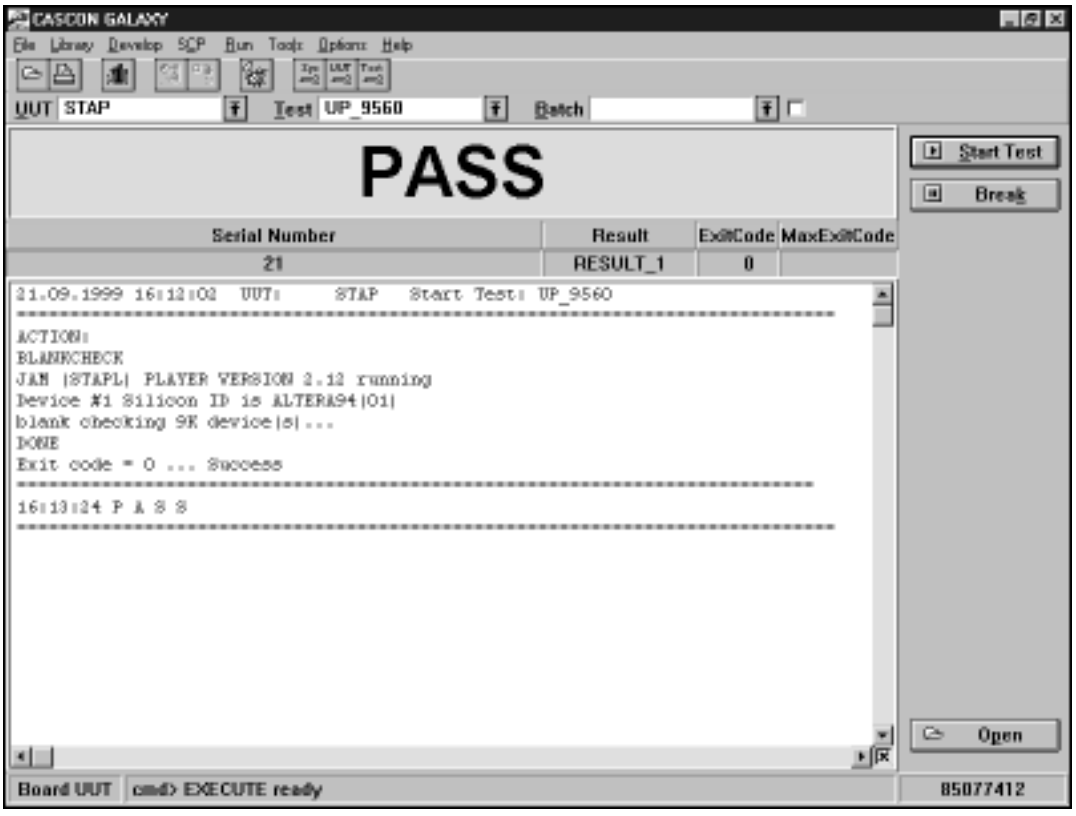
SYSTEM CASCON Software

SYSTEM CASCON, an industry-approved boundary-scan test (BST), verification, and programming software, is available as a complete testing solution or in specialized development, test, and repair packages. SYSTEM CASCON can be combined with any of GOEPEL electronic's testing hardware to offer a comprehensive laboratory, production, or service testing system.

Standardized Programming Languages Necessary

In recent years, more and more programmable logic devices (PLDs) programmed via the BST interface are integrated into complex designs to be functional and reduce manufacturing and service costs. However, many device suppliers defined their own programming interfaces, making it difficult for designers to become accustomed to one language. This problem led the PLD industry to develop formats such as the Serial Vector Format (SVF) and the Jam language, programming languages widely

Figure 1. Programming an EPM9560RC304 Device with Jam STAPL



accepted because of their vendor- and platform-independence.

Taking this idea of a standardized programming language one step further, Jam STAPL became JEDEC standard JESD-71 in May 1999, and is the first industrial standard for the in-system programming of PLDs via the IEEE Std. 1149.1 JTAG BST interface. In addition to being a standard, Jam STAPL creates programming files that are substantially smaller than files created with other programming languages. Unlike programming formats such as SVF, Jam STAPL is a comprehensive language that allows algorithmic programming based on high-level commands.

SYSTEM CASCON Easily Compatible with Jam STAPL

GOEPEL electronic is the first in-circuit tester vendor to integrate Jam STAPL support in its software. The SYSTEM CASCON software version 3.32 continues to support SVF and earlier versions of Jam formats in addition to Jam STAPL. Earlier versions of the Jam language developed by Altera are the fundamental basis for the creation of this vendor- and platform-independent, language-based programming solution.

The SYSTEM CASCON software automatically detects whether Jam STAPL or an earlier Jam format is used. Other devices included in the scanpath are handled automatically by the software as well; you do not need to manually modify the data. The SYSTEM CASCON software can manage testbus handlers such as Scanpath Linker ACT8997 from Texas Instruments or National Semiconductor's SCAN Bridge for hierarchical testing on the board and system level.

Conclusion

SYSTEM CASCON is available either as a complete testing solution or in specialized development, test, and repair packages. GOEPEL electronic's software is ideal for comprehensive laboratory, production, or service testing. By integrating Jam STAPL into its SYSTEM CASCON software, GOEPEL provides designers a simple, efficient way to program their devices in-system.

Superior Programming Times Using Jam STAPL & CASCON-GALAXY

Programming and re-programming PLDs mounted on a printed circuit board (PCB) in-system is essential for shorter time to market. CASCON-GALAXY, the high-end package of GOEPEL electronic's SYSTEM CASCON, combines testing and programming into one program execution. Tables 1 and 2 list programming times for Altera devices using various data formats. The devices are programmed with the same functional behavior to make programming times comparable. The scanpath contains Altera EPM9320RC208, EPM9560RC304, and EPM7192SQC160 devices operated at a t_{CK} frequency of 5 MHz. The tests were performed on a 200-MHz Pentium processor PC running the Windows NT operating system with a PCI bus boundary-scan controller PSC 1149.1-A.

Table 1. Programming & Verification Times with DOS

Device	Jam 1.1 (seconds)		Jam Byte-Code (seconds)		Jam STAPL (seconds)	
	Program	Verify	Program	Verify	Program	Verify
EPM7192SQC160	10	16	8	9	13	13
EPM9320RC208	17	48	10	26	14	23

Table 2. Programming Times with Windows NT

Device	Jam 1.1 (seconds)	Jam Byte-Code (seconds)	Jam STAPL (seconds)
EPM7192SQC160	7	7	9
EPM9320RC208	13	12	18

There are no significant differences between using either the DOS or Windows NT operating systems. However, devices were programmed much faster with Jam Byte-Code because ASCII information does not need to be interpreted. Other factors that influenced programming times are wait cycles and shifting cycles.

GOEPEL electronic GmbH
Goeschwitzer Str. 58/60
D-07745 Jena/Germany
(49) 3641-6896-63
http://www.goepel.com

Questions & Answers

Q *How can I zoom in and print a portion of a Graphic Design File (.gdf) in the MAX+PLUS® II Graphic Editor?*

A To print a selected area in the Graphic Editor, open the GDF in Graphic Editor mode and then follow the steps below.

1. Make sure that the arrow pointer icon is enabled on the Graphic Editor tool bar.
2. Capture the area you wish to print by left-clicking and dragging the mouse over the appropriate portion of the design.
3. Select **Print** (File menu).
4. Click on **Selected Area** and then **OK**.

Q *Which Altera® devices feature phase-locked loops (PLLs)?*

A All Altera devices with an "X" suffix at the end of the device ordering code contain ClockLock™ and ClockBoost™ circuitry, which includes one or more PLLs. APEX™ 20KE devices add the ClockShift™ capability to these two features and provide additional PLL enhancements. Current Altera devices featuring PLLs include APEX 20K, APEX 20KE, FLEX® 10KE, and FLEX 10K devices.

All Altera devices with an "X" suffix at the end of the device ordering code contain ClockLock and ClockBoost circuitry, which includes one or more PLLs.

Additionally, the EPF10K100 device features a "DX" suffix rather than the single "X" character.

For additional information regarding the PLL capabilities of these devices, see their respective data sheets, available on the Altera web site (**http://www.altera.com**).

Q *Can I configure an APEX 20K or FLEX 10K device with an EPC1064 or EPC1213 configuration device?*

A You cannot configure an APEX 20K or FLEX 10K device with an EPC1064 or EPC1213 configuration device for the following reasons:

- The EPC1064 and EPC1213 configuration devices do not have an on-chip oscillator, which is present in the EPC1, EPC1441, and EPC2 devices.
- The EPC1064 and EPC1213 configuration devices do not have a program length counter; EPC1, EPC1441, and EPC2 devices have this counter. The program length counter tells the device how long the programming file is, so it knows when it should receive a high signal on the `conf_done` pin. The program length counter allows for error detection during configuration. FLEX 8000, EPC1, EPC1441, and EPC2 devices have a program length counter; APEX 20K, FLEX 10K, FLEX 6000, EPC1064, and EPC1213 devices do not.

  Moving the program length counter and the oscillator into EPC1, EPC1441, and EPC2 configuration devices gives them full control over the configuration process.

Q *Why doesn't my* `lpm_fifo` *or* `scfifo` *fit in a FLEX 10K, FLEX 10KA, or EPF10K100B device?*

A Single clock first-in first-out (FIFO) buffers (`lpm_fifo` and `scfifo`) are implemented using interleaved memory in FLEX 10K, FLEX 10KA, and EPF10K100B devices. Each eight bits of FIFO width requires two embedded array blocks (EABs) to be implemented. Therefore, it is possible that, due to the width, the FIFO requires more EABs than are available in the chosen device.

One example is a 256 × 24 FIFO function targeted for an EPF10K10 device. An EPF10K10 device has three EABs; however, this FIFO function requires six EABs because its width is 24 bits.

The main purpose of using interleaved memory is to support simultaneous reads and writes. If simultaneous reads and writes are not required by the design, an arbitrated FIFO function would be an appropriate solution.

APEX 20K and FLEX 10KE devices contain dual-port RAM, which allows 8-bit FIFO functions to be implemented in one EAB.

Altera Programming Support

Programming Hardware Support

Table 1 contains the latest programming hardware information for Altera® MAX® 9000, MAX 7000, MAX 3000, and configuration devices. For correct programming, use the software version shown in "Current Software Versions" on page 6.

Table 1. Altera Programming Adapters (Part 1 of 3) *Note (1)*

Device	Package	Adapter
EPC1064 *(2)* EPC1064V *(2)* EPC1441 *(3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 *(3)* EPC1213 *(2)*	DIP, J-lead	PLMJ1213
EPC2 *(4)*	J-lead TQFP	PLMJ1213 PLMT1064
EPM9320	J-lead (84-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9000-208 PLMG9000-280
EPM9320A	J-lead (84-pin) RQFP (208-pin)	PLMJ9320-84 PLMR9000-208NC *(5)*
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304
EPM9560A	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208NC *(5)* PLMR9000-240NC *(5)*
EPM7032	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7032S EPM7032AE EPM7032B	J-lead (44-pin) TQFP (44-pin)	PLMJ7000-44 PLMT7000-44
EPM7064	J-lead (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100

Table 1. Altera Programming Adapters (Part 2 of 3) *Note (1)*

Device	Package	Adapter
EPM7064S	J-lead (44-pin) J-lead (84-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ7000-44 PLMJ7000-84 PLMT7000-44 PLMT7000-100NC *(5)*
EPM7064AE EPM7064B	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin) FineLine BGA (100-pin)	PLMJ7000-44 PLMT7000-44 PLMT7000-100NC *(5)* PLMF7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7128A EPM7128AE	J-lead (84-pin) TQFP (100-pin) TQFP (144-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMJ7000-84 PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMF7000-100 PLMF7000-256
EPM7128B	TQFP (100-pin) TQFP (144-pin) FineLine BGA (100-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMF7000-100 PLMF7000-256
EPM7128S	J-lead (84-pin) PQFP (100-pin) TQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMT7000-100NC *(5)* PLMQ7128/7160-160NC *(5)*
EPM7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160S	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100NC *(5)* PLMQ7128/7160-160NC *(5)*
EPM7192E	PGA (160-pin) PQFP (160-pin)	PLMG7192-160 PLMQ7192/7256-160
EPM7192S	PQFP (160-pin)	PLMQ7192/7256-160NC *(5)*

continued on page 38

Altera Programming Support, continued from page 37

Table 1. Altera Programming Adapters (Part 3 of 3) *Note (1)*

Device	Package	Adapter
EPM7256E	PQFP (160-pin) PGA (192-pin) PQFP (208-pin) RQFP (208-pin)	PLMQ7192/7256-160 PLMG7256-192 PLMR7256-208 PLMR7256-208
EPM7256A	TQFP (100-pin) TQFP (144-pin) PQFP (208-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMF7000-256
EPM7256S	PQFP (208-pin) RQFP (208-pin)	PLMR7256-208NC *(5)* PLMT7256-208NC *(5)*
EPM7256AE EPM7256B	TQFP (100-pin) FineLine BGA (100-pin) TQFP (144-pin) FineLine BGA (256-pin)	PLMT7000-100NC *(5)* PLMF7000-100 PLMT7000-144NC *(5)* PLMF7000-256
EPM7512AE EPM7512B	TQFP (144-pin) PQFP (208-pin) BGA (256-pin) FineLine BGA (256-pin)	PLMT7000-144NC *(5)* PLMR7256-208NC *(5)* PLMB7000-256 PLMF7000-256
EPM3032A	J-lead (44-pin) TQFP (44-pin)	PLMJ3000-44 PLMT3000-44
EPM3064A	J-lead (44-pin) TQFP (44-pin) TQFP (100-pin)	PLMJ3000-44 PLMT3000-44 PLMT3000-100NC *(5)*
EPM3128A	TQFP (100-pin) TQFP (144-pin)	PLMT3000-100NC *(5)* PLMT3000-144NC *(5)*
EPM3256A	TQFP (144-pin) PQFP (208-pin)	PLMT3000-144NC *(5)* PLMR3256-208NC *(5)*

Notes:

(1) Refer to the *Altera Programming Hardware Data Sheet* for device adapter information on Classic™ devices.
(2) FLEX® 8000 configuration device.
(3) FLEX 10K, FLEX 8000, or FLEX 6000 configuration device.
(4) APEX 20K, FLEX 10K, or FLEX 6000 configuration device.
(5) These devices are not shipped in carriers.

Third-Party Programming Support

Data I/O and BP Microsystems provide programming hardware support for selected Altera devices. Algorithms are supplied via Data I/O's Keep Current Express-Bulletin Board Service (KCE-BBS) and BP Microsystems' BBS. Programming support information for configuration, MAX 9000, and MAX 7000 devices is shown in Table 2. All information is subject to change.

Table 2. Third-Party Programming Hardware Support

Device	Data I/O *(1)*	BP Microsystems *(2)*
EPC1064	✓	✓
EPC1213	✓	✓
EPC1	✓	✓
EPC1441	✓	✓
EPC2	*(3)*	✓
EPM3032A	*(3)*	*(3)*
EPM3064A	*(3)*	*(3)*
EPM3128A	*(3)*	*(3)*
EPM3256A	*(3)*	*(3)*
EPM7032	✓	✓
EPM7032AE	*(3)*	✓
EPM7032S	✓	✓
EPM7064	✓	✓
EPM7064AE	✓	✓
EPM7064S	✓	✓
EPM7096	✓	✓
EPM7128A	✓	✓
EPM7128S	✓	✓
EPM7128AE	*(3)*	✓
EPM7128E	✓	✓
EPM7160E	✓	✓
EPM7192S	✓	✓
EPM7192E	✓	✓
EPM7256A	*(3)*	✓
EPM7256AE	*(3)*	*(3)*
EPM7256S	✓	✓
EPM7256E	✓	✓
EPM7512AE	*(3)*	✓ *(4)*
EPM9320	✓	✓
EPM9320A	✓	✓
EPM9400	✓	✓
EPM9480	✓	✓
EPM9560	✓	✓
EPM9560A	✓	✓

Notes to Table 2:
(1) These devices are supported by the Data I/O UniSite programmer version 6.1.
(2) These devices are supported by BP Microsystems programmers version 3.44.
(3) Contact Data I/O or BP Microsystems about programming support for these devices.
(4) Contact Data I/O or BP Microsystems about programming support for 256-pin ball-grid array (BGA) and FineLine BGA™ packages.

Download Cables

Table 3 provides programming and configuration compatibility information for the MasterBlaster™ serial or universal serial bus (USB) communications cable and the BitBlaster™ serial and ByteBlasterMV™ parallel port download cables. (The ByteBlaster™ download cable has been replaced with the ByteBlasterMV cable.)

Table 3. Download Cable Compatibility

Device	MasterBlaster *(1)*	ByteBlasterMV	BitBlaster *(2)*
APEX 20K	✓	✓ *(3)*	
APEX 20KE	✓	✓ *(3)*	
FLEX 10K	✓	✓	✓
FLEX 10KA	✓	✓	✓
FLEX 10KE	✓	✓	✓
FLEX 8000	✓	✓	✓
FLEX 6000	✓	✓	✓
MAX 9000	✓	✓	✓
MAX 9000A	✓	✓	✓
MAX 7000S	✓	✓	✓
MAX 7000A	✓	✓	✓
MAX 7000B	✓	✓ *(3)*	
MAX 3000	✓	✓	✓

Notes:
(1) The MasterBlaster communications cable can be used with the Quartus software for device download and SignalTap logic analysis. It can also be used with the MAX+PLUS II software version 9.3 for device downloads.
(2) The BitBlaster download cable must operate at 5.0 V.
(3) The ByteBlasterMV download cable must operate at 3.3 V for these devices. `VCCIO` pins can be set to either 2.5 V or 3.3 V.

How to Contact Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera.

Information Type	Access	U.S. & Canada	All Other Locations
Literature *(1)*	Altera Literature Services	(888) 3-ALTERA **lit_req@altera.com**	(408) 544-7144 *(2)* **lit_req@altera.com**
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 544-7000
	Fax	(408) 544-6403	(408) 544-6403
Technical Support	Telephone Hotline (6 a.m. to 6 p.m. Pacific Time)	(800) 800-EPLD (408) 544-7000	(408) 544-7000 *(2)*
	Fax	(408) 544-6401	(408) 544-6401 *(2)*
	Electronic Mail	**sos@altera.com**	**sos@altera.com**
	FTP Site	**ftp.altera.com**	**ftp.altera.com**
General Product Information	Telephone	(408) 544-7104	(408) 544-7104 *(2)*
	World-Wide Web	**http://www.altera.com** **https://websupport.altera.com**	**http://www.altera.com** **https://websupport.altera.com**

Notes:
(1) The *MAX+PLUS II Getting Started* and *Quartus Tutorial* manuals are available from the Altera web site. To obtain other Quartus™ and MAX+PLUS® II software manuals, contact your local distributor.
(2) You can also contact your local Altera sales office or sales representative. See the Altera web site for a listing.

Discontinued Devices Update

Altera has no new announcements regarding discontinued devices. Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera® sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's web site at **http://www.altera.com**.

Rochester Electronics, an after-market supplier, offers many discontinued Altera products. Contact Rochester Electronics at (978) 462-9332 or go to their web site at **http://www.rocelec.com**.

Altera Device Selection Guide

Current information for the Altera® APEX™ 20K, FLEX® 10K, FLEX 8000, FLEX 6000, MAX® 9000, MAX 7000, MAX 3000, and configuration devices is listed here. Information on other Altera products is located in the Altera *Component Selector Guide*.

For the most up-to-date information, go to the Altera web site at **http://www.altera.com**. Some of the devices listed may not yet be available. Contact Altera or your local sales office for the latest device availability.

APEX 20K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS[1]	I/O PINS[1]	SUPPLY VOLTAGE	LOGIC ELEMENTS	RAM BITS	MACROCELLS
EP20K60E	60,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 108, 151, 183, 204, 204	1.8 V	2,560	32,768	256
EP20K100	100,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	101, 108, 159, 189, 252, 252	2.5 V	4,160	53,248	416
EP20K100E	100,000	144-Pin TQFP, 144-Pin BGA[2], 208-Pin PQFP, 240-Pin PQFP, 324-Pin BGA[2], 356-Pin BGA	92, 108, 151, 183, 246, 246	1.8 V	4,160	53,248	416
EP20K160E	160,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2]	87, 143, 175, 273, 316	1.8 V	6,400	81,920	640
EP20K200	200,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[2]	144, 174, 279, 382	2.5 V	8,320	106,496	832
EP20K200E	200,000	208-Pin PQFP, 240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[2], 652-Pin BGA, 672-Pin BGA[2]	136, 168, 273, 376, 376, 376	1.8 V	8,320	106,496	832
EP20K300E	300,000	208-Pin RQFP, 240-Pin RQFP, 652-Pin BGA, 672-Pin BGA[2]	120, 152, 408, 408	1.8 V	11,520	147,456	1,152
EP20K400	400,000	652-Pin BGA, 655-Pin PGA, 672-Pin BGA[2]	502, 502, 502	2.5 V	16,640	212,992	1,664
EP20K400E	400,000	652-Pin BGA, 672-Pin BGA[2]	488, 488	1.8 V	16,640	212,992	1,664
EP20K600E	600,000	652-Pin BGA, 672-Pin BGA[2], 1,020-Pin BGA[2]	488, 483, 624	1.8 V	24,320	311,296	2,432
EP20K1000E	1,000,000	652-Pin BGA, 672-Pin BGA[2], 984-Pin PGA, 1,020-Pin BGA[2]	488, 483, 716, 716	1.8 V	38,400	327,680	2,560
EP20K1500E	1,500,000	652-Pin BGA, 984-Pin BGA[2], 1,020-Pin BGA[2]	488, 858, 858	1.8 V	51,840	442,368	3,456

Notes:
(1) Preliminary. Contact Altera for latest information.
(2) This package is a space-saving FineLine BGA package.

FLEX 10K Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	LOGIC ELEMENTS	RAM BITS
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	5.0 V	-3, -4	576	6,144
EPF10K10A	10,000	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	66, 102, 134, 150	3.3 V	-1, -2, -3	576	6,144
EPF10K20	20,000	144-Pin TQFP, 208-Pin RQFP, 240-Pin RQFP	102, 147, 189	5.0 V	-3, -4	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	5.0 V	-3, -4	1,728	12,288
EPF10K30A	30,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 246, 246	3.3 V	-1, -2, -3	1,728	12,288
EPF10K30E	30,000	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 176, 220	2.5 V	-1, -2, -3	1,728	24,576
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	5.0 V	-3, -4	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	5.0 V	-3, -4	2,880	20,480
EPF10K50V	50,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1]	189, 274, 291	3.3 V	-1, -2, -3, -4	2,880	20,480
EPF10K50E	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 484-Pin BGA[1]	102, 147, 189, 191, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K50S	50,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	102, 147, 189, 191, 220, 254	2.5 V	-1, -2, -3	2,880	40,960
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	5.0 V	-2, -3, -4	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	5.0 V	-3, -4	4,992	24,576
EPF10K100A	100,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA	189, 274, 369, 406	3.3 V	-1, -2, -3	4,992	24,576
EPF10K100B	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1]	147, 189, 191	2.5 V	-1, -2, -3	4,992	24,576
EPF10K100E	100,000	208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA[1], 356-Pin BGA, 484-Pin BGA[1]	147, 189, 191, 274, 338	2.5 V	-1, -2, -3	4,992	49,152
EPF10K130V	130,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-2, -3, -4	6,656	32,768
EPF10K130E	130,000	240-Pin PQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA 672-Pin BGA[1]	186, 274, 369, 424, 413	2.5 V	-1, -2, -3	6,656	65,536
EPF10K200E	200,000	599-Pin PGA, 600-Pin BGA, 672-Pin BGA[1]	470, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K200S	200,000	240-Pin RQFP, 356-Pin BGA, 484-Pin BGA[1], 600-Pin BGA, 672-Pin BGA[1]	182, 274, 369, 470, 470	2.5 V	-1, -2, -3	9,984	98,304
EPF10K250A	250,000	599-Pin PGA, 600-Pin BGA	470, 470	3.3 V	-1, -2, -3	12,160	40,960

FLEX 6000 Devices

DEVICE	GATES	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE	FLIP-FLOPS	LOGIC ELEMENTS
EPF6010A	10,000	100-Pin TQFP, 144-Pin TQFP	71, 102	3.3 V	-1, -2, -3	880	880
EPF6016	16,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA	117, 171, 199, 204	5.0 V	-2, -3	1,320	1,320
EPF6016A	16,000	100-Pin TQFP, 100-Pin BGA[1], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[1]	81, 81, 117, 171, 171	3.3 V	-1, -2, -3	1,320	1,320
EPF6024A	24,000	144-Pin TQFP, 208-Pin PQFP, 240-Pin PQFP, 256-Pin BGA, 256-Pin BGA[1]	117, 171, 199, 218, 218	3.3 V	-1, -2, -3	1,960	1,960

Configuration Devices for APEX & FLEX Devices

DEVICE	PIN/PACKAGE OPTIONS	SUPPLY VOLTAGE	DESCRIPTION
EPC1064	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	5.0 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1064V	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3 V	64-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1213	8-Pin PDIP, 20-Pin PLCC	5.0 V	213-Kbit serial configuration device designed to configure FLEX 8000 devices
EPC1441[1]	8-Pin PDIP, 20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	441-Kbit serial configuration device designed to configure all FLEX devices
EPC1[1]	8-Pin PDIP, 20-Pin PLCC	3.3/5.0 V	1-Mbit serial configuration device designed to configure all APEX and FLEX devices
EPC2[1]	20-Pin PLCC, 32-Pin TQFP	3.3/5.0 V	2-Mbit serial configuration device designed to configure all APEX, FLEX 10K, FLEX 10KE, and FLEX 6000 devices

Notes to Tables:

(1) This package is a space-saving FineLine BGA package.

(2) This device can be programmed by the user to operate at either 3.3 V or 5.0 V.

continued on page 42

Altera Device Selection Guide, continued from page 41

MAX 9000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM9320A	320	84-Pin PLCC, 208-Pin RQFP, 356-Pin BGA	60, 132, 168	5.0 V	-10
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA, 356-Pin BGA	60, 132, 168	5.0 V	-15, -20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	5.0 V	-15, -20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	5.0 V	-15, -20
EPM9560A	560	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-10
EPM9560	560	208-Pin RQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP, 356-Pin BGA	153, 191, 216	5.0 V	-15, -20

MAX 7000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM7032S	32	44-Pin PLCC/TQFP	36	5.0 V	-5, -6, -7, -10
EPM7032AE	32	44-Pin PLCC/TQFP	36	3.3 V	-4, -7, -10
EPM7032B	32	44-Pin PLCC/TQFP, 48-Pin TQFP, 49-pin BGA[1]	36, 36, 36	2.5 V	-3, -5, -7
EPM7064S	64	44-Pin PLCC/TQFP, 84-Pin PLCC, 100-Pin TQFP	36, 52, 68, 68	5.0 V	-5, -6, -7, -10
EPM7064AE	64	44-Pin PLCC/TQFP, 49-Pin BGA[1], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68	3.3 V	-4, -7, -10
EPM7064B	64	44-Pin PLCC/TQFP, 48-pin TQFP, 49-Pin BGA[1], 100-Pin TQFP, 100-Pin BGA[2]	38, 40, 40, 68, 68	2.5 V	-3, -5, -7
EPM7128S	128	84-Pin PLCC, 100-Pin PQFP/TQFP, 160-Pin PQFP	68, 84, 100	5.0 V	-6, -7, -10, -15
EPM7128A	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 256-Pin BGA[2]	68, 84, 84, 100, 100	3.3 V	-6, -7, -10, -12
EPM7128AE	128	84-Pin PLCC, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[1], 256-Pin BGA[2]	68, 84, 84, 100, 100, 100	3.3 V	-5,-7,-10
EPM7128B	128	44-Pin PLCC/TQFP, 48-pin TQFP, 100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 169-Pin BGA[1], 256-Pin BGA[2], 256-Pin BGA	36, 40, 84, 84, 100, 100, 100, 100	2.5 V	-4, -7, -10
EPM7160S	160	84-Pin PLCC, 100-Pin TQFP, 160-Pin PQFP	64, 84, 104	5.0 V	-7, -10, -15
EPM7192S	192	160-Pin PQFP	124	5.0 V	-7, -10, -15
EPM7256S	256	208-Pin PQFP	164	5.0 V	-7, -10, -15
EPM7256A	256	100-Pin TQFP, 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 120, 164, 164	3.3 V	-7, -10, -12
EPM7256AE	256	100-Pin TQFP, 100-Pin BGA[2], 144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2]	84, 84, 120, 164, 164	3.3 V	-5, -7, -10
EPM7256B	256	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[1], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 164, 164, 164	2.5 V	-5, -7, -10
EPM7512AE	512	144-Pin TQFP, 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	120, 176, 212, 212	3.3 V	-7, -10, -12
EPM7512B	512	100-Pin TQFP, 144-Pin TQFP, 169-Pin BGA[1], 208-Pin PQFP, 256-Pin BGA[2], 256-Pin BGA	84, 120, 140, 212, 212, 212	2.5 V	-6, -7, -10

Notes:
(1) This package is a space-saving Ultra FineLine BGA package, Altera's newest 0.8-mm BGA package.
(2) This package is a space-saving FineLine BGA package.

MAX 3000 Devices

DEVICE	MACROCELLS	PIN/PACKAGE OPTIONS	I/O PINS	SUPPLY VOLTAGE	SPEED GRADE
EPM3032A	32	44-pin PLCC, 44-pin TQFP	34, 34	3.3 V	-4, -7, -10
EPM3064A	64	44-pin PLCC, 44-pin TQFP, 100-pin TQFP	34, 34, 66	3.3 V	-4, -7, -10
EPM3128A	128	100-pin TQFP, 144-pin PQFP	80, 96	3.3 V	-5, -7, -10
EPM3256A	256	144-pin TQFP, 208-pin PQFP	116, 158	3.3 V	-5, -7, -10

FPGA Compiler II Altera Edition

FREE

Partners with a single vision.

Altera and Synopsys have teamed up to produce Synopsys FPGA Compiler II Altera Edition, giving you the highest quality of results for programmable logic design. The Altera/Synopsys design flow provides the industry's smoothest migration path from ASICs to programmable logic devices (PLDs), allowing you to easily target your existing design files and scripts to Altera® devices.

High-density design power.

FPGA Compiler II Altera Edition is optimized specifically for Altera APEX™ and FLEX® devices and is tightly integrated with the Altera Quartus™ and MAX+PLUS® II software. By designing with FPGA Compiler II Altera Edition, Design Compiler users will achieve significantly improved area and performance results for even the most complex System-on-a-Programmable-Chip™ designs.

One year. For free.

Right now, every Design Compiler license can activate a free 12-month license of FPGA Compiler II Altera Edition. Simply call (800) 388-9125 or visit the Synopsys web site at **http://www.synopsys.com/fpga** to get your license file. It's that easy!

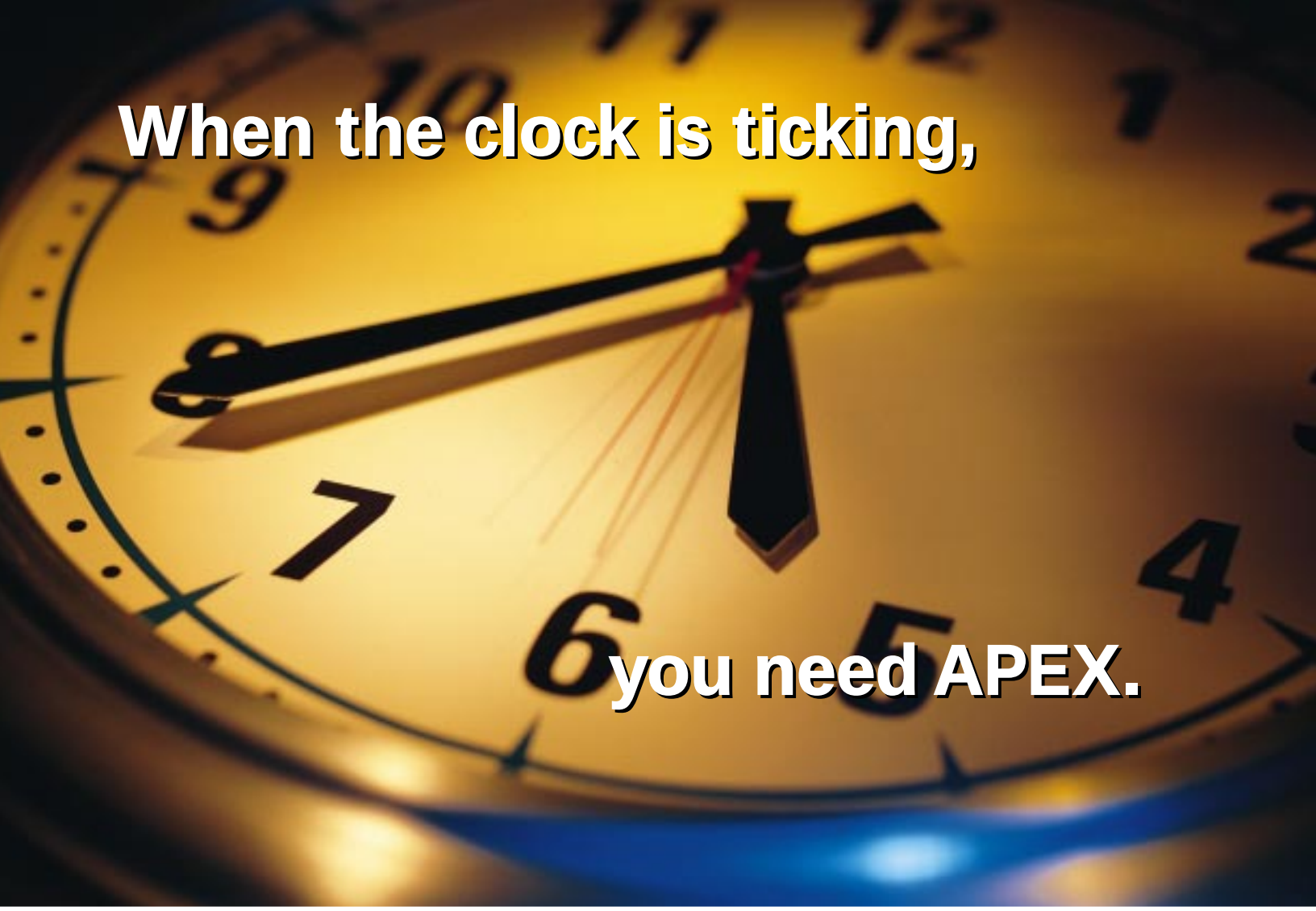
SYNOPSYS®

http://www.synopsys.com/fpga

ALTERA®

The ASIC Alternative™

http://www.altera.com



Get to Market Fast.

Your shrinking development cycles and tough time-to-market demands require a fast, flexible solution. Altera's APEX™ device family helps you get your product to market first and provides a true System-on-a-Programmable-Chip™ solution.

Fast System Performance.

Altera's revolutionary MultiCore™ architecture combines look-up table and product-term logic with embedded memory, allowing efficient integration into a single APEX device containing up to 1.5 million gates (2.5 million maximum system gates). The APEX architecture delivers optimum performance through features such as embedded LVDS circuitry to support I/O bandwidth of up to 622 Mbps.

Tools & IP that Speed Design.

Altera's Quartus™ development software enhances productivity and shortens design cycles. A variety of MegaCore™ and AMPP℠ intellectual property (IP) megafunctions, optimized for the APEX architecture, are available to further streamline development.

APEX Feature Overview

- 9 devices offering up to 1.5 million gates
- Low-power 1.8-V supply voltage
- Flexible memory, including CAM, dual-port RAM, FIFOs, and ROM
- LVDS for bandwidth up to 622 Mbps
- PLLs for improved timing
- FineLine BGA™ packages for board space savings

No Time to Lose.

The clock is ticking. Visit the Altera web site at **http://www.altera.com/clock** to find out how Altera's System-on-a-Programmable-Chip solution—the APEX solution—can help you meet your deadlines.

ALTERA®

The Programmable Solutions Company™

http://www.altera.com/clock

The System-on-a-Programmable-Chip Solution.