FLEX 10K
Price Reductions
See page 4

The Altera Advantage News & Views

Newsletter for Altera Customers ◆ Fourth Quarter ◆ November 1996

Altera Announces the 3.3-V FLEX 10KA Family

Altera® announces the FLEX®10KA family of 3.3-V programmable logic devices (PLDs), with projected densities up to an unprecedented 250,000 gates. This density combines with system speeds over 104MHz and 5.0-V input tolerance to make the FLEX10KA family the most advanced gate array replacement available today. The FLEX 10KA family directly addresses the need for increased performance in larger devices running on low power, and sets a new standard for programmable logic.

FLEX 10KA Offers Enhanced Performance

The FLEX 10KA family will extend the Altera FLEX10K architecture to a projected 250,000 gates. Based on reconfigurable CMOS SRAM elements, the family incorporates all the features necessary to implement common gate array functions. The FLEX10KA architecture features fast, efficient embedded array blocks (EABs) containing on-chip RAM and specialized logic, as well as a logic array for other logic functions. This combination of RAM and logic eliminates the tradeoff between logic and memory required by other architectures.

FLEX 10KA devices contain the ClockLock feature to minimize clock delay and skew and the ClockBoost feature for multiplying the system clock. With these features, FLEX 10KA devices deliver enhanced performance—even for the most complex functions. For example, an 8-bit, 16-tap finite impulse response (FIR) filter typically runs at 49 MHz in 5.0-V field-programmable gate arrays (FPGAs). However, in the 50,000-gate EPF10K50A device, the same filter runs at 104MHz.

Reduced Power Consumption

The amount of power used by a device is a function of the power supply voltage and the current used by the device. Optimizing a 0.35-micron process for 3.3-V performance should reduce the power supply voltage by 34% and the typical current consumption by approximately 45%. Therefore, the power consumption of FLEX 10KA devices is expected to be 70% lower than equivalent 5.0-V devices.

Mixed-Voltage Support

As the migration to 3.3-V devices moves forward, many systems will use both 5.0-V and 3.3-V power. In some cases, a 5.0-V device will drive the inputs of a 3.3-V device. See Figure 1.

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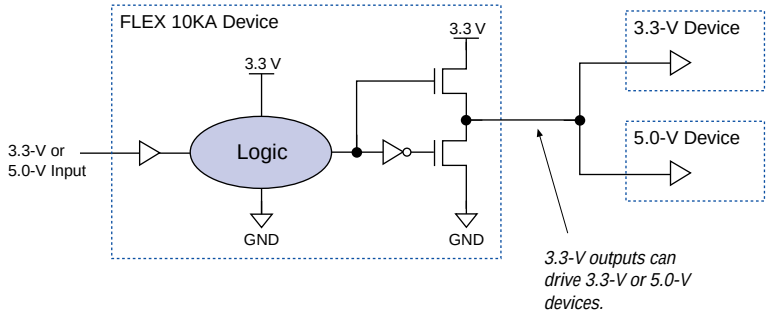
Figure 1. FLEX 10KA I/O Capability

FLEX 10KA devices have 3.3-V and 5.0-V input tolerance, and can drive both 3.3-V and 5.0-V devices.



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Altera Announces the 3.3-V FLEX 10KA Family continued from page 1

Because PLDs are often the interface between the devices on a board, high-performance PLDs with the ability to support the electrical requirements of both 5.0-V and 3.3-V devices provide the ideal interface for mixed-voltage systems. Altera gives designers maximum flexibility by including 5.0-V input tolerance in 3.3-V FLEX 10K and all FLEX 10KA devices. Additionally, FLEX 10KA devices can drive 5.0-V TTL logic levels.

Technology Advantages

FLEX 10KA devices are built on a 0.35-micron, quad-layer metal SRAM process that enables the smallest possible die size, improves yields, and lowers costs. This process is optimized for 3.3-V operation, which ensures low power consumption without sacrificing performance. Figure2 compares the 0.5-micron triple-layer metal die to the 0.35-micron quad-layer metal EPF10K50A die.

State-of-the-Art Packaging

The performance and process improvements in FLEX10KA devices are complemented by modern packaging technology that accommodates the higher lead counts in larger devices. FLEX 10KA devices are available in high-pin-count ball-grid array (BGA) packages, which greatly reduce the problem of bent leads, as well as in traditional quad flat pack packages. Pin migration will be supported, reducing costs for system engineers who want to place their design in a larger device without having to change device pin-outs or board layout. No other PLD offers the combination of density, performance, packaging, and pricing found in the FLEX10KA family.

Software Support

The FLEX10KA family will be supported by Altera's MAX+PLUS® II development system. Altera also provides MegaCore functions that are pretested and optimized for Altera architectures as MAX+PLUSII migration products. Altera currently offers a microperipheral function library and is planning to release fast Fourier transform (FFT) and peripheral component interconnect (PCI) functions with MAX+PLUS II version7.1. Future function will include more digital signal processing (DSP) and networking functions. For more information on the MegaCore design flow, see "Designing with MegaCore Functions" on page 10.

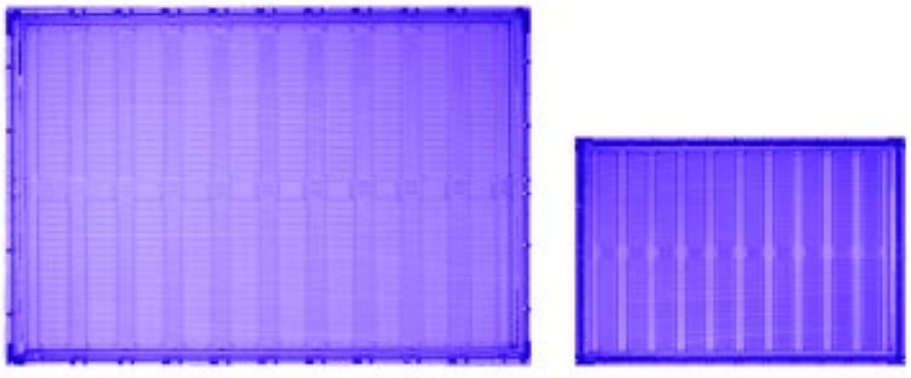
Available Now

3.3-V EPF10K50V devices on a 0.35-micron, triple-layer metal process are available now. Members of the FLEX10KA family, including the EPF10K250A with 250,000 gates of programmable logic, will be available by the end of 1997. Table 1 provides a summary of FLEX 10KA devices. For more information, contact Altera Customer Marketing.

Table 1. FLEX 10KA Devices

Device	Typical Density (Gates)
EPF10K250A	250,000
EPF10K130A	130,000
EPF10K100A	100,000
EPF10K70A	70,000
EPF10K50A	50,000
EPF10K40A	40,000
EPF10K30A	30,000
EPF10K20A	20,000
EPF10K10A	10,000

Figure 2. EPF10K50 Die Comparison



0.5-Micron Triple-Layer Metal

0.35-Micron Quad-Layer Metal

Devices & TOOLS

FLEX 10K

Altera Reduces FLEX 10K Prices up to 50%

On October 1, Altera reduced prices for the FLEX10K family up to 50%. The price reductions are a result of Altera's redundancy technology. Increased process and manufacturing efficiencies combined with the increased yield provided by redundancy have resulted in dramatic cost reductions.

Since its introduction in late 1995, the 100-unit list price for OEM direct orders of the EPF10K50 device has declined 80% to $195; the 100-unit list price for the EPF10K100 declined 40% in seven months to $595. By mid-1997, it is anticipated that the volume price of the EPF10K10 and EPF10K20 will be within two times the price of gate arrays with similar densities, making them a cost-effective solution compared to gate arrays. The following table shows sample pricing for currently available FLEX 10K devices.

FLEX 10K Pricing

Device	100-Unit Price *(1)*	1997 Volume Pricing *(1), (2)*
EPF10K10	$22.50	$10.00
EPF10K20	$53.50	$20.00
EPF10K30	$87.50	$35.00
EPF10K50	$195.00	$75.00
EPF10K100	$595.00	$250.00

(1) Price in U.S. dollars for OEM direct orders.

(2) Anticipated prices are for 25,000-unit quantities for EPF10K10, EPF10K20, and EPF10K30 devices, and 5,000-unit quantities for EPF10K50 and EPF10K100 devices.

New Devices Added to the FLEX 10K Family

With 10,000 to 100,000 usable gates and 150-MHz performance, FLEX 10K devices have the density and speed to satisfy the most demanding design requirements. All members of the FLEX 10K family are expected to be available by the end of the year, including new devices such as the EPF10K40 and EPF10K70; more package options and speed grades are also expected to be available for devices currently in production. The following table provides availability for FLEX 10K devices.

FLEX 10K Availability

Device	Package	Speed Grade	Availability
EPF10K10	84-pin PLCC	-4, -3	December 1996
	144-pin TQFP	-4, -3	Now
	208-pin RQFP	-4, -3	Now
EPF10K20	144-pin TQFP	-4, -3	December 1996
	208-pin RQFP	-4, -3	Now
	240-pin RQFP	-4, -3	Now
EPF10K30	208-pin RQFP	-4, -3	Now
	240-pin RQFP	-4, -3	Now
	356-pin BGA	-4, -3	December 1996
EPF10K40	208-pin RQFP	-4, -3	December 1996
	240-pin RQFP	-4, -3	December 1996
EPF10K50	356-pin BGA	-4, -3	Now
	240-pin RQFP	-4, -3	Now
	403-pin PGA	-4, -3	Now
EPF10K50V	240-pin RQFP	-4, -3	December 1996
EPF10K70	240-pin RQFP	-4, -3	January 1997
	503-pin PGA	-4, -3	December 1996
EPF10K100	503-pin PGA	-4, -3, -3DX	Now

FLEX 8000

Altera Introduces New FLEX 8000 Packages

FLEX 8000 devices are now available in several new packages that make the device family a viable gate array alternative. The EPF8820A is now available in 144-pin thin quad flat pack (TQFP) packages, providing a low-cost solution for high-volume, board-space-sensitive applications. In December, the EPF81188A and EPF81500A are expected to be available in 240-pin plastic quad flat pack (PQFP) packages, significantly closing the per unit price gap for gate arrays from 12,000 to 16,000 gates. With process migration, increased manufacturing efficiency, and low-cost packaging, FLEX 8000 devices provide the highest-performance, most cost-effective programmable logic solution in the industry. The following table provides projected pricing information for these new devices.

FLEX 8000 Price Projections

Device	Package	Speed Grade	Current 100-Unit Price *(1)*	Anticipated Mid-1997 Price *(1)*
EPF8820A	144-pin TQFP	-4	$23.00	$12.00
EPF81188A	240-pin PQFP	-4	$32.50	$16.50
EPF81500A	240-pin PQFP	-4	$39.50	$17.50

(1) Price in U.S. dollars for OEM direct orders.

MAX® 9000

New MAX 9000 Package Options

New package options for the MAX 9000 family are summarized below:

- EPM9560 devices in 208-pin power quad flat pack (RQFP) packages are now shipping as replacements for existing 208-pin ceramic quad flat pack (CQFP) packages. These new devices are form, fit, and functionally equivalent to EPM9560 devices in 208-pin CQFP packages.
- EPM9400 devices are now shipping in 84-pin plastic J-lead chip carrier (PLCC) packages.
- EPM9560 devices in 356-pin ball-grid array (BGA) packages, the first BGA package for the MAX 9000 family, will be available in December.

MAX 7000

MAX 7000S Availability

Altera has expanded production for MAX7000S devices. EPM7128S and EPM7192S are currently in production. EPM7256S and EPM7064S devices are available as engineering samples; production quantities are anticipated to be available in December and January, respectively. MAX7000S device availability is shown below.

MAX 7000S Availability

Device	Package	Speed Grade	Projected Availability
EPM7192S	160-pin PQFP	-10, -15	Now
EPM7128S	160-pin PQFP	-7, -10, -15	Now
	100-pin PQFP	-7, -10, -15	Now
	100-pin TQFP	-7, -10, -15	December 1996
EPM7256S	160-pin PQFP	-10, -15	December 1996
	208-pin RQFP	-10, -15	December 1996
EPM7064S	44-pin PLCC	-7, -10	January 1997
	44-pin TQFP	-7, -10	Q1 1997
	100-pin PQFP	-7, -10	January 1997
EPM7032S	44-pin PLCC	-5, -6, -7, -10	Q1 1997
	44-pin TQFP	-5, -6, -7, -10	Q1 1997
EPM7096S	100-pin PQFP	-7, -10, -15	Q2 1997
	100-pin TQFP	-7, -10, -15	Q2 1997
	160-pin PQFP	-7, -10, -15	Q2 1997
EPM7160S	100-pin TQFP	-7, -10, -15	Q2 1997
	84-pin PLCC	-7, -10, -15	Q2 1997

MAX 7000S: The Fastest Devices with ISP

Following the performance leadership of the MAX 7000 product family, MAX 7000S devices offer the highest performance with in-system programmability (ISP) on the market today (see the table below). MAX 7000S devices offer a performance of up to 125 MHz for a 16-bit loadable, up/down counter.

Comparison of Devices with ISP *Note (1)*

Feature	Altera EPM7128S	Xilinx XC95108	Lattice ispLSI2128	AMD MACH 5-128
Memory Elements	EEPROM	FLASH	EECMOS	EEPROM
Macrocells	128	108	128	128
t_{PD} (ns)	7.5	10	10	7.5
Package	160-pin PQFP	160-pin PQFP	176-pin TQFP	160-pin PQFP
Availability	Now	Now	Now	Q4 1996

Note:

(1) Statistics in this table were obtained from the world-wide web sites of Xilinx, Lattice, and AMD.

Altera Migrates EPM7192E to 0.65-Micron Process

In January 1997, Altera expects to ship EPM7192E devices fabricated on a 0.65-micron process. Evaluation packets for qualification are available—containing reliability data, device samples, and documentation—from your local Altera representative.

MAX 5000 & Classic

Product Transitions

Altera is migrating existing MAX 5000 and Classic devices from a 0.8-micron process to a 0.65-micron process. Evaluation packets (containing device samples and documentation) are available from your local Altera sales representative. The table below outlines the migration schedule:

Product Migration Schedule

Description *(1)*	Reference	Device	Date
MAX 5000 devices fabricated on a 0.65-micron process *Note (2)*	PCN 9407 ADV 9515 ADV 9606	EPM5032	Q1 1997
		EPM5064	Q2 1997
		EPM5128	Complete
		EPM5130	May 1, 1997
		EPM5192	October 1, 1996
Classic devices fabricated on a 0.65-micron process	PCN 9510 ADV 9607	EP6*xx*	Complete
		EP9*xx*	September 1, 1996
		EP18*xx*	March 1, 1997

Notes:

(1) This process transition will not result in any changes to data sheet parameters or ordering codes.

(2) Devices manufactured on the 0.65-micron process must be programmed with new programming adapters.

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Devices & Tools
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New Altera programming adapters are required to program the 0.65-micron devices. Altera will exchange existing EPM5032, EPM5064, and EPM5130 programming adapters for new adapters *for free*. These new adapters are backwards-compatible and support all existing die revisions. The table below lists the existing MAX 5000 adapters that can be exchanged for new adapters. Altera has already completed an exchange program for EPM5128 and EPM5192 programming adapters.

Contact Altera's Customer Service Department or your local Altera sales representative for more information.

MAX 5000 Replacement Adapters

Existing Adapter	New Adapter
PLED5032	PLMD5032A
PLMD5032	PLMD5032A
PLEJ5032	PLMJ5032A
PLM5032	PLMJ5032A
PLES5032	PLMS5032A
PLEJ5064	PLMJ5064A
PLMJ5064	PLMJ5064A
PLEG5130	PLMG5130A
PLEJ5130	PLMJ5130A
PLMJ5130	PLMJ5130A
PLEQ5130	PLMQ5130A
PLMQ5130	PLMQ5130A

MAX+PLUS II

MAX+PLUS II 7.1 To Ship In December

Altera is expanding offerings of devices and packages at a rapid pace. By December of this year, Altera plans to add a total of seven new device/packages to the FLEX 10K and MAX 9000 families. MAX+PLUS II, version 7.1 will be available in December to support these new devices.

In addition to new device support, MAX+PLUS II version 7.1 provides improved VHDL capability. Message location is improved, and support for additional structures and VHDL '93 syntax are provided. Altera is also improving timing models for Synopsys, which will result in better timing-driven synthesis results within Synopsys tools.

Altera's software maintenance program ensures that you will have the most up-to-date support for Altera's devices, as well as the latest features and capabilities. For more information on purchasing a maintenance agreement, contact your local Altera representative.

Fast Fourier Transform Function Available in December

Altera will be releasing the fast Fourier transform (FFT) MegaCore function as a migration product to MAX+PLUS II version 7.1. With this new function, Altera continues to provide the broadest support for digital signal processing (DSP) applications. DSP megafunctions optimized for FLEX devices provide flexibility that is critical to high-performance applications such as radio frequency (RF) rate communications systems for cable and wireless networks.

Fastest FFT Solution Available

The fully parameterized FFT megafunction performs significantly faster than DSP processors and substantially faster than previously available programmable logic implementations. In the past, high-performance FFT functions were available only as expensive DSP standard product and multiprocessor solutions, or as inflexible ASIC solutions. With FLEX10K devices, designers have the option of using embedded array blocks (EABs) as on-chip RAM. Table1 shows the FFT function performance for Altera FLEX 10K devices using EABs.

Table 1. FFT Performance & Device Utilization with EABs

Length (Points)	Precision	Memory	Size (LEs)	Speed (µs)
512	16 Data, 8 Twiddle	Single	2,000	186
512	8 Data, 8 Twiddle	Dual	1,150	94
512	12 Data, 12 Twiddle	Dual	1,970	94
512	16 Data, 16 Twiddle	Single	2,993	190

Table 2 provides FFT function performance for Altera FLEX 10K devices using standard synchronous SRAM.

Table 2. FFT Performance & Utilization with External RAM

Length (Points)	Precision	Memory	Size (LEs)	Speed
1,024	16 Data, 16 Twiddle	Single	2,993	411 µs
1,024	16 Data, 16 Twiddle	Dual	2,993	207 µs
32 K	16 Data, 16 Twiddle	Dual	3,100	9.8 ms

Parameterized for Ease of Use

Designers can optimize the FFT megafunction for specific applications by customizing a variety of parameters. The FFT length can be specified as any power of 2 and the data width and the twiddle width

can be configured to any positive number. The FFT function permits 1 or 2 data bank memory architectures. This flexibility ensures that the compiled megafunction is optimized for both area and speed to support specific customer applications.

AMPP Support

To encourage the development of large DSP applications, Altera will provide the low-level, architecture-optimized information in the FFT MegaCore function to partners in the Altera Megafunction Partners Program (AMPP) for integration into more complex functions. AMPP partners are also working on FFT implementations.

Pricing and Availability

The FFT MegaCore function is priced at $7,995 and will be available as a migration product for MAX+PLUS II version 7.1 in December 1996. The ordering code for the library is PLSM-FFT.

High-Performance BGA Package Now Available

Ball-grid array (BGA) packages are low-profile, high-power packages with performance benefits over traditional surface-mount packages. A BGA package contains an integrated circuit that is mounted to a small circuit board. Input and output pins are replaced with solder balls, which are arranged in a matrix on the bottom of the board. The final device is then soldered directly to printed circuit boards in a process similar to standard surface-mount technology.

BGA packages have advanced substrate designs with integrated copper heat sinks for enhanced thermal performance. BGA packages also utilize proven assembly practices and materials to ensure high reliability and performance. Available in a variety of ball (I/O) counts and standard JEDEC body sizes, BGA packages are supported by an industry infrastructure that includes contract manufacturing.

To ensure the highest level of reliability, the latest BGA package from Amkor/Anam (named SuperBGA) uses the newest materials and process technologies. Incorporating the die and I/O on the same side of the package improves signal integrity and speed. The enhanced multilayer package delivers even greater performance by increasing speed, decreasing inductance, and reducing noise.

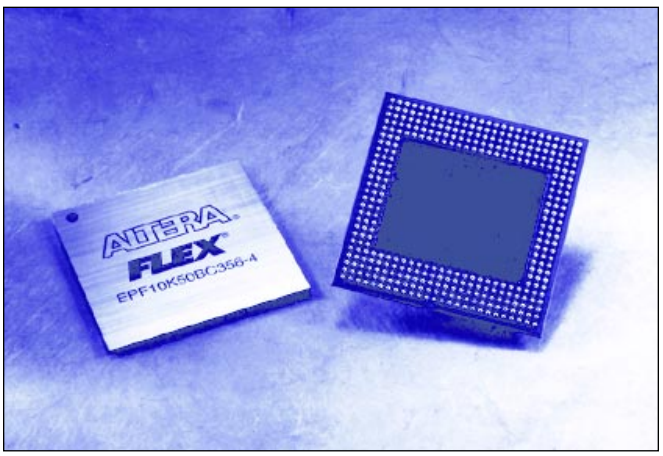
The SuperBGA package couples high-performance with dramatic size and weight refinements. A typical 35 × 35 mm SuperBGA package has a mounted height of less than 1.4 mm and weighs 7.0 grams.

The increased performance and space savings of the SuperBGA package make it ideal for high-density, high-performance devices. Therefore, Altera has teamed with Amkor/Anam to offer FLEX10K devices in the SuperBGA package.

The EPF10K50 in a 35-mm, 356-pin BGA package provides the following advantages over traditional packages:

- 52 more user I/O pins than the 304-pin thermally enhanced quad flat pack (QFP)
- Weight of approximately 26 grams
- Footprint of 42.6 mm^2

The new BGA package provides a size savings of over 32% with 17% more user I/O pins.



Discontinued Devices

In recent months, Altera has announced that various products will be discontinued (see the table below). Altera distributes advisories (ADVs) and product discontinuance notices (PDNs) that provide information on discontinued devices. To obtain a copy of a specific ADV or PDN, contact your local Altera sales representative. Selected ADVs, PDNs, and a complete listing of discontinued devices are also available on Altera's world-wide web site at **http://www.altera.com**. Rochester Electronics, an after-market supplier, offers support for many discontinued Altera products. Contact Rochester Electronics at (508)462-9332 for more information.

Discontinued Device Ordering Codes

Device Family	Device	Last Order Date	Last Shipment Date	Reference
FLEX 8000	Military products (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513 PDN 9517
MAX 7000	Military products (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513
FLASHlogic	EPX740 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
MAX 5000	Military EPM5130W device	10/31/96	12/31/96	PDN 9513
	Selected MAX 5000 ordering codes	9/30/96	12/31/96	ADV 9609
	EPM5016 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
Classic	Military products (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513
	EP220, EP224, EP312, EP324 (all packages, temperature grades, and speed grades)	3/31/97	9/30/97	PDN 9516
	Selected EP9*xx* ordering codes	9/30/96	12/31/96	ADV 9608
	Selected EP18*xx* ordering codes	3/31/97	6/30/97	ADV 9608
Function-Specific	EPS448, EPC1213 military (all 883B, DESC, and military temperature grades)	10/31/96	12/31/96	PDN 9513 PDN 9517
	EPS448, EPS464 (all commercial and industrial temperature grades; military devices have earlier last order and last shipment dates)	3/31/97	9/30/97	PDN 9516

New Altera Publications

New Altera publications are available from Altera Literature Services, and Altera Express. Individual documents are available on the Altera world-wide web site. Document part numbers are shown in italics.

- **Altera Digital Library** *P-CD-ADL-01*
  Provides a complete electronic collection of current Altera technical literature for all Altera device families and development software. A multimedia presentation highlighting the FLEX10K family is also provided.
- **Microperipheral MegaCore Library Data Book** *A-DB-MEGA-01*
  Provides data sheets for the a8237 DMA controller, a6402 UART, a16450 UART, a8251 UART, a6850 UART, and a8255 programmable peripheral interface adapter MegaCore functions. The microperipheral library is a migration product for MAX+PLUS II version 7.1 and higher.
- **Solution Brief 1: Reed-Solomon CODEC** *A-SB-001-01*
  Gives a description, including parameters, of the Reed-Solomon CODEC megafunction from Object Oriented Hardware.
- **Solution Brief 2: FIR Filter** *A-SB-002-01*
  Provides a description, block diagram, and parameters for the FIR filter megafunction from Integrated Silicon Solutions, Ltd.
- **Solution Brief 3: Biquad IIR Filter** *A-SB-003-01*
  Gives a description, block diagram, and parameters for the biquad IIR filter megafunction from Integrated Silicon Solutions, Ltd.

Technical ARTICLES

Creating Optimized, Fixed-Coefficient 2-D Video Convolvers

Video convolution involves transforming an image by running a two-dimensional (2-D) window over pixels that represent an image, multiplying the corresponding elements, and summing them. Often, the convolution window is fixed, i.e., the coefficients (or weights) do not change, only the data changes.

Video convolvers can be used in image processing applications such as filtering, sharpening, edge detection, and interpolation. Altera FLEX 10K and FLEX 8000 devices are ideally suited for convolvers, especially when the convolution window is fixed.

Many convolution windows used for common image processing applications have the following characteristics:

- The coefficients are small integer multiples of a common factor.
- The coefficient matrix is sparse, i.e., many of the coefficients are zero.

Designers can use these characteristics to increase logic efficiency and speed.

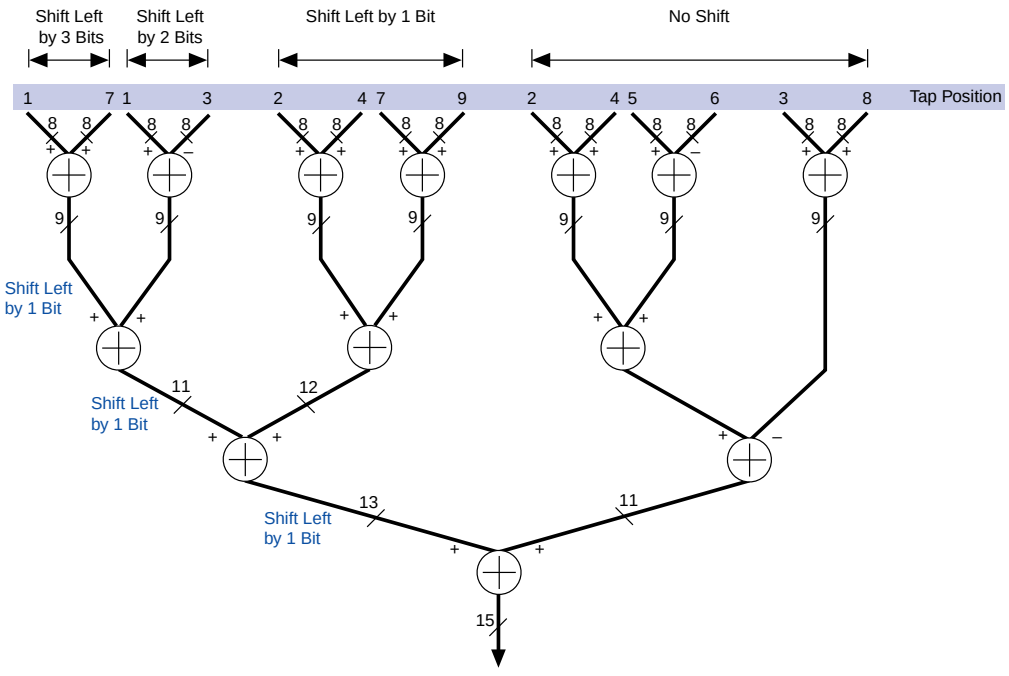
Figure 1 shows a sample convolution window and Figure 2 provides a block diagram of the optimized convolver. The optimized convolver consists only of adders—i.e., multipliers are no longer required. Optimized, the convolver requires only 215 logic elements (LEs). In contrast, this same design using the vector multiplier approach described in *AN 73 (Implementing FIR Filters in FLEX Devices)* required 539 LEs. The difference between methods is a resource savings of 60%.

More information on this optimization technique—including an Altera Hardware Description Language (AHDL) example—is provided in *AN 82 (Highly Optimized 2-D Convolvers in FLEX Devices)*, which will be available in December 1996. For more information on filters, go to *AN 73 (Implementing FIR Filters in FLEX Devices)*, which is currently available on Altera's world-wide web site at **http://www.altera.com**.

Figure 1. Sample Convolution Window

1.5	0.375	–0.625
0.375	0.125	–0.125
1.25	–0.125	–0.250

Figure 2. Block Diagram of Optimized Convolver



Designing with MegaCore Functions

Many of today's designs use predesigned functions, often without explicit involvement from the designer. For example, many synthesis tools offer a feature known as module generation, which is the capability to recognize a logic structure—in many cases involving a mathematical operator—in a design and apply a predefined, device-specific implementation to the function. Module generation permits a designer to focus on the functional behavior of each logic block rather than the gate-level implementation.

Using MegaCore functions in a design is analogous to module generation. MegaCore functions are common system-level functions, which have predesigned, device-specific implementations that can be instantiated in a design and functionally simulated. Using MegaCore functions, the designer can focus on the higher-level behavior of the system, resulting in a more efficient design flow.

Design Flow

A top-down design flow is an effective way to incorporate MegaCore functions into a design. By focusing on system-level behavior, a designer can identify and define functional blocks for implementation with a MegaCore function. Deciding to use a MegaCore function early in the design process is important because integrating MegaCore functions into a design often requires some implementation. For example, a peripheral component interconnect (PCI) interface usually requires the designer to build logic between the interface and the back-end system.

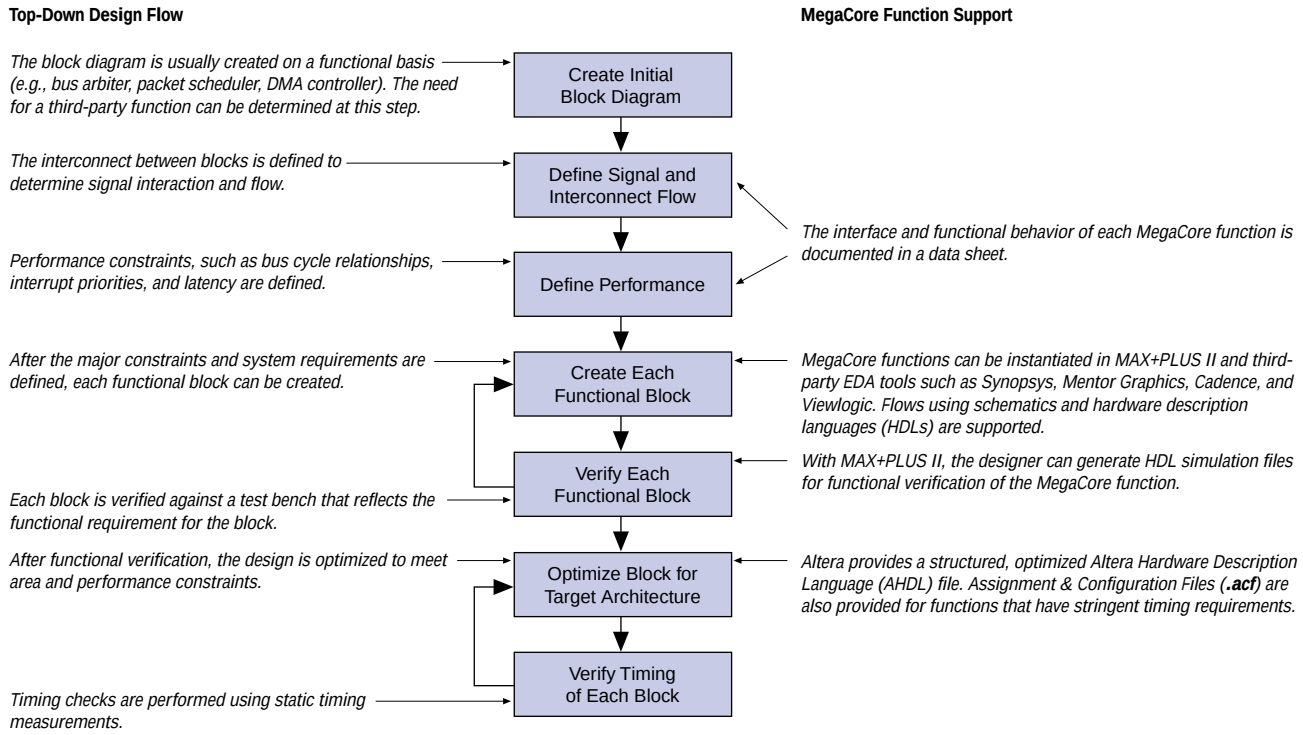
Figure 1 describes a typical top-down design flow. In this flow, the engineer builds the design incrementally, and each block is functionally verified before optimization. Functional verification is an important step because changes in functionality usually require the engineer to re-optimize the design.

Altera Supports the Design Flow

Altera provides MegaCore function support for each step in the design flow, including:

- Schematic and HDL support
- HDL simulation files
- Optimization and timing
- Documentation

Figure 1. Top-Down Design Flow with MegaCore Functions



Altera has optimized MegaCore functions for Altera devices. Therefore, designers can use MegaCore functions without modifications, ensuring that the function's optimization is preserved. Designers can customize functions as needed using a variety of parameters. For example, designers can specify the length, data width, and twiddle width of the fast Fourier transform (FFT) MegaCore function.

Conclusion

A design flow with MegaCore functions is similar to the one used by gate array designers today. A top-down design strategy helps identify opportunities to use MegaCore functions early in the process, leaving the designer free to focus on system behavior.

Using the genmem Utility

You can use Synopsys tools and Altera's **genmem** utility to create designs for FLEX 10K embedded array blocks (EABs) that implement RAM and ROM. The **genmem** utility produces three output files:

- *Functional simulation model*—**genmem** can create both VHDL and Verilog HDL simulation models to support pre-synthesis and post-synthesis, pre-place-and-route functional simulation.
- *Library timing model*—This model contains timing information that can be used by Synopsys tools for timing-driven synthesis and timing estimation.
- *Component Declaration*—For VHDL, **genmem** creates a file containing a Component Declaration for the element to be instantiated. This Component Declaration is required by synthesis and simulation tools. When using Verilog HDL, the module declaration found in the functional simulation model can be instantiated.

How to Use genmem

First, generate the necessary output **.v** and **.lib** files for the memory function you desire. For example, to create output files for dual-port RAM that is 64 words deep and 8 bits wide in Verilog HDL, type the following at a UNIX command prompt:

```
genmem csdpram 64x8 -verilog
```

The **genmem** utility will produce the file **csdp_ram_64x8.v** for simulation and the file **csdp_ram_64x8.lib** for synthesis.

Using genmem for Synthesis

Perform the steps below to use the utility for synthesis:

1. Instantiate the RAM. For example, in Verilog HDL, include the following in your design:

   ```
   csdp_ram_64x8 <RAM Name> (DataA,
      DataB, AddressA, AddressB, WEa,
      WEb, Clock, Clockx2, QA, QB, Busy);
   ```

   You can obtain the port names from MAX+PLUS II Help or the **genmem** functional simulation model.

2. Add the **.lib** file to the library of your choice. For example, to add the RAM from Step 1 to the FLEX10K library (**flex10k.db**), type the following at the Synopsys tool command line:

   ```
   read -f db flex10k.db ↵
   update_lib flex10k csdp_ram_64x8.lib ↵
   write_lib flex10k -o flex10k.db ↵
   ```

3. Apply the `dont_touch` property to the RAM so that the Synopsys tools will pass this instance of the RAM into an EDIF file as a hollow-body component. During compilation, MAX+PLUSII will map the RAM to a dual-port RAM with a depth of 64 and a width of 8.

You do not need to read in the simulation model file for synthesis.

Using genmem for Functional Simulation (Before Place & Route)

The **genmem** utility creates a functional simulation model that describes the behavior of the RAM. To use the simulation model, read it into the simulation tool with the rest of the functional design description and the test bench, and then simulate the design.

Using genmem for Functional Simulation (After Place & Route)

You do not need to use the **genmem** utility for post-place and route simulation. MAX+PLUS II includes all of the necessary information in the VHDL and VerilogHDL output files.

Clock Management with ClockLock & ClockBoost

As programmable logic devices (PLDs) increase in density, on-device clock distribution becomes increasingly important for device performance. To help manage clocking in Altera high-density PLDs, Altera provides the ClockLock and ClockBoost features. The ClockLock feature incorporates a phase-locked loop (PLL) with a balanced clock tree to minimize on-device clock delay and skew. The ClockBoost feature provides clock multiplication, which increases clock frequencies by as much as four times the incoming clock rate, improving system bandwidth. For example, a 100-MHz design can be fed by a 50-MHz clock, which is then doubled in the Altera device. Clock multiplication simplifies printed circuit board (PCB) designs because the clock path on the PCB does not require the distribution of a high-speed clock signal.

Clock Delay & Skew

The delay from the clock pin to a register can be significant—especially for large devices—and can decrease both on- and off-device performance. The equation for calculating the pin-to-pin clock-to-output time is shown below.

$$t_{CO} = t_{CLOCK} + t_{SKEW} + t_{REGISTER\_CO} + t_{OUTPUT}$$

The t_{CLOCK} and t_{SKEW} parameters account for a significant portion of the total clock-to-output delay in large devices. Therefore, reducing the t_{CLOCK} delay will minimize the clock-to-output time. A large clock delay also decreases the performance of the signal driving into the device because it can cause positive hold times for the input register. To create a zero hold time, a built-in delay is added to the data path. However, this added data delay increases the setup time for the register. The equations for setup and hold times are shown below.

$$t_{SU} = t_{REGISTER\_SU} + t_{DATA} - t_{CLOCK} - t_{SKEW}$$
$$t_{H} = t_{CLOCK} + t_{SKEW} + t_{REGISTER\_H} - t_{DATA}$$

Clock skew—the difference between clock delays to different registers—can also increase the setup time. To ensure a zero hold time, the built-in delay is increased to account for the longest clock delay to any register. However, increased data delay also increases the setup time of other registers with shorter clock delays. The ClockLock and ClockBoost features help mitigate clock delay and skew.

ClockLock: Faster System Performance

The ClockLock feature minimizes clock delay by using a PLL, which locks onto the incoming clock and generates a clock signal that leads the incoming clock. The difference between the incoming clock at the pin and the ClockLock-generated clock approximates the delay from the ClockLock circuitry to the register, minimizing the apparent delay from the clock pin to the register. Figure 1 shows a schematic of the clock distribution circuit.

Figure 1. ClockLock Clock Distribution

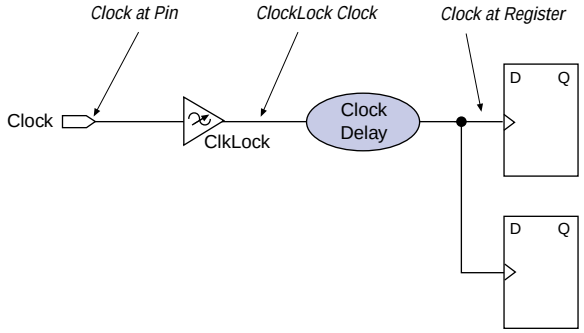
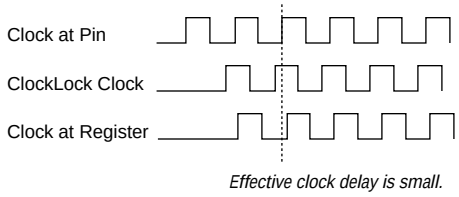


Figure 2 shows the waveform for the ClockLock circuitry.

Figure 2. Waveform of ClockLock-Generated Clock



External connections or devices are not required and tight control of timing is maintained because the entire ClockLock circuit is implemented within the PLD. The ClockLock circuit uses a phase comparator to compare the incoming clock to an internally generated delayed clock. The delay from the voltage-controlled oscillator (VCO) models the delay of the internally generated clock to the registers in the device. The phase comparator controls the VCO that drives the clock throughout the device. See Figure 3.

The ClockLock circuit generates a clock signal with minimal delay from the clock pin to the registers. The

potential for skew across the device still exists because the signal must propagate through metal lines in the device. To minimize skew, Altera added tuned delays into the clock distribution network; registers close to the ClockLock circuit have an added delay. Thus, the total delay from the ClockLock circuit to any register is the same, regardless of the distance to the register.

By reducing clock delay and skew, the ClockLock circuit improves on- and off-device performance and maintains a zero hold time. Table 1 shows the improvement in setup and clock-to-output times for an Altera EPF10K100 device in a -3 speed grade.

Table 1. Timing Improvement with ClockLock *Note (1)*

Parameter	Without ClockLock	With ClockLock
Setup time	8.0 ns	4.8 ns
Hold time	0 ns	0 ns
Clock-to-output time	9.1 ns	5.1 ns
Device-to-device performance	58 MHz	80 MHz

Note:

(1) Timing information is preliminary. Contact Altera Applications for more information.

ClockBoost: Increased System Bandwidth & Reduced Area

The ClockBoost feature provides designers with the capability to multiply the incoming clock by two times, i.e., to double the clock speed. To implement clock multiplication, the delay element in the ClockLock circuit is augmented with a clock divider. The phase comparator sets the VCO so that the divided clock matches the incoming clock. Therefore, the output of the VCO is multiplied from the incoming clock. The divider determines the clock multiplication. For example, a divide-by-two operation results in a doubled clock.

This clock-multiplication technique is commonly used in microprocessors. By multiplying the clock on-device, the designer is not required to distribute a high-speed clock on the PCB. In addition, with the ClockBoost feature, designers can create time-domain-multiplexed designs for reducing logic element (LE) usage.

High-speed clock distribution can be difficult because a fast clock has fast edge rates, which require transmission-line design techniques to avoid ringing, undershoot, and overshoot. Designers can distribute a low-speed clock on the PCB with ClockBoost, similar to the method used to distribute a microprocessor clock. For example, instead of distributing an 80-MHz clock throughout the PCB, the designer can distribute a 40-MHz clock that is internally multiplied to 80 MHz.

ClockBoost also allows designers to implement time-domain multiplexed applications. The circuit is clocked by the multiplied clock, permitting it to operate twice per system cycle. With time-domain multiplexing, functions can be implemented with fewer LEs or embedded array blocks (EABs).

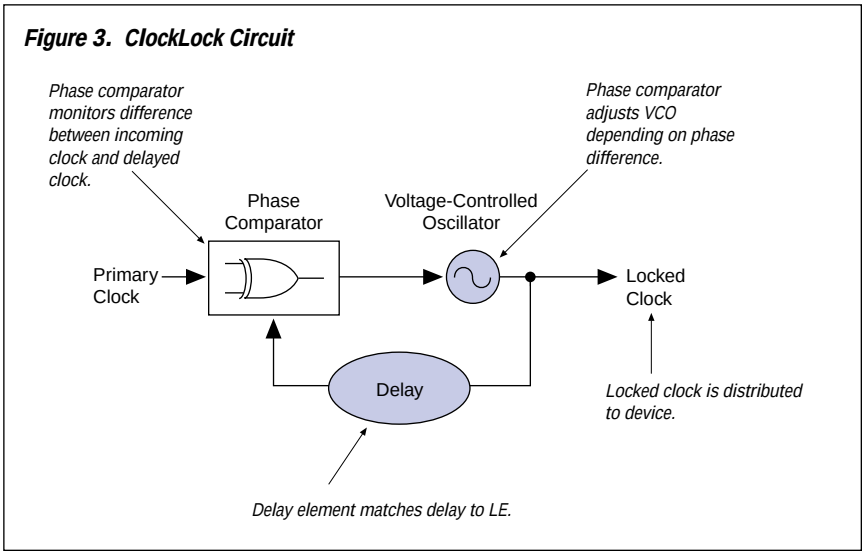
In a circuit using two 8×8 multipliers, each multiplier uses 4 EABs and 21 LEs, for a total of 8 EABs and 42 LEs. Using ClockBoost, the circuit can be implemented as one multiplier that is used twice per clock cycle. The input of the multiplier is multiplexed so that it can switch between the two sets of inputs. The output is demultiplexed so that it can drive out the two multiplication results. Although some LEs are required to accomplish the multiplexing, the cost is outweighed by the savings in EABs. As a result, the same functionality is accomplished with fewer logic resources.

Using the ClockLock & ClockBoost Features

Altera's MAX+PLUS II development software simplifies the use of the ClockLock and ClockBoost circuits. MAX+PLUS II version 7.0 and higher provides

continued on page 15

Figure 3. ClockLock Circuit



Evaluating Power in Altera Devices

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

You should complete a power evaluation early in the design process to help identify potential heat-related problems in the system and to prevent the system from exceeding the device's maximum allowed junction temperature.

The actual power dissipated by most applications is significantly lower than the power the package can dissipate. However, a thermal analysis should be performed for all projects. To perform a power evaluation, follow these steps:

- Estimate the power consumption of the application.
- Calculate the maximum power allowed for the device and package.
- Compare the estimated power and maximum power values.

The following figure shows a worksheet that you can use for evaluating power. For more information, refer to *AN 74 (Evaluating Power for Altera Devices)* in the ***1996 Data Book***.

Figure 1. Sample Worksheet for Evaluating Power (Part 1 of 2)

Design:_____ Device:_____

Estimating the Power Consumption of the Application

Internal Power Calculation

FLEX 10K & FLEX 8000 Devices

Standby current ($I_{CC_{STANDBY}}$)	$I_{CC_{STANDBY}}$ = _____ mA
Coefficient for I_{CC} calculation. See the appropriate device family data sheet for this value.	K = _____ µA/MHz × LE
Highest clock frequency of the design ($\mathbf{f_{MAX}}$)	$\mathbf{f_{MAX}}$ = _____ MHz
Logic elements used (N)	N = _____
Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125)	$\mathbf{tog_{LC}}$ = _____
Total internal current ($I_{CC_{INT}}$) $I_{CC_{INT}} = I_{CC_{STANDBY}} + K \times \mathbf{f_{MAX}} \times N \times \mathbf{tog_{LC}}$	$I_{CC_{INT}}$ = _____ µA
Convert to mA (i.e., divide by 1,000)	$I_{CC_{INT}}$ = _____ mA
Total internal power (P_{INT}) $P_{INT} = V_{CC} \times I_{CC_{INT}}$	P_{INT} = _____ mW

MAX 9000 & MAX 7000 Devices

Coefficients for I_{CC} calculation. See the appropriate device family	A = _____
data sheet for these values.	B = _____
	C = _____
Number of macrocells used with turbo bit on (MC_{TON})	MC_{TON} = _____
Number of macrocells used with turbo bit off (MC_{TOFF})	MC_{TOFF} = _____
Number of macrocells in the design ($MC_{USED} = MC_{TON} + MC_{TOFF}$)	MC_{USED} = _____
Highest clock frequency of the design ($\mathbf{f_{MAX}}$)	$\mathbf{f_{MAX}}$ = _____ MHz
Average ratio of logic cells toggling ($\mathbf{tog_{LC}}$) at each clock (typically 0.125)	$\mathbf{tog_{LC}}$ = _____
Total internal current ($I_{CC_{INT}}$) $I_{CCINT} = (A \times MC_{TON}) + (B \times MC_{TOFF}) + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$	$I_{CC_{INT}}$ = _____ mA
Total internal power (P_{INT}) $P_{INT} = V_{CC} \times I_{CC_{INT}}$	P_{INT} = _____ mW

Figure 1. Sample Worksheet for Evaluating Power (Part 2 of 2)

External Power Calculation

Power consumed by the DC output load ($P_{DC_{OUT}}$) — $P_{DC_{OUT}}$ = _____ mW

$$P_{DC_{OUT}} = \sum_{n=1}^{OUT} P_{DC_n}$$

Average capacitive load (C_{AVE}) at output pins — C_{AVE} = _____ pF

Number of output or bidirectional pins in design (OUT) — OUT = _____

Average ratio of I/O pins toggling (**tog_{IO}**) at each clock (typically 0.125) — **tog_{IO}** = _____

Power consumed by AC output load ($P_{AC_{OUT}}$) — $P_{AC_{OUT}}$ = _____ µW

$$P_{AC_{OUT}} = 1/2 \times OUT \times C_{AVE} \times 3.8V\ ^{(1)} \times \mathbf{f_{MAX}} \times \mathbf{tog_{IO}} \times V_{CCIO}$$

Convert to mW (i.e., divide by 1,000) — $P_{AC_{OUT}}$ = _____ mW

Total external power (P_{IO}) — P_{IO} = _____ mW

$$P_{IO} = P_{DC_{OUT}} + P_{AC_{OUT}}$$

Total Power Calculation

Estimated total power (P_{EST}) — P_{EST} = _____ mW

$$P_{EST} = P_{INT} + P_{IO}$$

Calculating Maximum Allowed Power for the Device & Package

Thermal resistance of the device — θ_{JA} = _____ C/W

Maximum junction temperature (T_J) as specified in the appropriate device family data sheet — T_J = _____ ° C

Ambient temperature (T_A) of the design — T_A = _____ ° C

Maximum power (P_{MAX}) allowed for the device — P_{MAX} = _____ W

$$P_{MAX} = \frac{T_J - T_A}{\theta_{JA}}$$

Comparing Maximum Power Allowed & Estimated Power

Is $P_{EST} < P_{MAX}$? — Yes or No

Note:
(1) This value should be 3.3 V when V_{CCIO} = 3.3 V or for 3.3-V devices; this value should be 5.0 V for the EPF8282A.

Clock Management with ClockLock & ClockBoost continued from page 13

a new function called CLKLOCK, which represents this circuitry. The CLKLOCK function is parameterized, allowing the designer to specify the ClockBoost clock multiplication factor. Designers can implement the CLKLOCK function in any of the MAX+PLUS II design editors, as well as in third-party schematic design tools.

Designers can also use third-party HDL tools to implement the ClockLock and ClockBoost features. Altera supplies a utility called **genclklk**, which generates a model for the circuits. MAX+PLUS II and the **genclklk** utility also generate HDL simulation models.

Conclusion

As PLDs increase in density, on-clock distribution is increasingly important for device performance. The ClockLock circuit reduces clock delay and skew, and provides faster device-to-device performance. ClockBoost circuitry allows designers to create time-domain multiplexed designs via clock multiplication. Designers are also able to distribute a low-speed clock on the PCB, reducing layout issues. The combination of easy-to-use software and advanced on-device clock management provides high performance at high densities.

Customer APPLICATION

MAX 7000 Devices Speed VMIC to Market

"There is no other way to develop a board design this fast without the use of PLDs."
— Ed Danford, Design Manager, VMIC

The development of high-performance workstations has created the need for advanced networking technology. To fill this need, VME Microsystems International Corporation (VMIC) has developed reflective memory network boards for high-speed communication. With reflective memory, each board shares memory data with all other reflective memory boards on the network. VMIC reflective memory boards permit computers or workstations with varying operating systems—or no operating systems—to share data instantaneously.

Short Development Time Provides the Challenge

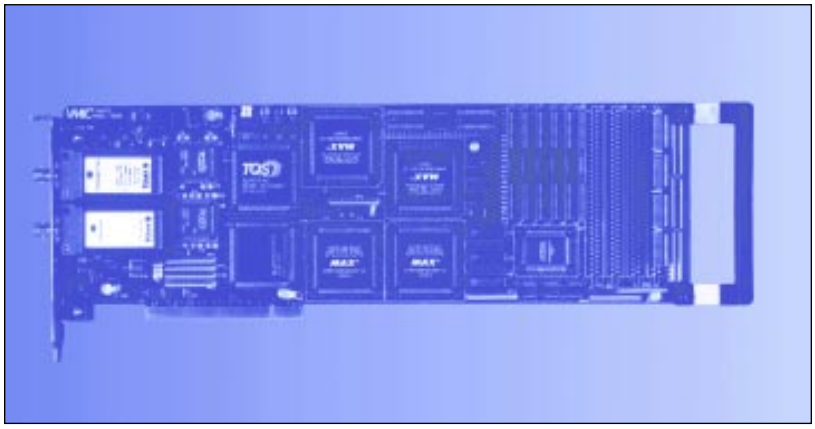
When VMIC designers set out to create the VMIPCI-5588 PCI-compliant reflective memory board, their goal was to produce a PCI bus reflective memory board that was network-compatible with VMIC's existing VME-based reflective memory board in a short time frame. See Figure 1. The final specifications for the board included:

- High-speed fiber-optic connection (1.2 Gbaud serially)
- Data transfer rate of 29.5 Mbytes per second without redundant transfer (14.8 Mbytes with redundant transfer)
- Error detection
- PCI interface
- Configurable endian conversions for multiple network architectures

VMIC designers had an aggressive development schedule for the VMIPCI-5588 board: they had 6 months to deliver prototypes, including design, board layout, and testing. Because of the short time frame, VMIC designers used programmable logic devices (PLDs) for the specialized logic on the board. Design manager Ed Danford stated, "There is no other way to develop a board design this fast without the use of PLDs."

If VMIC had used ASICs, simulation would have been much more costly and time-consuming. Design issues that take hours to resolve in PLDs require months with ASICs. In addition, the expected production volume of the VMIPCI-5588 board was not high enough to make developing an ASIC cost-effective. By using PLDs, VMIC was able to save time and expense. "I would estimate it would have been a year and a half to do this design with ASICs and it would have been very expensive," explained Danford.

Figure 1. VMIC VMIPCI-5588 Reflective Memory Board



MAX 7000 Meets the Challenge

VMIC used Altera MAX 7000 devices to perform the following functions (see Figure2):

- Transmit packet encoding (EPM7192EQC160-12)
- Receive packet decoding (EPM7192EQC160-12)
- Local bus arbitration and PCI secondary bus control (EPM7192EQC160-12 and EPM7096QC100-10)

One EPM7192E device obtains a packet of data from the input FIFO function, converts it from a 72-bit wide data word to three 32-bit transfers, and presents the three transfers to the ENDEC transmitter. Another EPM7192E device performs the inverse process for the ENDEC receiver. The devices also provide parity encoding during transmit operations and parity checking during receive operations to remove corrupt data transfers from the communications link. An EPM7192E and an EPM7096 provide interrupt logic, control logic, address control, and an endian swap buffer.

The data communications link for the VMIPCI-5588 runs at a serial rate of 1.2Gbaud. The data stream is converted to a 32-bit wide, 30-MHz data stream by Fibre Channel ASIC chip sets. The EPM7192E devices provide the interface to this data stream, convert it to a 72-bit wide data stream, and perform parity checking at the same time. In addition, the local bus portion of the design runs at 33MHz. Because of these timing constraints, VMIC used 10- and 12-ns MAX 7000 devices.

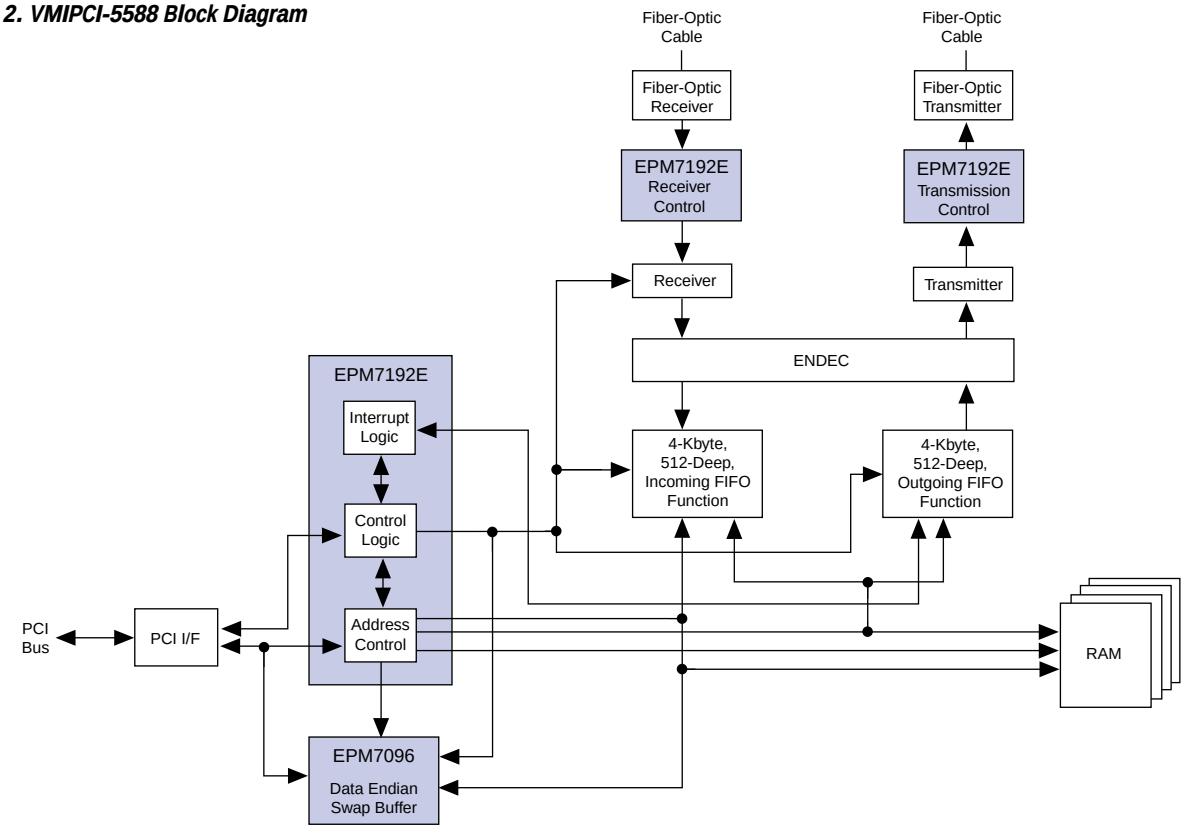
"MAX+PLUS II has been an excellent, unified design/simulation environment for EPLD development," said Danford. "We have always been successful in PLD development using MAX+PLUS II."

Software Tools Aid Development

Compilation and simulation for the initial design of the VMIPCI-5588 was performed using MAX+PLUS II. The resulting design was incorporated into

continued on page 21

Figure 2. VMIPCI-5588 Block Diagram



Questions & ANSWERS

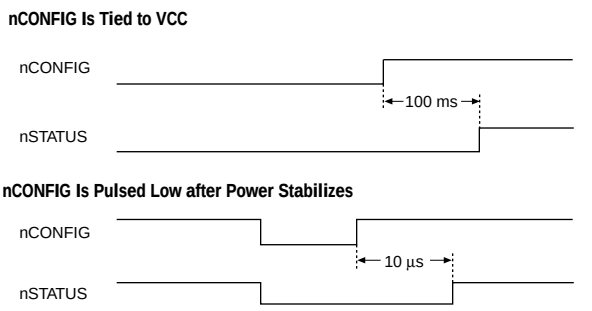
Q *When I try to compile my design for the EPF10K10T144, MAX+PLUS II version 7.0 won't create a Programmer Object File (**.pof**). What's wrong?*

A You must enter the password 4RT5XN for MAX+PLUS II version 7.0 to create a POF for the EPF10K10T144.

Q *When configuring FLEX devices, how long does it take* nSTATUS *to go high after* nCONFIG *is driven high?*

A During configuration, the FLEX device can receive configuration data after nCONFIG is driven high, nSTATUS is released, and nSTATUS is pulled high by the pull-up resistor. The delay between nCONFIG and nSTATUS being released depends on how nCONFIG is driven. If nCONFIG is tied to VCC and the FLEX device configures immediately upon power-up, nSTATUS will stay low for 100 ms after power-up. If nCONFIG is reset after the power is stabilized, the time difference is approximately 10 µs. See the following figure.

Waveforms for nCONFIG & nSTATUS



Q *I am using the mixed-voltage I/O capability of Altera devices. In what order should I power-up the* VCC *for the I/O and the internal* VCC*? Is there any time limit on the power-up sequence?*

A For most Altera devices with mixed-voltage I/O, the power-up sequence does not matter and no time limit exists; you can power-up the internal VCC while leaving the I/O VCC alone for a long period of time without harming the device.

FLEX 8000 devices configured in active mode with a serial configuration EPROM are an exception to this rule. The order of power-up does not matter. However, if the internal VCC is powered first, the I/O VCC must be powered within 100 ms to ensure successful configuration. If the I/O VCC is powered before the internal VCC, pins with design-controlled tri-state buffers will drive out.

Q *Why do I receive an error during in-system programming when a non-Altera device is in the JTAG chain?*

A When you include non-Altera devices in a JTAG chain, you must specify JTAG information for the non-Altera device in MAX+PLUS II by performing the following steps:

1. In the MAX+PLUS II Programmer, choose **Multi-Device JTAG Chain Setup** (JTAG menu).
2. Choose **JTAG Device Attributes**. The **JTAG Device Attributes** dialog box is displayed.
3. Enter the name, instruction register length, boundary scan length, and JTAG ID code for the non-Altera device. Choose **OK**.

When you choose **OK**, the information you entered about the non-Altera device is stored in a file named **jtaginfo.crf**. Usually, this file is stored in the **maxplus2** directory for PCs or the **/usr/maxplus2/common/** directory for workstations.

Q *When I try to install MAX+PLUS II on my PC, I receive the following error:*

```
Install caused a general protection fault in
module installw.bin
```

What's wrong?

A You need to include your CD-ROM drive in the path of your **autoexec.bat** file. For example:

```
path = C:\DOS; <CD-ROM drive letter>
```

Q I just installed the latest version of MAX+PLUS II on my PC. When I try to run the software, I receive errors that MAX+PLUS II cannot find several ***.dll*** *files. How can I get those files?*

A If you received this error after performing a full installation (i.e., not a custom installation), verify that you have a minimum of 16 MBytes of physical RAM and 16MBytes of permanent virtual RAM. Also, if you are running memory management software such as QEMM, turn the software off while you are installing MAX+PLUS II.

If you received this error after performing a custom installation of MAX+PLUS II, you may not have installed all of the files that MAX+PLUS II requires. You can install these missing files separately. For example, if you receive an error that you are missing the **j2p.dll** file, you can extract the file from the MAX+PLUS II installation CD-ROM by performing the following steps:

1. At a DOS command prompt, go to the **maxplus2** directory.
2. Type in the following command:

```
<CD-ROM drive>:\pc\maxplus2\maxzip -x
<CD-ROM drive>:\pc\prog\p.azp j2p.dll↵
```

The **j2p.dll** file will be extracted from the CD-ROM into the current directory.

Q I'm creating a VHDL design for an Altera device using Synopsys tools. How do I instantiate global buffers?

A You can use a Component Instantiation Statement to insert an instance of a primitive or macrofunction. For example:

```
COMPONENT global
     PORT (a_in :  IN STD_LOGIC;
          (a_out : OUT STD_LOGIC);
END COMPONENT;

BEGIN
     u1 : global
       PORT MAP (clk, gclk)
END;
```

Q When I try to bring an EDIF file into MAX+PLUSII from a third-party tool, I receive the following error:

`Can't find design file <filename>.`

What's wrong?

A If you do not have the most recent Altera libraries installed, you may receive this error. Verify that you are using current Altera libraries—MAX+PLUS II version 7.0 is available now, and version 7.1 will be available in December 1996.

Q I created a design for the EPX780 device, but I would like to use the EPX880 instead. How can I compile the design and program the EPX880?

A You can compile the design for the EPX880 device using Altera's PLDshell Plus software version5.1. This software is available for free on the Altera world-wide web site at **http://www.altera.com**. Program the EPX880 device as you would the EPX780 device, using the FLASHlogic Download Cable (ordering code PL-FLDLC). You can also use the ByteBlaster and MAX+PLUS II or PLDshell Plus to program EPX880 devices.

Now Available: Altera Digital Library CD-ROM

The Altera Digital Library contains an electronic version of all current Altera technical literature, including updates and supplements released after printing. The CD-ROM also provides a multimedia presentation on the FLEX 10K family. To obtain a copy of the Altera Digital Library, contact Altera Literature Services at (888) 3-ALTERA or send e-mail to **lit_req@altera.com**.

Altera
NEWS

Advantages of Carry Chains in FLEX 8000 Devices

Carry chains are high-speed data paths that connect adjacent logic elements (LEs) without using other interconnect resources. The carry chain operation in programmable logic architecture has a significant impact on the performance of arithmetic functions in a device. The FLEX 8000 carry chain provides a very fast (less than 1 ns) carry-forward function between LEs, which can implement the sum of a single-bit adder and carry-generation logic within a single LE. See Figure 1. Optimizing speed and efficiency, the FLEX 8000 carry chain provides twice the performance and uses 50% fewer logic resources than competing low-cost FPGAs.

In contrast, some FPGAs are less efficient because each logic cell only calculates a half sum; an adjacent logic cell must be used to complete the addition. See Figure2. Because the critical path in an FPGA adder or counter includes the additional logic cell required to implement the full-add operation, an additional logic delay is incurred, which results in significantly slower arithmetic performance.

While some FPGAs require an additional logic cell to initialize the carry chain, the FLEX 8000 LE can initialize its own carry chain. Where some FPGAs require two logic cells to implement the full addition, the FLEX 8000 architecture implements the same operation in a single LE. Implementing an n-bit counter requires $2n+1$ logic cells in some FPGAs and only n LEs in FLEX 8000 devices. Similarly in adders, an n-bit adder requiring $2n+1$ logic cells in some FPGAs, requires only $n+1$ LEs in FLEX 8000 devices. This resource efficiency is illustrated in Figure 3.

In the FLEX 8000 architecture, the carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, feeding into the look-up table (LUT) and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. Using the MAX+PLUS II Compiler, carry chains can be created automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 1. FLEX 8000 Carry Chain

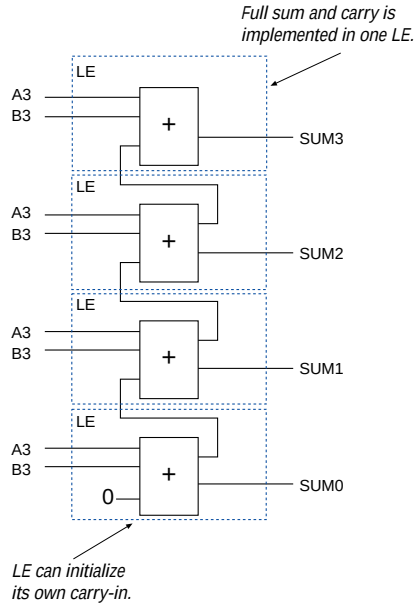
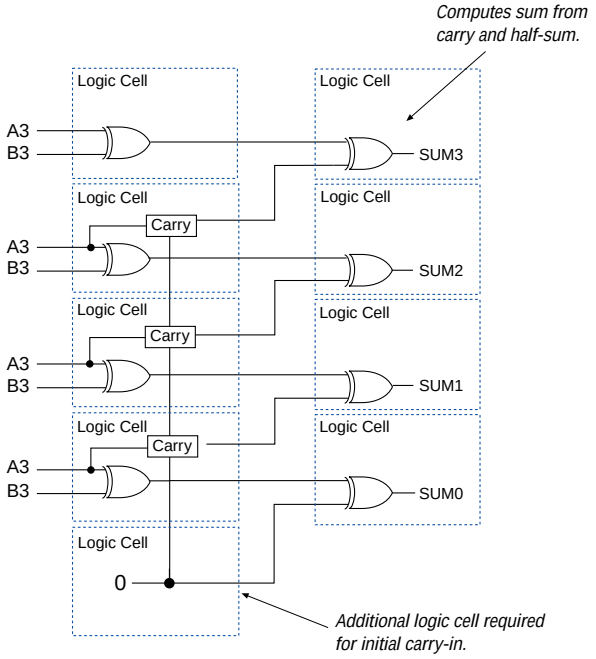
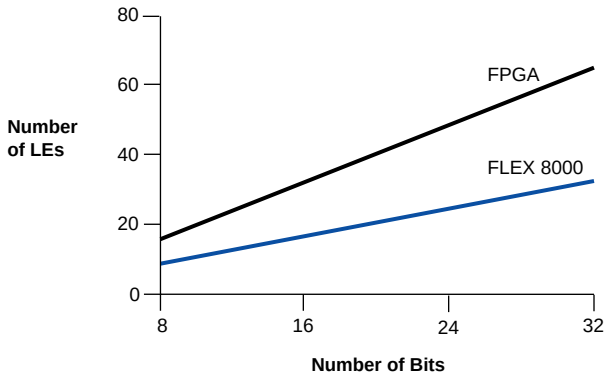


Figure 2. FPGA Carry Chain



Carry chains make FLEX 8000 devices the optimal solution for arithmetic-intensive applications such as digital signal processing. The architecture of the FLEX8000 device allows tradeoffs between speed, resource utilization, and easy fitting. FLEX 8000 devices provide twice the performance of comparable FPGAs and save the designer money by providing the flexibility to fit a given design into a smaller FLEX 8000 device.

Figure 3. Resource Efficiency of FLEX 8000 vs. FPGAs



Advantages of Redundancy in High-Density PLDs

The semiconductor manufacturing process demands cleanliness because it only takes one microscopic dust particle to damage a transistor. The transistor is the basic building block in any device and even one failing transistor can cause an entire device to fail. To eliminate transistor failure, semiconductor manufacturers have added redundant circuitry to high-density devices. Redundant circuits are "spare" functional blocks that can be substituted for defective blocks, without affecting the functionality or timing of a device.

With redundancy, manufacturers can save devices that were traditionally discarded due to defects. Therefore, redundancy results in higher yields and lower costs. For example, without redundancy, 16-Mbit and 64-Mbit DRAM would not be economically feasible. Redundancy significantly improves yields and reduces costs for these devices, making them competitive.

Because redundancy requires a slightly larger die, it is most effective in high-density devices. Altera's patented redundancy is used in the FLEX10K, FLEX8000, and MAX 9000 device families. For more information on redundancy in Altera devices, contact Altera Customer Marketing.

MAX 7000 Devices Speed VMIC to Market
continued from page 17

a schematic board design, which was used to lay out the board. During testing, as problems were found in the design, the VMIC designers performed additional simulation and made changes to the PLD design as necessary. Simulation was used to confirm fixes before the devices were reprogrammed.

VMIC used the Altera Hardware Description Language (AHDL) to create the designs for the MAX 7000 devices. The design team found that the easy-to-use MAX+PLUS II software simplified their task of determining if a device was fast enough to perform the desired logic task. "MAX+PLUS II has been an excellent, unified design/simulation environment for EPLD development," said Danford. "We have always been successful in PLD development using MAX+PLUS II."

Altera Provides Time-to-Market Advantage

With PLDs, many design errors can be corrected by simple reprogramming without having to change board layout. This process saves time and money when developing new products. "Time-to-market is very important to us, so we will choose the products that get us there as quickly as possible," Danford said. Using Altera's MAX 7000 devices and MAX+PLUS II software, VMIC was able to meet their aggressive time schedule: the VMIPCI-5588 reflective memory board got to market on time.

FLEX 10K vs. FPGA Performance

The Altera FLEX 10K programmable logic device (PLD) family combines the flexibility of programmable logic and the density and efficiency of embedded gate arrays. FLEX 10K devices contain both a logic array and an embedded array that can be used for RAM, ROM, or complex logic functions. With the added capability of the embedded array, the FLEX 10K family offers up to 100,000 gates—a breakthrough in programmable logic—and satisfies the density requirements of over 80% of gate array design starts (source: Dataquest). Altera's new FLEX 10KA family will provide up to 250,000 gates. Refer to "Altera Announces the 3.3-V FLEX 10KA Family" on page 1 for more information.

FLEX 10K Provides Faster Performance

The FLEX 10K family features the largest device in the programmable logic industry, and also provides faster performance than field-programmable gate arrays (FPGAs). In addition, with the introduction of new -3 speed grade and enhanced -4 speed grade devices, the FLEX 10K family further extends its performance leadership.

The following table compares the performance of FLEX10K devices and FPGAs. The data is based on the performance of Altera, Xilinx, and Lucent devices for industry-standard benchmarks.

FLEX 10K Performance Migration

FLEX 10K devices provide a high-density logic solution to gate array designs and faster performance than FPGAs. In general, the slowest FLEX 10K device can outperform the fastest FPGA. In addition, FLEX10K devices provide performance migration, which allows designers to migrate their designs to even higher-performance FLEX 10K devices. Rather than being restricted by the performance limitations of FPGAs, designers can use FLEX 10K devices to satisfy their highest-performance design needs. With higher density and higher performance, the Altera FLEX 10K device family offers a faster and more efficient design solution than FPGAs.

Comparison of FLEX 10K & FPGA Performance

Logic Implementation	PLD	FPGA	
	Altera FLEX 10K *(1)*	**Xilinx XC4000E-2**	**Lucent OR2C15A-4S208** *(2)*
FIR Filter (8-bit, 16-tap)	101 MSPS	65 MSPS, *Note (3)*	*Note (4)*
8 x 8 Multiplier (Pipelined)	125 MHz	52 MHz, *Note (5)*	89 MHz
8 x 8 Multiplier (Non-Pipelined)	38 MHz	28 MHz, *Note (5)*	15 MHz
12 x 12 Multiplier (Pipelined)	87 MHz	38 MHz, *Note (5)*	*Note (4)*
12 x 12 Multiplier (Non-Pipelined)	25 MHz	20 MHz, *Note (5)*	*Note (4)*
16 x 16 Multiplier (Pipelined)	75 MHz	*Note (4)*	55 MHz
16 x 16 Multiplier (Non-Pipelined)	23 MHz	18 MHz, *Note (5)*	7 MHz
256 x 8 RAM (Registered Inputs and Outputs)	105 MHz	80 MHz, *Note (6)*	*Note (4)*

Notes:

(1) Source: Altera Applications. Data is for -3 speed grade FLEX 10K devices.
(2) Source: *Synario App Review*, September 9, 1996, page 11.
(3) Source: *Xilinx XC4000 Series FPGA Product Specification*, ver. 1.02, page 4-3.
(4) No data reported.
(5) Source: *Synario App Review*, September 9, 1996, page 20.
(6) Source: *Xilinx XC4000 Series FPGA Product Specification*, ver. 1.02, page 4-3.

The Target Applications Advantage

The Altera Target Applications program provides tools for improving design cycles and supporting customer time to market. Currently, Target Applications focuses on three areas: digital signal processing (DSP), bus interfaces—peripheral component interconnect (PCI) and universal serial bus (USB)—and communications.

The *Target Applications Selector Guide*, planned for the end of 1996, will summarize Target Applications support with a complete listing of megafunctions, reference designs, and technical documentation. A Target Applications CD-ROM is also planned, which will provide a complete reference library for these applications, including reference designs and documentation.

DSP

Altera presented the FLEX DSP solution at the International Conference on Signal Processing Applications and Technology (ICSPAT)/DSP World Expo in Boston on October 7-10. Altera exhibited megafunctions for fast Fourier transform (FFT) functions and high-speed adaptive finite impulse response (FIR) filters, and the complete FLEX DSP solution. Altera presented the following two papers at the conference:

- *Tools for FFT Processor Design* discussed Altera's new fully parameterized FFT megafunction, which performs 1,024-point FFTs in 207 µs.
- *High-Speed Filtering Functions in Programmable Logic* discussed interpolation, decimation, and convolution in Altera FLEX architectures.

AMPP Functions

Integrated Silicon Systems Ltd. (ISS), a partner in the Altera Megafunction Partners Program (AMPP), specializes in advanced DSP ASICs and DSP ASIC megafunctions. The adaptive FIR filter megafunction from ISS operates at over 90 MHz and is ideal for high-speed applications. The ISS infinite impulse response (IIR) filter is fully parameterized and ready for delivery. Contact ISS directly for more information on their library of DSP megafunctions. Object Oriented Hardware, another AMPP partner, has produced a Reed-Solomon CODEC function. See page 24.

MegaCore Functions

DSP megafunctions to support FFT and adaptive FIR filter designs will be available as a migration product to MAX+PLUS II version 7.1. For more information on the FFT MegaCore function, go to "Fast Fourier Transform Function Available in December" on page 6. Performance for the FFT MegaCore function from Altera is summarized in the table below.

FFT Performance

Length (Points)	Precision	Memory	Logic Cells	Speed
512	8 Data, 8 Twiddle	Dual-Internal	1,150	94 µs
512	12 Data, 12 Twiddle	Dual-Internal	1,970	94 µs
1,024	16 Data, 16 Twiddle	Dual-Internal	2,993	207 µs
32 K	16 Data, 16 Twiddle	Dual-Internal	3,100	9.8 ms

Bus Interfaces

PCI megafunctions are now available from the AMPP program and Altera's MegaCore program. Eureka Technology, an AMPP partner, has delivered target megafunctions running at 33 MHz; the Altera MegaCore master/target megafunction will be available in December 1996.

CAE Technology and Sand Microelectronics provide USB megafunctions, including drivers, firmware, and test/verification. For more information, go to the Altera world-wide web site at **http://www.altera.com**.

Communications

Altera's FLEX devices combine design flexibility and high performance to provide the ideal solution for asynchronous transfer mode (ATM) designs. The Reed Solomon CODEC from Object Oriented Hardware, a new communications megafunction, is featured on page 24. Optimized for the FLEX 10K architecture, the Reed-Solomon CODEC function provides a complete solution for implementing both encoding and decoding.

Reed-Solomon CODEC Megafunction

ALTERA MEGAFUNCTION PARTNERS PROGRAM

Target Applications: *Communications, Digital Signal Processing*
Device Family: *FLEX 10K*
Vendor: *Object Oriented Hardware*
10-16 Tiller Road
Docklands, London E14 8PX
England, UK
Tel. 44 (0) 7000 664664
Fax 44 (0) 7000 664329
Fax 44 (0) 171 538 2323
WWW http://www.ooh.com

Features

- Foundry Independent Standard Product (FISP)
- Fully parameterized
- Corrects up to 2*n* erasures or *n* errors per block
- Continuous or burst mode operation
- Programmable generator and primitive polynomials
- Complies with Intelsat IESS-308, Revision 6B or RTCA DO-217 Appendix F, Revision D
- Independent encoding and decoding
- Statistics and error rate gathering options
- Fully synthesizable VHDL-RTL code
- Interface ports
  - Support for serial and parallel data formats
  - FISPbus generic microprocessor interface
- Applications
  - Satellite communications
  - Digital video
  - Magnetic and optical tape and disk drives
  - High performance modems
  - Local and wide area networks

General Description

The Reed-Solomon CODEC megafunction provides a complete solution for encoding and decoding data. The megafunction also provides statistical information about the number of correctable and uncorrectable errors that occur over the decoder channel. It is implemented in VHDL and is optimized for the Altera FLEX 10K device architecture.

Reed-Solomon Encoder

The encoder receives raw data and adds check symbols. The codeword length and the number of check symbols are assigned using the FISPbus interface or via direct inputs to the data block. The output produces the original data with the check symbols appended. The delay between input and output depends directly on the number of check symbols and the clocking mode. See Figure 1.

Reed-Solomon Decoder

The Reed-Solomon decoder can correct up to *n* symbol errors or 2*n* erasures in each block of data. The received data can be continuous and the delay between input and corrected output is independent of the number of errors or erasures. The time required to perform the correction depends on the codeword length and the number of check bits. The decoder accepts data in either serial or parallel; the start of the block and any erasure symbols are flagged. The decoder sequence, illustrated in Figure2, is summarized below:

- Syndrome and error locator polynomials are generated.
- Modified Euclid algorithm is performed.
- Chien search is performed.
- Statistical information is generated.

Figure 1. Reed-Solomon Encoder

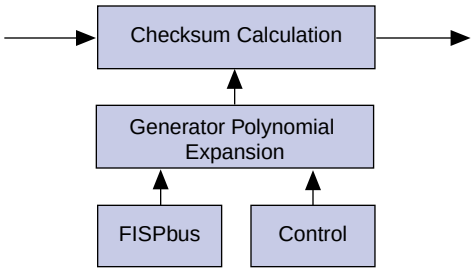
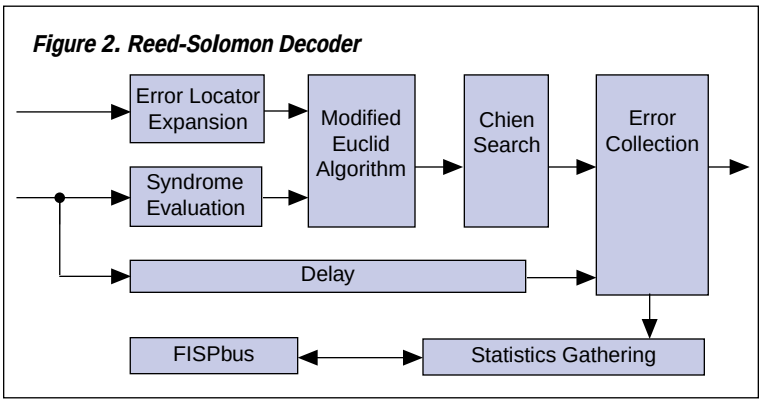


Figure 2. Reed-Solomon Decoder



Reed-Solomon CODEC Parameters

The following table summarizes the parameters that can be defined by the user.

Reed-Solomon CODEC Parameters	
Parameter	**Description**
Number of symbols in the longest codeblock	Expressed as two figures, (*n*, *k*), where *n* is the number of symbols in the codeblock after check bits are added, and *k* is the original data length. The largest value of *n* sets the required size of the Galois field.
Symbol width	Number of bits required to represent the maximum codeblock length in binary.
Required check bits and differing values of *n* and *k*	Each corrected error requires two check bits. For correction codes, this value is the maximum value of *n* and *k*. A small number of check bits reduces the encoder size.
Primitive polynomial	Normally expressed in the form: $P(x) = xm + xa + xb + xc + ... + 1$
Generator polynomial	The generator polynomial is shown below (where R is the number of check bits): $G(x) \prod_{j=B}^{(B-1)+R} (x - \alpha^j)$
Number of erasures	Errors at known positions. Erasures at fixed positions (i.e., end of codeblock) enable logic savings.
System clock frequency	High clock frequencies reduce the latency (and hence the size of the delay line) in the decoder.
Statistic gathering functions	Typically counters for errors corrected, uncorrectable codeblocks, and codeblocks received.
Serial or parallel data interfaces	Internal data paths are parallel. If serial interfaces are needed, shift registers can be added.

In Every ISSUE

Altera Device Selection Guide

All current information for the Altera FLEX 10K, FLEX 8000, MAX 9000, and MAX 7000 devices is listed here. Information on other Altera products is located in the Altera ***1996 Data Book***. Contact Altera or your local sales office for current product availability.

FLEX 10K Devices

Device	Typical Gates	Pin/Package Options	I/O Pins *(1)*	Temp.	Speed Grade	Flip-flops	Logic Elements	RAM Bits
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	C	-3	720	576	6,144
EPF10K10	10,000	84-Pin PLCC, 144-Pin TQFP, 208-Pin PQFP	59, 102, 134	C, I	-4	720	576	6,144
EPF10K20	20,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C	-3	1,344	1,152	12,288
EPF10K20	20,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C, I	-4	1,344	1,152	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	C	-3	1,968	1,728	12,288
EPF10K30	30,000	208-Pin RQFP, 240-Pin RQFP, 356-Pin BGA	147, 189, 246	C, I	-4	1,968	1,728	12,288
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C	-3	2,576	2,304	16,384
EPF10K40	40,000	208-Pin RQFP, 240-Pin RQFP	147, 189	C, I	-4	2,576	2,304	16,384
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	C	-3	3,184	2,880	20,480
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	C	-4	3,184	2,880	20,480
EPF10K50	50,000	240-Pin RQFP, 356-Pin BGA, 403-Pin PGA	189, 274, 310	C, I	-5	3,184	2,880	20,480
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	C	-3	4,096	3,744	18,432
EPF10K70	70,000	240-Pin RQFP, 503-Pin PGA	189, 358	C, I	-4	4,096	3,744	18,432
EPF10K100	100,000	503-Pin PGA	406	C	-3	5,392	4,992	24,576
EPF10K100	100,000	503-Pin PGA	406	C, I	-4	5,392	4,992	24,576

(1) Six I/O pins are dedicated inputs.

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Altera Device Selection Guide
continued from page 25

FLEX 8000 Devices

Device	Usable Gates	Pin/Package Options	I/O Pins *(1)*	Temp.	Speed Grade	Flip-flops	Logic Elements
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C	A-2	282	208
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-3	282	208
EPF8282A	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C, I	A-4	282	208
EPF8282AV *(2)*	2,500	84-Pin PLCC, 100-Pin TQFP	68, 78	C	A-4	282	208
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C	A-2	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C, I	A-3	452	336
EPF8452A	4,000	84-Pin PLCC, 100-Pin TQFP, 160-Pin PGA/PQFP	68, 120	C, I	A-4	452	336
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 110, 136	C	A-2	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 110, 136	C	A-3	636	504
EPF8636A	6,000	84-Pin PLCC, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP	68, 110, 136	C, I	A-4	636	504
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	120, 152	C	A-2	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	120, 152	C	A-3	820	672
EPF8820A	8,000	144-Pin TQFP, 160-Pin PQFP, 192-Pin PGA, 208-Pin PQFP, 225-Pin BGA	120, 152	C, I	A-4	820	672
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C	A-2	1,188	1,008
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-3	1,188	1,008
EPF81188A	12,000	208-Pin PQFP, 232-Pin PGA, 240-Pin PQFP	148, 184	C, I	A-4	1,188	1,008
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-2	1,500	1,296
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C, I	A-3	1,500	1,296
EPF81500A	16,000	240-Pin PQFP, 280-Pin PGA, 304-Pin RQFP	181, 208	C	A-4	1,500	1,296

(1) Four I/O pins are dedicated inputs.
(2) V indicates 3.3-V voltage supply.

MAX 9000 Devices

Device	Macrocells	Pin/Package Options	I/O Pins (1)	Temp.	Speed Grade
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA	60, 132, 168	C	-15
EPM9320	320	84-Pin PLCC, 208-Pin RQFP, 280-Pin PGA	60, 132, 168	C, I	-20
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C	-15
EPM9400	400	84-Pin PLCC, 208-Pin RQFP, 240-Pin RQFP	59, 139, 159	C, I	-20
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C	-15
EPM9480	480	208-Pin RQFP, 240-Pin RQFP	146, 175	C, I	-20
EPM9560	560	208-Pin CQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP	153, 191, 216	C	-15
EPM9560	560	208-Pin CQFP, 240-Pin RQFP, 280-Pin PGA, 304-Pin RQFP	153, 191, 216	C, I	-20

(1) Four I/O pins are dedicated inputs.

MAX 7000 Devices

Device	Macrocells	Pin/Package Options	I/O Pins *(1)*	Temp.	Speed Grade	t_{PD} (ns)	f_{CNT} (MHz)
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-5	5	178.6
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-6	6	150
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C	-7	7.5	125
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C, I	-10	10	100
EPM7032	32	44-Pin PLCC/TQFP	36	C, I	-12	12	90.9
EPM7032, EPM7032S	32	44-Pin PLCC/TQFP	36	C, I	-15	15	76.9
EPM7032V *(2)*	32	44-Pin PLCC/TQFP	36	C	-12	12	90.9
EPM7032V *(2)*	32	44-Pin PLCC/TQFP	36	C	-15	15	76.9
EPM7032V *(2)*	32	44-Pin PLCC/TQFP	36	C, I	-20	20	62.5
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-6	6	150
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-7	7.5	125
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C, I	-10	10	100
EPM7064	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C	-12	12	90.9
EPM7064, EPM7064S	64	44-Pin PLCC/TQFP, 68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	36, 52, 68	C, I	-15	15	76.9
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-6	6	150
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-7	7.5	125
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C, I	-10	10	100
EPM7096	96	68-Pin PLCC, 64-Pin PLCC, 100-Pin PQFP	52, 64, 76	C	-12	12	90.9
EPM7096, EPM7096S	96	68-Pin PLCC, 84-Pin PLCC, 100-Pin PQFP	52, 64, 76	C, I	-15	15	76.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-7	7.5	125
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-10(P)	10	100
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12	12	90.9
EPM7128E, EPM7128S	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-15	15	76.9
EPM7128E	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20	20	62.5
EPM7128SV *(2)*	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 100	C	-10	10	100
EPM7128SV *(2)*	128	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 100	C	-15	15	76.9
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 104	C	-7	7.5	125
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 104	C, I	-10(P)	10	100
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C	-12	12	90.9
EPM7160E, EPM7160S	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	64, 84, 104	C, I	-15	15	76.9
EPM7160E	160	84-Pin PLCC, 100-Pin PQFP, 160-Pin PQFP	68, 84, 100	C, I	-20	20	62.5
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA	124	C	-7	7.5	125
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA	124	C	-10	10	100
EPM7192E	192	160-Pin PQFP/PGA	124	C	-12(P)	12	90.9
EPM7192E, EPM7192S	192	160-Pin PQFP/PGA	124	C, I	-15	15	76.9
EPM7192E	192	160-Pin PQFP/PGA	124	C, I	-20	20	62.5
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C	-7	7.5	125
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C	-10	10	100
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C	-12(P)	12	90.9
EPM7256E, EPM7256S	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C, I	-15	15	76.9
EPM7256E	256	160-Pin PQFP, 192-Pin PGA, 208-Pin RQFP	132, 164	C, I	-20	20	62.5

(1) Four I/O pins are dedicated inputs.
(2) V indicates 3.3-V voltage supply.

Data I/O Programming Support

Data I/O provides programming hardware support for select Altera devices. Algorithms are supplied via Data I/O's Keep Current Express - Bulletin Board Service (KCE-BBS). Programming support for Configuration EPROM, MAX 9000, MAX 7000, and FLASHlogic devices is shown below. All information is subject to change. Data I/O customers with a current maintenance agreement can obtain qualified algorithms electronically from the KCE-BBS.

The following Configuration EPROM devices are supported by the 2900 version 5.3, the 3900 version 5.3, and UniSite version 5.3 (Hex Files only).

- EPC1213P-8
- EPC1213L-20
- EPC1064P-8
- EPC1064L-20
- EPC1064T-20
- EPC1064VL
- EPC1064VT
- EPC1P-8
- EPC1LC-20

The following MAX 9000, MAX 7000, and FLASHlogic devices are supported by the 3900 version 5.3 and UniSite version 5.3.

MAX 9000 Devices

- EPM9320LC84
- EPM9320GC280
- EPM9320RC208
- EPM9400RC208
- EPM9400RC240
- EPM9480RC208
- EPM9480RC240
- EPM9560GC280
- EPM9560RC240
- EPM9560WC208
- EPM9560RC304

MAX 7000 Devices

- EPM7032L-44
- EPM7032Q-44
- EPM7032T-44
- EPM7032VL-44
- EPM7032VT-44
- EPM7064L-44
- EPM7064L-68
- EPM7064L-84
- EPM7064Q-100
- EPM7096L-68 (EPROM)
- EPM7096L-84 (EPROM)
- EPM7096Q-100 (EPROM)
- EPM7096L-68 (EEPROM)
- EPM7096L-84 (EEPROM)
- EPM7096Q-100 (EEPROM)
- EPM7128L-84
- EPM7128Q-100
- EPM7128Q-160
- EPM7128EL-84
- EPM7128EQ-100
- EPM7128EQ-160
- EPM7160L-84
- EPM7160Q-160
- EPM7160EL-84
- EPM7160EQ-100
- EPM7160EQ-160
- EPM7192G-160
- EPM7192Q-160
- EPM7192EG-160
- EPM7192EQ-160
- EPM7256G-192
- EPM7256W-208
- EPM7256M-208
- EPM7256EG-192
- EPM7256EG-160
- EPM7256ER-208

FLASHlogic Devices

- EPX880

Software Utilities

eau000.exe Overview of electronic utilities
eau003.exe EP310 to EP330 JEDEC File converter
eau005.exe JEDPACK JEDEC File compactor
eau007.exe JEDSUM JEDEC checksum generator
eau017.exe LEF2AHDL converts A+PLUS LEF files to AHDL
eau018.exe PLD2EQN PAL/GAL/PLA file converter
eau019.exe ABEL2MAX file converter
eau020.exe PASM2TDF PALASM file converter
eau022.exe PLA2PDS PLA to PALASM file converter

Utilities are available from the Altera BBS via modem at (408) 954-0104 and the Altera FTP site at **ftp.altera.com**.

Programming Hardware Compatibility

The following tables contain the latest programming hardware information. To ensure correct programming, you should always use the software version shown in "Current Software Versions" below. PLM-prefix adapters can be used only with the Master Programming Unit (MPU).

Programming with the BitBlaster & ByteBlaster

Device	Package	Hardware
FLEX 10K	All packages	PL-BITBLASTER PL-BYTEBLASTER
FLEX 8000	All packages	PL-BITBLASTER PL-BYTEBLASTER
MAX 9000	All packages	PL-BITBLASTER PL-BYTEBLASTER
MAX 7000S	All packages	PL-BITBLASTER PL-BYTEBLASTER
EPX880	All packages	PL-BITBLASTER PL-BYTEBLASTER, *Note (1)*
FLASHlogic	All packages	PL-FLDLC, PL-BITBLASTER, PL-BYTEBLASTER *Notes (1), (2)*

Current Software Versions

The latest versions of Altera software products are shown below:

- MAX+PLUS II version 7.1, available December 1996 (PC, Sun SPARCstation, HP 9000 Series 700, and IBMRISC System/6000 platforms)
- PLDshell Plus version 5.1 (PC only)

Programming Adapters

Device	Package	Adapter
EPC1064, EPC1064V, EPC1213 (all FLEX 8000 devices), *Note (3)*	DIP, J-lead TQFP	PLMJ1213 PLMT1064
EPC1 (all FLEX 10K and FLEX 8000 devices), *Note (3)*	DIP J-lead	PLMJ1213 PLMJ1213
EPM9320	PGA J-lead (84-pin) RQFP (208-pin)	PLMG9000-280 PLMJ9320-84 PLMR9000-208
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240
EPM9480	RQFP (208-pin) RQFP (240-pin)	PLMR9000-208 PLMR9000-240
EPM9560	PGA RQFP (208-pin) RQFP (240-pin) RQFP (304-pin)	PLMG9000-280 PLMR9000-208 PLMR9000-240 PLMR9000-304
EPM7032, EPM7032V	J-lead PQFP TQFP	PLMJ7000-44 PLMQ7000-44 PLMT7000-44
EPM7064	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100
EPM7128, EPM7128E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7160, EPM7160E	J-lead PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160
EPM7192, EPM7192E	PGA PQFP	PLMG7192-160 PLMQ7192/7256-160
EPM7256E	PGA MQFP, RQFP PQFP	PLMG7256-192 PLMR7256-208 PLMQ7192/7256-160
EPX780	J-lead	PLMJ780-84
MAX 5000 devices	All packages	*Note (4)*
Classic devices	All packages	*Note (4)*
EPS448	All packages	*Note (4)*

Notes to tables:

(1) MAX+PLUS II version 7.0 and higher provides programming support for all FLASHlogic devices via the BitBlaster and ByteBlaster.

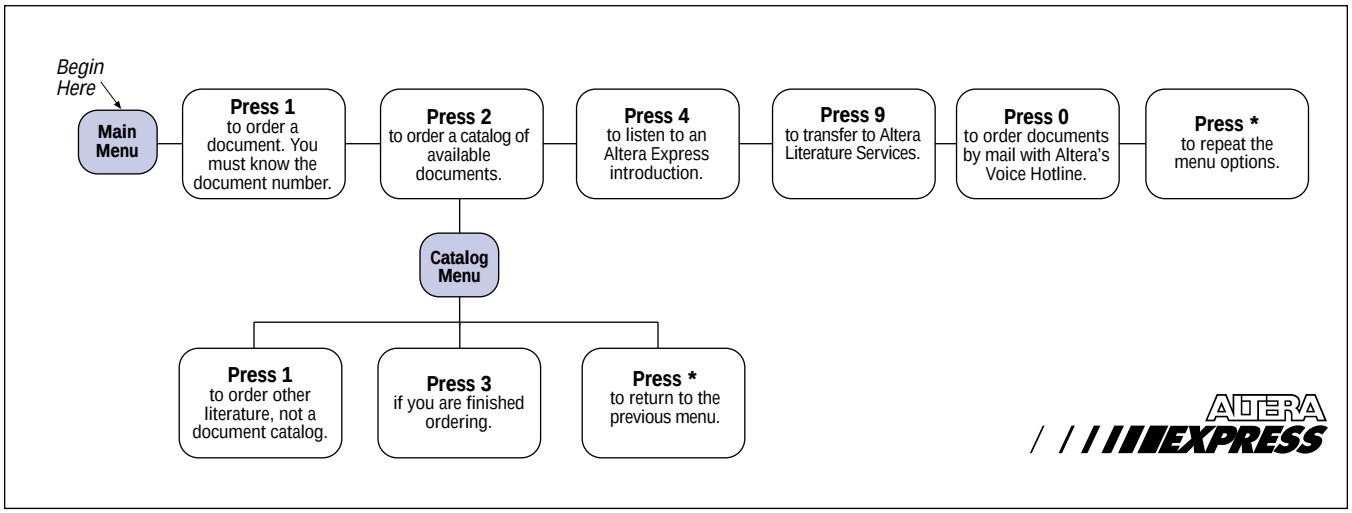
(2) You can use the FLASHlogic Download Cable (PL-FLDLC) with PLDshell Plus to program and configure all FLASHlogic devices.

(3) The hardware products for these devices are included with the FLEX Download Cable.

(4) Refer to the Altera ***1996 Data Book*** for device adapter information. Altera offers an adapter exchange program for 0.8-micron EPM5032, EPM5064, and EPM5130 programming adapters. See "Product Transitions" on page 5 of this newsletter for more information.

How to Request Altera Publications

Altera publications are available through Altera Express, a 24-hour, 7-day-a-week, automated fax service. In the U.S. and Canada, call (800) 5-ALTERA; international callers can retrieve information by calling (408) 894-7850 from a fax phone. See the following figure. Documents can also be obtained from Altera Literature Services at (888) 3-ALTERA or the Altera world-wide web site at **http://www.altera.com**.



How to Access Altera

Getting information and services from Altera is now easier than ever. The table below lists some of the ways you can reach Altera:

Altera Contact Information

Information Type	Access	U.S. & Canada	All Other Locations
Literature	Altera Express	(800) 5-ALTERA	(408) 894-7850
	Altera Literature Services	(888) 3-ALTERA lit_req@altera.com	(408) 894-7144 *(1)* lit_req@altera.com
	World-Wide Web	http://www.altera.com	http://www.altera.com
Non-Technical Customer Service	Telephone Hotline	(800) SOS-EPLD	(408) 894-7000
	Fax	(408) 954-8186	(408) 954-8186
Technical Support	Telephone Hotline (8 a.m. to 5 p.m. Pacific Time)	(800) 800-EPLD (408) 894-7000	(408) 894-7000 *(1)*
	Fax	(408) 954-0348	(408) 954-0348 *(1)*
	Bulletin Board Service	(408) 954-0104	(408) 954-0104
	Electronic Mail	sos@altera.com	sos@altera.com
	FTP Site	ftp.altera.com	ftp.altera.com
	CompuServe	go altera	go altera
General Product Information	Telephone	(408) 894-7104	(408) 894-7104 *(1)*
	World-Wide Web	http://www.altera.com	http://www.altera.com

Note:
(1) You can also contact your local Altera sales office or sales representative. See the Altera ***1996 Data Book*** for a list of sales offices and representatives.

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