Bringing ARM7™ to the Masses

White Paper

April 2006

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Market Environment

As performance requirements increase, the implementation of control elements in embedded applications is moving from 8 bits to 32 bits. At the same time, the implementation vehicle of choice for embedded applications is changing from ASICs to FPGAs due to cost and time to market pressures. This paradigm shift is causing significant change in the choices designers are making for the execution of embedded applications. This is most evident in consumer, industrial, and automotive applications, which are the fastest growing segments of the FPGA market. The ARM7 processor is widely used in these segments. Implementing the ARM7 processor in Actel Flash-based devices allows users to take maximum advantage of this industry standard processor as well as the changes that are occurring in the embedded market.

There are a number of other soft intellectual property (IP) processor solutions available for implementation in FPGAs, but all of these are based on proprietary architectures with limited tools, support, and designer experience. The ARM7 processor, in contrast to these proprietary processors, is an industry standard architecture with a huge ecosystem of tools, support, and embedded designer knowledge. It is the most widely implemented 32-bit processor, with billions in use. As a result, new development tools are created for ARM® first, and all major design houses have experience with ARM7 designs.

To enable embedded designers to take advantage of the ARM7 processor with programmable logic, Actel and ARM have worked together to minimize the size and maximize the speed of the processor for Actel ARM-enabled M7 ProASIC®3, ProASIC3E, and M7 Fusion FPGAs. These Flash-based FPGA devices are ideal for use in consumer, industrial, and automotive applications, further enhancing the benefit and usability of the ARM7 processor. To ease implementation of ARM7 in M7 devices, Actel has created a full development tool suite, which includes the Actel Libero® Integrated Design Environment (IDE) tools and a new frontend tool, CoreConsole. CoreConsole enables users to quickly implement a processor subsystem and assemble their system-level designs. Combining the flexibility of Actel Flash-based devices with the industry standard ARM7 creates a complete and powerful product that is easy to use. Actel and ARM are bringing a superior solution to market that will greatly expand the usability of ARM7 for everything from high-volume to low-volume and prototype applications. In effect, Actel is making ARM7 available to the masses.

Embedded Market Change

Until recently, the embedded market has been primarily the domain of 8-bit microcontrollers. While embedded applications existed for 32-bit processors, they were limited to a few high-performance areas. The level of processing required for many embedded applications is increasing dramatically due to the convergence of communication and consumer applications and the delivery of higher levels of content, including video and high-end audio. This is driving the increasing usage of 32-bit processors in system-level integration (SLI) applications. A common requirement that runs through the consumer, automotive, industrial, and military/aerospace markets is the growing need for a 32-bit processor, driven by the increasing sophistication and complexity of the designs in these markets. Figure 1 on page 4 shows the forecasted change in embedded designs that incorporate a processor.

At the same time, a transition is occurring in SLI implementation. Designs in markets from communications to consumer and automotive are moving from ASICs to FPGAs due to increasing mask and silicon costs. As ASIC development costs increase, the break-even volume required to justify the expense is also increasing, pushing a larger number of designs into programmable devices. Figure 2 on page 4 shows the forecasted changes in the percentage distribution of the FPGA markets from 2002 to 2008.

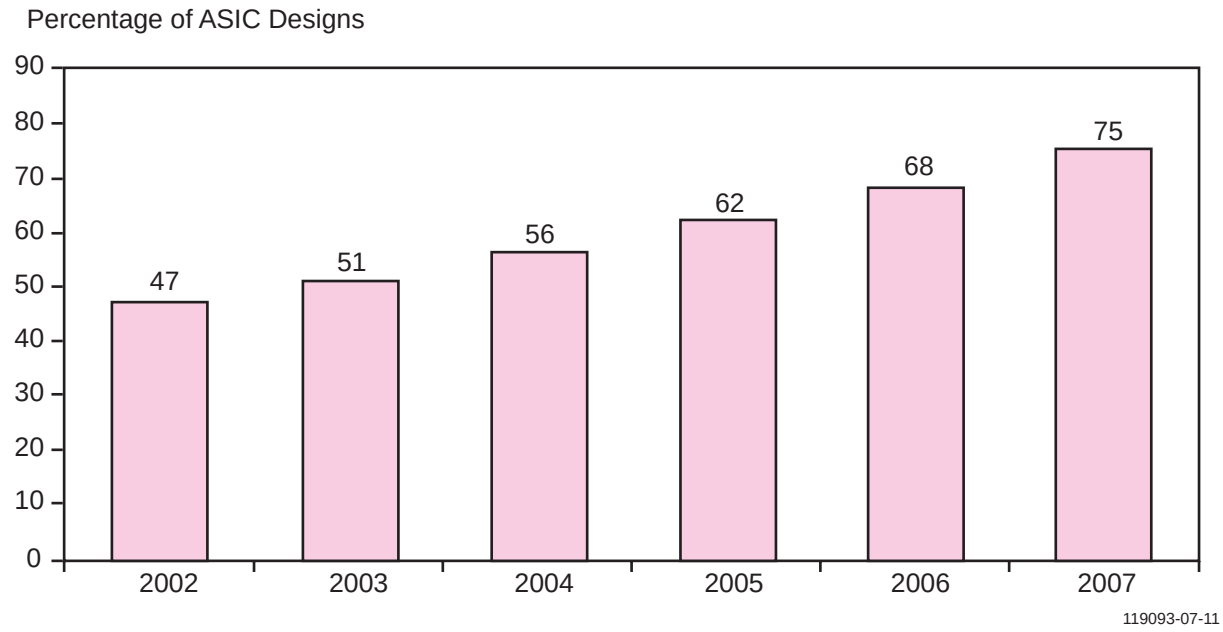

Figure 1: **Percentage of SLI Implementation in Embedded Designs[1]**

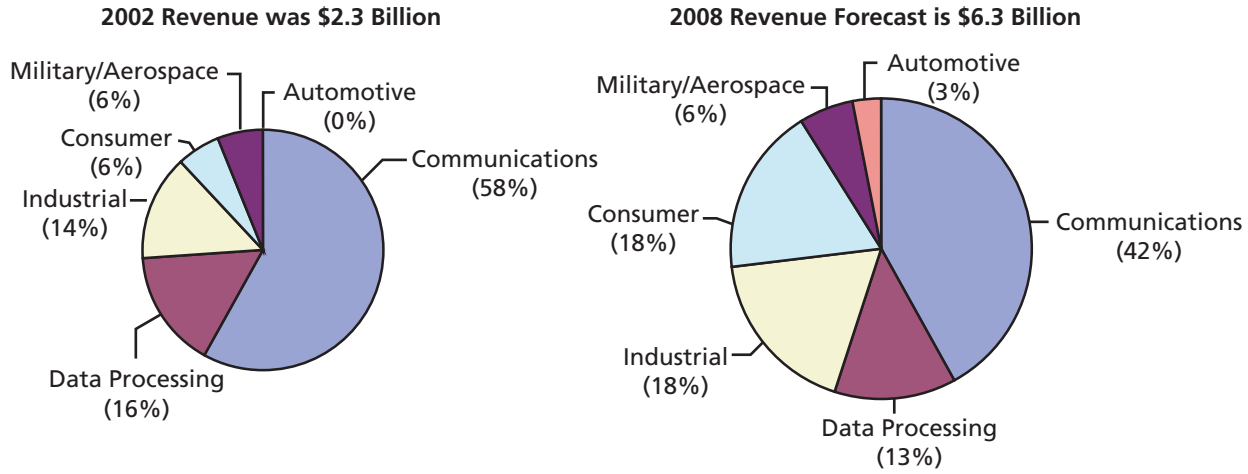

Figure 2: **FPGA Market Segment Changes from 2002 to 2008[1]**

The same market and process dynamics that are causing ASIC costs to increase are also reducing the cost per gate of FPGAs, and allowing a dramatic increase in the level of integration within these devices. This is leading to larger devices that are capable of supporting complex system-level applications. Just a few years ago, such applications could only be implemented in ASICs. When coupled with the fast time to market that FPGAs offer, this implementation shift will continue, presenting programmable logic vendors with a huge market opportunity.

1. *Gartner Dataquest (December 2003).*

ARM7 Synergy with ProASIC3/E and Fusion

The architecture with the largest share of the market and the highest name recognition in the 32-bit embedded space is ARM. The ARM architecture holds an incredible 80 percent share of the market. As a result, there is a huge selection of hardware and software development tools that support ARM7. There is also broad industry knowledge and experience with ARM7. Both of these factors benefit designers because there is a huge volume of existing program code and many tools that can be used for system-level designs, reducing risk and time to market.

There are a growing number of microcontroller suppliers (more than 10) who are selling ARM7-based microcontrollers. While it may seem counterintuitive to pursue a market with the same processor that the microcontroller vendors are offering, it is an excellent strategy if the timing is right and the processor ends up dominating the market. A microcontroller is a good solution for an embedded design if the part has all of the features needed for the application. Often this is not the case and the designer must use an external part (usually an FPGA) with the microcontroller to incorporate the needed functionality. The implementation of a soft ARM7 processor in an Actel M7 ProASIC3/E or M7 Fusion FPGA gives designers the flexibility to achieve their design requirements and keep everything in one chip. ARM7 is poised to dominate the 32-bit embedded space, which is why so many microcontroller vendors are developing products based on it. The market is still small but growing rapidly, and there is not yet a dominant player. This gives Actel and its customers the opportunity to enter into the market, become established, and grow along with the 32-bit embedded space, also taking advantage of the benefits that ARM7 offers.

The ARM7 family processor is synergistic with the Actel Flash-based ProASIC3/E and Fusion FPGA families. Both target the consumer and industrial markets, and there is growing interest in ARM7 for use in military applications, a market Actel has served for many years. Actel M7 devices offer ARM a unique vehicle for the deployment of the ARM7 processor. Not only are these devices programmable and low cost, but they are also single-chip and highly secure, offering ARM an ideal vehicle to increase access to ARM7 while protecting the processor IP. In addition, Actel Fusion devices are the only mixed-signal FPGAs available, and when combined with ARM7, offer powerful single-chip solution designs. This synergy with Actel Flash devices has been recognized by ARM, and is beneficial to designers because ARM7 in M7 devices offers a unique and programmable industry standard solution for embedded SLI designs.

CoreMP7 Features

The Actel CoreMP7 is a soft IP version of the popular ARM7TDMI-S™ core that has been optimized to maximize speed and minimize size in Actel M7 ProASIC3/E and M7 Fusion FPGAs. CoreMP7 executes the ARMv4T instruction set architecture with the Thumb® extensions. The processor has a 3-stage pipeline, 32-bit ALU, 32-bit register file, a single external address and data bus interface unit, and JTAG debug interface with support for on-chip trace.The main features and benefits of the CoreMP7 soft IP ARM7 family processor are as follows:

- Compatible with the ARM7TDMI-S processor
- 32/16-bit RISC ARMv4T architecture
- 32-bit ARM instruction set
- 16-bit Thumb instruction set
- 32-bit Arithmetic Logic Unit
- 3-stage pipeline
- 32-bit external bus interface – both Advanced High-Performance Bus (AHB) and native ARM7 bus
- Embedded real-time debug – JTAG interface
- Optimized for Actel Flash-based ProASIC3/E and Fusion FPGA devices
- Implemented fully in the fabric
- All I/Os are accessible to the user
- Users can add and connect their IP to the processor
- CoreMP7 and user IP can be erased and reprogrammed into the devices
- Support for secure in-system programming
- Seamless FPGA design and debug tool flow and integration

The CoreMP7 soft IP processor top-level block diagram is identical to ARM7TDMI-S, shown in Figure 3 on page 7.

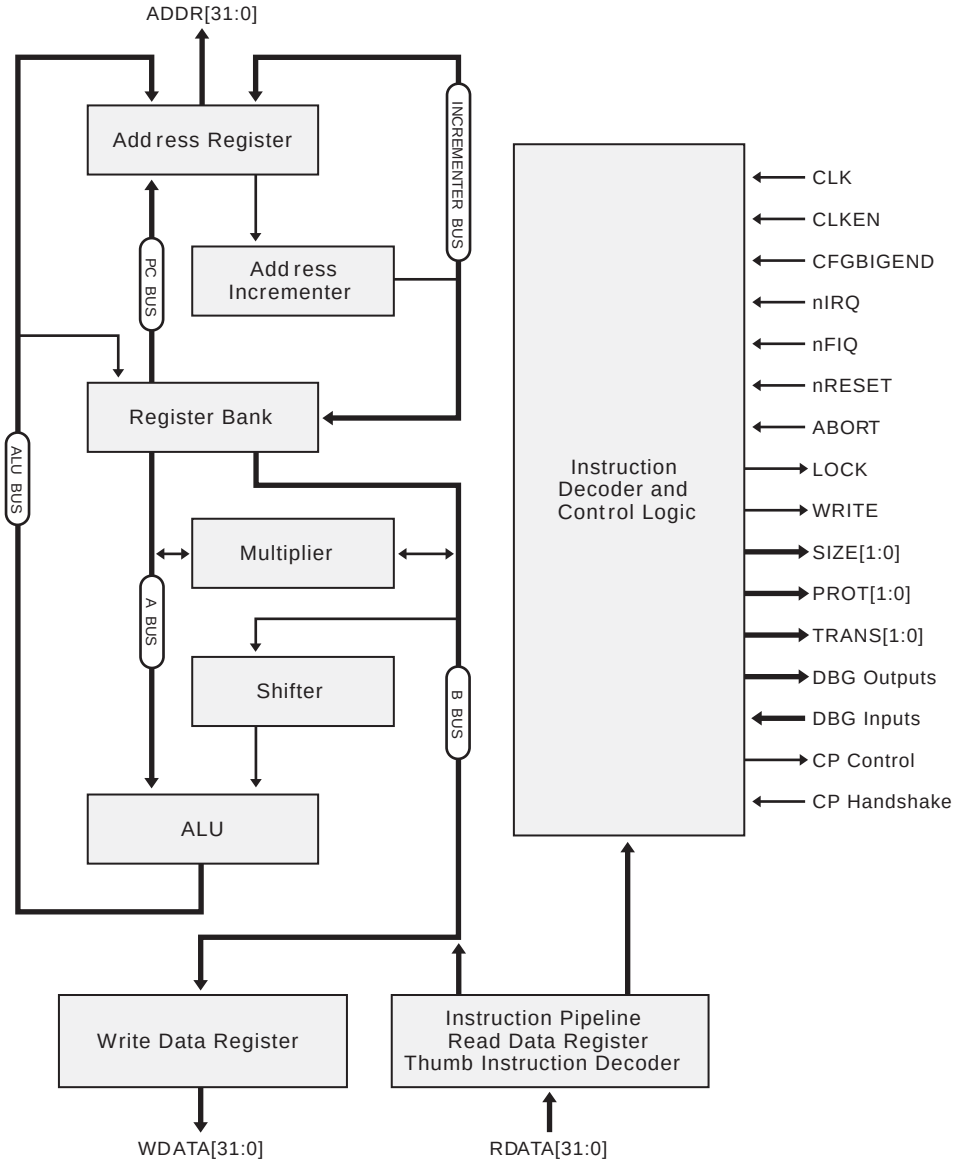

Figure 3: **CoreMP7 Block Diagram**

CoreMP7 Implementation Details

Architecture

CoreMP7 implements the ARMv4T instruction set and is compatible with ARM7TDMI-S. The core is based on the von Neumann architecture with a 32-bit data bus that carries both instructions and data. Load, store, and swap instructions can access data from memory. CoreMP7 implements all 32-bit ARM7 instructions and all 16-bit Thumb instructions. The core supports 8-, 16-, and 32-bit data types. CoreMP7 supports all of the standard ARM7 operating modes.

Bus Interface

CoreMP7 implements the 32-bit ARM7 native bus, and includes a configurable AHB interface wrapper that can be used to connect the native bus to an on-chip AHB interconnect bus.

Instruction Pipeline

CoreMP7 is implemented with a three-stage pipeline that increases the flow of instructions through the processor. This allows multiple simultaneous operations to take place and continuous operation of the processing and memory systems. The instructions are executed in three stages: Fetch, Decode, and Execute. The pipeline is shown in Figure 4.

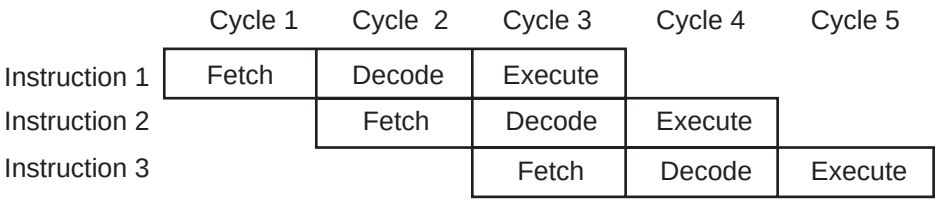

Figure 4: **CoreMP7 Pipeline**

Registers

CoreMP7 implements 31 32-bit general purpose registers in the register file and 6 status registers. There are 16 general-purpose registers and one or two status registers available at any one time in ARM mode, and 8 general registers are available in Thumb mode. There are 7 additional registers that are banked and accessible during a fast interrupt request.

Memory Interface

The 32-bit memory interface on CoreMP7 is designed to allow optimum performance and minimize memory usage. CoreMP7 is delivered with an AHB bus wrapper, which can be easily removed if the user wants to connect to a design with the native ARM7 interface.

Debug Features

CoreMP7 incorporates hardware that implements advanced debugging features to simplify the development and debug of application software, operating systems, and hardware. The debug hardware allows the core to be forced into the debug state. The internal state of the ARM7 core can be examined using a JTAG interface that allows the insertion of instructions into the core pipeline without using the external data bus. The optional debug hardware in CoreMP7 can be configured to monitor the core activity for specific instruction fetches and data accesses, and execution halts with breakpoints or watchpoints. Configuration of the CoreMP7 debug hardware is done through the JTAG interface.

Exceptions

CoreMP7 supports seven types of exceptions: fast interrupt (FIQ), normal interrupt (IRQ), data abort, prefetch abort, software interrupt, undefined instruction, and reset. All exceptions have banked registers for R14 and R13. After an exception, R14 holds the return address for exception processing. This address is used both to return after the exception is processed, and also to address the instruction that caused the exception. R13 is banked across exception modes to provide each exception handler with a private stack pointer. The fast interrupt mode also banks registers 8 to 12 so that interrupt processing can begin without the need to save or restore these registers.

Subsystem Peripherals

The subsystem peripherals are an important set of functional blocks for a microprocessor. These implement all of the low-level functionality that must be added around the processor so it can be used in an application. The CoreMP7 subsystem peripherals include: an AHB bus interface, APB bus interface, AHB to APB bridge, memory controller, interrupt controller, times, serial interface, and buffered I/O interface. The CoreMP7 subsystem peripherals are configurable RTL, and delivered as part of the CoreConsole IP Deployment Platform development tool.

M7 ProASIC3/E and M7 Fusion Families Overview

CoreMP7 is available in M7 ProASIC3/E and M7 Fusion devices that are part of the Actel Flash product line. The M7 devices have all of the features of other ProASIC3/E family devices in addition to being ARM-enabled, which allows the user to program CoreMP7 into them. The M7 devices are based on nonvolatile Flash technology and the M7 ProASIC3/E devices support 250 k to 3 M gates and up to 616 high-performance I/Os, while the M7 Fusion devices support 600 k to 1.5 M gates with a 12-bit ADC and up to 40 analog inputs.

Each of the M7 FPGAs is a secure, low power, live at power-up (LAPU), single-chip solution. Each is reprogrammable and offers time to market benefits at an ASIC-level unit cost. These features enable engineers to create high-performance, high-density system applications with ARM7, using existing FPGA design tools and flows. In addition, M7 devices offer an on-chip, user nonvolatile memory storage and clock conditioning circuitry based on up to six on-board phase-locked loops (PLLs). The M7 Fusion devices feature integrated analog capabilities.

Actel Flash-based M7 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for battery-operated and other power-sensitive applications. With M7 devices, there is no power-on current surge and no high-current transition that exists on many SRAM FPGAs. The devices also have low static and dynamic power consumption, further maximizing power savings. The M7 devices are listed in Table 1, which shows package and I/O count.

Table 1: **M7 ProASIC3/E and M7 Fusion Devices**

	I/Os: Single/Double-Ended								I/Os: Single/Double-Ended (Analog)	
	Devices	**M7A3P250**	**M7A3P400**	**M7A3P600**	**M7A3P1000**	**M7A3PE600**	**M7A3PE1500**	**M7A3PE3000**	**M7AFS600**	**M7AFS1500**
Packages	VQ100	68/13								
	PQ208	151/34	151/33	154/35	154/35	147/65	147/65	147/65	95/46 (40)	
	FG144	97/24	97/24	97/24	97/25					
	FG256		178/38	179/45	177/44	165/79			119/58 (40)	119/58 (40)
	FG484		194/38	227/56	300/74	270/135	280/136	280/136	172/86 (40)	228/86 (40)
	FG676						439/209			278/139 (40)
	FG896							616/300		

CoreMP7 Tools Overview

Actel has assembled a full suite of tools for the development of designs with CoreMP7 in M7 FPGA devices. These include the Libero IDE tool suite, CoreConsole, a block stitcher and IP deployment platform, the ARM RealView® tool kit, and a development/debug board that allows users to quickly evaluate and debug designs in an M7 device. Figure 5 shows a diagram of the development flow for the CoreMP7 tools.

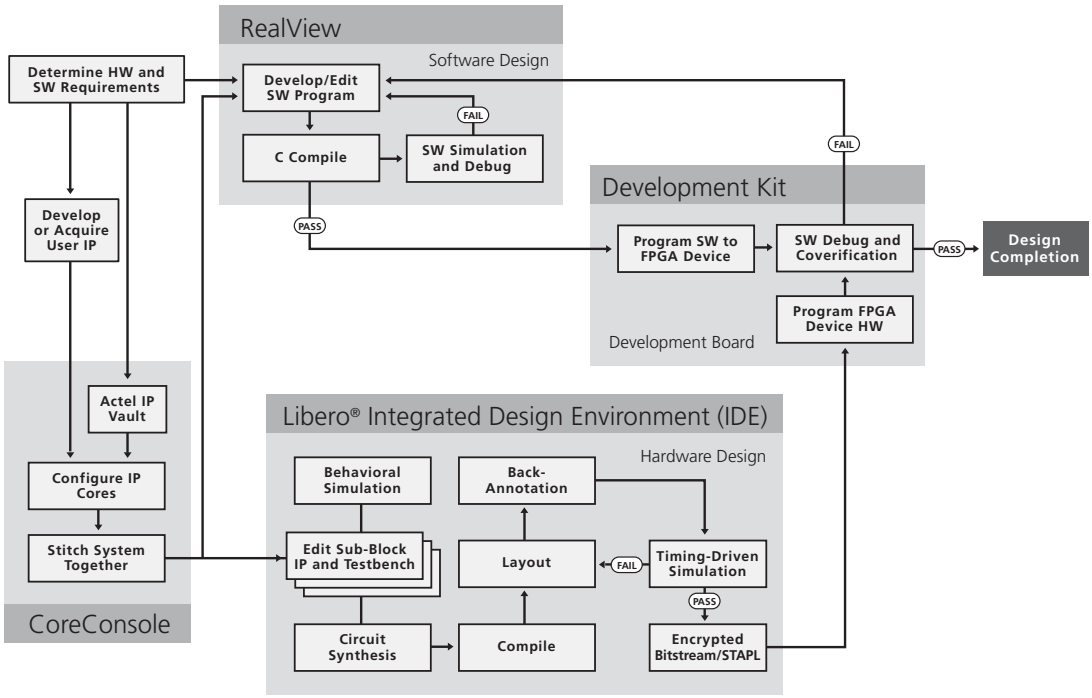

Figure 5: **CoreMP7 Development Tool Flow**

CoreConsole

Using ARM7 in system applications requires the implementation of other IP blocks and a subsystem around the processor. To facilitate and simplify the construction of the subsystem and assembly of the IP blocks, Actel has developed an IP Deployment Platform (IDP) tool with a block stitcher called CoreConsole. This new tool has an intuitive and easy to use graphical user interface that facilitates rapid assembly of system applications around CoreMP7. CoreConsole consists of two components: the CoreConsole IDP tool and an IP vault. The tool supports the integration of processor subsystem functions (timers, UARTs, etc.) with Actel DirectCores delivered in the IP Vault, as well as third-party and user-defined IP blocks. CoreConsole allows users to reduce system development time, perform system level evaluation, and focus on the system rather than components.

The CoreConsole user interface is graphical, intuitive, and easy to use. The tool supports the instantiation and configuration of user IP and canned IP blocks. CoreConsole is used at the design entry phase of the design process and deals mainly with RTL, allowing it to integrate easily with Libero IDE and other tools. CoreConsole enables users to configure IP blocks for use in their application, and also generates a system interconnect testbench that can be used to debug and validate the connection of the user's application within the FPGA fabric. It can also output drives and other files to the software development tools to enable faster development of the programs that run on the CoreMP7 soft processor.

Libero IDE

CoreMP7 and the M7 ProASIC3/E and M7 Fusion devices are fully supported by the Actel Libero IDE and Designer software tools. Libero IDE, which includes Designer, is the most comprehensive FPGA design and development software available, providing start-to-finish design flow guidance and control for novice and experienced users. Libero IDE includes all necessary design tools to bring M7 products to market quickly with the highest possible device performance.

By combining the Actel internally developed tools with EDA tools from industry leaders such as Magma Design Automation™, Mentor Graphics®, Synplicity®, and SynaptiCAD™ into a single package, Libero IDE provides a "one-stop shopping" approach. The Libero IDE ensures complete tool interoperability, a streamlined design flow, management of all source, design, run, and log files, and seamless passing of all design data between tools from schematic/HDL entry through synthesis, simulation, place-and-route, and device programming.

FlashPro3

The FPGA fabric on M7 devices can be programmed and debugged with a FlashPro3 programmer (Figure 6). M7 ProASIC3/E and M7 Fusion devices both support in-system programming (ISP) and programming of a device mounted on a board through an ISP header. The configuration data is supplied through a standard JTAG interface from a microprocessor, Silicon Sculptor II, or FlashPro3. The FlashPro3 programmer, with its small size, ease of portability, and USB programming port connections, is ideal for prototyping. FlashPro3 supports high-speed programming, and even the largest M7 devices can be programmed in less than two minutes.

Figure 6: **FlashPro3 Device Programmer**

RealView

ARM has developed an Actel RealView Developer Kit (RVDK) for CoreMP7 that provides tools for building, debugging, and managing software development projects that run on the processor. The toolkit contains an optimized C compiler, debugger, assembler, and instruction set simulator, and is available from Actel. Designers can use the RVDK to develop, build, and debug C, C++, and assembly language programs for CoreMP7.

Development Kit

The CoreMP7 Development Kit is a complete package consisting of a board with an M7 ProASIC3 device, Actel Libero IDE Gold, CoreConsole, C program development tools and debugger, the FlashPro3 programmer with a USB cable, a power supply, tutorials, and support documentation. Designers can develop their application or explore the various benefits of CoreMP7 in nonvolatile M7 ProASIC3 devices, including ISP, device serialization, and FlashLock® on-chip system security. Additionally, this kit enables fast and efficient evaluation of the performance and functionality of potential designs.

ARM7 Ecosystem

Because it is based on the industry standard ARM7 architecture, a major benefit of the CoreMP7 soft processor is the availability of a huge ecosystem of tools and design support. With an 80 percent share of market and the highest name recognition in the embedded 32-bit space, third-party suppliers have built up an immense ecosystem in support of the ARM architecture. The presence of this ecosystem greatly reduces the risk and amount of work that designers face to get their System-on-a-Chip (SoC) applications developed and released into the market. If a designer is familiar with a microprocessor development tool, it is almost certain that there is a version of it that will support CoreMP7.

Summary

With the increasing requirement for a 32-bit processor and the embedded market's transition to programmable logic, the combination of the CoreMP7 optimized ARM7 family processor with Actel Flash-based FPGAs provides a powerful application solution to designers. While there are other soft IP processors available for implementation in FPGAs, they are based on proprietary architectures with limited tools, support, and designer experience. By bringing ARM7TDMI-S to M7 ProASIC3/E and M7 Fusion devices, CoreMP7 enables designers to implement their embedded designs with the ARM7 industry standard architecture. The Actel CoreMP7 soft processor and M7 devices are supported by a complete suite of development tools and the huge ecosystem of software and tools that exist for ARM7, reducing design risk and time to market. By combining the flexibility of Actel Flash-based ProASIC3/E and Fusion devices with the industry standard ARM7 processor, Actel has created a superior solution that expands the usability of ARM7 from high-volume down to low-volume and prototype applications, bringing ARM7 to the masses.

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